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Solder layer degradation measurement for SiC-MOSFET Modules under accelerated power cycling conditions

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Abstract

Die-attach solder layer and bond wires are the two weakest parts in power modules. In order to distinguish the solder layer and bond wire degradation during accelerated tests, a simultaneous on-line measurement method is proposed in this paper. By means of auxiliary source terminal, both the solder layer resistance increase and bond wire resistance increase can be measured and monitored separately. To measure accurately the solder layer degradation, the intrinsic diode is used as heating source in place of the MOSFET switch. In this way, the measurement method becomes intrinsically insensitive to possible threshold voltage shifts, typical of accelerated tests of SiC power MOSFETs. Finally, the experimental results are presented to verify the feasibility of the proposed test method. It is revealed that the solder layer resistance increases linearly with the number of cycles in good approximation.

1 Introduction

Silicon Carbide (SiC) is characterized by higher critical electric field, higher saturated velocity and higher thermal conductivity in respect to silicon [1]. These superior performances make it possible to increase the converter power density and improve the maximum operation temperature of power conversion systems [2]. However, the elevated operation temperature will put forward higher requirements in terms of package-related reliability. Thermal cycling tests and power cycling tests can be regarded as two kinds of reliability evaluation methods for power modules. By means of accelerated cycling tests, both die and packaging reliability issues can be detected and investigated thoroughly. The conventional cross section structure of a SiC power module is depicted in Figure 1 [3].

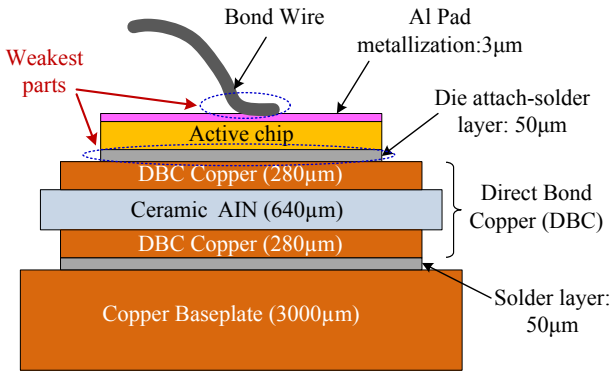

Figure 1 Schematic cross-section of a SiC power module.

According to previous studies, the most vulnerable parts in power modules after long-term accelerated cycling tests are bond wires and solder layer [4], [5]. Due to the thermal expansion coefficient mismatch among the different materials, the power module packages experience an irreversible degradation over long-term operation. So far, a lot of studies have been devoted to evaluate and monitor the bond wire degradation process. Considering the bond wire lift-off failure, the voltage drop across the bond wire can be treated as an aging precursor. However, few of the mentioned studies have addressed the solder layer degradation. In fact, since the die backside is not accessible, there is no possible way to measure the voltage on the solder layer directly. In practice, the solder layer degradation is usually evaluated by means of thermal impedance measurement and scanning acoustic microscopy (SAM) method after the power cycling tests [6]. In fact, because of the delamination, cracks and voids appear in the solder layer, leading to higher junction temperature under the same power losses. Furthermore, the location and size of voids can be scanned and investigated by means of SAM.

In this paper, a solder layer degradation measurement method for SiC-MOSFET modules during power cycling test is proposed. Taking the advantage of the auxiliary source terminal, both the solder layer resistance and the bond wire degradation can be measured. Hence, both the conventional bond wire degradation and the solder layer degradation can be monitored and evaluated simultaneously. In order to avoid the SiC die degradation caused by the threshold voltage shift [7], the intrinsic diode is used for load current conduction. More importantly, the intrinsic diode is the first used to measure solder layer degradation. Finally, the resistance increase of the die attached solder layer can also be distinguished from SiC die degradation itself.

2 Proposed method

2.1 Problem statements in conventional DC-based power cycling test method

The equivalent circuit of SiC power module considering the parasitic resistances and the external measurement terminals is shown in Figure 2 [8]. R_{Pbw} is the parasitic resistance of positive power terminal, R_{cop} is the parasitic resistance of copper layer, R_{Nbw} is the parasitic resistance of negative power terminal, R_{das} is , the die attached solder layer resistance, V_{ds} is SiC die voltage under load current I_{load}, R_{bw} is die attached bond wire resistance and R_{Nbw} is the parasitic resistance of negative power terminal. In order to avoid the common source resistances R_{bw} and R_{Nbw}, an additional terminal known as the Kelvin-source (s) is used for gating the power device.

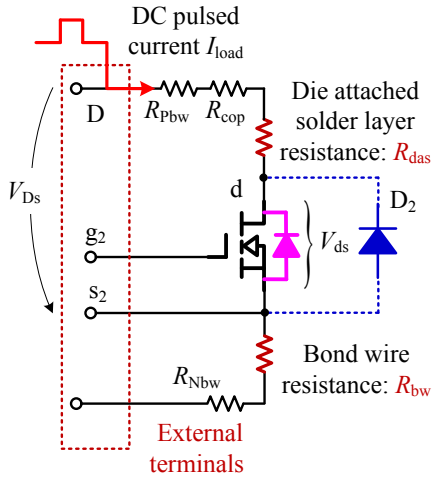

Figure 2 Equivalent circuit of a SiC power device considering parasitic resistances

According to the independent measurement method proposed in [8], the die attached solder layer resistance increase R_{das} can be measured indirectly by means of the voltage V_{Ds}. Correspondingly, the measurable voltage V_{Ds} consists of the SiC die resistance V_{ds}, R_{das}, R_{cop} and R_{Pbw}. Since the power terminal related bond wire parts are far away from the die during the test, R_{Pbw} and R_{cop} can be considered as constant. However, another additional challenge is the question of threshold voltage shift under highly power cycling conditions. Under elevated temperature and gating voltage conditions, the gradual threshold voltage shift would lead to SiC die degradation, which corresponding causes the die resistance change in the condition of fixed I_{load}. In that case, the measured voltage V_{Ds} contains both die voltage V_{ds} change and the solder layer increase. Therefore, the conventional measurement method using MOSFET die cannot be applied to the solder layer resistance increase measurement.

2.2 Proposed measurement method

In order to obtain the accurate solder layer resistance increase, the potential threshold voltage shift related die degradation should be avoided. Since the SiC MOSFET die contains intrinsic body diode, the internal diode can also be used as the heating source in the power cycling test. More importantly, there is no die degradation mechanism for intrinsic diode such as the threshold voltage shift. Hence, the increased voltage during the test can be attributable to the package related degradation rather than the die degradation. In this work, the DC pulsed load current is controlled to flow through the intrinsic diode to generate the intended temperature swing. Taking the commercial SiC MOSFET module from CREE (CCS020M12CM2) as an example, the internal layout for single phase bridge is depicted in Figure 3(a). Besides, the related equivalent circuit and measurement principle are depicted in Figure 3(b).

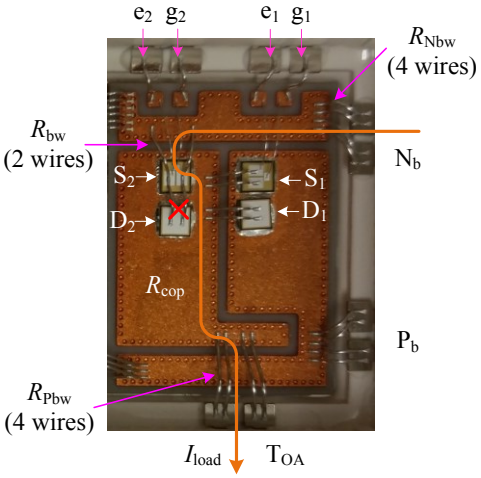

Figure 3(a) Equivalent circuit of a SiC power device considering parasitic resistances

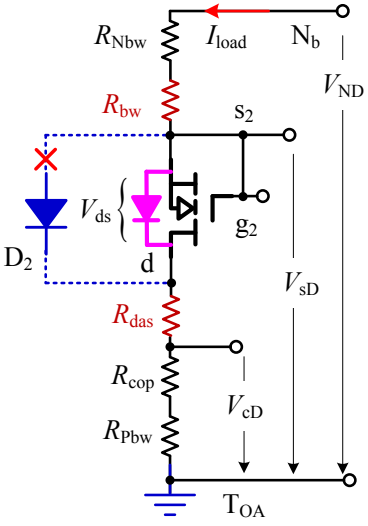

Figure 3(b) Equivalent circuit considering external measurement terminals

In order to bypass the external diode D_2, the two bond wires are cut as shown in Figure 3(b). As depicted in Figure 3(b), there are three measurable voltages V_{cD}, V_{sD} and V_{ND} under specific DC load current. Among them, voltages V_{sD} and V_{ND} contain the packaging related degradation information. Considering the voltage V_{sD}, it contains three parts of voltages, as expressed by

$$V_{sD}=V_{ds}+V_{cD}+I_{load}\cdot R_{das} \quad (1)$$

Assuming there is no degradation on the intrinsic diode (V_{ds}), copper layer (R_{cop}) and power terminal bond wires (R_{pbw}), the die attached solder layer resistance increase ΔR_{das} can be calculated by

$$\Delta R_{das}=\Delta V_{sD}/I_{load} \quad (2)$$

In general, the parasitic resistance R_{das} cannot be obtained directly, but the related resistance increase ΔR_{das} can be measured.

Another conventional failure case we consider is the bond wire degradation. Since R_{Nbw} can be regarded as constant during the tests, the bond wire resistance can be calculated by

$$V_{ND}= V_{sD} +I_{load}\cdot(R_{bw}+R_{Nbw}) \quad (3)$$

In case of fixed load current, the bond wire resistance increase ΔR_{bw} can be obtained by the voltage difference between V_{ND} and V_{sD}, as expressed by

$$\Delta R_{bw}=\Delta(V_{ND}- V_{sD})/I_{load} \quad (4)$$

Therefore, two kinds of packaging failures can be monitored during the test: the solder layer degradation and the bond wire resistance increase.

3 Test conditions

In order to validate the proposed separation method, a power cycling test platform was built and one SiC module from CREE (CCS020M12CM2) has been tested. The test conditions for the SiC modules are listed in Table I. The intended temperature swing is in the range of 25°C to 85°C ($\Delta T_j \approx 60$°C). The average temperature was adjusted by means of an external heating system. The injected load current was 17 A.

TABLE I. TEST CONDITIONS FOR CREE MODULE

Parameters	Conditions	Parameters	Conditions
Maximum T_j	85 °C	Period/duration	4s / 8s
Minimum T_j	25 °C	Base plate temperature	≈ 23 °C
Delta T_j	60 °C	Drain current I_{DS}	17 A

The on-time junction temperature is realized by isolated optical fiber from Opsens [9]. Moreover, the measurement positions for the optical fibres as well as the voltage probes are essential to get the accurate measurement results. In Figure 4, the implementations of the voltage and temperature measurement are depicted. Considering the junction temperature swing, one test point is selected at the center of SiC die. In order to investigate the thermal stress for the power terminal bond wires, the fibre test point 2 is selected at the copper area connected to the bond wires.

In Figure 5, the on-line temperature waveforms for the SiC die and power terminal bond wires have been reported. It is shown that the temperature swing for the power terminal bond wires is around 2 °C. This means that the parasitic resistance R_{Nbw} can be regarded as constant since the temperature stress is negligible.

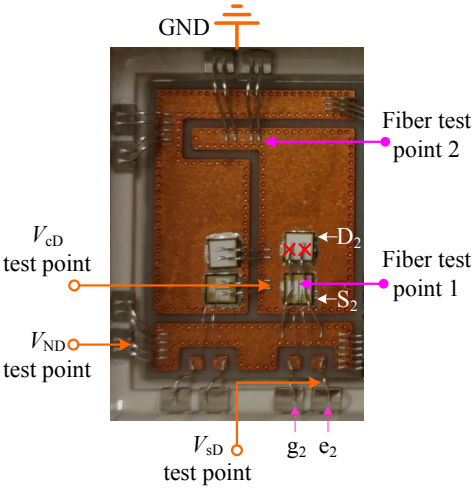

Figure 4 Selected measurement points for temperature swings monitoring and voltage measurements.

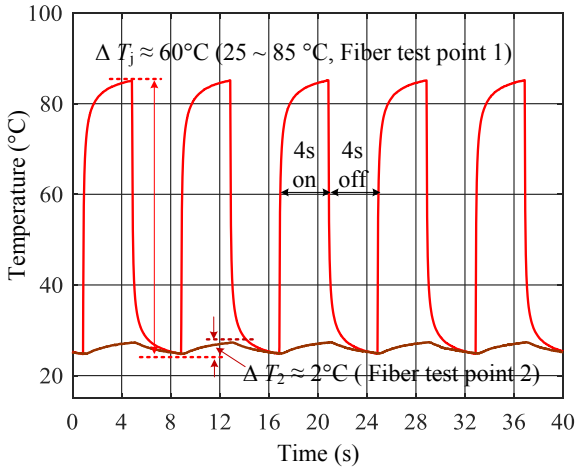

Figure 5 Selected measurement points for temperature swings and voltage measurements.

4 Experimental results

The measured voltage V_{ND} after 30 k and 100 k cycles are depicted in Figure 6 for the sake of comparison. The increased voltage contains two parts of resistance increase: bond wire resistance increase and solder layer resistance increase. However, based merely on V_{ND}, the solder layer resistance increase cannot be distinguished from the bond wire resistance increase.

In Figure 7, the key voltage waveforms after 100 cycles are depicted. The final average voltage for V_{ND} is around 3.81 V, which includes the bond wire resistance increase and solder layer resistance increase. Since the resistance R_{cop} and R_{Nbw} are constant, the voltage V_{sD} increase can be attributed to the solder layer resistance increase. Besides, the average V_{sD} during the conduction pulse is around 3.63 V.

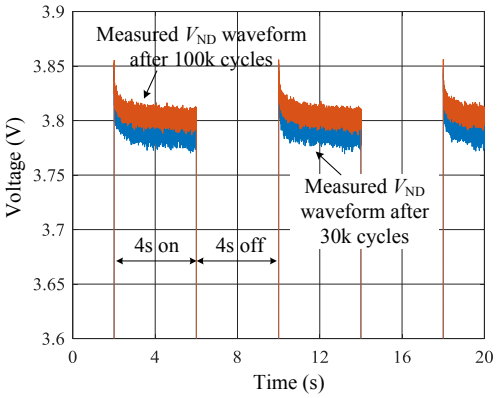

Figure 6 Key waveform comparisons for measured voltage V_{ND} after 30k and 100k cycles.

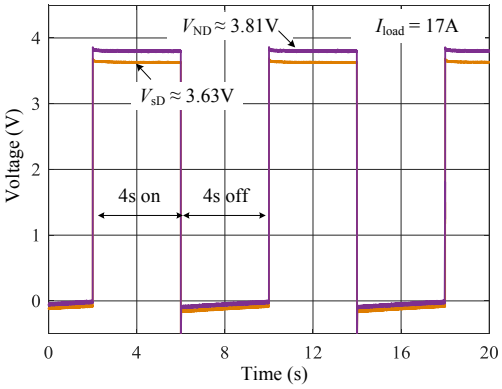

Figure 7 Experimental waveforms of measured V_{ND} and V_{sD} after around 100 k cycles**.**

In Figure 8, the measured V_{cD} and bond wire voltage are depicted. In case of I_{load}=17A, the voltage V_{cD} is around 17 mV. In addition, the bond wire voltage can be worked out by subtracting V_{sD} from V_{ND}. After around 100k cycles, the measured average bond wire voltage is 172 mV. Different with the diode die resistance, the measured waveforms on copper layer and power bond wires are independent of the junction temperature variation.

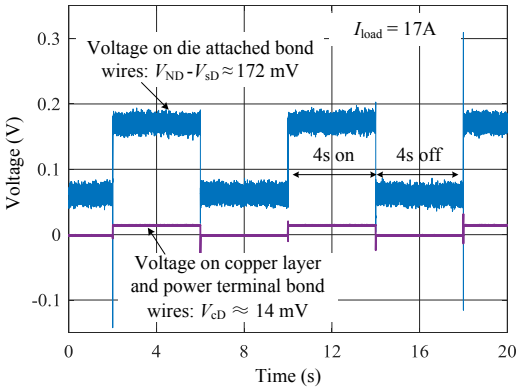

Figure 8 Experimental waveforms of measured (V_{ND}-V_{sD}) and V_{cD} after around 100 k cycles**.**

The recorded voltages and related polynomial fitting curves for the device under test are plotted in Figure 9. According to the polynomial fitting curve for voltage V_{sD}, there is around 0.55% increase after 100k cycles. Correspondingly, the voltage increase is around 20 mV, and the related resistance increase ΔR_{das} is 1.18 mΩ. Meanwhile, the measured voltage V_{ND} increases from 3.77V to 3.82 V after 100k cycles.

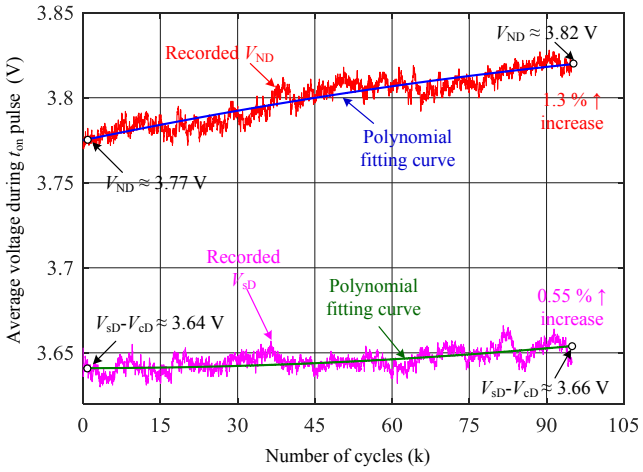

Figure 9 Key waveforms of bond wire degradation

5 Conclusion

This paper has presented a measurement method for solder layer degradation monitoring under power cycling tests. By means of the auxiliary source terminal, both the solder layer resistance increase and bond wire resistance increase can be measured separately. In order to avoid the die resistance change due to the threshold voltage shift, the intrinsic diode is not only used as a heating source, but to get rid of the MOSFET threshold voltage dependence on aging process during the power cycling tests. Experiments were implemented to verify the effectiveness of the proposed method. With the number of cycles, the

solder layer resistance increases linearly in good approximation.

6 Reference

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