Triple-Phase-Shift Control Strategy for Full-Bridge Three-Level (FBTL) DC/DC Converter

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Triple-Phase-Shift Control Strategy for Full-Bridge Three-Level (FBTL) DC/DC Converter

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***Abstract*—This paper proposes a triple-phase-shift (TPS) control strategy for the full-bridge three-level (FBTL) DC/DC converter to reduce the voltage stress and harmonics on the transformer. The proposed control strategy is composed of three phase-shift delays to keep the maximum voltage changes (ΔV) on the transformer's primary side at only half of the input voltage ($V_{in}/2$), which is different from the conventional control strategies causing the higher voltage changes with value of V_{in}. Therefore, the proposed control strategy can effectively reduce the voltage change rate (dv/dt) and voltage harmonics on the transformer due to the benefits of multi-level voltage produced by the three phase-shift delays. Additionally, the proposed TPS control strategy has two working modes, which can thus have wide voltage gain. Finally, the experimental results are presented to verify the proposed control strategy.**

Keywords—full-bridge (FB); phase-shift control; three-level (TL) DC/DC converter; wide voltage gain.

I. INTRODUCTION

Normally, the power electronic converters can be mainly classified into three categories including AC/DC rectifier, DC/AC inverter [1], and DC/DC converter. The DC-DC converters aims to change the voltage levels for the DC applications [2-5]. Among various types of DC/DC converters, three-level (TL) based DC/DC converters are one of most attractive choices for high voltage applications because the voltage stress on the power switches in TL based DC/DC converters is only half of the input voltage ($V_{in}/2$) [6-8]. Normally, the full-bridge DC/DC converter is more suitable for higher power applications [9], [10] in comparison with the half-bridge DC/DC converter because of the current stress on the power switches in the full-bridge DC/DC converter is half of that in the half-bridge DC/DC converter. Reference [11] proposed a chopping plus phase-shift (CPS) control strategy for the FBTL DC/DC converter based on the control strategy for the hybrid three-level DC/DC converter in [12]. Furthermore, a double phase-shift (DPS) control strategy for the FBTL DC/DC converter was proposed in [13], which improves the converter's efficiency in comparison with the CPS control strategy. The CPS and DPS control strategies both have the wide voltage gain, but these two control strategies cause the high voltage change rate (dv/dt) on the transformer, which would result in high harmonics on the transformer and large electromagnetic interference. In order to reduce such high voltage change rate (dv/dt) on the transformer, an improved FBTL DC/DC converter with corresponding control strategy was proposed in [14]. However, a passive filter needs to be added in the transformer's primary side, which would reduce the converter's efficiency and voltage conversion rate. A new double phase-shift control strategy was also proposed in [15] to reduce the high voltage change rate (dv/dt) on the transformer, but this control strategy cannot satisfy the wide input voltage range in comparison with the control strategies [11], [13].

In this paper, a triple-phase-shift (TPS) control strategy is proposed for the FBTL DC/DC converter, which can not only reduce the voltage stress on the transformer but also satisfy the wide input voltage range. Under conventional control strategies, there exist high voltage changes on the transformer, but the proposed control strategy can decrease the maximum voltage changes on the primary side of the transformer to half of the input voltage ($V_{in}/2$) by utilizing three phase-shift delays. Therefore, the voltage change rate (dv/dt), voltage stress, and voltage harmonics on the transformer can be effectively reduced by utilizing the proposed control strategy. Additionally, the proposed control strategy includes two working modes to achieve the wide voltage gain. Finally, the experimental results validate the proposed TPS control strategy.

II. OPERATION PRINCIPLE

Fig. 1 presents the structure of FBTL DC/DC converter, in which C_{i1} and C_{i2} are two input capacitors; S_1 - S_8 and D_1 - D_8 are power switches and power diodes; C_1 - C_8 are parasitic capacitors of S_1 - S_8; C_{s1} and C_{s2} are two flying capacitors; D_9 - D_{12} are four clamped diodes; T_r is the transformer; L_r is the leakage inductor of the transformer T_r; D_{r1} - D_{r4} are four output rectifier diodes; L_o and C_o are output filter inductor and capacitor, respectively. In Fig. 1, V_1 and V_2 are voltages on C_{i1} and C_{i2}, respectively; V_{in} is the input voltage; V_{ab} is the voltage between point a and b; i_p is the primary current of the transformer T_r; i_{Lo} is the current flowing through the output filter inductor L_o; V_o and I_o are the output voltage and output current; n is the turns ratio of the transformer T_r.

In addition, some assumptions are made to simplify the following analysis: 1) S_1 - S_8 and D_1 - D_{12} are ideal switches and diodes; 2) C_{i1}, C_{i2} are large enough to be considered as constant voltage sources with the value of the half of input voltage ($V_{in}/2$); 3) L_o is large enough to be regarded as a constant current source; 4) C_{s1} and C_{s2} are larg enough to be considered as two voltage sources with the values of $V_{in}/2$

and only provide charging and discharging paths for the switches' parasitic capacitors.

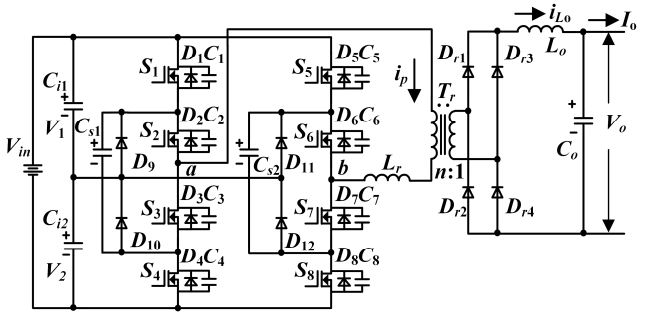
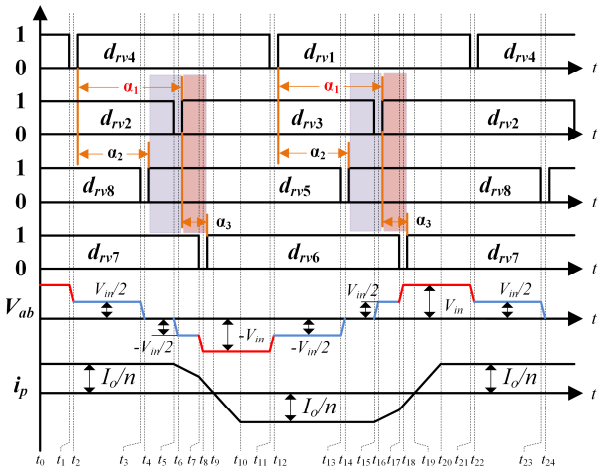


Fig. 1. FBTL DC/DC converter.

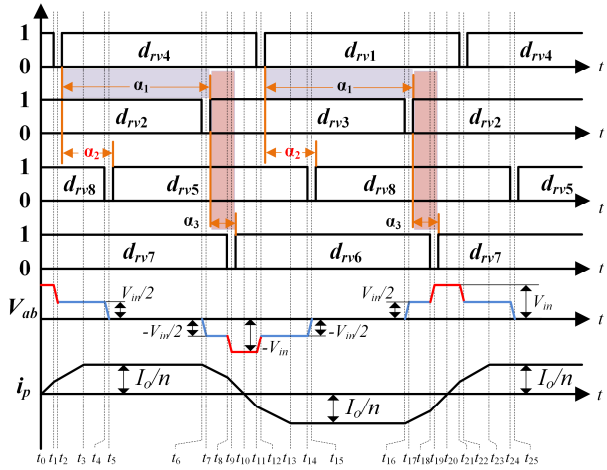
A. Proposed TPS Strategy

The proposed TPS control strategy includes three phase-shift delays and has two working modes to satisfy the wide input voltage range. Figs. 2(a) and (b) present the working mode I and II of the proposed strategy respectively, in which d_{rv1} - d_{rv8} are driving signals of switches S_1 - S_8; α_1, α_2, and α_3 are three phase-shift delays.

- ***Working mode I*** is utilized for the low input voltage. In the working mode I, α_1 - α_2 and α_3 are both kept constant as highlighted in Fig. 2(a); and the output voltage V_o is controlled by adjusting α_1. By adjusting the value of α_1, the time length of third-level voltages (V_{in} and $-V_{in}$) as marked by red color in Fig. 2(a) would be changed, which can thus adjust the output voltage V_o. For instance, if increasing α_1, the time length of the third-level voltages (V_{in} and $-V_{in}$) would decrease, which means that the output voltage V_o would decrease.
- ***Working mode II*** is utilized for the high input voltage when α_1 reaches to its maximum value. The output voltage V_o is controlled by adjusting α_2. By adjusting the value of α_2, the time length of second-level voltage ($V_{in}/2$ and $-V_{in}/2$) as marked by blue color in Fig. 2(b) would be changed, which can thus adjust the output voltage V_o. For instance, if decreasing α_2, the time length of the second-level voltages ($V_{in}/2$ and $-V_{in}/2$) would decrease, which means that the output voltage V_o would decrease.



(a)



(b)

Fig. 2. Main waveforms. (a) Working mode I. (b) Working mode II.

From Fig. 2, it can be observed that the maximum voltage changes on the transformer's primary side in the two working modes are both kept at half of the input voltage ($V_{in}/2$) by utilizing the three phase-shift delays.

B. Working Mode I

The operation principle of half cycle in the working mode I (shown in Fig. 2(a)) is analyzed as below. Fig. 3 presents four selected equivalent circuits in the working mode I. The other equivalent circuits can be derived according to the operation analysis below, which are not repeated here.

Stage 1 [before t_1]: In this period, S_1, S_2, S_7, and S_8 are all on, so V_{ab} is V_{in} and the input power transfers to the load from D_{r1} and D_{r4}. In this stage, the primary current of the transformer i_p is I_o/n.

Stage 2 [t_1 - t_2]: At t_1, S_1 is switched off, then the output current I_o is reflected to the primary side, which means i_p is still I_o/n to charge C_1 and discharge C_4 via C_{s1}. Accordingly, V_{c1} increases and V_{c4} decreases linearly.

Stage 3 [t_2 - t_3]: At t_2, V_{c1} increases to $V_{in}/2$ and D_9 conducts, clamping V_{c4} at 0 V. Therefore, S_4 would be switched on with zero-voltage. In this stage, V_{ab} is $V_{in}/2$ and i_p remains I_o/n.

Stage 4 [t_3 - t_4]: At t_3, S_8 is switched off; i_p maintains at I_o/n to charge C_8 and discharge C_5 via C_{s2}. V_{c8} increases and V_{c5} decreases linearly.

Stage 5 [t_4 - t_5]: At t_4, V_{c8} increases to $V_{in}/2$ and V_{c5} decreases to 0 V. Then D_{12} conducts, clamping the voltages of S_5 at 0 V. Accordingly, S_5 would be switched on with zero-voltage. In this stage, V_{ab} is 0 V and i_p is I_o/n.

Stage 6 [t_5 - t_6]: At t_5, S_2 is switched off. Then C_2 is charged and C_3 is discharged; V_{ab} changes to negative. The current i_p starts to decrease and is not enough to provide output current I_o, so the output rectifier diodes D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V. Accordingly, the voltage on L_r is V_{ab}. In this stage, L_r resonates with C_2 and C_3.

Stage 7 [t_6 - t_7]: At t_6, V_{c2} increases to $V_{in}/2$; V_{c3} decreases to 0 V; V_{ab} decreases to $-V_{in}/2$. Then D_3 conducts,

clamping the voltage of S_3 at 0 V, so S_3 can be switched on with zero-voltage. Because D_{r1}, D_{r2}, D_{r3}, and D_{r4} still keep conducting, the voltage on L_r is $-V_{in}/2$, thus i_p decreases linearly.

Stage 8 [t_7 - t_8]: At t_7, S_7 is switched off; C_7 is charged and C_6 is discharged; V_{ab} starts to decrease from $-V_{in}/2$. In this stage, i_p continues to decrease because D_{r1}, D_{r2}, D_{r3}, and D_{r4} still conducts, clamping the primary and secondary voltage of the transformer at 0 V. In this stage, L_r resonates with C_6 and C_7.

Stage 9 [t_8 - t_9]: At t_8, the voltage of S_7 is $V_{in}/2$ and D_6 conducts, clamping the voltage of the switch S_6 at 0 V. Accordingly, S_6 would be switched on with zero-voltage.

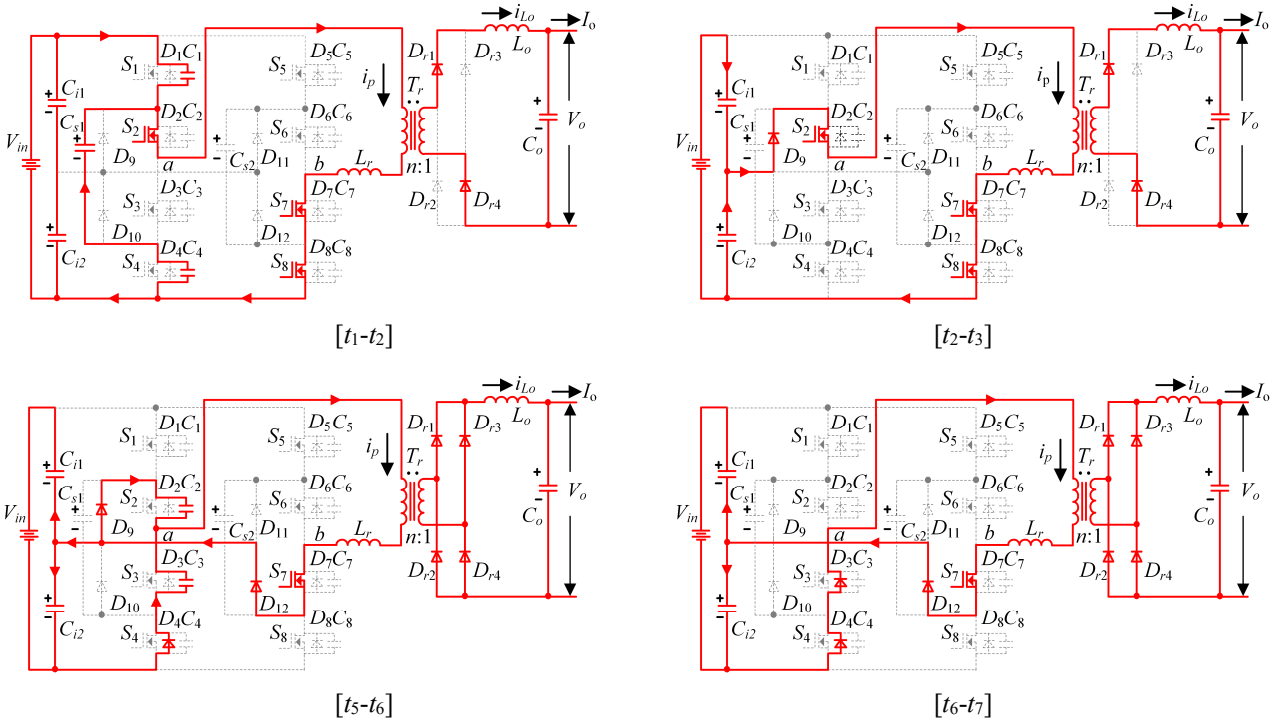


Fig. 3. Selected equivalent circuits in working mode I.

C. Working Mode II

The operation principle of half cycle in the working mode II (shown in Fig. 2(b)) is analyzed as below. Fig. 4 presents four selected equivalent circuits in the working mode II. The other equivalent circuits can be derived according to the operation analysis below, which are not repeated here.

Stage 1 [before t_1]: In this period, although S_1, S_2, S_7, and S_8 are all on-state, the primary current i_p is not enough to provide I_o and increases linearly. Therefore, D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, clamping the primary and secondary voltage at 0 V. The primary current i_p increases linearly.

Stage 2 [t_1 - t_2]: At t_1, S_1 is switched off. The primary current i_p charges C_1 and discharges C_4 via C_{s1}. Therefore, V_{c1} increases and V_{c4} decreases.

Stage 3 [t_2 - t_3]: At t_2, V_{c1} increases to $V_{in}/2$, V_{c4} decreases to 0 V, and D_9 conducts, clamping V_{c4} at 0 V. Therefore, S_4 can be switched on with zero-voltage. In this stage, V_{ab} is $V_{in}/2$ and i_p still increases linearly.

D_{r1}, D_{r2}, D_{r3}, and D_{r4} keep conducting. In this stage, the voltage on L_r is $-V_{in}$, thus i_p decreases linearly.

Stage 10 [t_9 - t_{10}]: At t_9, i_p decreases to 0 A, then the current direction of i_p changes. The voltage on L_r maintains $-V_{in}$, so i_p remains decreasing linearly.

Stage 11 [t_{10} - t_{11}]: At t_{10}, i_p decreases to $-I_o/n$ (the negative reflected output current). Then, D_{r1}, D_{r4} are switched off, and D_{r2}, D_{r3} is utilized to transfer the input power to load.

At t_{11}, S_4 is switched off. The second half cycle [t_{11} - t_{21}] starts. The following analysis is similar to the first half cycle [t_1 - t_{11}], which is not repeated here.

Stage 4 [t_3 - t_4]: At t_3, i_p increases to I_o/n (the positive reflected output current). Then D_{r2} and D_{r3} are switched off, and then D_{r1} and D_{r4} are utilized to transfer the input power to load.

Stage 5 [t_4 - t_5]: At t_4, S_8 is switched off. Then I_o is reflected to the primary side, i_p is still I_o/n to charge C_8 and discharge C_5 via the flying capacitor C_{s2}. V_{c8} increases linearly, and V_{c5} decreases linearly.

Stage 6 [t_5 - t_6]: At t_5, V_{c8} increases to $V_{in}/2$, V_{c5} decreases to 0V, and D_{12} conducts, clamping V_{c5} at 0 V. Therefore, S_5 would be switched on with zero-voltage. In this stage, V_{ab} is 0 V and i_p remains the positive reflected output current I_o/n.

Stage 7 [t_6 - t_7]: At t_6, S_2 is switched off. Then C_2 is charged and C_3 is discharged; V_{ab} changes to negative. The current i_p starts to decrease and is not enough to provide I_o, so D_{r1}, D_{r2}, D_{r3}, and D_{r4} conduct simultaneously, clamping the primary and secondary voltage at 0 V. Thus, the voltage on L_r is V_{ab}. In this stage, L_r resonates with C_2 and C_3.

Stage 8 [t_7 - t_8]: At t_7, V_{c2} increases to $V_{in}/2$; V_{c3} decreases to 0 V; and V_{ab} decreases to $-V_{in}/2$. Then, D_3

conducts, clamping the voltage of S_3 at 0 V, so S_3 can be switched on with zero-voltage. Because D_{r1}, D_{r2}, D_{r3}, and D_{r4} keep conducting, the voltage on L_r is $-V_{in}/2$, so i_p decreases linearly.

Stage 9 [t_8 - t_9]: At t_8, S_7 is switched off; C_7 is charged and C_6 is discharged; V_{ab} starts to decrease from $-V_{in}/2$. In this stage, i_p remain decreasing and D_{r1}, D_{r2}, D_{r3}, and D_{r4} still conduct, clamping both the primary and secondary voltage of the transformer at 0 V. In this stage, L_r resonates with C_6 and C_7.

Stage 10 [t_9 - t_{10}]: At t_9, V_{c7} increases to $V_{in}/2$, V_{c7} decreases to 0 V, and D_6 conducts, clamping the voltage of S_6 at 0 V, thus S_6 would be switched on with zero-voltage. D_{r1}, D_{r2}, D_{r3}, and D_{r4} keep conducting, thus the voltage on L_r is $-V_{in}$ and i_p decreases linearly.

Stage 11 [t_{10} - t_{11}]: At t_{10}, i_p decreases to 0 A, then the current direction of i_p changes. The voltage on L_r is still $-V_{in}$, so i_p remains decreasing linearly.

At t_{11}, S_4 is switched off. The second half cycle [t_{11} - t_{21}] starts. The following analysis is similar to the first half cycle [t_1 - t_{11}], which is not repeated here.

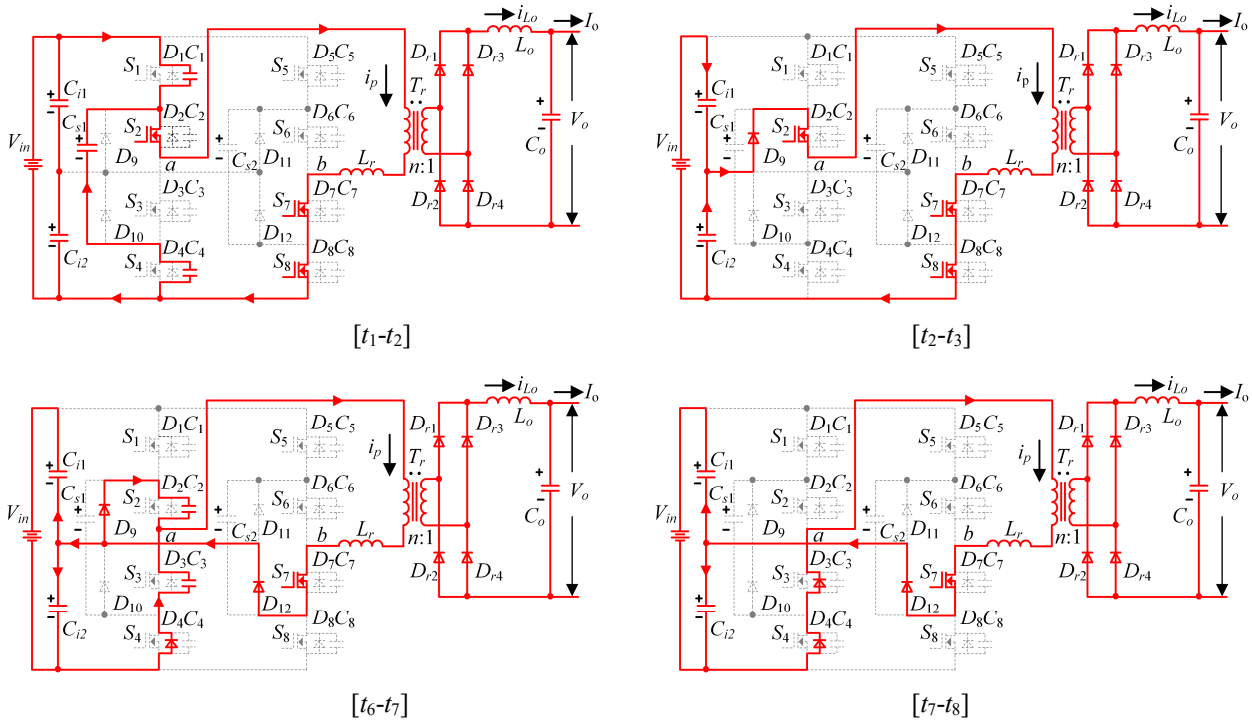


Fig. 4. Selected equivalent circuits in working mode II.

III. Characteristic and Performance Analysis

A. Duty Cycle Loss

In the working mode I as shown in Fig. 2(a), the time periods [t_5 - t_{10}] and [t_{15} - t_{20}] are the time of duty cycle losses in one switching period. If neglecting the quite short time periods [t_5 - t_6] and [t_7 - t_8], the two time periods [t_5 - t_{10}] and [t_{15} - t_{20}] can be given by (1).

$$t_{10}-t_5=t_{20}-t_{15}=\frac{\alpha_3}{2}+\frac{2\cdot L_r\cdot I_o}{n\cdot V_{in}} \tag{1}$$

Based on (1), the duty cycle loss in one switching period in the working mode I namely D_{loss_I} can be calculated by (2).

$$D_{loss\_I}=\frac{(t_{10}-t_5)+(t_{20}-t_{15})}{T_s}=\frac{\alpha_3}{T_s}+\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s} \tag{2}$$

In the working mode II as shown in Fig. 2(b), the time of duty cycle losses are [t_6 - t_{13}] and [t_{16} - t_{23}] in one switching period. If neglecting the quite short time periods [t_6 - t_7], [t_8 - t_9], and [t_{11} - t_{12}], the two time periods [t_6 - t_{13}] and [t_{16} - t_{23}] are the same and can be given by (3).

$$t_{13}-t_6=t_{23}-t_{16}=\alpha_1+\alpha_3+\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}}-\frac{T_s}{2} \tag{3}$$

Based on (3), the duty cycle loss in one switching period in the working mode II namely D_{loss_II} can be calculated by (4).

$$D_{loss\_II}=\frac{(t_{13}-t_6)+(t_{23}-t_{16})}{T_s}=\frac{2\cdot(\alpha_1+\alpha_3)}{T_s}+\frac{8\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}-1 \tag{4}$$

B. Output Characteristic

In the practical operations, the duty cycle loss would affect the output voltage. Therefore, the average output voltage in the working mode I namely V_{o_I} can be calculated by (5) when considering the duty cycle loss (2).

$$\begin{aligned}V_{o\_I}&=\frac{V_{in}}{n}\cdot\left(1-\frac{2\cdot\alpha_1}{T_s}-D_{loss\_I}\right)+\frac{V_{in}}{2\cdot n}\cdot\frac{2\cdot\alpha_2}{T_s}\\&=\frac{V_{in}}{n}\cdot\left(1-\frac{2\cdot\alpha_1}{T_s}-\frac{\alpha_3}{T_s}+\frac{\alpha_2}{T_s}-\frac{4\cdot L_r\cdot I_o}{n\cdot V_{in}\cdot T_s}\right)\end{aligned} \tag{5}$$

Considering the duty cycle loss (4), the average output voltage in the working mode II namely V_{o_II} can be calculated by (6).

$$V_{o\_II} = \frac{V_{in}}{2 \cdot n} \cdot (1 + \frac{2 \cdot \alpha_2 - 2 \cdot \alpha_1}{T_s} - D_{loss\_II}) = \frac{V_{in}}{n} \cdot (1 + \frac{\alpha_2}{T_s} - \frac{\alpha_3}{T_s} - \frac{2 \cdot \alpha_1}{T_s} - \frac{4 \cdot L_r \cdot I_o}{n \cdot V_{in} \cdot T_s}) \quad (6)$$

C. Output Filter Inductor

In the working mode I, there are two working operations that $V_o \geq V_{in}/2n$ and $V_o < V_{in}/2n$.

If $V_o \geq V_{in}/2n$, the ripple current on the output filter inductor namely Δi_{Lo} can be calculated by (7). If $V_o < V_{in}/2n$, the ripple current on the output filter inductor can be calculated by (8).

$$\Delta i_{Lo} = \frac{V_{in}/n - V_o}{L_o} \cdot (\frac{2 \cdot n \cdot V_o}{V_{in}} - 1 + D_{loss\_I}) \cdot \frac{T_s}{2} \quad (7)$$

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot D_{loss\_I} \cdot \frac{T_s}{2} \quad (8)$$

In the working mode II, the ripple current on the output filter inductor can be calculated by (9).

$$\Delta i_{Lo} = \frac{V_o}{L_o} \cdot (1 - \frac{2 \cdot n \cdot V_o}{V_{in}}) \cdot \frac{T_s}{2} \quad (9)$$

According to (7), (8), and (9), the output filter inductance under the proposed TPS control strategy can be obtained by (10).

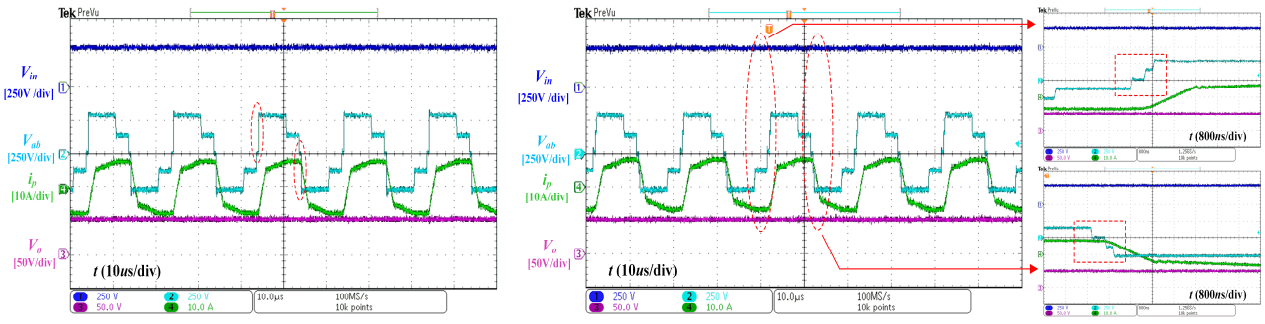
$$L_o = \begin{cases} \dfrac{(\frac{V_{in}}{n} - V_o) \cdot (\frac{2 \cdot n \cdot V_o}{V_{in}} - 1 + D_{loss\_I}) \cdot T_s}{2 \cdot \Delta i_{Lo}} & \text{working mode I } (V_o \geq \frac{V_{in}}{2 \cdot n}) \\ \dfrac{V_o \cdot D_{loss\_I} \cdot T_s}{2 \cdot \Delta i_{Lo}} & \text{working mode I } (V_o < \frac{V_{in}}{2 \cdot n}) \\ \dfrac{V_o \cdot (1 - \frac{2 \cdot n \cdot V_o}{V_{in}}) \cdot T_s}{2 \cdot \Delta i_{Lo}} & \text{working mode II} \end{cases} \quad (10)$$

IV. Experimental Verification

A down-scaled experimental prototype is established to verify the proposed TPS control strategy. The circuit parameters of established experimental prototype are listed in Appendix.

Figs. 5 - 6 show the comparison experimental results between the DPS control strategy and proposed TPS control strategy when the output voltage V_o is 50 V and output power P_o is 1 kW, which include the voltages V_{in}, V_{ab}, V_o and current i_p. From Figs. 5 - 6, it can be observed that: 1) the proposed working mode I and II are used for the low input voltage 280 V and high input voltage 420 V respectively, which is consistent with the above theoretical analysis in Section II; 2) the maximum voltage changes on the transformer's primary side in the three-level operation mode of the DPS control strategy is about 280 V as shown in Fig. 5(a), but the maximum voltage changes on the transformer's primary side in the working mode I of the proposed control strategy are reduced to about 140 V as marked in Fig. 5(b); and 3) the maximum voltage changes on the transformer's primary side in the two-level operation mode of the conventional DPS control strategy is about 420 V as shown in Fig. 6(a), but the maximum voltage changes on the transformer's primary side in the working mode II of the proposed control strategy are reduced to about 210 V as marked in Fig. 6(b). Based on the above analysis of 2) and 3), it can be concluded that the maximum voltage changes on the transformer's primary side are about only half of the input voltage ($V_{in}/2$) by using the proposed control strategy.

Figs. 7 - 8 present the experimental results about the voltage harmonics on the transform under the DPS control strategy and proposed control strategy. From Figs. 7(a) and 7(b), it can be observed that: 1) the total harmonic distortion (THD) is 32.53% in the three-level operation mode of the DPS control strategy as marked in Fig. 7(a), but the THD is reduced to 28.35% in the working mode I of the proposed control strategy as marked in Fig. 7(b); 2) the THD is 63.14% in the two-level operation mode of the conventional DPS control strategy as marked in Fig. 8(a), but the THD is reduced to 59.22% in the working mode II of the proposed control strategy as marked in Fig. 8(b); 3) based on 1) and 2), the voltage harmonics on the transformer under the proposed TPS control strategy can be improved by utilizing the three phase-shift delays due to the benefits of the multi-level voltage [16] in comparison with the DPS control strategy.



(a) (b)

Fig. 5. Experimental results (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (a) Three-level operation mode of DPS control strategy. (b) Working mode I of proposed control strategy.

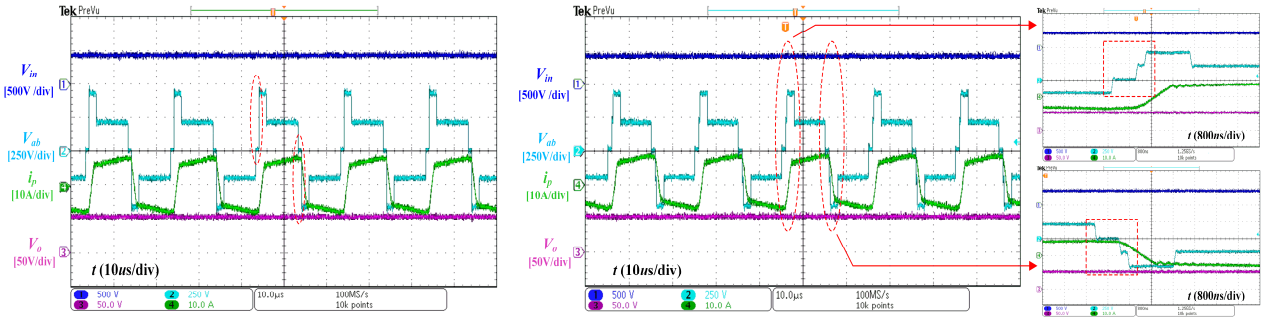


Fig. 6. Experimental results (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW). (a) Two-level operation mode of DPS control strategy. (b) Working mode II of proposed control strategy.

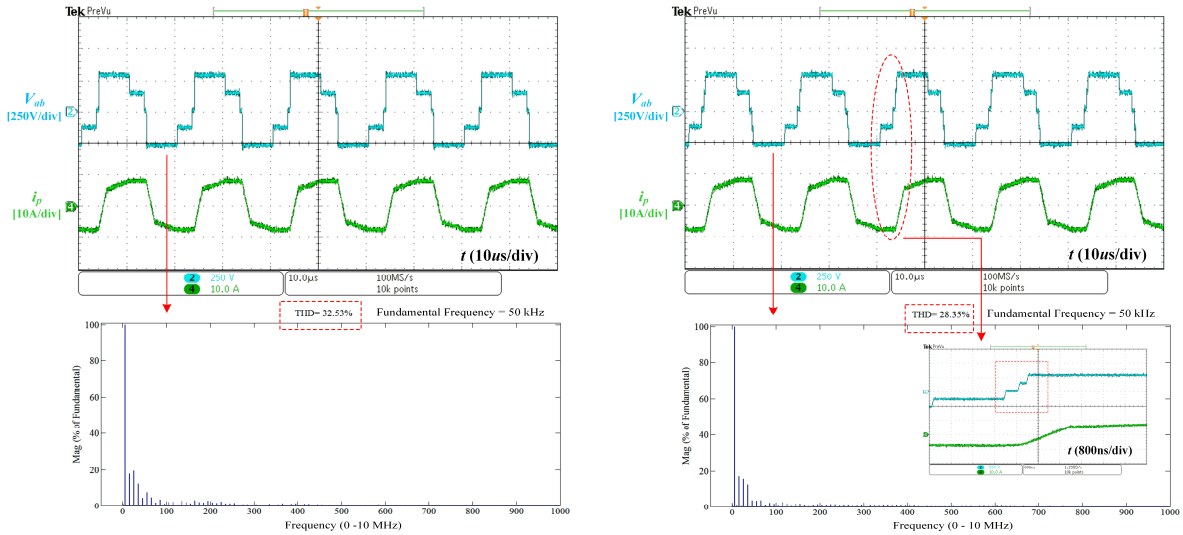


Fig. 7. Experimental analysis about voltage harmonics (V_{in} = 280 V, V_o = 50 V, P_o = 1 kW). (a) Three-level operation mode of DPS control strategy. (b) Working mode I of proposed control strategy.

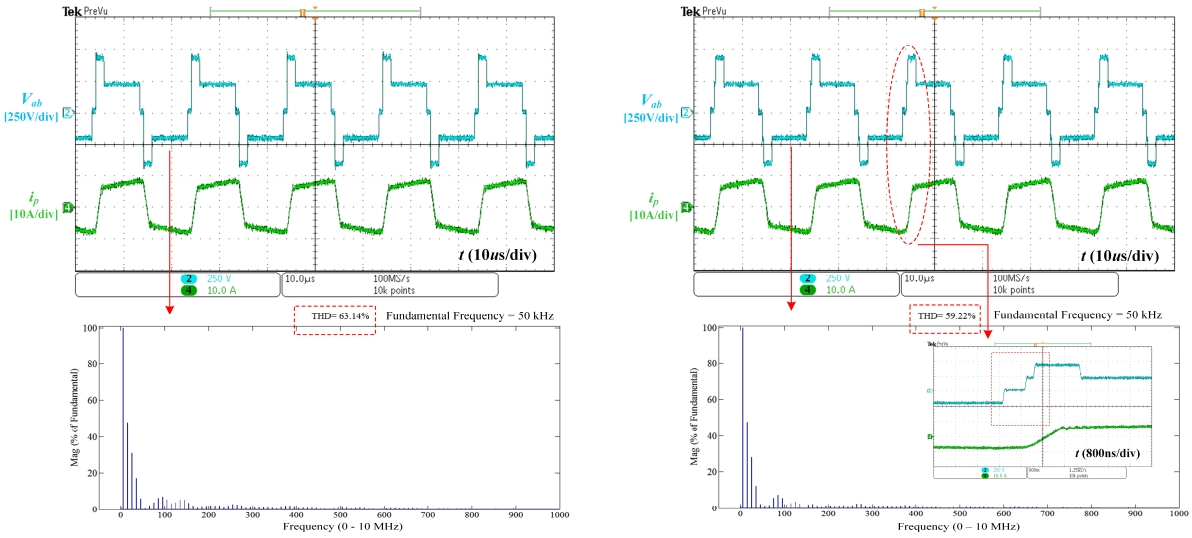


Fig. 8. Experimental analysis about voltage harmonics (V_{in} = 420 V, V_o = 50 V, P_o = 1 kW). (a) Two-level operation mode of DPS control strategy. (b) Working mode II of proposed control strategy.

V. CONCLUSION

This paper proposes a triple-phase-shift (TPS) control strategy for the FBTL DC/DC converter to reduce the transformer's voltage stress. The proposed control strategy includes three phase-shift delays, which can make the voltage changes on the transformer only half of the input voltage (V_{in}/2). Therefore, the proposed control strategy can effectively reduce the voltage change rate (dv/dt), voltage stress, and voltage harmonics on the transformer in comparison with the conventional control strategies. In addition, the proposed control strategy has two working modes to satisfy the wide voltage gain. Finally, the experimental results verify the effectiveness of the proposed TPS control strategy.

APPENDIX

TABLE I. PARAMETERS OF ESTABLISHED EXPERIMENTAL PROTOTYPE

Component	**Description**
Power Switches S_1 - S_4 (D_1 - D_8)	SPW47N60C3
Clamping Diodes D_9 - D_{12}	DSEI30-10AR
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of the Transformer T_r (n : 1)	25 : 8
Leakage Inductance L_r (uH)	47.7
Input Capacitors C_{i1} and C_{i2} (uF)	470
Flying Capacitors C_{s1} and C_{s2} (uF)	100
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Switching Frequency (kHz)	50

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