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# Triple-Phase-Shift Control Strategy for Full-Bridge Three-Level (FBTL) DC/DC Converter 

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#### Abstract

This paper proposes a triple-phase-shift (TPS) control strategy for the full-bridge three-level (FBTL) DC/DC converter to reduce the voltage stress and harmonics on the transformer. The proposed control strategy is composed of three phase-shift delays to keep the maximum voltage changes $(\Delta V)$ on the transformer's primary side at only half of the input voltage ( $V_{i n} / 2$ ), which is different from the conventional control strategies causing the higher voltage changes with value of $V_{i n}$. Therefore, the proposed control strategy can effectively reduce the voltage change rate $(d v / d t)$ and voltage harmonics on the transformer due to the benefits of multi-level voltage produced by the three phase-shift delays. Additionally, the proposed TPS control strategy has two working modes, which can thus have wide voltage gain. Finally, the experimental results are presented to verify the proposed control strategy.


Keywords-full-bridge (FB); phase-shift control; three-level (TL) DC/DC converter; wide voltage gain.

## I. Introduction

Normally, the power electronic converters can be mainly classified into three categories including AC/DC rectifier, DC/AC inverter [1], and DC/DC converter. The DC-DC converters aims to change the voltage levels for the DC applications [2-5]. Among various types of DC/DC converters, three-level (TL) based DC/DC converters are one of most attractive choices for high voltage applications because the voltage stress on the power switches in TL based $\mathrm{DC} / \mathrm{DC}$ converters is only half of the input voltage $\left(V_{\text {in }} / 2\right)$ [68]. Normally, the full-bridge $\mathrm{DC} / \mathrm{DC}$ converter is more suitable for higher power applications [9], [10] in comparison with the half-bridge $\mathrm{DC} / \mathrm{DC}$ converter because of the current stress on the power switches in the full-bridge DC/DC converter is half of that in the half-bridge DC/DC converter. Reference [11] proposed a chopping plus phaseshift (CPS) control strategy for the FBTL DC/DC converter based on the control strategy for the hybrid three-level DC/DC converter in [12]. Furthermore, a double phase-shift (DPS) control strategy for the FBTL DC/DC converter was proposed in [13], which improves the converter's efficiency in comparison with the CPS control strategy. The CPS and DPS control strategies both have the wide voltage gain, but these two control strategies cause the high voltage change rate $(d v / d t)$ on the transformer, which would result in high harmonics on the transformer and large electromagnetic interference. In order to reduce such high voltage change rate $(d v / d t)$ on the transformer, an improved FBTL DC/DC converter with corresponding control strategy was proposed
in [14]. However, a passive filter needs to be added in the transformer's primary side, which would reduce the converter's efficiency and voltage conversion rate. A new double phase-shift control strategy was also proposed in [15] to reduce the high voltage change rate $(d v / d t)$ on the transformer, but this control strategy cannot satisfy the wide input voltage range in comparison with the control strategies [11], [13].

In this paper, a triple-phase-shift (TPS) control strategy is proposed for the FBTL DC/DC converter, which can not only reduce the voltage stress on the transformer but also satisfy the wide input voltage range. Under conventional control strategies, there exist high voltage changes on the transformer, but the proposed control strategy can decrease the maximum voltage changes on the primary side of the transformer to half of the input voltage ( $V_{i n} / 2$ ) by utilizing three phase-shift delays. Therefore, the voltage change rate $(d v / d t)$, voltage stress, and voltage harmonics on the transformer can be effectively reduced by utilizing the proposed control strategy. Additionally, the proposed control strategy includes two working modes to achieve the wide voltage gain. Finally, the experimental results validate the proposed TPS control strategy.

## II. Operation Principle

Fig. 1 presents the structure of FBTL DC/DC converter, in which $C_{i 1}$ and $C_{i 2}$ are two input capacitors; $S_{1}-S_{8}$ and $D_{1}$ $D_{8}$ are power switches and power diodes; $C_{1}-C_{8}$ are parasitic capacitors of $S_{1}-S_{8} ; C_{s 1}$ and $C_{s 2}$ are two flying capacitors; $D_{9}-D_{12}$ are four clamped diodes; $T_{r}$ is the transformer; $L_{r}$ is the leakage inductor of the transformer $T_{r}$; $D_{r 1}-D_{r 4}$ are four output rectifier diodes; $L_{o}$ and $C_{o}$ are output filter inductor and capacitor, respectively. In Fig. 1, $V_{1}$ and $V_{2}$ are voltages on $C_{i 1}$ and $C_{i 2}$, respectively; $V_{i n}$ is the input voltage; $V_{a b}$ is the voltage between point $a$ and $b ; i_{p}$ is the primary current of the transformer $T_{r} ; i_{L o}$ is the current flowing through the output filter inductor $L_{o} ; V_{o}$ and $I_{o}$ are the output voltage and output current; $n$ is the turns ratio of the transformer $T_{r}$.

In addition, some assumptions are made to simplify the following analysis: 1) $S_{1}-S_{8}$ and $D_{1}-D_{12}$ are ideal switches and diodes; 2) $C_{i 1}, C_{i 2}$ are large enough to be considered as constant voltage sources with the value of the half of input voltage $\left.\left(V_{i n} / 2\right) ; 3\right) L_{o}$ is large enough to be regarded as a constant current source; 4) $C_{s 1}$ and $C_{s 2}$ are larg enough to be considered as two voltage sources with the values of $V_{i n} / 2$
and only provide charging and discharging paths for the switches' parasitic capacitors.


Fig. 1. FBTL DC/DC converter.

## A. Proposed TPS Strategy

The proposed TPS control strategy includes three phaseshift delays and has two working modes to satisfy the wide input voltage range. Figs. 2(a) and (b) present the working mode I and II of the proposed strategy respectively, in which $d_{r v 1}-d_{r v 8}$ are driving signals of switches $S_{1}-S_{8} ; \alpha_{1}, \alpha_{2}$, and $\alpha_{3}$ are three phase-shift delays.

- Working mode $I$ is utilized for the low input voltage. In the working mode I, $\alpha_{1}-\alpha_{2}$ and $\alpha_{3}$ are both kept constant as highlighted in Fig. 2(a); and the output voltage $V_{o}$ is controlled by adjusting $\alpha_{1}$. By adjusting the value of $\alpha_{1}$, the time length of third-level voltages ( $V_{i n}$ and $-V_{i n}$ ) as marked by red color in Fig. 2(a) would be changed, which can thus adjust the output voltage $V_{o}$. For instance, if increasing $\alpha_{1}$, the time length of the third-level voltages ( $V_{i n}$ and $-V_{i n}$ ) would decrease, which means that the output voltage $V_{o}$ would decrease.
- Working mode II is utilized for the high input voltage when $\alpha_{1}$ reaches to its maximum value. The output voltage $V_{o}$ is controlled by adjusting $\alpha_{2}$. By adjusting the value of $\alpha_{2}$, the time length of second-level voltage ( $V_{i n} / 2$ and $-V_{i n} / 2$ ) as marked by blue color in Fig. 2(b) would be changed, which can thus adjust the output voltage $V_{o}$. For instance, if decreasing $\alpha_{2}$, the time length of the second-level voltages ( $V_{i n} / 2$ and $V_{\text {in }} / 2$ ) would decrease, which means that the output voltage $V_{o}$ would decrease.

(a)

(b)

Fig. 2. Main waveforms. (a) Working mode I. (b) Working mode II.
From Fig. 2, it can be observed that the maximum voltage changes on the transformer's primary side in the two working modes are both kept at half of the input voltage $\left(V_{i n} / 2\right)$ by utilizing the three phase-shift delays.

## B. Working Mode I

The operation principle of half cycle in the working mode I (shown in Fig. 2(a)) is analyzed as below. Fig. 3 presents four selected equivalent circuits in the working mode I. The other equivalent circuits can be derived according to the operation analysis below, which are not repeated here.

Stage 1 [before $t_{1}$ ]: In this period, $S_{1}, S_{2}, S_{7}$, and $S_{8}$ are all on, so $V_{a b}$ is $V_{i n}$ and the input power transfers to the load from $D_{r 1}$ and $D_{r 4}$. In this stage, the primary current of the transformer $i_{\mathrm{p}}$ is $I_{0} / n$.

Stage $2\left[t_{1}-t_{2}\right]$ : At $t_{1}, S_{1}$ is switched off, then the output current $I_{0}$ is reflected to the primary side, which means $i_{p}$ is still $I_{o} / n$ to charge $C_{1}$ and discharge $C_{4}$ via $C_{s 1}$. Accordingly, $V_{c 1}$ increases and $V_{c 4}$ decreases linearly.

Stage $3\left[t_{2}-t_{3}\right]$ : At $t_{2}, V_{c 1}$ increases to $V_{i n} / 2$ and $D_{9}$ conducts, clamping $V_{c 4}$ at 0 V . Therefore, $S_{4}$ would be switched on with zero-voltage. In this stage, $V_{a b}$ is $V_{i n} / 2$ and $i_{\mathrm{p}}$ remains $I_{o} / n$.

Stage $4\left[t_{3}-t_{4}\right]$ : At $t_{3}, S_{8}$ is switched off; $i_{p}$ maintains at $I_{o} / n$ to charge $C_{8}$ and discharge $C_{5}$ via $C_{s 2}$. $V_{c 8}$ increases and $V_{c 5}$ decreases linearly.

Stage $5\left[t_{4}-t_{5}\right]$ : At $t_{4}, V_{c 8}$ increases to $V_{i n} / 2$ and $V_{c 5}$ decreases to 0 V . Then $D_{12}$ conducts, clamping the voltages of $S_{5}$ at 0 V . Accordingly, $S_{5}$ would be switched on with zero-voltage. In this stage, $V_{a b}$ is 0 V and $i_{p}$ is $I_{o} / n$.

Stage $6\left[t_{5}-t_{6}\right]$ : At $t_{5}, S_{2}$ is switched off. Then $C_{2}$ is charged and $C_{3}$ is discharged; $V_{a b}$ changes to negative. The current $i_{p}$ starts to decrease and is not enough to provide output current $I_{o}$, so the output rectifier diodes $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V . Accordingly, the voltage on $L_{r}$ is $V_{a b}$. In this stage, $L_{r}$ resonates with $C_{2}$ and $C_{3}$.

Stage $7\left[t_{6}-t_{7}\right]$ : At $t_{6}, V_{c 2}$ increases to $V_{i n} / 2 ; V_{c 3}$ decreases to $0 \mathrm{~V} ; V_{a b}$ decreases to $-V_{i n} / 2$. Then $D_{3}$ conducts,
clamping the voltage of $S_{3}$ at 0 V , so $S_{3}$ can be switched on with zero-voltage. Because $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ still keep conducting, the voltage on $L_{r}$ is $-V_{i n} / 2$, thus $i_{p}$ decreases linearly.

Stage $8\left[t_{7}-t_{8}\right]$ : At $t_{7}, S_{7}$ is switched off; $C_{7}$ is charged and $C_{6}$ is discharged; $V_{a b}$ starts to decrease from $-V_{i n} / 2$. In this stage, $i_{\mathrm{p}}$ continues to decrease because $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ still conducts, clamping the primary and secondary voltage of the transformer at 0 V . In this stage, $L_{r}$ resonates with $C_{6}$ and $C_{7}$.

Stage $9\left[t_{8}-t_{9}\right]$ : At $t_{8}$, the voltage of $S_{7}$ is $V_{i n} / 2$ and $D_{6}$ conducts, clamping the voltage of the switch $S_{6}$ at 0 V . Accordingly, $S_{6}$ would be switched on with zero-voltage.


Fig. 3. Selected equivalent circuits in working mode I.

## C. Working Mode II

The operation principle of half cycle in the working mode II (shown in Fig. 2(b)) is analyzed as below. Fig. 4 presents four selected equivalent circuits in the working mode II. The other equivalent circuits can be derived according to the operation analysis below, which are not repeated here.

Stage 1 [before $t_{1}$ ]: In this period, although $S_{1}, S_{2}, S_{7}$, and $S_{8}$ are all on-state, the primary current $i_{p}$ is not enough to provide $I_{o}$ and increases linearly. Therefore, $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ conduct simultaneously, clamping the primary and secondary voltage at 0 V . The primary current $i_{p}$ increases linearly.

Stage $2\left[t_{1}-t_{2}\right]$ : At $t_{1}, S_{1}$ is switched off. The primary current $i_{p}$ charges $C_{1}$ and discharges $C_{4}$ via $C_{s 1}$. Therefore, $V_{c 1}$ increases and $V_{c 4}$ decreases.

Stage $3\left[t_{2}-t_{3}\right]$ : At $t_{2}, V_{c 1}$ increases to $V_{i n} / 2, V_{c 4}$ decreases to 0 V , and $D_{9}$ conducts, clamping $V_{c 4}$ at 0 V . Therefore, $S_{4}$ can be switched on with zero-voltage. In this stage, $V_{a b}$ is $V_{i n} / 2$ and $i_{\mathrm{p}}$ still increases linearly.
$D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ keep conducting. In this stage, the voltage on $L_{r}$ is $-V_{i n}$, thus $i_{p}$ decreases linearly.

Stage $10\left[t_{9}-t_{10}\right]$ : At $t_{9}, i_{p}$ decreases to 0 A , then the current direction of $i_{p}$ changes. The voltage on $L_{r}$ maintains $V_{i n}$, so $i_{p}$ remains decreasing linearly.

Stage $11\left[t_{10}-t_{11}\right]$ : At $t_{10}, i_{p}$ decreases to $-I_{o} / n$ (the negative reflected output current). Then, $D_{r 1}, D_{r 4}$ are switched off, and $D_{r 2}, D_{r 3}$ is utilized to transfer the input power to load.

At $t_{11}, S_{4}$ is switched off. The second half cycle [ $t_{11}-t_{21}$ ] starts. The following analysis is similar to the first half cycle [ $t_{1}-t_{11}$ ], which is not repeated here.


Stage $4\left[t_{3}-t_{4}\right]$ : At $t_{3}, i_{p}$ increases to $I_{o} / n$ (the positive reflected output current). Then $D_{r 2}$ and $D_{r 3}$ are switched off, and then $D_{r 1}$ and $D_{r 4}$ are utilized to transfer the input power to load.

Stage $5\left[t_{4}-t_{5}\right]$ : At $t_{4}, S_{8}$ is switched off. Then $I_{0}$ is reflected to the primary side, $i_{p}$ is still $I_{o} / n$ to charge $C_{8}$ and discharge $C_{5}$ via the flying capacitor $C_{s 2} . V_{c 8}$ increases linearly, and $V_{c 5}$ decreases linearly.

Stage $6\left[t_{5}-t_{6}\right]$ : At $t_{5}, V_{c 8}$ increases to $V_{i n} / 2, V_{c 5}$ decreases to 0 V , and $D_{12}$ conducts, clamping $V_{c 5}$ at 0 V . Therefore, $S_{5}$ would be switched on with zero-voltage. In this stage, $V_{a b}$ is 0 V and $i_{\mathrm{p}}$ remains the positive reflected output current $I_{o} / n$.

Stage $7\left[t_{6}-t_{7}\right]$ : At $t_{6}, S_{2}$ is switched off. Then $C_{2}$ is charged and $\mathrm{C}_{3}$ is discharged; $V_{a b}$ changes to negative. The current $i_{p}$ starts to decrease and is not enough to provide $I_{o}$, so $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ conduct simultaneously, clamping the primary and secondary voltage at 0 V . Thus, the voltage on $L_{r}$ is $V_{a b}$. In this stage, $L_{r}$ resonates with $C_{2}$ and $C_{3}$.

Stage $8\left[t_{7}-t_{8}\right]$ : At $t_{7}, V_{c 2}$ increases to $V_{i n} / 2 ; V_{c 3}$ decreases to 0 V ; and $V_{a b}$ decreases to $-V_{i n} / 2$. Then, $D_{3}$
conducts, clamping the voltage of $S_{3}$ at 0 V , so $S_{3}$ can be switched on with zero-voltage. Because $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ keep conducting, the voltage on $L_{r}$ is $-V_{i n} / 2$, so $i_{p}$ decreases linearly.

Stage $9\left[t_{8}-t_{9}\right]$ : At $t_{8}, S_{7}$ is switched off; $C_{7}$ is charged and $C_{6}$ is discharged; $V_{a b}$ starts to decrease from $-V_{i n} / 2$. In this stage, $i_{\mathrm{p}}$ remain decreasing and $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ still conduct, clamping both the primary and secondary voltage of the transformer at 0 V . In this stage, $L_{r}$ resonates with $C_{6}$ and $C_{7}$.


Fig. 4. Selected equivalent circuits in working mode II.

## III. Characteristic and Performance Analysis

## A. Duty Cycle Loss

In the working mode I as shown in Fig. 2(a), the time periods $\left[t_{5}-t_{10}\right]$ and $\left[t_{15}-t_{20}\right]$ are the time of duty cycle losses in one switching period. If neglecting the quite short time periods $\left[t_{5}-t_{6}\right]$ and $\left[t_{7}-t_{8}\right]$, the two time periods $\left[t_{5}-t_{10}\right]$ and [ $t_{15}-t_{20}$ ] can be given by (1).

$$
\begin{equation*}
t_{10}-t_{5}=t_{20}-t_{15}=\frac{\alpha_{3}}{2}+\frac{2 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n}} \tag{1}
\end{equation*}
$$

Based on (1), the duty cycle loss in one switching period in the working mode I namely $D_{\text {loss }_{-} I}$ can be calculated by (2).

$$
\begin{equation*}
D_{\text {loss }-I}=\frac{\left(t_{10}-t_{s}\right)+\left(t_{20}-t_{15}\right)}{T_{s}}=\frac{\alpha_{3}}{T_{s}}+\frac{4 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n} \cdot T_{s}} \tag{2}
\end{equation*}
$$

In the working mode II as shown in Fig. 2(b), the time of duty cycle losses are $\left[t_{6}-t_{13}\right]$ and $\left[t_{16}-t_{23}\right]$ in one switching period. If neglecting the quite short time periods $\left[t_{6}-t_{7}\right],\left[t_{8}-\right.$ $\left.t_{9}\right]$, and $\left[t_{11}-t_{12}\right]$, the two time periods $\left[t_{6}-t_{13}\right]$ and $\left[t_{16}-t_{23}\right]$ are the same and can be given by (3).

Stage $10\left[t_{9}-t_{10}\right]$ : At $t_{9}, V_{c 7}$ increases to $V_{i n} / 2, V_{c 7}$ decreases to 0 V , and $D_{6}$ conducts, clamping the voltage of $S_{6}$ at 0 V , thus $S_{6}$ would be switched on with zero-voltage. $D_{r 1}, D_{r 2}, D_{r 3}$, and $D_{r 4}$ keep conducting, thus the voltage on $L_{r}$ is $-V_{i n}$ and $i_{p}$ decreases linearly.

Stage $11\left[t_{10}-t_{11}\right]$ : At $t_{10}, i_{p}$ decreases to 0 A , then the current direction of $i_{p}$ changes. The voltage on $L_{r}$ is still $-V_{i n}$, so $i_{p}$ remains decreasing linearly.

At $t_{11}, S_{4}$ is switched off. The second half cycle $\left[t_{11}-t_{21}\right]$ starts. The following analysis is similar to the first half cycle [ $t_{1}-t_{11}$ ], which is not repeated here.


$$
\begin{equation*}
t_{13}-t_{6}=t_{23}-t_{16}=\alpha_{1}+\alpha_{3}+\frac{4 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n}}-\frac{T_{s}}{2} \tag{3}
\end{equation*}
$$

Based on (3), the duty cycle loss in one switching period in the working mode II namely $D_{\text {loss_II }}$ can be calculated by (4).

$$
\begin{equation*}
D_{\text {lass_II }}=\frac{\left(t_{13}-t_{6}\right)+\left(t_{23}-t_{16}\right)}{T_{s}}=\frac{2 \cdot\left(\alpha_{1}+\alpha_{3}\right)}{T_{s}}+\frac{8 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n} \cdot T_{s}}-1 \tag{4}
\end{equation*}
$$

## B. Output Characteristic

In the practical operations, the duty cycle loss would affect the output voltage. Therefore, the average output voltage in the working mode I namely $V_{o_{-} I}$ can be calculated by (5) when considering the duty cycle loss (2).

$$
\begin{align*}
V_{o_{-} I} & =\frac{V_{\text {in }}}{n} \cdot\left(1-\frac{2 \cdot \alpha_{1}}{T_{s}}-D_{\text {loss }_{-} I}\right)+\frac{V_{\text {in }}}{2 \cdot n} \cdot \frac{2 \cdot \alpha_{2}}{T_{s}} \\
& =\frac{V_{i n}}{n} \cdot\left(1-\frac{2 \cdot \alpha_{1}}{T_{s}}-\frac{\alpha_{3}}{T_{s}}+\frac{\alpha_{2}}{T_{s}}-\frac{4 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n} \cdot T_{s}}\right) \tag{5}
\end{align*}
$$

Considering the duty cycle loss (4), the average output voltage in the working mode II namely $V_{o_{-} I I}$ can be calculated by (6).

$$
\begin{align*}
V_{o_{-} I I} & =\frac{V_{i n}}{2 \cdot n} \cdot\left(1+\frac{2 \cdot \alpha_{2}-2 \cdot \alpha_{1}}{T_{s}}-D_{\text {loss }_{-} I I}\right)  \tag{6}\\
& =\frac{V_{i n}}{n} \cdot\left(1+\frac{\alpha_{2}}{T_{s}}-\frac{\alpha_{3}}{T_{s}}-\frac{2 \cdot \alpha_{1}}{T_{s}}-\frac{4 \cdot L_{r} \cdot I_{o}}{n \cdot V_{i n} \cdot T_{s}}\right)
\end{align*}
$$

## C. Output Filter Inductor

In the working mode I, there are two working operations that $V_{o} \geq V_{i n} / 2 n$ and $V_{o}<V_{i n} / 2 n$.

If $V_{o} \geq V_{i n} / 2 n$, the ripple current on the output filter inductor namely $\Delta i_{L o}$ can be calculated by (7). If $V_{o}<V_{i n} / 2 n$, the ripple current on the output filter inductor can be calculated by (8).

$$
\begin{gather*}
\Delta i_{t o}=\frac{V_{i n} / n-V_{o}}{L_{o}} \cdot\left(\frac{2 \cdot n \cdot V_{o}}{V_{i n}}-1+D_{\text {loss }-I}\right) \cdot \frac{T_{s}}{2}  \tag{7}\\
\Delta i_{L_{o}}=\frac{V_{o}}{L_{o}} \cdot D_{\operatorname{loss}-I} \cdot \frac{T_{s}}{2} \tag{8}
\end{gather*}
$$

In the working mode II, the ripple current on the output filter inductor can be calculated by (9).

$$
\begin{equation*}
\Delta i_{L o}=\frac{V_{o}}{L_{o}} \cdot\left(1-\frac{2 \cdot n \cdot V_{o}}{V_{i n}}\right) \cdot \frac{T_{s}}{2} \tag{9}
\end{equation*}
$$

According to (7), (8), and (9), the output filter inductance under the proposed TPS control strategy can be obtained by (10).

$$
L_{o}= \begin{cases}\frac{\left(\frac{V_{\text {in }}}{n}-V_{o}\right) \cdot\left(\frac{2 \cdot n \cdot V_{o}}{V_{i n}}-1+D_{\text {loss }_{-} I}\right) \cdot T_{s}}{2 \cdot \Delta i_{L o}} & \text { working mode } \mathrm{I}\left(\mathrm{~V}_{\mathrm{o}} \geq \frac{V_{\text {in }}}{2 \cdot n}\right) \\ \frac{V_{o} \cdot D_{\text {loss }-I} \cdot T_{s}}{2 \cdot \Delta i_{L o}} & \text { working mode } \mathrm{I}\left(\mathrm{~V}_{\mathrm{o}}<\frac{V_{\text {in }}}{2 \cdot n}\right) \\ \frac{V_{o} \cdot\left(1-\frac{2 \cdot n \cdot V_{o}}{V_{\text {in }}}\right) \cdot T_{S}}{2 \cdot \Delta i_{L o}} & \text { working mode II }\end{cases}
$$

## IV. Experimental Verification

A down-scaled experimental prototype is established to verify the proposed TPS control strategy. The circuit
parameters of established experimental prototype are listed in Appendix.

Figs. 5-6 show the comparison experimental results between the DPS control strategy and proposed TPS control strategy when the output voltage $V_{o}$ is 50 V and output power $P_{o}$ is 1 kW , which include the voltages $V_{i n}, V_{a b}, V_{o}$ and current $i_{p}$. From Figs. 5-6, it can be observed that: 1) the proposed working mode I and II are used for the low input voltage 280 V and high input voltage 420 V respectively, which is consistent with the above theoretical analysis in Section II; 2) the maximum voltage changes on the transformer's primary side in the three-level operation mode of the DPS control strategy is about 280 V as shown in Fig. 5(a), but the maximum voltage changes on the transformer's primary side in the working mode I of the proposed control strategy are reduced to about 140 V as marked in Fig. 5(b); and 3) the maximum voltage changes on the transformer's primary side in the two-level operation mode of the conventional DPS control strategy is about 420 V as shown in Fig. 6(a), but the maximum voltage changes on the transformer's primary side in the working mode II of the proposed control strategy are reduced to about 210 V as marked in Fig. 6(b). Based on the above analysis of 2) and 3), it can be concluded that the maximum voltage changes on the transformer's primary side are about only half of the input voltage $\left(V_{i n} / 2\right)$ by using the proposed control strategy.

Figs. 7-8 present the experimental results about the voltage harmonics on the transform under the DPS control strategy and proposed control strategy. From Figs. 7(a) and 7(b), it can be observed that: 1) the total harmonic distortion (THD) is $32.53 \%$ in the three-level operation mode of the DPS control strategy as marked in Fig. 7(a), but the THD is reduced to $28.35 \%$ in the working mode I of the proposed control strategy as marked in Fig. 7(b); 2) the THD is $63.14 \%$ in the two-level operation mode of the conventional DPS control strategy as marked in Fig. 8(a), but the THD is reduced to $59.22 \%$ in the working mode II of the proposed control strategy as marked in Fig. 8(b); 3) based on 1) and 2), the voltage harmonics on the transformer under the proposed TPS control strategy can be improved by utilizing the three phase-shift delays due to the benefits of the multi-level voltage [16] in comparison with the DPS control strategy.


Fig. 5. Experimental results ( $V_{i n}=280 \mathrm{~V}, V_{o}=50 \mathrm{~V}, P_{o}=1 \mathrm{~kW}$ ). (a) Three-level operation mode of DPS control strategy. (b) Working mode I of proposed control strategy.


Fig. 6. Experimental results ( $V_{i n}=420 \mathrm{~V}, V_{o}=50 \mathrm{~V}, P_{o}=1 \mathrm{~kW}$ ). (a) Two-level operation mode of DPS control strategy. (b) Working mode II of proposed control strategy.


Fig. 7. Experimental analysis about voltage harmonics ( $V_{i n}=280 \mathrm{~V}, V_{o}=50 \mathrm{~V}, P_{o}=1 \mathrm{~kW}$ ). (a) Three-level operation mode of DPS control strategy. (b) Working mode I of proposed control strategy.


Fig. 8. Experimental analysis about voltage harmonics ( $V_{i n}=420 \mathrm{~V}, V_{o}=50 \mathrm{~V}, P_{o}=1 \mathrm{~kW}$ ). (a) Two-level operation mode of DPS control strategy. (b) Working mode II of proposed control strategy.

## V. CONCLUSION

This paper proposes a triple-phase-shift (TPS) control strategy for the FBTL DC/DC converter to reduce the transformer's voltage stress. The proposed control strategy includes three phase-shift delays, which can make the voltage changes on the transformer only half of the input voltage ( $V_{i n} / 2$ ). Therefore, the proposed control strategy can effectively reduce the voltage change rate $(d v / d t)$, voltage stress, and voltage harmonics on the transformer in comparison with the conventional control strategies. In addition, the proposed control strategy has two working modes to satisfy the wide voltage gain. Finally, the experimental results verify the effectiveness of the proposed TPS control strategy.

## Appendix

TABLE I. PARAMETERS OF ESTABLISHED EXPERIMENTAL PROTOTYPE

| Component | Description |
| :--- | :--- |
| Power Switches $S_{1}-S_{4}\left(D_{1}-D_{8}\right)$ | SPW47N60C3 |
| Clamping Diodes $D_{9}-D_{12}$ | DSEI30-10AR |
| Rectifier Diodes $D_{r 1}-D_{r 4}$ | MBR40250TG |
| Turns Ratio of the Transformer $T_{r}(n: 1)$ | $25: 8$ |
| Leakage Inductance $L_{r}(u \mathrm{H})$ | 47.7 |
| Input Capacitors $C_{i 1}$ and $C_{i 2}(u \mathrm{~F})$ | 470 |
| Flying Capacitors $C_{s 1}$ and $C_{s 2}(u \mathrm{~F})$ | 100 |
| Output Filter Capacitor $C_{o}(u \mathrm{~F})$ | 470 |
| Output Filter Inductor $L_{o}(u \mathrm{H})$ | 140 |
| Switching Frequency $(\mathrm{kHz})$ | 50 |

## References

[1] R. Xu, Y. Yu, R. F. Yang, and G. L. Wang, "A novel control method for transformerless H -Bridge cascaded STATCOM with star configuration," IEEE Trans. on Power Electron., vol. 30, no. 3, pp. 1189-1202, Mar. 2015.
[2] S. Hou, J. Chen, T. Sun, and X. Bi, "Multi-input Step-Up Converters Based on the Switched-Diode-Capacitor Voltage Accumulator", IEEE Trans. Power Electron., vol.31, no.1, pp. 381-393, Jan. 2016.
[3] D. Liu, Y. Wang, F. Deng, Q. Zhang, and Z. Chen, "Zero-voltage switching full-bridge T-type DC/DC converter with wide input
voltage range and balanced switch currents," IEEE Trans. on Power Electron., Early Access, DOI: 10.1109/TPEL.2018.2800902.
[4] X. Guo, D. Sha, Y. Xu, and X. Liao, "Hybrid-bridge-based DAB converter with voltage match control for wide voltage Conversion Gain Application," IEEE Trans. on Power Electron., vol. 33, no. 2, pp. 1378-1388, Feb. 2018.
[5] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high frequency isolated bidirectional full-bridge dc-dc converter: comprehensive theoretical analysis and experimental verification," IEEE Trans. on Power Electron., vol. 29, no. 4, pp. 1667-1680, Apr. 2014.
[6] D. Liu, F. Deng; Z. Gong, and Z. Chen, "Input-parallel output-parallel (IPOP) three-level (TL) DC/DC converters with interleaving control strategy for minimizing and balancing capacitor ripple currents," IEEE Journal of Emerging and Selected Topics in Power Electron., vol. 5, no. 3, pp. 1122-1132, Sep. 2017.
[7] D. Liu, F. Deng, and Z. Chen, "Five-level active-neutral-pointclamped DC/DC converter for medium voltage DC grids," IEEE Trans. on Power Electron., vol. 32, no. 5, pp. 3402-3412, May. 2017.
[8] D. Liu, F. Deng, Q. Zhang, and Z. Chen, "Periodically swapping modulation (PSM) strategy for three-level (TL) DC/DC Converter with Balanced Switch Currents," IEEE Trans. on Industrial Electron., vol. 65, no. 1, pp. 412-423, Jan. 2018.
[9] H. Bai, A. Taylor, W. Guo, G. Szatmari-Voicu, N. Wang, J. Patterson, and J. Kane, "Design of an 11 kW power factor correction and 10 kW ZVS DC/DC converter for a high-efficiency battery charger in electric vehicles", IET Power Electron., vol. 5, no. 9, pp. 1714-1722, Nov. 2012.
[10] I.-O. Lee and G. W. Moon, "Soft-Switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage applications," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 112122, Jan. 2013.
[11] Z. Zhang and X. Ruan, "Zero-voltage-switching PWM full-bridge three-level converter", in Proc. 4th Int. Power Electron. Motion Control Conf., Xi'an, China, Aug. 2004, pp. 1085-1090.
[12] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter", IEEE Trans. Power Electron., vol. 20, no. 2, pp. 395-404, Mar. 2015.
[13] Z. Zhang and X. Ruan, "A novel double phase-shift control scheme for full-bridge three-level converter", in Proc. 20th Annu. IEEE Appl. Power Electron. Conf. Expos., Austin, USA, Mar. 2005, pp. 12401245.
[14] F. Deng and Z. Chen, "Control of improved full-bridge three-level DC/DC converter for wind turbines in a DC grid", IEEE Trans. Power Electron., vol. 28, no. 1, pp. 314-324, May. 2012.
[15] D. Liu, F. Deng, and Z. Chen, "A double phase-shift control strategy for a full-bridge three-level DC/DC converter", in Proc. IECON Conf, Florence, Italy, Oct. 2016, pp. 1202-1207.
[16] C. Sun, J. Zhang, X. Cai, and G. Shi, "Analysis and arm voltage control of isolated modular multilevel DC-DC converter with asymmetric branch impedance", IEEE Trans. Power Electron., vol. 32, no. 8, pp. 5978-5990, Aug. 2017.

