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An Improved Stray Capacitance Model for Inductors

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***Abstract*—This paper proposes an improved analytical stray capacitance model for inductors. It considers the capacitances between the winding and the central limb, side limb, and yoke of the core. The latter two account for a significant proportion of the total capacitance with the increase of the core window utilization factor. The potential of the floating core/shield is derived analytically, which enables the model to apply not only for the grounded core/shield, but also for the floating core/shield cases. Based on the improved model, an analytical optimization method for the stray capacitance in inductors is proposed. Moreover, a global Pareto optimization is carried out to identify the trade-offs between the stray capacitance and ac resistance in the winding design. Finally, the analysis and design are verified by finite element method (FEM) simulations and experimental results on a 100 kHz dual active bridge (DAB) converter.**

***Index Terms*—Inductor, Stray capacitance, Core/shield-related capacitance, Optimization, Dual active bridge converter.**

I. Introduction

The stray capacitance of inductors arises more and more attention with the increasing operation frequency of power electronic converters. It changes the impedance of inductors significantly in the high-frequency range and therefore limits their operation frequency. It also leads to an inrush charging current and high-frequency oscillations in the circuit, which results in higher EMI and lower efficiency [1]. For instance, the realization of zero-voltage switching (ZVS) turn on of MOSFETs requires a certain amount of switching current to charge/discharge the output capacitances of MOSFETs within the deadtime interval [2]. However, it also leads to high-frequency current oscillations due to the parasitic capacitance. Therefore, an analytical stray capacitance model of inductors is essential to limiting its impact by design of the parasitics.

A typical equivalent circuit model of the inductor consists of the inductance L, stray capacitance $C_{\rm ind}$, equivalent magnetic loss resistance $R_{\rm p}$, and equivalent ac resistance $R_{\rm s}$, as illustrated in Fig. 1(a). An accurate model of the stray capacitance $C_{\rm ind}$ requires solving the capacitance network, which includes the capacitance for the intra-winding $C_{\rm wwT}$ and the capacitance between the winding and core/shield $C_{\rm cwT}$, as shown in Fig. 1(b). There is mature research on the analytical models of $C_{\rm wwT}$ of the single-layer windings [3–5], multi-layer and multi-section windings [6, 7], and multiple windings of the transformer or EMI chokes [8–13]. In [14], a detailed review is conducted to compare them.

The models in [5, 8–12] do not consider the core/shield-related capacitance $C_{\rm cwT}$, which is valid when the distance between the winding and core/shield is long enough. In other cases, e.g., when the winding winds directly on the core [3, 4, 15], or the area of the core window is limited and the winding utilization factor is high [16, 17], or in planar magnetics the winding is not only very close but also has the large facing area to the core [18], $C_{\rm cwT}$ makes a considerable contribution to the total capacitance. Moreover, the shield-related capacitance could be significant due to the large facing area between the winding and shield. For instance, the flux band is wrapped around the magnetics to reduce the stray flux and shield the electromagnetic interference (EMI); and the Faraday shield is inserted between the primary and secondary windings to suppress the capacitive coupling in the insulation transformer. Those common practices add the shield-related capacitance to the total stray capacitance.

The finite element method (FEM) is usually with a higher accuracy compared to analytical models, especially for complex winding and core configurations. A 2D FEM model is used in [19] to obtain a lumped note-to-node capacitance network, including the capacitance between the winding and core. The 3D FEM model proposed in [20] results in a better field distribution and more accurate solution compared to the 2D FEM model. The analytical model, on the other hand, is time-efficient and suitable for the model-based design and optimization. A recent advance in [5] gives an analytical model through the curve fitting of a set of FEM simulations of the standard cells. The intra-winding capacitance of the single layer air core inductance is calculated. It shows a significant error reduction compared to the field-analysis-based analytical results, and is extendable to multi-layer winding structures. However, there is no systematic research on the analytical modeling of core/shield-related capacitance $C_{\rm cwT}$. Four further issues need to be overcome:

a) How to extract the equivalent capacitance $C_{\rm ind}$ with a floating core/shield? Generally, there are three methods to solve $C_{\rm ind}$ from a capacitance network. Firstly, if the core or shield is grounded, its voltage potential $U_{\rm c}$ is known, and $C_{\rm ind}$ is obtained through the energy method [7, 21]. Secondly, if the core or shield is floating, $U_{\rm c}$ and the total energy are then unknown. However, the circuit analysis can be used if the structure is two-directional symmetrical [3, 4, 15]. For instance, in Fig. 1(b), the cross-section of the inductor is naturally symmetrical with axis $\xi 1$. If the number of layers p is 1, the two end ports of the winding have the identical position with each other and have an additional symmetry axis

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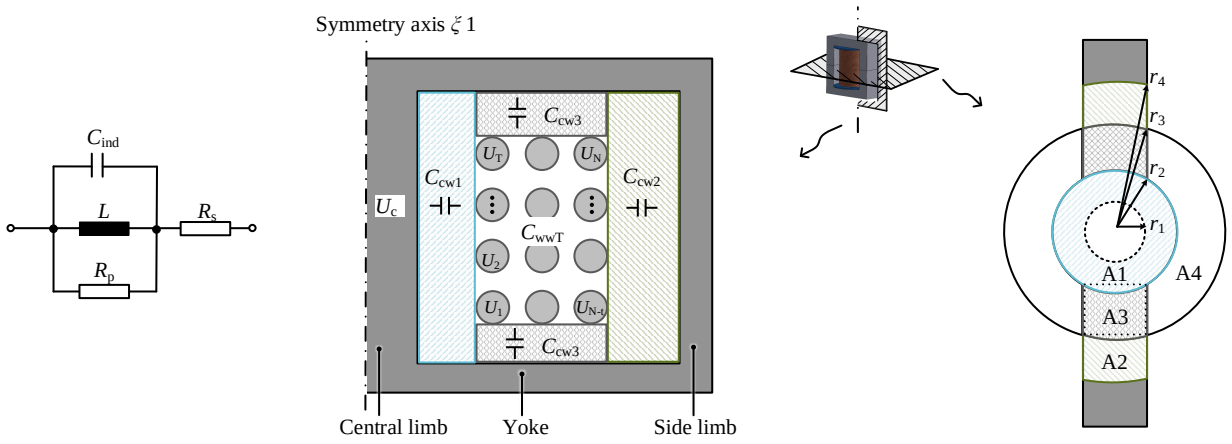


(a) Equivalent circuit model.

(b) The cross section of an ETD core inductor. C_{cw1}, C_{cw2}, C_{cw3}, and C_{wwT} are the central-limb, side limb, yoke, and intra-winding capacitance, respectively, the former three C_{cwi} constitute the core-related capacitance C_{cwT}.

(c) The top view with the corresponding energy storage area: A1 to A4. C_{cw1}, C_{cw2}, C_{cw3}, and C_{wwT} are related to area A1, A2, A3, and A4, respectively.

Fig. 1. Stray capacitance model of an inductor: the equivalent circuit model and the capacitance distribution in a detailed structure.

$\xi 2$. U_c is then located in the middle of the potential of the two ports U_1 and U_N, which is $(U_1 + U_N)/2$. C_{ind} is then solved using the circuit analysis method. Exceptions are in [16, 17], where the circuit analysis is performed for the asymmetrical structure by neglecting the intra-winding capacitance C_{wwT}. If the number of layers p is larger than 1, the second symmetry axis disappears. U_c of the floating core is unknown and the circuit analysis method is not applicable anymore. The third method in [18] uses the electric field decomposition (EFD) and energy approach in two four-step-procedures to extract the capacitance network. It is further improved with the semi-analytical method based on multi-layered Green's function to deal with irregular and asymmetrical structure. This method is specifically for the planar transformers and not directly applicable to winded winding magnetics. The total capacitance network is considered and programs are used to solve the matrix due to its complexity. Another contribution of [18] is that the potential of the floating core is determined in a specific case when one conductor is 1V and others are 0V. However, a general expression for the potential of the floating core with an arbitrary voltage distribution in the winding is still missing. Until now, there is no general closed-form equation predicting the capacitance of floating magnetics.

b) Are the existing models for the core/shield-related capacitance C_{cwT} integrity? In [7, 21], only the central-core/shield capacitance C_{cw1} is considered. In reality, the side limb and yoke also surround the winding and contribute to the total stray capacitance with C_{cw2} and C_{cw3}, respectively, as illustrated in Fig. 1(b). In [22], the six-capacitance-network is extracted considering the tank surrounding the winding in all directions. However, it is for transformers and difficult to be applied for inductors. The tank is grounded, so its voltage potential is known, and an analytical solution is derived based on the energy method. Moreover, the winding capacitance is neglected due to its small contribution, which is not the case for inductors.

c) In which scenarios should the core/shield-related capacitance C_{cwT} be considered and how can the application criteria be quantified?

d) How to optimize the winding design in terms of its capacitance and ac resistance? Compared with the ac resistance optimization [23–26], there is not much research on the optimization of winding capacitance, as it is usually performed by changing the layer insulation distance directly or employing different winding structures [1, 27]. A systematic method to reduce or control the total capacitance for the winding optimization is still missing.

To address the aforementioned four issues, this paper develops an analytical formula for the parasitic capacitance of inductors considering the core/shield capacitance, and proposes a method for winding optimization. The derived formula is generic which considers the side limb and yoke capacitance. The potential of the core/shield is derived analytically, which enables the equation applicable to core/shield regardless of grounded or floating. The formula itself is in closed-form, and the application criteria are simple. The ETD, P shape cores, and flux bands are used for the case studies, and the formula can be extended to other core/shield structures. The core-related capacitance C_{cwT} is also extracted in both finite element simulation (FEM) and experimental results, which are in well agreement with the proposed model. Based on the model, an analytical optimization method is proposed to reduce the winding capacitance to the minimum. By changing the position and layer insulation thickness of the winding, C_{cwT} of existing inductors can be reduced without affecting other parameters, such as the ac resistance. Finally, a winding design flow is presented for the optimization of ac resistance and capacitance, and it is applied in a case study of the inductor in a dual active bridge (DAB) converter.

Our previous conference publication in [28] proposes the core-related capacitance formula and the winding optimization method of the inductor. This paper is an expansion of it by adding the analytical solution for the potential of the core/shield, the shield-related capacitance, the criteria

to determine core/shield-related capacitance, the analytical capacitance optimization, and case studies with experimental verifications. The rest of the paper is organized as follows. In Section II, the analytical expression of the stray capacitance of inductors is derived. The detailed constitution of core/shield-related capacitance is verified in Section III and the criteria to determine it are given in Section IV. In Section V, an analytical capacitance optimization method is proposed. Combined with the ac resistance optimization, the Pareto optimization for the winding is also presented. Section VI provides a case study for the winding design of the inductor in a dual active bridge converter. The proposed formula and optimization procedure reduce the current ringing and improve the system efficiency. Finally, conclusions are drawn in Section VII.

II. Winding Stray Capacitance Modeling

A. General Equations

There are four kinds of stray capacitances in an inductor: the intra-winding capacitance C_{ww} and three capacitances between the winding and the different core parts, i.e., central limb capacitance C_{cw1}, side limb capacitance C_{cw2}, and top and bottom yoke capacitance C_{cw3}. Multiplied by each coefficients k_{ww}, k_{cw1}, k_{cw2}, and k_{cw3}, the product of the first item is the winding capacitance C_{wwT}, and the sum of the latter three products is the core-related capacitance C_{cwT}. Adding them together, the total capacitance of the inductor C_{ind} seen from the two ports of winding is obtained:

$$\begin{aligned} C_{\mathrm{ind}} &= \underbrace{k_{\mathrm{ww}} \cdot C_{\mathrm{ww}}}_{C_{\mathrm{wwT}}} + \underbrace{k_{\mathrm{cw1}} \cdot C_{\mathrm{cw1}} + k_{\mathrm{cw2}} \cdot C_{\mathrm{cw2}} + k_{\mathrm{cw3}} \cdot C_{\mathrm{cw3}}}_{C_{\mathrm{cwT}}}, \\ &= \sum k_x \cdot C_x, \\ x &= \mathrm{ww},\ \mathrm{cw1}, \mathrm{cw2} \text{ and } \mathrm{cw3}, \end{aligned} \tag{1}$$

where C_x is inherent capacitances including C_{ww} and $C_{\mathrm{cw}i}$, k_x is potential coefficient including k_{ww} and $k_{\mathrm{cw}i}$. In the following, the expressions of each part are derived. All the equations are summarized in Fig. 2 with specific parameter definitions. Moreover, those equations are also applicable to the shield-to-winding capacitance.

B. Inherent Capacitances

Generally, the static capacitance reflects the capability of the structure to store the electrical field energy. The well-known capacitance models for the parallel plate and coaxial cylindrical are [29]:

$$\begin{aligned} C_x &= \begin{cases} \alpha_x \cdot \varepsilon_0 \varepsilon_x \frac{A_x}{d_x} = \alpha_x \cdot \varepsilon_0 \varepsilon_x \frac{2\pi h_x r_x}{d_x}, \\ \alpha_x \cdot \varepsilon_0 \varepsilon_x \frac{2\pi h_x}{\ln\left(1+\frac{d_x}{r_x}\right)}, \end{cases} \\ x &= \mathrm{ww},\ \mathrm{cw1}, \mathrm{cw2} \text{ and } \mathrm{cw3}, \end{aligned} \tag{2}$$

where ε_0 and ε_x are the vacuum and relative permittivity, respectively, h_x and r_x are the height and radius of the structure, respectively, A_x is the area of the plate, d_x is the effective distance between the two plates or cylinders, α_{cw} is the weighting factor. (2) can model the inherent capacitance in inductors by assuming that the winding is winded in order and the facing plate or cylinder is smooth [14].

1) Intra-winding Capacitance C_{ww}: The modeling of the intra-winding capacitance C_{ww} uses (2) and is given as [7, 14, 30]:

$$\begin{aligned} &\alpha_{\mathrm{ww}} = 1, \quad h_{\mathrm{ww}} = t \cdot d_{\mathrm{e}}, \quad d_{\mathrm{ww}} = d_{\mathrm{eff}}, \\ &r_{\mathrm{ww}} = l_{\mathrm{MLT}}/(2\pi), \quad \varepsilon_{\mathrm{ww}} = \frac{\varepsilon_{\mathrm{wire}} \varepsilon_{\mathrm{t}} a_{\mathrm{iso}}}{\varepsilon_{\mathrm{wire}} \delta_{\mathrm{t}} + 2\varepsilon_{\mathrm{t}} \delta_{\mathrm{wire}}}, \end{aligned} \tag{3}$$

where d_{eff} is the effective distance between layers, for orthogonal winding:

$$d_{\mathrm{eff}} = a_{\mathrm{iso}} - 0.15 d_{\mathrm{i}} + 0.26(h_{\mathrm{iso}} + d_{\mathrm{i}}), \tag{4}$$

for orthocylic winding:

$$d_{\mathrm{eff}} = \begin{cases} a_{\mathrm{iso}} - 0.15 d_{\mathrm{i}} + 0.26(h_{\mathrm{iso}} + d_{\mathrm{i}}) & a_{\mathrm{iso}} \geq 2\delta_{\mathrm{wire}} \\ 0.5 a_{\mathrm{iso}} + \frac{\sqrt{a_{\mathrm{iso}}^2 + (h_{\mathrm{iso}} + d_{\mathrm{i}})^2/4}}{2} - 0.65 d_{\mathrm{i}} & \\ \quad +0.26(h_{\mathrm{iso}} + d_{\mathrm{i}}) & a_{\mathrm{iso}} < 2\delta_{\mathrm{wire}} \end{cases} \tag{5}$$

$\varepsilon_{\mathrm{ww}}$ is the effective permittivity of the series connected tape and wire coating. Other parameters are defined in Fig. 2, and are not discussed again here and in the following analysis.

2) Central Limb Capacitance C_{cw1}: The MnZn ferrite has a high relative permittivity above 10^4 in a wide frequency of range [21, 31]. In the electrostatic analysis, the electric field distribution and the capacitance behavior of the high permittivity core are equivalent to a perfect conductor, as proved in [18]. The core is therefore assumed as a perfect conductor in the analytical modeling, following [3, 21]. For NiZn ferrite widely used in radio frequency (RF) applications, the relativity permittivity is below 100. The perfect core assumption becomes weak and the accuracy of the analytical model decreases.

The central limb capacitance C_{cw1} is the capacitance between the first layer of the winding and the central limb. With a bobbin in between, it is regarded as a series connection of the air and bobbin filled capacitance, and is calculated by (2) and:

$$\begin{aligned} &\alpha_{\mathrm{cw1}} = 1, \quad h_{\mathrm{cw1}} = h_c, \quad d_{\mathrm{cw1}} = r_2 - r_1 + d_{\mathrm{e}}/2, \\ &r_{\mathrm{cw1}} = r_1 + d_{\mathrm{cw1}}/2, \quad \varepsilon_{\mathrm{cw1}} = \frac{\varepsilon_{\mathrm{a}} \varepsilon_{\mathrm{b}} d_{\mathrm{cw1}}}{\varepsilon_{\mathrm{a}} \delta_{\mathrm{b}} + \varepsilon_{\mathrm{b}} (r_2 - r_1 - \delta_{\mathrm{b}})}, \end{aligned} \tag{6}$$

where h_{cw2} is the height of the window, d_{cw1} is the distance from the inner layer to the core, r_{cw1} is the distance from the symmetrical axis to the middle point of the inner layer and central limb, and $\varepsilon_{\mathrm{cw1}}$ is the equivalent relative permittivity of the air and bobbin.

3) Side Limb Capacitance C_{cw2}: If the number of layers p increases, the outer radius of the winding r_3 is close to the inner radius of side limb core r_4. The side limb capacitance C_{cw2} between them begins to increase and is modeled by (2) and:

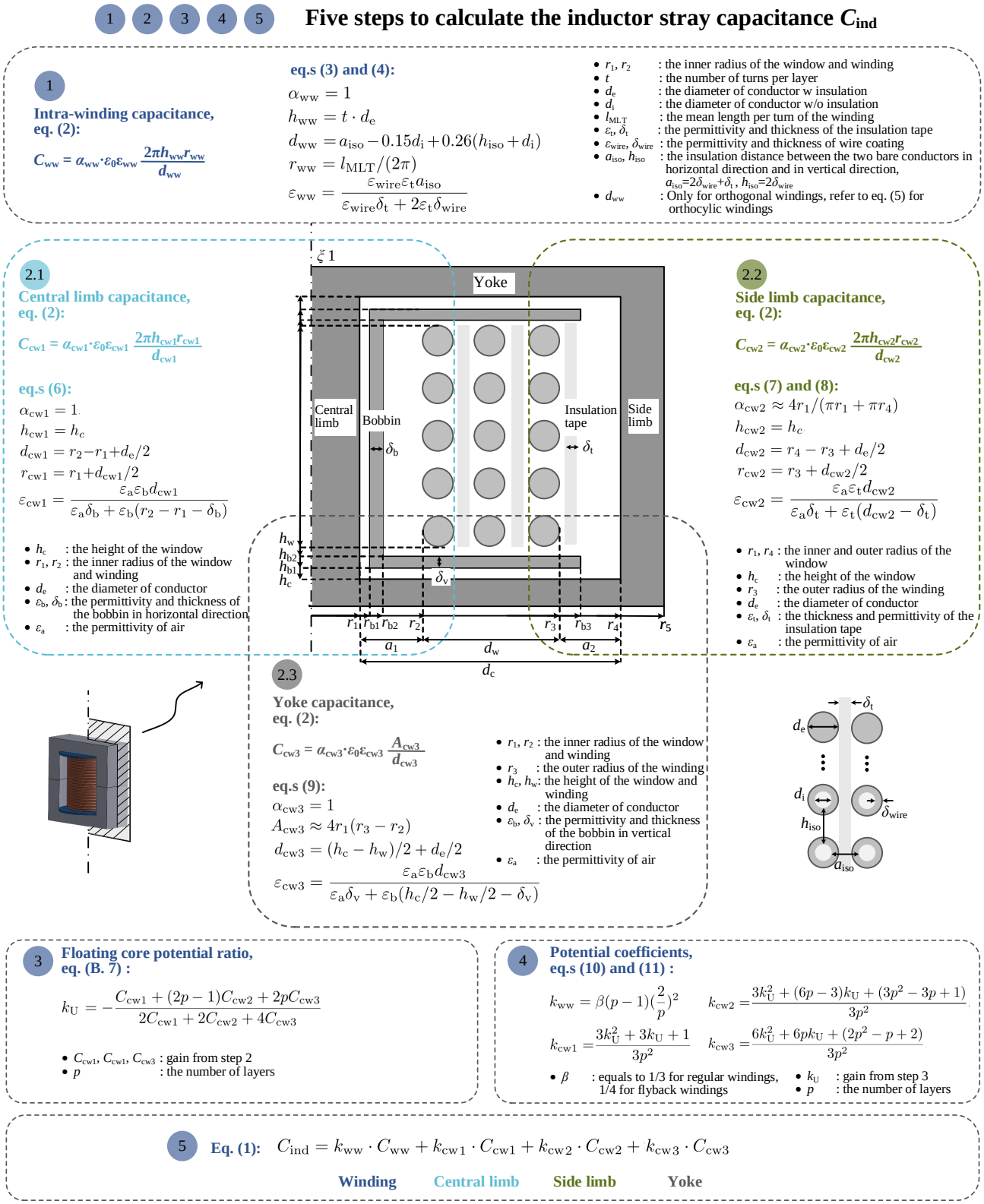


Fig. 2. Five steps to calculate the total inductor stray capacitance C_{ind}, including the intra-winding capacitance C_{ll} (step 1), central limb capacitance C_{cw1} (step 2.1), side limb capacitance C_{cw2} (step 2.2), top and bottom yoke capacitance C_{cw3} (step 2.3), the definition of each quantity is circuited in related box. They are related to the top view of their corresponding energy storage area: A4, A1, A2 and A3 in Fig. 1(c), respectively.

$$h_{\mathrm{cw2}} = h_c, \quad d_{\mathrm{cw2}} = r_4 - r_3 + d_{\mathrm{e}}/2,$$
$$r_{\mathrm{cw2}} = r_3 + d_{\mathrm{cw2}}/2, \quad \varepsilon_{\mathrm{cw2}} = \frac{\varepsilon_{\mathrm{a}}\varepsilon_{\mathrm{t}} d_{\mathrm{cw2}}}{\varepsilon_{\mathrm{a}}\delta_{\mathrm{t}} + \varepsilon_{\mathrm{t}}(d_{\mathrm{cw2}} - \delta_{\mathrm{t}})}, \tag{7}$$

where h_{cw2} is the height of the window, d_{cw2} is the distance from the outer layer to the side limb core, r_{cw2} is from the symmetrical axis to the middle point of the outer layer and side limb. For an ETD core, there is no bobbin between the outer winding and side limb. $\varepsilon_{\mathrm{cw2}}$ is the equivalent permittivity of the air and outside tape. The side limb of the ETD core partially surrounds the winding instead of a full circle, as illustrated in Fig. 1 (c). It is modified by a weighting factor α_{cw2} referring to the ERXP model in [32]:

$$\alpha_{\mathrm{cw2}} \approx 4r_1/(2\pi r_3) \approx 4r_1/(\pi r_1 + \pi r_4). \tag{8}$$

The weighting factor changes according to different core structures.

4) Yoke Capacitance C_{cw3}: The top and bottom yoke capacitance C_{cw3} increases with the number of layers p, and is calculated by (2) and:

$$\alpha_{\mathrm{cw3}} = 1, \quad A_{\mathrm{cw3}} \approx 4r_1(r_3 - r_2),$$
$$d_{\mathrm{cw3}} = (h_{\mathrm{c}} - h_{\mathrm{w}})/2 + d_{\mathrm{e}}/2,$$
$$\varepsilon_{\mathrm{cw3}} = \frac{\varepsilon_{\mathrm{a}}\varepsilon_{\mathrm{b}} d_{\mathrm{cw3}}}{\varepsilon_{\mathrm{a}}\delta_{\mathrm{v}} + \varepsilon_{\mathrm{b}}(h_{\mathrm{c}}/2 - h_{\mathrm{w}}/2 - \delta_{\mathrm{v}})}, \tag{9}$$

where d_{cw3} is the distance from the upper or lower side of the winding to the yoke, A_{cw3} is twice of the area A3 in Fig. 1 (c), and it is approximated by the area in the dot frame with the side length of $2r_1$ and $(r_3 - r_2)$, $\varepsilon_{\mathrm{cw3}}$ is the equivalent permittivity of the air and inserted bobbin yoke.

C. Potential Coefficients

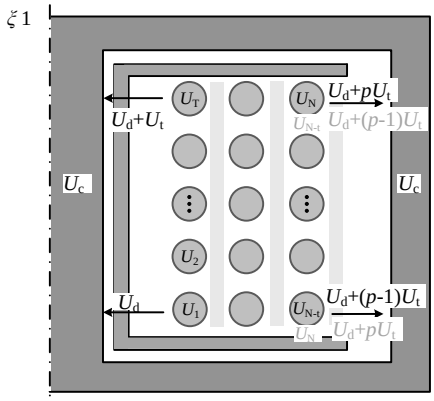
The inherent capacitances (2) are based on the parallel plate and coaxial cylinder model. They are values seen from one layer to another layer or the core, and are with a unity voltage distribution on each electrode. In reality, the capacitance value C_{ind} are seen from the two end ports of the winding as marked U_1 and U_{N} in Fig. 3(a), and the voltage potential is different at each turn of the winding. The potential coefficients k_x transfer the inherent capacitances to C_{ind} and are introduced below.

1) Intra-winding Coefficient k_{ww}: The potential coefficient for connecting the intra-winding capacitance C_{ww} is given as [7, 33]:

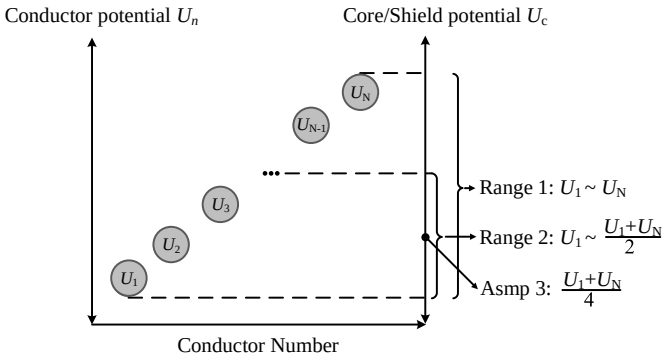
$$k_{\mathrm{ww}} = \beta(p-1)(\frac{2}{p})^2, \tag{10}$$

where β depends on the winding direction. It equals to 1/3 for regular windings, and 1/4 for flyback windings, respectively.

2) Core-related Coefficient $k_{\mathrm{cw}i}$: The core-related coefficient $k_{\mathrm{cw}i}$ is obtained through the energy stored in the winding-core-combined system, and the detailed derivation is given in Appendix A:



(a) Potential distribution in the inductor.



(b) Potential assumptions of the core/shield compared with each turn.

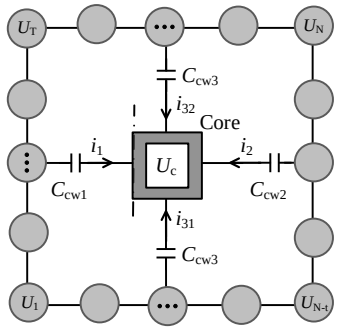
Fig. 3. Assumptions of the potential of core/shield. In (a), the winding is numbered from 1 to N according to the wiring order, the potential of each turn is from U_1 to U_{N}, $U_{\mathrm{t}} = U_{\mathrm{T}} - U_1$ is the voltage difference between the first and last turn in each layer, and U_{c} is the potential of the core. The voltage near the arrow is the voltage difference between the related turn to the core. In (b), Range 1 is the typical range of the core in all cases, Range 2 is based on the assumption that the winding is more close to the central limb than the side limb, Assumption 3 (Asmp 3) is the final simple assumption.

$$k_{\mathrm{cw1}} = \frac{3k_{\mathrm{U}}^2 + 3k_{\mathrm{U}} + 1}{3p^2},$$
$$k_{\mathrm{cw2}} = \frac{3k_{\mathrm{U}}^2 + (6p-3)k_{\mathrm{U}} + (3p^2 - 3p + 1)}{3p^2},$$
$$k_{\mathrm{cw3}} = \frac{6k_{\mathrm{U}}^2 + 6pk_{\mathrm{U}} + (2p^2 - p + 2)}{3p^2},$$
$$\text{or} \quad k_{\mathrm{cw3}} = \frac{6k_{\mathrm{U}}^2 + 6pk_{\mathrm{U}} + (2p^2 - p + 1)}{3p^2}, \tag{11}$$

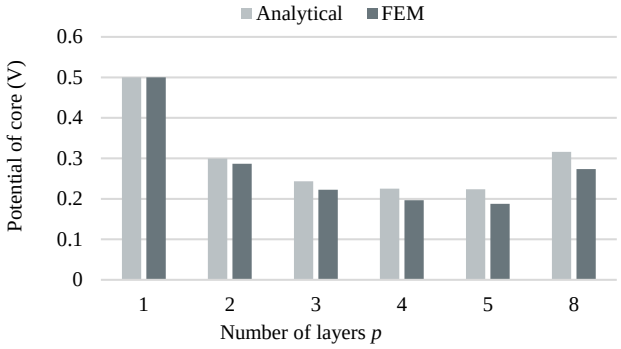
where k_{U} is the voltage ratio defined as $U_{\mathrm{d}}/U_{\mathrm{t}}$, U_{d} is the voltage difference between the first turn and the core $U_{\mathrm{d}} = U_1 - U_{\mathrm{C}}$ in Fig. 3(a). The second k_{cw3} is for the end winding in the different direction, and the voltage potential is illustrated in gray letters. Considering the negligible difference between the two k_{cw3}, only the former one is used below.

D. Potential of the Floating Core/Shield

The assumptions for the relation of the potential between the core and each turn are illustrated in Fig. 3(b). In most power



(a) The equivalent circuit to determine U_c with KCL.



(b) Potential of the core in Prototypes P1 to P8.

Fig. 4. Determination of the potential of core/shield U_c. In (a), the electrical field problem of the winding and core system maps to the electrical circuit problem. U_c is solved by Kirchhoff's Current Law (KCL). In (b), the analytical equation of U_c is verified by finite element method (FEM) simulation results. The simulation is with the same core and winding diameter, but with the different number of layers p in each case. The potential of the first turn U_1 is 0 V, and the last turn U_N is 1 V. In most cases, the potential of the core is around 0.25 V, which verifies Asmp 3 in Fig. 3(b).

TABLE I
PROTOTYPE WINDING SPECIFICATION OF P1 TO P8

Parameters	Value	Units
Core type	ETD 59/31/22	
Core material	N97 (MnZn ferrite)	
Bobbin type	B66398	
Number of layers p	1, 2, 3, 4, 5, 8	
Turns in one layer t	34	
Winding diameter d_i	1	mm

electronic applications, the inductor core is floating, so U_c is between U_1 and U_N. In a normal situation, the winding wraps directly attached to the bobbin, i.e., $r_2 = r_{b2}$, $r_2 - r_1 < r_4 - r_3$. The inner side of the winding is closer to the central limb core than the outer side winding to the side limb. U_c is more closer to the potential of the inner side of the winding due to the smaller distance. Therefore, U_c is limited to $U_1 < U_c < (U_1 + U_N)/2$, and a simple assumption is $(U_1 + U_N)/4$.

The potential of the core is also derived analytically, based on the simplified circuit in Fig. 4(a). With the known voltages of the winding, the potential of the core is calculated with Kirchhoff's Current Law:

$$U_c = U_1 + \frac{C_{cw1} + (2p-1)C_{cw2} + 2pC_{cw3}}{2C_{cw1} + 2C_{cw2} + 4C_{cw3}} U_t, \qquad (12)$$

the detailed derivation is illustrated in Appendix B where k_U is derived as (B.7). The equation is under the assumption that the two pieces of the cores are connected physically and so that electrically. It is valid when the inductor has a gap in the central limb or two gaps in side limbs. When the core has three gaps in all the limbs, the potential of the two pieces of cores are not the same. It can be derived again followed by the process in Appendix B.

A series of inductor prototypes are built and simulated, named P1, P2, P3, P4, P5, and P8 to verify the analytical results. They are with the same configuration except for the number of layers p, as in Table I. The simulation is conducted with the software Finite Element Method Magnetics (FEMM) [34]. It is with the two-dimensional electrostatics field. The axisymmetrical cross section of the inductor in Fig. 2 is used for the simulation, as also shown in Fig. 5 in the case study in the next section. The step-increased voltage from U_1 to U_N is applied to each turn, and the equivalent capacitance is obtained through the stored electrostatic energy W_{sim}:

$$C_{ind} = 2W_{sim}/(U_N - U_1)^2. \qquad (13)$$

Moreover, unlike C_{cw1}, the C_{cw2} and C_{cw3} are not formed by the full circle of winding and core. A coefficient is introduced in the 2D simulation to adjust the permittivity in those regions, as it is applied in [35] to modify the permeability. For region A2 it is expressed as:

$$k_{sim2} = 4r_1/(2\pi r_3), \qquad (14)$$

and for region A3 it is expressed as:

$$k_{sim3} = 4r_1/(\pi r_2 + \pi r_3). \qquad (15)$$

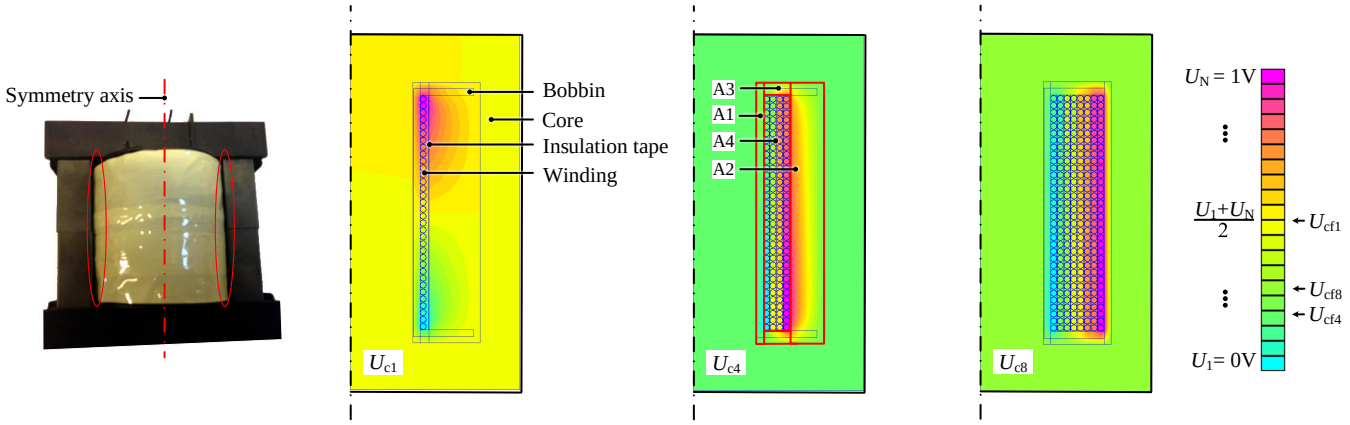
Further, in a FEMM electrostatic field, it is not possible to set up the conductivity. To obtain the electric field which is normal to the core surface, a very high relative permittivity value, i.e., $2 \cdot 10^5$, is set for the core with high conductivity. It introduces a neglectable error as verified in [18].

Their core potentials are compared in Fig. 4(b). When p =1, the contributions of k_{cw2} and k_{cw3} are negligible, the core potential U_c is close to 0.5V, which is in the middle of the two ports. When $p \geq 2$, $U_c \approx 0.25$V even when p = 8, which verifies the Assumption 3 in Fig. 3(b) and the analytical equation (12).

III. MODELING ANALYSIS AND VERIFICATION: TWO CASES STUDIES

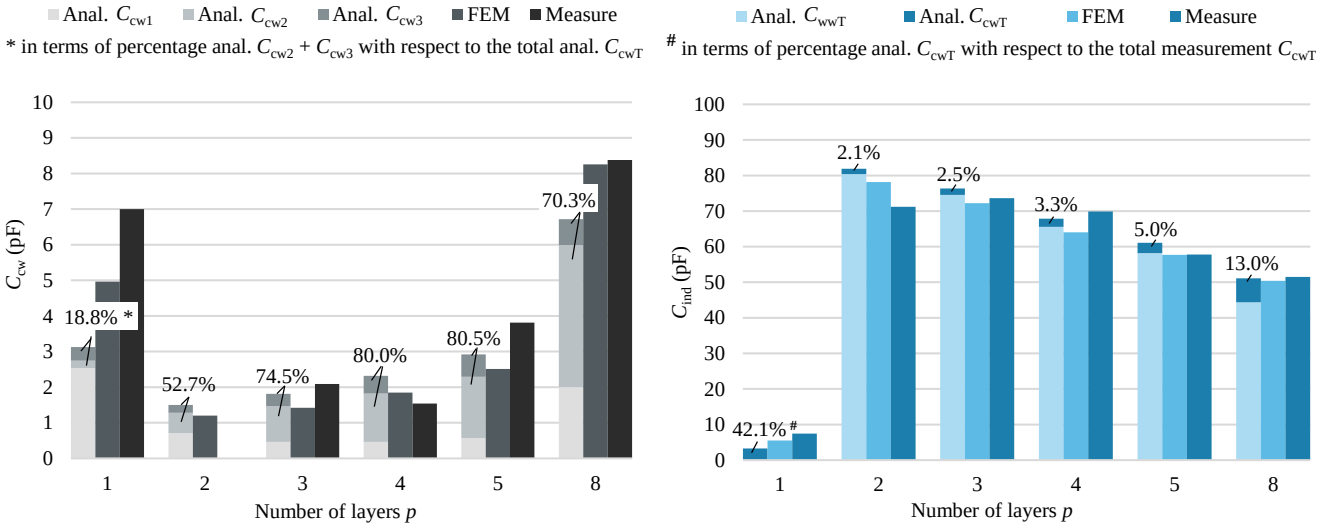
A. Case 1: EE Core Inductor w/o Flux Band

Fig. 5 presents the photo of the prototype P8 and the simulation results of the prototypes P1, P4, and P8. Fig. 6 shows the comparative results of the six prototypes with the number of layers of 1, 2, 3, 4, 5, and 8. The experiment is conducted with the resonant method using a Keysight impedance analyzer E4990A [21, 36]. The total capacitance C_{ind} is measured with



(a) Prototype P8. (b) P1 (p = 1 layer) simulation. (c) P4 (p = 4 layers) simulation. (d) P8 (p = 8 layers) simulation.

Fig. 5. The photo of prototype P8 and simulation results of P1, P4 and P8. (a) is the photo of the P8 and (b), (c), and (d) are the simulation results with 1 layer, 4 layers, and 8 layers, respectively. The color of the related core area indicates the potential of the floating cores U_{c1}, U_{c4}, and U_{c8}, which are very close to the analytical results in Fig. 4(b). A1, A2... Ai are related energy area to calculate C_{cwi} in Fig. 1(c), the permittivity for simulation in A2 and A3 area are modified with (14) and (15), respectively.



(a) Core-related capacitance C_{cw}, floating core. (b) Total capacitance C_{ind}, floating core.

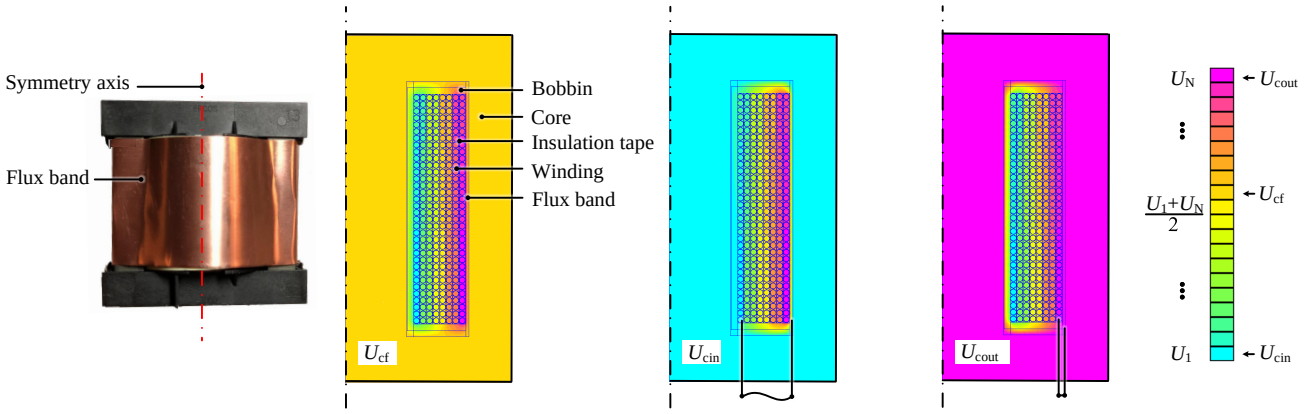
Fig. 6. The analytical, simulation, and experimental results of the capacitance of the inductor with different numbers of layers p in the floating core situation. The percentages in (a) indicate the analytical result of $(C_{\mathrm{cw}2} + C_{\mathrm{cw}3})/C_{\mathrm{cwT}}$ and they are in the two upper bars. The percentages in (b) indicate how much percentage that the analytical C_{cwT} takes of the measurement result.

the core, while the winding capacitance C_{wwT} is measured without the core. The core-related capacitance C_{cwT} is then calculated by subtraction C_{ind} from C_{wwT}.

The Analytical result of $C_{\mathrm{cw}\,i}$, the finite element simulation and measurement results of C_{cwT} for the floating core are illustrated in Fig. 6(a). The errors among them come from three aspects. The first is related to the simplification of the analytical model, which includes the perfect conductive core assumption, the neglection of the turn-to-turn capacitance, etc. In reality, the core is with a finite conductivity and permittivity, and the impact of the grain insulation in the ferrite core should be considered as well [37]. The equivalent circuit of the core is frequency-dependent and is modeled as a complex combination of inductance, capacitance, and resistance in [18, 38]. The electric field induced by the magnetic field stores energy in the core. It is modeled by a parallel capacitance added to the winding ports [39]:

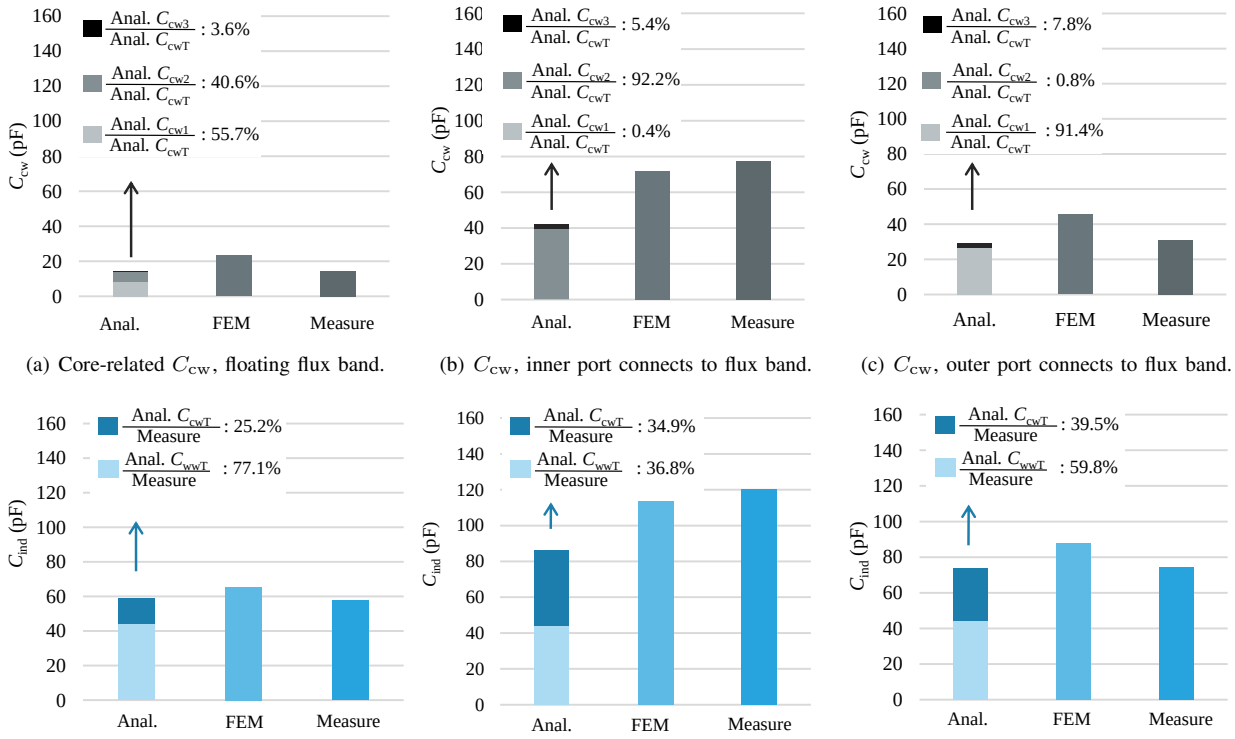
$$C_{\mathrm{core}} = \frac{\varepsilon_{\mathrm{core}}\varepsilon_0}{8\pi N^2}, \tag{16}$$

where l is the magnetic path length, $N = pt$ is the number of turns. The permittivity of a core material $\varepsilon_{\mathrm{core}}$ is difficult to measure and obtain, and it is frequency-dependent. For the N97 MnZn material, the relative permittivity listed in [31] under 100 kHz is approximately $2 \cdot 10^5$. Substituting the geometry parameters of the core into (16), we can obtain the core capacitance C_{core} of the one-layer inductor, which is 8.5 pF. The original analytical equation calculates a value of 3.3 pF, which is 42.1% of the measured value 7.4 pF, as given in Fig. 6. Adding C_{core} to the analytical results leads to



(a) Prototype 8f with flux band. (b) Floating flux band. (c) Inner port connects to flux band. (d) Outer port connects to flux band.

Fig. 7. The photo and simulation results of the prototype P8f. (a) is the photo. (b), (c), and (d) are the simulation results of the inductor with floating flux band, the inner port of the winding connects to the flux band ($U_{\mathrm{cin}} = U_1$), and the outer port connects to the flux band ($U_{\mathrm{cout}} = U_{\mathrm{N}}$), respectively.



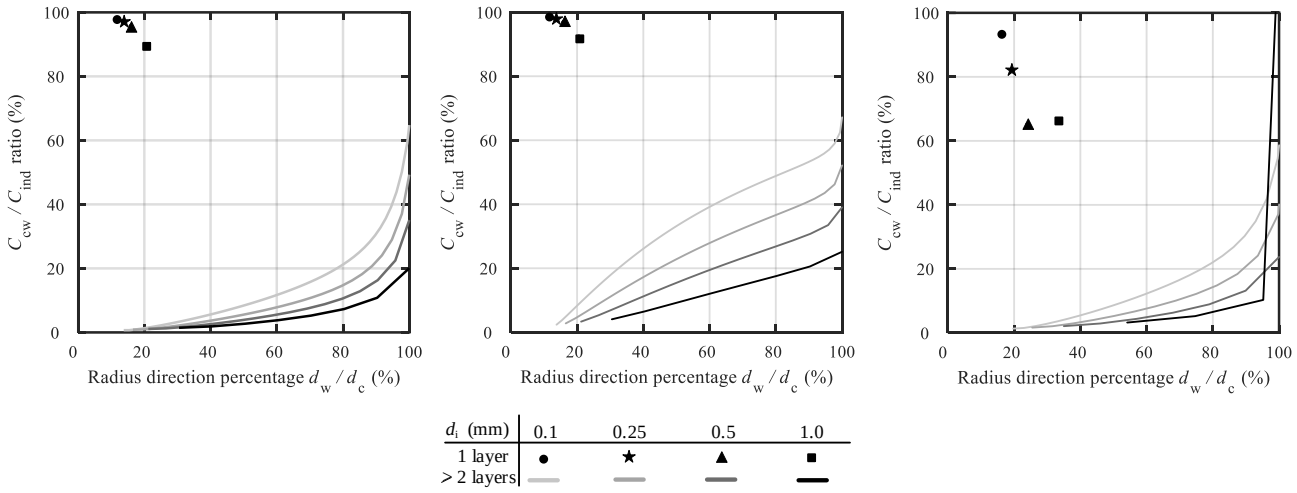
(a) Core-related C_{cw}, floating flux band. (b) C_{cw}, inner port connects to flux band. (c) C_{cw}, outer port connects to flux band.

(d) Total capacitance C_{ind}, floating flux band. (e) C_{ind}, inner port connects to flux band. (f) C_{ind}, outer port connects to flux band.

Fig. 8. The analytical, simulation, and experimental results of the prototype P8f. The percentage in (a), (b) and (c) indicate the analytical result of $C_{\mathrm{cw1}}/C_{\mathrm{cwT}}$ and $C_{\mathrm{cw2}}/C_{\mathrm{cwT}}$ and $C_{\mathrm{cw3}}/C_{\mathrm{cwT}}$, with increasing darker color, respectively. The percentage in (d), (e) and (f) indicate how much percentage that the analytical C_{wwT} and C_{cwT} take of the measurement result, respectively.

11.8 pF, which is 1.6 times the measured capacitance. Thus, the error is still significant with (16). C_{core} decreases dramatically and becomes neglectable with the increased number of layers. The second error stem from the displacement windings, which is the orthocyclic winding with or without insulation tape between layers. Compared to the orthogonal winding as designed, the displacement decreases or increases the intra-winding capacitance C_{ww}, under different permittivity, wire radius and wire coating thickness [40]. Thirdly, the dimension and electrical measurement also contribute errors. The winding wraps directly on the bobbin, $r_2 = r_{\mathrm{b2}}$ and $h_{\mathrm{w}} = h_{\mathrm{b2}}$. The outside diameter of the winding $2r_3$ and the bobbin $2r_{\mathrm{b2}}$, and the height of the bobbin h_{b2} are measured. The insulation distance between the two bare conductors in horizontal direction a_{iso} and in vertical direction h_{iso} are calculated:

$$\begin{aligned} a_{\mathrm{iso}} &= \frac{2r_3 - 2r_{\mathrm{b2}}}{2p} - d_{\mathrm{i}}, \\ h_{\mathrm{iso}} &= \frac{h_{\mathrm{b2}} - d_{\mathrm{i}} - 2\delta_{\mathrm{iso}}}{t-1} - d_{\mathrm{i}}. \end{aligned} \tag{17}$$



(a) ETD 59/31/22 core w/o flux band (b) ETD 59/31/22 core w/ flux band (c) P 30/19 w/o flux band

Fig. 9. The percentage of the core/shield-related to the total inductor capacitance $C_{\rm cw}/C_{\rm ind}$, the x-axis indicates the percentage of the winding width $d_{\rm w}$ to the core width $d_{\rm c}$. (a) is with ETD 59/31/22 core and different winding diameters $d_{\rm i}$ from 0.1 mm to 1.0 mm, (b) is with ETD 59/31/22 core and the flux band covering the winding and core, (c) is with P 30/19 pot-type core.

The equations assume the evenly distributed turn and insulation distance $a_{\rm iso}$ and $h_{\rm iso}$, which are difficult to control especially in the hand-made prototypes. Despite of the three reasons, the errors between the analytical, FEM and experimental results are within a reasonable range. One exception occurs at $p = 2$, the measured capacitance of P2 with the core is even smaller than that without the core, implying that the capacitance decreases after assembling the core. The measurement value is set to be zero there. It is due to the assumption that the core is a perfect conductor, as is introduced above. Nevertheless, the variation of the measured value is the impact of the core circuit, and the affected range is limited.

$C_{\rm cw1}$ is the largest when in the single layer winding. $C_{\rm cw2}$, on the other hand, keeps growing with the number of layers p and dominates $C_{\rm cwT}$ when p is large, despite of a small facing area compared with $C_{\rm cw1}$. $C_{\rm cw3}$ grows stably and becomes significant when $p = 8$. From the comparison of percentage of each $C_{{\rm cw}i}$ with respect to the total core-related capacitance, the conventional core/shield capacitance models in [7, 21] considers the central-limb capacitance $C_{\rm cw1}$ only, and they underestimate the total core-related capacitance. The analytical $C_{\rm wwT}$, $C_{\rm cwT}$, the simulation, and the measurement results of $C_{\rm ind}$ for the floating core are given in Fig. 6(b). $C_{\rm cwT}$ takes almost half with the single layer. It drops when $p = 2$, and then increases with p. Its percentage with respect to the measurement result follows the same trend. Therefore, $C_{\rm cwT}$ is important to be considered with the single layer winding, or when the winding is close to the side limb. It takes 42.1% and 13.0% of the total measurement capacitance in each case, respectively. In other cases, the winding capacitance $C_{\rm wwT}$ is dominant, and it is not necessarily to consider $C_{\rm cwT}$.

B. Case 2: EE Core Inductor w/ Flux Band

The flux band is a conductive shield enclosing the magnetics closely to eliminate the effect of flux leakage and electromagnetic interference. It is either floating or grounded for safety considerations. Prototype P8f with a flux band and its simulation results are given in Fig. 7. Its core and winding configurations are the same with prototype P8 in Table I. The analytical potential of the floating shield is $0.57(U_1 + U_{\rm N})$, which is very close to the simulation results $U_{\rm cf}$ shown in Fig. 7(b). Two cases with the inner or outer port of the winding connected to the shield are also given, and a comparison is illustrated in Fig. 8. $C_{\rm cwT}$ of the floating flux band is the lowest, compared to the case that is connected to the inner or outer port of the winding. In reality, the shield may be grounded, and the core may be stick on the heat sink for cooling and thus is also grounded. The voltage in the total winding changes according to the ac voltage excitation. The potential of the core/shield is then located either between or outside of U_1 and $U_{\rm N}$. The capacitance of the total inductor changes according to the results shown in Figs. 8(c) and (d). So the grounding of the shield increases the dynamic capacitance of the magnetics in those cases.

IV. Criteria to Determine Core/Shield-related Capacitance

To obtain the criteria for whether to consider the core/shield-related capacitance, three cases are analyzed and below. Fig. 9 gives an analytical comparison of $C_{\rm cw}/C_{\rm ind}$ for different cores (ETD 59/31/22 and P 30/19) with or without a flux band. The y-axis is the percentage of core/shield-related capacitance with respect to the total capacitance, while the x-axis is the percentage of the winding width to the core window width, which is proportional to the number of layers p. In all cases for single layer windings, the core/shield-capacitance ratio is above 60%. It drops dramatically when $p \geq 2$ due to the layer capacitance. After that, the capacitance ratio increases to between 20% and 100%. The change trend and range of the capacitance ratio can be extended to other types of cores.

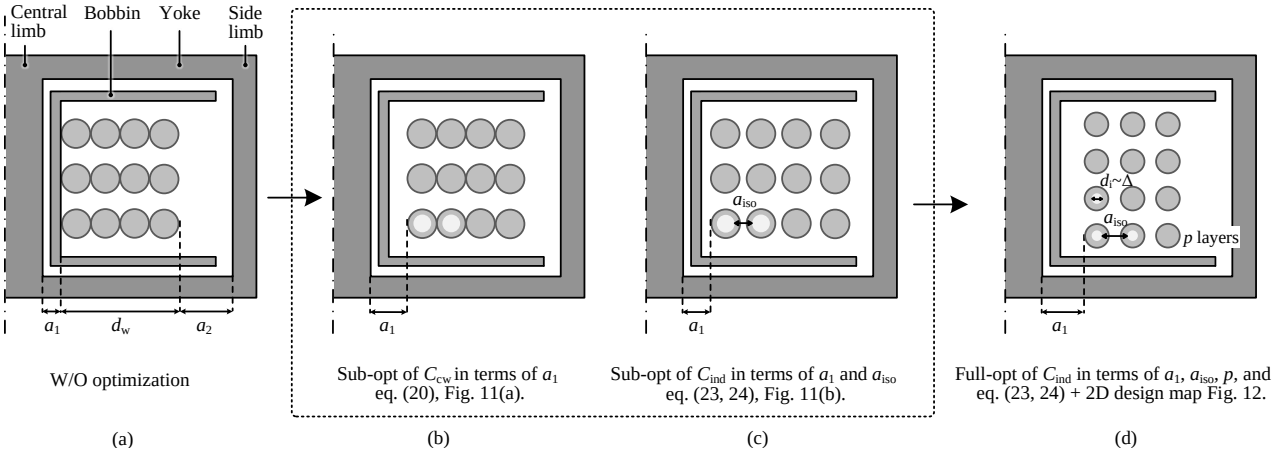


Fig. 10. Comparison of different sub and full-optimizations. The winding without optimization (a) is directly attached to the bobbin, the sub-optimization of $C_{\rm cw}$ (b) moves the overall winding by increase a_1 to gain $(C_{\rm cw})_{\rm min}$, the sub-optimization of $C_{\rm ind}$ (c) changes both a_1 and $a_{\rm iso}$ to gain $(C_{\rm ind})_{\rm min}$ in each (p, $\triangle$) case, the full-optimization (d) changes p, $\triangle$, a_1 and $a_{\rm iso}$ to get the global $(C_{\rm ind})_{\rm min}$, the 2D design map optimization refers to [41].

The side limb of the pot core P 30/19 surrounds the whole winding, which results in a higher capacitance percentage in Fig. 9.(c) than the ETD core in Fig. 9.(a). The high-frequency thinner wire also leads to the capacitance percentage increase.

As can be seen from Fig. 9, when $C_{\rm cw}/C_{\rm ind}$ exceeds 10%, the neglection of the core-related capacitance $C_{\rm cw}$ introduces a significant error when calculating the total stray capacitance $C_{\rm ind}$. Therefore, $C_{\rm cw}/C_{\rm ind} \geq 10\%$ is used as the criteria to consider the core-related capacitance. As a rule of thumb, from Fig. 9, those cases include the inductors:

1) with a single layer winding;
2) with a shield;
3) with a window radius direction percentage $d_{\rm w}/d_{\rm c}$ above 50% for E and P type cores.

V. Optimization of Winding Parasitics

A. Ac Resistance Optimization

To calculate the ac resistance $R_{\rm ac}$ of the round and Litz wire, the analytical model in [42] is used due to its extensibility to the analytical winding optimization [23, 26, 41]. It is:

$$\begin{aligned} R_{\rm ac} =& R_{\rm dc}F_{\rm r} \\ =& R_{\rm dc} \triangle [\frac{\sinh(2\triangle)+\sin(2\triangle)}{\cosh(2\triangle)-\cos(2\triangle)} \\ &+ \frac{2}{3}(p_{\rm Litz}^2-1)\frac{\sinh\triangle-\sin\triangle}{\cosh\triangle+\cos\triangle}], \end{aligned} \tag{18}$$

where:

$$\begin{aligned} &R_{\rm dc} = \frac{4\rho N l_{\rm LMT}}{k\pi d_{\rm Litz}^2}, \qquad p_{\rm Litz} = p\sqrt{k}, \\ &\triangle = (\frac{\pi}{4})^{0.75}\frac{d_{\rm Litz}}{\delta}\sqrt{\frac{t\sqrt{k}d_{\rm Litz}}{h_{\rm c}}}, \end{aligned} \tag{19}$$

$d_{\rm Litz}$ is the strand diameter, k is the number of strands, $p_{\rm Litz}$ is the effective number of strand layers, $F_{\rm r}$ is the ac resistance factor, δ is the skin depth, t is the number of bundles per layer, $h_{\rm c}$ is the winding height, p is the number of layers. If p and the frequency f are decided, there is an optimum winding diameter $d_{\rm i}$ yielding a minimum ac resistance [23, 26]. However, p is difficult to determine at the beginning of winding design. In [41], a design map is used by only taking the total number of turns N as design input instead of p. It is used in this paper for the ac resistance optimization. The detailed procedure is not repeated here due to the focus and page limitation of the paper.

B. Parasitic Capacitance Optimization

Unlike the ac resistance optimization [23–26], there is no analytical method for the optimization of winding capacitance. It is due to the fact that the total capacitance $C_{\rm ind}$ is more structure-dependent and mainly depends on four variables: the number of layer p, penetration ratio $\triangle$, layer insulation distance $a_{\rm iso}$, and winding to central limb distance a_1, where $\triangle = d_{\rm i}/\delta$, $d_{\rm i}$ is the bare diameter of conductor, δ is the skin depth. In the following, three optimization methods are presented and summarized in Fig. 10. They are to minimize the core/shield-related capacitance $C_{\rm cwT}$ in a_1 domain, winding capacitance $C_{\rm ind}$ in (a_1, $a_{\rm iso}$) domain, and $C_{\rm ind}$ in (a_1, $a_{\rm iso}$, p, $\triangle$) domain, respectively.

The first optimization focus on the winding position. Generally, there is no air space between layers except the insulation tape, as the case in Fig. 10(a). The right side endpoint of a_1 is also close to the bobbin radius $r_{\rm b2}$, meaning wrapping the winding on the bobbin directly. However, a careful selection of a_1 is helpful to reduce the core-related capacitance $C_{\rm cwT}$, as shown in Fig. 10(b). If p, $\triangle$, and $a_{\rm iso}$ are fixed, the center limb capacitance $C_{\rm cw1}$ decreases with the increase of a_1, the side limb capacitance $C_{\rm cw2}$ increases with a_1, and the yoke capacitance $C_{\rm cw3}$ keeps stable. So $C_{\rm cwT}$ is a function of a_1: $C_{\rm cwT} = f_1(a_1)$. An optimal a_1 is derived and leads to a minimum $C_{\rm cwT}$:

$$\begin{aligned} a_{1\rm opt} =& \frac{k_2(k_1-d_{\rm e}/2)+2d_{\rm e}k_{\rm cw2}\varepsilon_{\rm cw2}r_1r_{\rm b3}}{k_2-4k_{\rm cw2}\varepsilon_{\rm cw2}r_1r_{\rm b3}} \\ &- \frac{2k_1\sqrt{k_{\rm cw2}\varepsilon_{\rm cw2}r_1r_{\rm b3}k_2}}{k_2-4k_{\rm cw2}\varepsilon_{\rm cw2}r_1r_{\rm b3}}, \end{aligned} \tag{20}$$

with:

$$\begin{aligned} k_1 =& a_{\mathrm{w}} - (p-1)a_{\mathrm{iso}} + d_{\mathrm{e}}, \\ k_2 =& \pi r_{\mathrm{b2}} k_{\mathrm{cw1}} \varepsilon_{\mathrm{cw1}} (r_1 + r_4), \end{aligned} \tag{21}$$

where the relevant parameters are defined in Fig. 2 and 10, $a_{\mathrm{w}} = a_1 + a_2 + (p-1)a_{\mathrm{iso}}$ is the total layer to layer and layer to core insulation distance in horizontal direction. Fig. 11(a) gives a verification of the above optimization formula, where $p = 7$ and $\triangle = 0.2$. The other winding restrictions are the same as in the case given in Table I. A comparison between the iteration result (filled circle) and analytical result with (20) (hollow circle) shows an insignificant difference under different a_{iso} conditions, considering the error introduced by the iteration step and the estimation of $\varepsilon_{\mathrm{cw1}}$, $\varepsilon_{\mathrm{cw2}}$. Besides, a proper a_1 keeps the winding away from the air gap of the core, which helps reducing the additional ac resistance due to the fringing effect [43, 44].

The second optimization assumes fixed p and $\triangle$, and the core-related capacitance C_{cw} is the function of a_1 and a_{iso}: $C_{\mathrm{cw}} = f_3(a_1, a_{\mathrm{iso}})$. The winding capacitance changes with a_{iso}: $C_{\mathrm{wwT}} = f_2(a_{\mathrm{iso}})$, as shown in Fig. 10(c). By combining f_2 and f_3, the total stray capacitance C_{ind} becomes a function of a_1 and a_{iso}:

$$C_{\mathrm{ind}} = f_4(a_1, a_{\mathrm{iso}}). \tag{22}$$

The optimal (a_1, a_{iso}) for a minimum C_{ind} is obtained by solving (22) as a two-variable optimization problem:

$$a_{\mathrm{isoopt}} = \frac{k_3 a_{\mathrm{w}}}{k_3(p-1) + pk_4(1+k_3)}, \tag{23}$$

$$a_{\mathrm{1opt}} = \frac{pk_4 a_{\mathrm{w}}}{k_3(p-1) + pk_4(1+k_3)}, \tag{24}$$

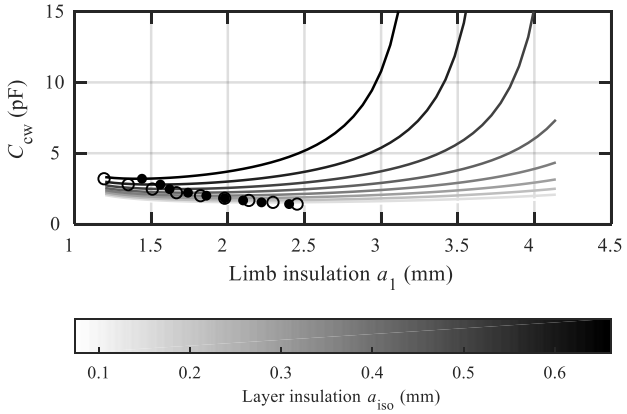
where:

$$\begin{aligned} k_3 =& \sqrt{\frac{4k_{\mathrm{cw2}}\varepsilon_{\mathrm{cw2}} r_{\mathrm{b3}} r_1}{\pi k_{\mathrm{cw1}} \varepsilon_{\mathrm{cw1}} r_{\mathrm{b2}} (r_1 + r_4)}}, \\ k_4 =& \sqrt{\frac{2k_{\mathrm{cw2}}\varepsilon_{\mathrm{cw2}} r_{\mathrm{b3}} r_1 h_{\mathrm{c}}}{\pi \beta \varepsilon_{\mathrm{ww}} h_{\mathrm{w}} (r_1 + r_4)^2}}. \end{aligned} \tag{25}$$

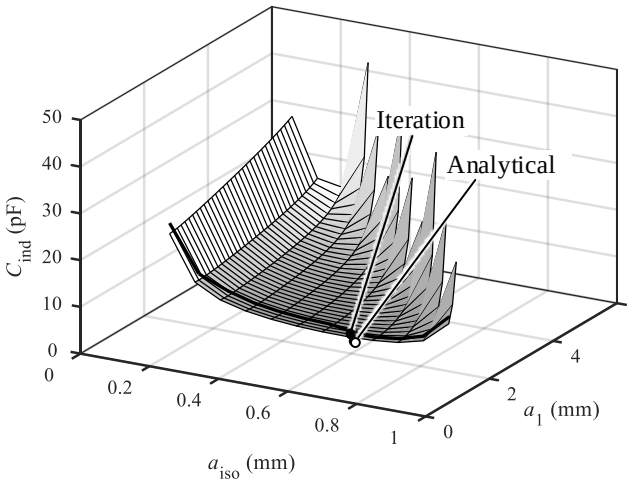
The detailed derivations of (20), (23) and (24) are given in Appendix C and D. With a_{1opt} and a_{isoopt} in (23) and (24), an analytical solution of the minimum C_{ind} can be obtained, as illustrated in Fig. 11(b), where $p = 7$ and $\triangle = 0.2$. The other constructions are the same as these given in Table I. Compared with the iteration result, the analytical (a_{1opt}, a_{isoopt}) point ignores the conductor diameter d_{e} and the slight change of C_{cw3}, and estimates $\varepsilon_{\mathrm{cw1}}$, $\varepsilon_{\mathrm{cw2}}$, $\varepsilon_{\mathrm{cw3}}$ and other structural parameters. In the meanwhile, the accuracy is not affected too much.

The third optimization is the full optimization of all four parameters (p, $\triangle$, a_{1opt}, a_{isoopt}) , as shown in Fig. 10(d). The core window width and height restrictions are:

$$r_{\mathrm{b3}} - r_{\mathrm{b2}} \geqslant pd_{\mathrm{i}} + (p-1)a_{\mathrm{iso}}, \tag{26}$$



(a) Sub-optimization of C_{cw} with a_1, the iteration minimum result is marked with the dark filled circle, and the analytical calculated result with (20) is marked with the hollow circle.



(b) Sub-optimization of C_{ind} versus a_1 and a_{iso}, the iteration minimum result is marked with a dark filled circle, and the analytical calculation result with (23) and (24) is marked with a hollow circle.

Fig. 11. Verification of the two sub-optimizations of the core-related capacitance C_{cw} and total capacitance C_{ind}.

$$h_{\mathrm{b2}} \geqslant td_{\mathrm{i}} + (t-1)h_{\mathrm{iso}}, \tag{27}$$

where the relevant parameters are defined in Fig. 2. Firstly, the (a_{1opt}, a_{isoopt}) in each (p, $\triangle$) case is obtained with the second optimization method. The sub-opt of C_{ind} in each (p, $\triangle$) case is acquired. The four dimensional optimization problem is simplified as a two-dimensional one. Secondly, plot all possible groups of (p, $\triangle$) in the two-dimensional design map. The global minimum capacitance point is therefore obtained with the width and heigh restriction (26,27), as illustrated in Fig. 12.

C. Pareto Optimization Considering Ac Resistance and Parasitic Capacitance

An overall winding design flow considering the ac resistance and capacitance is performed through the Pareto optimization,

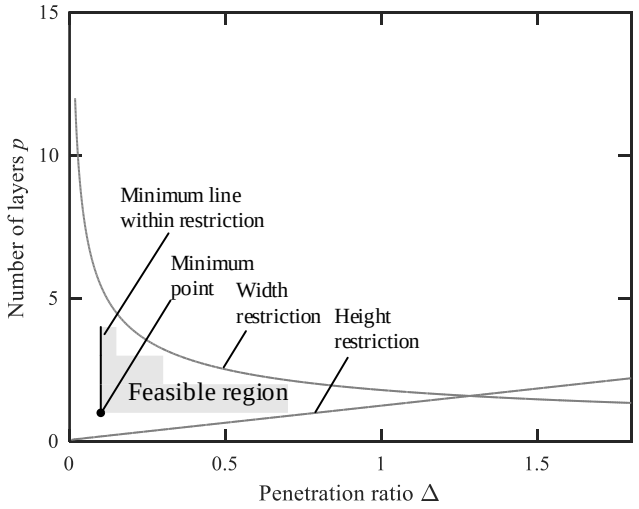


Fig. 12. Full optimization of $C_{\rm ind}$ in terms of a_1, $a_{\rm iso}$, p, and $\triangle$ with design map. The width and height restrictions are with (26) and (27), respectively. The minimum point in the feasible region is obtained by iteration.

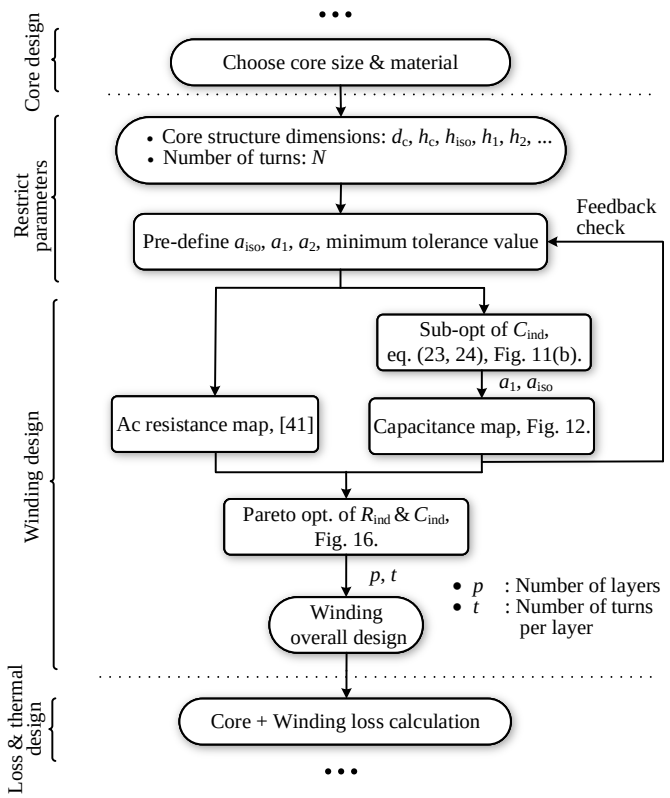


Fig. 13. Overall winding design with Pareto optimization of the ac resistance and stray capacitance.

as shown in Fig. 13. This system uses a set of parameters to evaluate multiple performance factors of an inductor, e.g., the ac resistance and stray capacitance. The Pareto optimization is used to find a set of conditions where there is no alternative condition to improve one parameter without reducing the performance of any other parameters [45].

The winding design procedure is usually followed after the core design, so the input parameters (e.g., core and bobbin

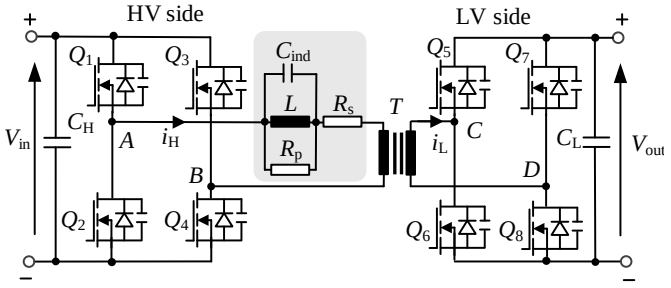


Fig. 14. The topology of a dual active bridge (DAB) converter with the equivalent circuit of the series inductor in gray shadow.

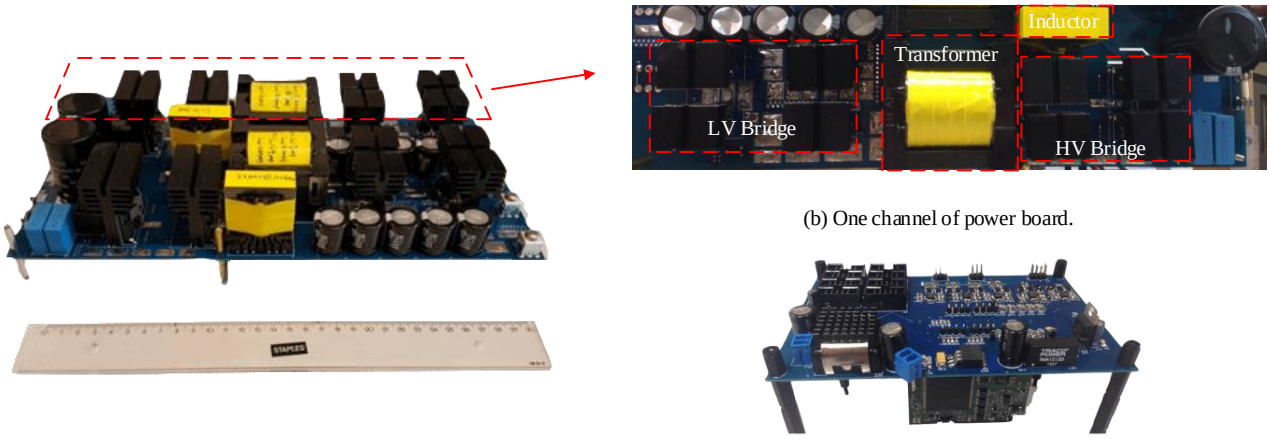
TABLE II
WINDING DESIGN INPUTS

Parameters	Value	Units
Core type	ETD 44/22/15	
Core material	N87	
Bobbin type	B66366	
Number of turns p	12	
Number of strands $k_{\rm str}$	90	
Distance restrictions, minimum torrence value:		
Layer insulation $a_{\rm iso}$	0.074	mm
Winding to central limb a_1	1.4	mm
Winding to side limb a_2	1.4	mm
Turn-to-turn insulation $h_{\rm iso}$	0.074	mm
Winding to bottom yoke h_1	1.4	mm
Winding to top yoke h_2	1.4	mm

restrictions) and the number of turns N are known. By predefined minimum insulation distances such as $a_{\rm iso}$, a_1 and a_2, an optimal ac resistance is obtained in the ac resistance map. Meanwhile, the capacitance design has four variables, i.e., p, $\triangle$, $a_{\rm iso}$ and a_1. With the sub-optimization of $C_{\rm ind}$, it is simplified to the 2D optimization. Further, with full optimization of $C_{\rm ind}$ in the capacitance design map, the minimum capacitance point is found. Finally, a global winding optimization is performed by combining the results of the corresponding points in both ac resistance and capacitance maps.

VI. Optimal Winding Design: A Case Study for the Series Inductor in a Dual Active Bridge Converter

The parasitic parameters of magnetic components have a significant impact on the performance of power electronics converters [1, 46–48]. A dual active bridge converter (DAB) prototype is adopted as an application case to verify the proposed capacitance model as well as the winding design method. The topology of the DAB converter is in Fig. 14. Two



(a) The power board of a two channel dual active bridge converter prototype.

(b) One channel of power board.

(c) Sampling and control board.

Fig. 15. Inductors placed in a 100 kHz dual active bridge (DAB) converter prototype. The power board is with two channels of DAB, and only one channel is used in the experiment.

TABLE III
WINDING DESIGN OUTPUTS AFTER OPTIMIZATION

Parameters	Value	Units
Number of layers p	1	
Turns in one layer t	12	
Winding diameter d_{i} output	0.15	mm
Winding diameter d_{i} chose	0.10	mm
Layer insulation distance a_{iso}	0	mm
Winding to central limb distance a_1	3.9	mm
Winding resistance R_{ac} @ 100 kHz	12.6	mΩ
Total Capacitance C	1.4	pF

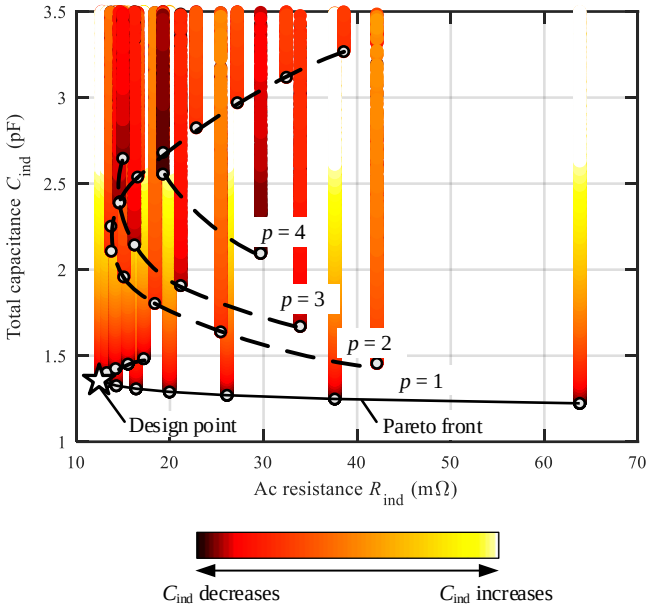


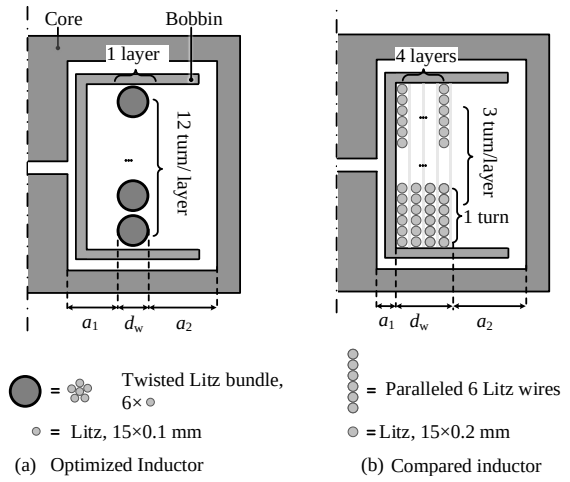
Fig. 16. Pareto optimization of the ac resistance and total capacitance. The dotted line ties all the design points of the minimum capacitance with the same number of layer p. The Pareto front is with the full line and is part of the $p = 1$ line. The smallest capacitance design point is with the largest ac resistance and locates on the right side of the Pareto front. However, the left side point of the Pareto front is chosen as the design point, after a trade-off between the stray capacitance and ac resistance.

100-kHz inductors are fabricated, measured, and implemented in the DAB converter prototype (c.f. Fig. 15).

The core, bobbin, winding, and distance restrictions as the design input are in Table II. In the design procedure, the relationship between C_{ind} and R_{ac} is plotted in Fig. 16 and the Pareto front is represented by the full black line. All the points on the Pareto front are with the $p = 1$ situation. The slope of the front is not large, so the capacitance of the point at the right and left side of the front are all in an acceptable range. However, the ac resistance of the left side point is reduced dramatically, and it is chosen as the design point. The final design output is illustrated in Table III.

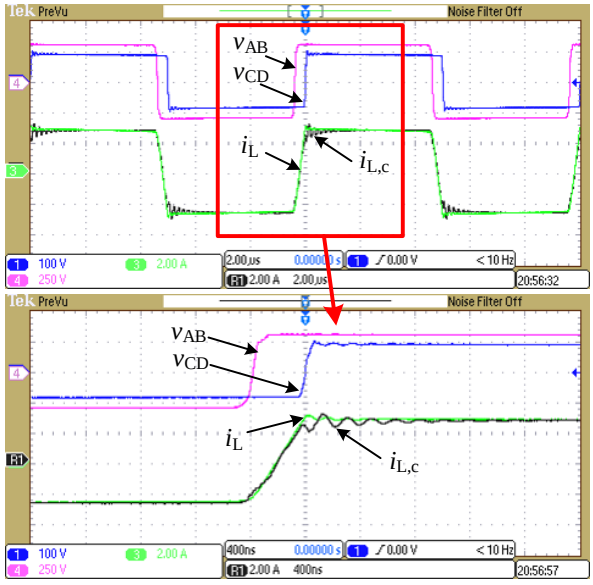
The self-capacitance of Litz wire is not considered [49]. A design with the same core, bobbin but larger strand diameter Litz ($6 \times 15 \times 0.2$ mm) is also presented for comparison. The detail of winding configurations are illustrated in Fig. 17. The designed inductor has a total measured capacitance of 1.9 pF, while the compared one has a value of 80.8 pF. The increase of the capacitance is due to the decrease of winding and core distance a_1, the compact wrapping of the winding (decrease of a_{iso}), and the large facing area which is caused by the vertically parallel wrapping of six Litz wires. Those situations are common in some applications and should be avoided in order to decrease the capacitance. Without magnetic cores, the measured ac resistances (at 100 kHz) of the optimized and compared inductors are 40.2 mΩ and 43.6 mΩ, respectively. When magnetic cores are inserted, their resistances are measured as 79.4 mΩ and 169.6 mΩ, respectively. The ac resistance of both inductors without the core is very close. However, after assembling the same core, the winding of the compared one is closer to the air gap and the fringing field, and the ac resistance increases dramatically.

The inductors are placed on the high-voltage (HV) side of

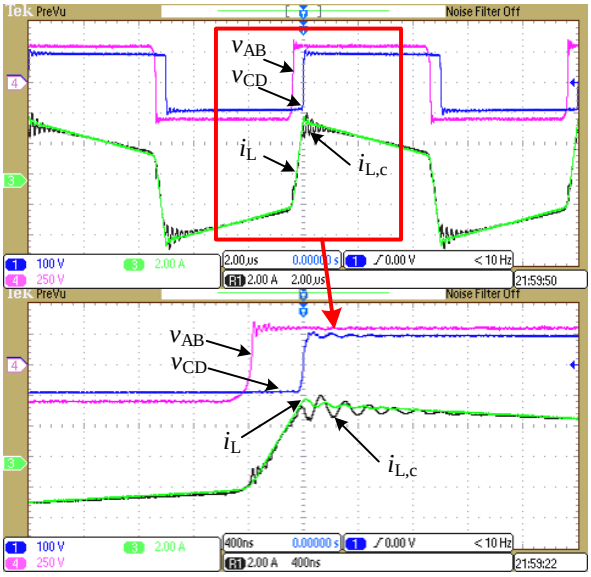


(a) Optimized Inductor (b) Compared inductor

Fig. 17. Winding configurations of the optimized and the compared inductor. The optimum design twists six bundle of 15 strands 0.1 mm Litz wire together, which is 90 strands of 0.1 mm Litz wire. The compared one uses 6 bundles 15 strands 0.2 mm wires in parallel, and wraps directly on the bobbin, meaning $a_1 = r_{b2} - r_1$. The number of layers $p = 4$ and the layer insulation distance $a_{iso} = 0.11$ mm.



(a) The primary and secondary voltages are matched with the transformer.



(b) The primary and secondary voltages are unmatched with the transformer.

Fig. 18. The experimental waveform when the primary and secondary voltages are matched and unmatched with the transformer, with a zoomed view below each.

the DAB, as in Fig. 15(b). The experimental results when the primary and secondary voltages are matched and unmatched with the transformer are shown in Fig. 18(a) and Fig. 18(b), respectively. v_{AB}, v_{CD} and i_L are HV and low-voltage (LV) side voltages and HV side current of the optimized inductor, respectively. $i_{L,c}$ is HV side current of the compared inductor. Both cases have the same input voltage of 302.5V, but the output voltages are different. In the matched operation point, the optimum one has a measured total system efficiency of 97.0%, whereas the comparative inductor only achieves the efficiency of 96.8%. In the unmatched operation point, it is 97.4% for the optimum one and 97.2% for compared one. The difference between the ac resistance of two inductors is 90.2 mΩ, leading to a 0.7W ac resistive loss reduction for the optimum inductor in the match operation point. The DAB system loss with the optimum and compared inductor is 24.6W and 23.4W, respectively. Compared with the compared inductor, a 1.2W loss reduction is achieved for the optimal one. The 0.5W difference between the total loss and ac resistive loss reduction results from the reduced stray capacitance. It is seen from Fig. 18(a) that the current ringing in the optimized inductor is reduced significantly. The current RMS value during the switching period decreases, which decreases the loss on both active devices (power semiconductors) and passive components (inductors, transformers, capacitors, etc.) in the circuit [1, 2]. Therefore, the decrease of capacitance contributes to the efficiency increase.

Finally, with different application scenarios, the full version of the optimization procedure in Fig. 13 can be adapted accordingly. Normally, the resonance frequency between the stray capacitance and inductance locates well beyond a few hundred kHz. For inductors operating at low frequencies, e.g., low-pass filters, the optimization of stray capacitance is not of much significance. For inductors used in above hundred kHz applications, e.g., high-frequency power electronic converters, radio frequency power amplifiers, EMC filters, the consideration of resonance becomes necessary. The parasitic capacitance may change the resonant frequency and generate an adverse effect on the performance of converters. Besides, the fast switching behavior of wide-band-gap semiconductor devices may be impaired by the stray capacitance. It causes current ringing and is independent of the switching frequency and topology. For those applications the consideration of the stray capacitance is essential.

In the study case of this paper, the resonant frequencies of the optimized and compared inductors are 19.0 MHz and 2.9 MHz, respectively, which are far beyond the 100 kHz switching frequency of the DAB converter. However, the switching time of Si MOSFETs is normally within a

few tens of ns, which corresponds to a few tens of MHz. Therefore, during such a high-frequency switching process, the inductor may perform as a capacitive element, which significantly deteriorates the switching behavior and increases system losses.

VII. Conclusions

A closed-form equation of the stray capacitance of inductors is derived considering the core/shield-related capacitance. All parts of the core/shield-related capacitance, i.e., the central limb, side limb, and yoke capacitance, are included. The potential of the floating core/shield is derived analytically, which makes the model applicable for the core/shield regardless of being grounded or not. Six prototypes are built, and the finite element method (FEM) simulation and experimental results verify the proposed model and analysis. As a rule of thumb, the core/shield-related capacitance should be taken into account for inductors with a single layer winding, or a shield, or when the winding width exceeds 50% of the window width of ETD and P cores. An analytical stray capacitance optimization is proposed, enabling the winding optimization considering both the ac resistance and stray capacitance. An inductor winding design case for a dual active bridge converter is presented. The proposed optimization procedure results in a 2.4% of stray capacitance compared to a reference design, yielding a smaller current ringing and 0.2% converter-level efficiency improvement.

Appendix A
Derivation of the Core-related Coefficients

In a parallel plate model, assuming the voltage difference between the two plates is constant, the inherent capacitance C_x is calculated with (2). If a linear potential distribution is assumed along the two plates, the voltage difference at one side is U_{D1} and at the other side is U_{D2}, the total system energy is [7]:

$$W = \frac{C_x}{6}(U_{D1}^2 + U_{D1}U_{D2} + U_{D2}^2). \tag{A.1}$$

Assume a linear voltage distribution along the winding and core, the voltage difference between them are given in Fig. 3(a). Following (A.1), the energy stored by C_{cw1}, C_{cw2}, and C_{cw3} are expressed as W_1, W_1, and W_3 with (A.2)(A.3)(A.4)(A.5), respectively. They are at the bottom of the page. (A.5) is based on the voltage distribution of the winding ended with the different direction, as is illustrated by the gray letter in Fig. 3(a).

On the other hand, the total energy is expressed as the core-related capacitance C_{cwT}:

$$W_{\mathrm{cwT}} = \frac{C_{\mathrm{cwT}}}{2}(pU_{\mathrm{t}})^2. \tag{A.6}$$

Equaling $W_{\mathrm{cw}} = W_1 + W_2 + W_3$ and comparing the factors of C_{cw1} to C_{cw3}, (11) is obtained.

Appendix B
Derivation of the Potential of the Core/ Shield

The electrical field problem of the winding and core system is mapped to the electrical circuit problem, as is illustrated in Fig. 4(a). The voltage potential of the conductors are known, the voltage distribution between the first turn U_1 and the last turn in the first layer U_{T} is:

$$U_y = U_1 + (U_{\mathrm{T}} - U_1)\frac{y}{h_{\mathrm{w}}}, \tag{B.1}$$

where y is the distance from the first turn, h_{w} is the winding height. The capacitance between the winding and central limb at y is:

$$C_y = \alpha_{\mathrm{cw1}} \cdot \varepsilon_0\varepsilon_{\mathrm{cw1}}\frac{2\pi r_{\mathrm{cw1}}\mathrm{d}y}{d_{\mathrm{cw1}}}. \tag{B.2}$$

Neglecting the current contribution of adjacent layers, the current through the first layer to the central limb is:

$$i_1 = \int_0^{h_{\mathrm{w}}}(U_y - U_{\mathrm{c}})C_y = \frac{U_1 + U_{\mathrm{T}} - 2U_{\mathrm{c}}}{2}C_{\mathrm{cw1}}. \tag{B.3}$$

i_2, i_{31}, and i_{32} are derived in the same way:

$$W_1 = C_{\mathrm{cw1}}\frac{U_{\mathrm{d}}^2 + U_{\mathrm{d}}(U_{\mathrm{d}} + U_{\mathrm{t}}) + (U_{\mathrm{d}} + U_{\mathrm{t}})^2}{6}, \tag{A.2}$$

$$W_2 = C_{\mathrm{cw2}}\frac{[U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}]^2 + (U_{\mathrm{d}} + pU_{\mathrm{t}})^2 + [U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}](U_{\mathrm{d}} + pU_{\mathrm{t}})}{6}, \tag{A.3}$$

$$W_3 = C_{\mathrm{cw3}}\frac{U_{\mathrm{d}}^2 + U_{\mathrm{d}}[U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}] + [U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}]^2 + (U_{\mathrm{d}} + U_{\mathrm{t}})^2 + (U_{\mathrm{d}} + pU_{\mathrm{t}})^2 + (U_{\mathrm{d}} + U_{\mathrm{t}})(U_{\mathrm{d}} + pU_{\mathrm{t}})}{6}, \tag{A.4}$$

or

$$W_3 = C_{\mathrm{cw3}}\frac{U_{\mathrm{d}}^2 + U_{\mathrm{d}}(U_{\mathrm{d}} + pU_{\mathrm{t}}) + (U_{\mathrm{d}} + pU_{\mathrm{t}})^2 + (U_{\mathrm{d}} + U_{\mathrm{t}})^2 + [U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}]^2 + (U_{\mathrm{d}} + U_{\mathrm{t}})[U_{\mathrm{d}} + (p-1)U_{\mathrm{t}}]}{6}, \tag{A.5}$$

$$
\begin{aligned}
i_2 &= \frac{U_1 + pU_\mathrm{t} + U_1 + (p-1)U_\mathrm{t} - 2U_\mathrm{c}}{2} C_{\mathrm{cw}2}, \\
i_{31} &= \frac{U_1 + U_1 + (p-1)U_\mathrm{t} - 2U_\mathrm{c}}{2} C_{\mathrm{cw}3}, \\
i_{32} &= \frac{U_\mathrm{T} + U_1 + pU_\mathrm{t} - 2U_\mathrm{c}}{2} C_{\mathrm{cw}3}.
\end{aligned} \tag{B.4}
$$

With Kirchhoff's Current Law:

$$
i_1 + i_2 + i_{31} + i_{32} = 0, \tag{B.5}
$$

the potential of the core U_c is:

$$
U_\mathrm{c} = U_1 + \frac{C_{\mathrm{cw}1} + (2p-1)C_{\mathrm{cw}2} + 2pC_{\mathrm{cw}3}}{2C_{\mathrm{cw}1} + 2C_{\mathrm{cw}2} + 4C_{\mathrm{cw}3}} U_\mathrm{t}. \tag{B.6}
$$

k_U is obtained by the definition:

$$
\begin{aligned}
k_\mathrm{U} =& \frac{U_\mathrm{d}}{U_\mathrm{t}} = \frac{U_1 - U_\mathrm{c}}{U_\mathrm{t}} \\
=& -\frac{C_{\mathrm{cw}1} + (2p-1)C_{\mathrm{cw}2} + 2pC_{\mathrm{cw}3}}{2C_{\mathrm{cw}1} + 2C_{\mathrm{cw}2} + 4C_{\mathrm{cw}3}}.
\end{aligned} \tag{B.7}
$$

i_{31} and i_{32} can exchange according to the gray voltage distribution in Fig. 3(a), and the final results do not change.

Appendix C
Sub-Optimization of the Core-related Capacitance

With the parallel plate model and following the five steps in Fig. 2, the core-related capacitance is expressed by:

$$
\begin{aligned}
C_{\mathrm{cw}\mathrm{T}} =& k_{\mathrm{cw}1} \cdot C_{\mathrm{cw}1} + k_{\mathrm{cw}2} \cdot C_{\mathrm{cw}2} + k_{\mathrm{cw}3} \cdot C_{\mathrm{cw}3} \\
=& k_{\mathrm{cw}1}\varepsilon_0\varepsilon_{\mathrm{cw}1} \frac{2\pi h_\mathrm{c}(r_1 + d_{\mathrm{cw}1}/2)}{d_{\mathrm{cw}1}} \\
&+ \frac{4r_1 k_{\mathrm{cw}2}}{\pi(r_1 + r_4)} \cdot \varepsilon_0\varepsilon_{\mathrm{cw}2} \frac{2\pi h_\mathrm{c}(r_3 + d_{\mathrm{cw}2}/2)}{d_{\mathrm{cw}2}} \\
&+ k_{\mathrm{cw}3}\varepsilon_0\varepsilon_{\mathrm{cw}3} \frac{4r_1(r_3 - r_2)}{(h_\mathrm{c} - h_\mathrm{w})/2 + d_\mathrm{e}/2}.
\end{aligned} \tag{C.1}
$$

$r_{\mathrm{b}2}$ and $r_{\mathrm{b}3}$ are used to approximate the equivalent mean radius for $C_{\mathrm{cw}1}$ and $C_{\mathrm{cw}2}$, respectively. $C_{\mathrm{cw}3}$ is a constant and independent on a_1. With the parameter definition in Fig. 2 and 10, substituting $a_1 = r_2 - r_1$, $a_\mathrm{w} = a_1 + a_2 + (p-1)a_\mathrm{iso}$ and $a_2 = r_4 - r_3$ into (C.1), $C_{\mathrm{cw}\mathrm{T}}$ is a function of a_1:

$$
\begin{aligned}
C_{\mathrm{cw}\mathrm{T}} \approx& f_{\mathrm{apx}1}(a_1) \\
=& k_{\mathrm{cw}1}\varepsilon_0\varepsilon_{\mathrm{cw}1} \frac{2\pi h_\mathrm{c} r_{\mathrm{b}2}}{a_1 + d_\mathrm{e}/2} \\
&+ k_{\mathrm{cw}2} \cdot \frac{4r_1\varepsilon_0\varepsilon_{\mathrm{cw}2}}{\pi(r_1 + r_4)} \cdot \frac{2\pi h_\mathrm{c} r_{\mathrm{b}3}}{a_\mathrm{w} - a_1 - (p-1)a_\mathrm{iso} + d_\mathrm{e}/2} \\
&+ k_{\mathrm{cw}3} \cdot C_{\mathrm{cw}3},
\end{aligned} \tag{C.2}
$$

$a_{1\mathrm{opt}}$ is obtained by solving $\frac{df_{\mathrm{apx}1}}{da_1} = 0$:

$$
\begin{aligned}
a_{1\mathrm{opt}} =& \frac{k_2(k_1 - d_\mathrm{e}/2) + 2d_\mathrm{e}k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_1 r_{\mathrm{b}3}}{k_2 - 4k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_1 r_{\mathrm{b}3}}, \\
&\pm \frac{2k_1\sqrt{k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_1 r_{\mathrm{b}3}k_2}}{k_2 - 4k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_1 r_{\mathrm{b}3}},
\end{aligned} \tag{C.3}
$$

with:

$$
\begin{aligned}
k_1 =& a_\mathrm{w} - (p-1)a_\mathrm{iso} + d_\mathrm{e}, \\
k_2 =& \pi r_{\mathrm{b}2} k_{\mathrm{cw}1}\varepsilon_{\mathrm{cw}1}(r_1 + r_4).
\end{aligned} \tag{C.4}
$$

Usually, the solution with symbol '$-$' in front of $2k_1\sqrt{k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_1 r_{\mathrm{b}3}k_2}$ is taken, since another solution leads to a negative a_iso.

Appendix D
Sub-Optimization of the Total Capacitance

The equivalent mean radius r_ww, winding height h_ww, and effective layer distance d_ww are approximated by:

$$
r_\mathrm{ww} \approx 1/2(r_1 + r_4), \quad h_\mathrm{ww} \approx h_\mathrm{w}, \quad \text{and} \quad d_\mathrm{ww} \approx a_\mathrm{iso}, \tag{D.1}
$$

respectively, as illustrated in Fig. 2 and 10. The full formation of the winding capacitance is:

$$
C_{\mathrm{ww}\mathrm{T}} \approx \beta \cdot (p-1)(\frac{2}{p})^2 \cdot \varepsilon_0\varepsilon_\mathrm{ww} \frac{2\pi h_\mathrm{w} \cdot 1/2 \cdot (r_1 + r_4)}{a_\mathrm{iso}}. \tag{D.2}
$$

Adding the core-related capacitance (C.2) together and eliminating d_e term, the total capacitance is a two-variable function of (a_1, a_iso) in (22): C_ind = $f_4(a_1, a_\mathrm{iso})$. $C_{\mathrm{cw}3}$ is regarded as a constant with the variation of a_1 and a_iso. The partial derivatives of C_ind with respect to a_1 and a_iso are expressed as (D.3) and (D.4). They are at the top of the next page. By simplifying the equations using restrictions:

$$
a_2 = a_\mathrm{w} - a_1 - (p-1)a_\mathrm{iso} > 0, \tag{D.5}
$$

a_w is obtained as:

$$
a_\mathrm{w} = (1 + k_1)a_1 + (p-1)a_\mathrm{iso}, \tag{D.6}
$$

$$
a_\mathrm{w} = a_1 + (p - 1 + pk_2)a_\mathrm{iso}, \tag{D.7}
$$

with:

$$
\begin{aligned}
k_3 =& \sqrt{\frac{4k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_{\mathrm{b}3}r_1}{\pi k_{\mathrm{cw}1}\varepsilon_{\mathrm{cw}1}r_{\mathrm{b}2}(r_1 + r_4)}}, \\
k_4 =& \sqrt{\frac{2k_{\mathrm{cw}2}\varepsilon_{\mathrm{cw}2}r_{\mathrm{b}3}r_1 h_\mathrm{c}}{\pi\beta\varepsilon_\mathrm{ww}h_\mathrm{w}(r_1 + r_4)^2}}.
\end{aligned} \tag{D.8}
$$

By solving (D.6) and (D.7), the stationary point is derived as:

$$
a_{\mathrm{isoopt}} = \frac{k_3 a_\mathrm{w}}{k_3(p-1) + pk_4(1 + k_3)}, \tag{D.9}
$$

$$
a_{1\mathrm{opt}} = \frac{pk_4 a_\mathrm{w}}{k_3(p-1) + pk_4(1 + k_3)}. \tag{D.10}
$$

Solving the second derivatives for f_4 leads to: $f_{4\mathrm{a}_1\mathrm{a}_1} f_{4\mathrm{a}_\mathrm{iso}\mathrm{a}_\mathrm{iso}} - f^2_{4\mathrm{a}_1\mathrm{a}_\mathrm{iso}} > 0$ and $f_{4\mathrm{a}_1} > 0$. Therefore, C_ind has a minimum in $(a_{\mathrm{isoopt}}, a_{1\mathrm{opt}})$.

$$f_{4a_1} = -2\frac{\varepsilon_0 k_{cw1}\varepsilon_{cw1}\pi h_c r_{b2}}{{a_1}^2} + 8\frac{\varepsilon_0 k_{cw2}\varepsilon_{cw2}\pi h_c r_{b3} r_1}{(a_w - a_1 - (p-1)a_{iso})^2(\pi r_1 + \pi r_4)} = 0, \tag{D.3}$$

$$f_{4a_{iso}} = 4\beta\frac{\varepsilon_0\varepsilon_{ww}\pi h_w \cdot 1/2 \cdot (r_1 + r_4)(2p-2)}{{a_{iso}}^2 p^2} + 8k_{cw2}\frac{\varepsilon_0\varepsilon_{cw2}\pi h_c r_{b3} r_1(1-p)}{(a_w - a_1 - (p-1)a_{iso})^2(\pi r_1 + \pi r_4)} = 0. \tag{D.4}$$

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