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# Capacitive DC Links in Power Electronic Systems-Reliability and Circuit Design

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**Abstract:** Capacitive DC links are an important part in voltage source power electronic converters, which contribute to cost, size and failure rate on a considerable scale. With more and more stringent constraints brought by industrial applications, the capacitive DC links encounter reliability aspect challenges. This paper presents a review on the reliability design and improvement of capacitive DC links from three aspects: 1) Quantitative reliability prediction for DC-link capacitors; 2) Reliability-oriented design of passive DC-link capacitor banks; and 3) Advanced active DC links to exceed the limits of passive DC-link capacitors. Key solutions for each aspect are highlighted and discussed with case studies. This review serves to provide a picture of state-of-the-art research on the reliability design and improvement of capacitive DC links, highlight the key milestones in this area, and identify the corresponding challenges and future research directions.

**Keywords:** Reliability, capacitor, DC link, power electronics.

## 1 Introduction

Capacitive DC links are widely used in power electronic systems to filter the harmonic currents, buffer the instantaneous power difference between the input source and output load, and minimize the voltage variation in the DC link<sup>[1]</sup>. In three-phase applications such as Adjustable Speed Drive(ASD), and Wind Turbine(WT) systems, the instantaneous power is six times that of the fundamental frequency under grid voltage balanced condition, and two times that of fundamental frequency under unbalances<sup>[2-3]</sup>. In single-phase rectifier or inverter applications such as Photovoltaic(PV), and Fuel Cell(FC) system, the conversion between DC and AC power will typically introduce a double fundamental frequency pulsation power and ripple voltage harmonics at the DC link of the power conversion system<sup>[4]</sup>. The low-frequency voltage harmonics are detrimental to the DC side utility of the converter, deviate Maximum Power Point Tracking (MPPT) in a renewable energy system, and impact the power quality and reliability of the power grid<sup>[5-6]</sup>. In order to decouple the impact between the two stages connected through DC links, capacitive DC links are applied.

The most commonly used passive DC links are capacitive ones, which are one of the highest failure rate components in power electronic systems and contributes to more than 20% failures in certain applications<sup>[7]</sup>. From the system-level aspect, capacitor is the bottleneck of the power electronic systems<sup>[8]</sup>. The failure probability contribution of a DC-DC converter system discussed in [8] is shown in Fig.1. It reveals that the DC-link capacitors contribute to the highest failure probability among other components and mostly determine the lifetime of the power electronic system.

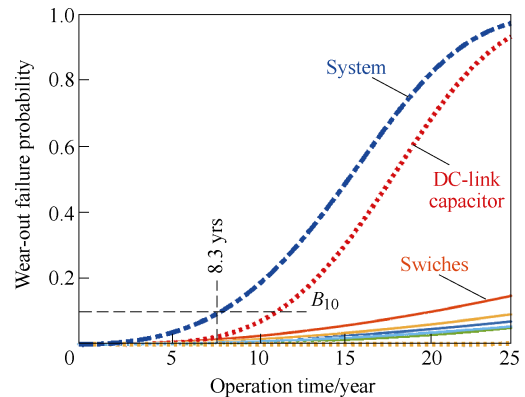


Fig.1 Failure probability of components and system in a DC-DC converter application<sup>[8]</sup>

With more stringent reliability constraints brought by automotive, aerospace, and energy industries, the design of DC links encounters the following challenges<sup>[1,9]</sup>: ①Capacitors are one kind of the stand-out components in terms of failure rate in field operation of power electronic systems; ②Cost reduction pressure from global competition dictates minimum design margin of capacitors without undue risk; ③Capacitors are to be exposed to more harsh environments (e.g., high ambient temperature, high humidity, etc.) in emerging applications, and ④Constraints on volume and thermal dissipation of capacitors with the trends for high power density power electronic systems.

From the capacitor end-user perspective, the effort of overcoming the challenges can be divided into three categories which are reviewed in this paper: ①Electro-thermal-lifetime modeling to support model-based sizing of capacitors<sup>[10-15]</sup>; ②Multi-objective optimization of passive capacitor banks in terms of cost, size, efficiency, and reliability<sup>[16-19]</sup>; ③New capacitor concepts based on active switching circuits<sup>[20-35]</sup>. The first effort is an analysis tool to predict the reliability performance of the capacitive DC links. Based on the reliability assessment,

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the reliability-oriented design and optimization solutions for the applied passive capacitor bank can be provided. In the third effort, active DC links with power electronic circuit to exceed the physical limits of the passive DC-link capacitors are reviewed. The challenges and opportunities for future research direction are finally addressed.

The structure of this paper is as follows: Section 2 presents the reliability prediction of capacitors with physical of failure understanding; Section 3 and 4 present the advanced technologies for reliability improvement in terms of passive and active DC links, followed by the conclusions.

## 2 Lifetime prediction of DC-link capacitors

DC-link capacitors can fail due to intrinsic and extrinsic factors, such as design defect, material wear-out, operating temperature, voltage, current, moisture, mechanical stress, and so on. Generally, the failures can be divided into catastrophic failures due to single-event overstress and wear-out failures due to the long-term degradation of capacitors. The state-of-the-art methods for lifetime prediction of capacitors for the wear-out failures can be divided into two categories: lifetime prediction for constant operating condition and lifetime prediction for long-term mission profile.

### 2.1 Lifetime prediction for constant operating condition

For the constant operating condition, lifetime prediction with a simplified lifetime model is commonly used in power electronic applications. The most widely used lifetime model for capacitors is shown in (1), which describes the influence of temperature and voltage stress<sup>[1]</sup>:

$$L = L_0 \times \left( \frac{V}{V_0} \right)^{-n} \times \exp \left[ \left( \frac{E_a}{K_B} \right) \left( \frac{1}{T} - \frac{1}{T_0} \right) \right] \quad (1)$$

where  $L$  and  $L_0$  are the lifetime under the using condition

and testing condition, respectively.  $V$  and  $V_0$  are the voltage at use condition and test condition, respectively.  $T$  and  $T_0$  are the temperature in Kelvin at use condition and test condition, respectively.  $E_a$  is the activation energy,  $K_B$  is Boltzmann's constant  $8.62 \times 10^{-5}$  eV/K, and  $n$  is the voltage stress exponent. Therefore, the values of  $E_a$  and  $n$  are the key parameters to be determined in the above model. In [36], the  $E_a$  and  $n$  are found to be 1.19 and 2.46, respectively, for high dielectric constant ceramic capacitors. In [37], the ranges of  $E_a$  and  $n$  for MLC-Caps are 1.3~1.5 and 1.5~1.7, respectively. The large discrepancies could be attributed to the ceramic materials, dielectric layer thickness, testing conditions, etc. With the trend for smaller size and thinner dielectric layer, the MLC-Caps will be more sensitive to the voltage stress, implying a higher value of  $n$ . Moreover, under different testing voltages, the value of  $n$  might be different as discussed in [38].

### 2.2 Lifetime prediction for long-term mission profile

In the above lifetime prediction method shown in section 2.1, the operating condition is assumed to be constant. However, in real power electronic applications, the conditions are always changing with the environment (e.g., ambient temperature, relative humidity and vibration), user's behavior (e.g., loading conditions and input variations) and the status of the system itself (e.g., parameter variation and devices degradation)<sup>[11]</sup>.

In recent years, lifetime prediction for long-term mission profile has been proposed<sup>[8-11]</sup>. Differing from the lifetime prediction in constant operating condition, this method takes into account the long-term and variable loading conditions. Furthermore, various sources of uncertainties exist (e.g., tolerances in component parameters, modeling errors) Therefore, a statistical approach based on Monte-carlo simulation is applied<sup>[39]</sup>. Compared with the method in section 2.1, the lifetime prediction for long-term mission profile is more closely related to the real operating condition. The lifetime estimation procedure is shown in Fig.2. It includes three

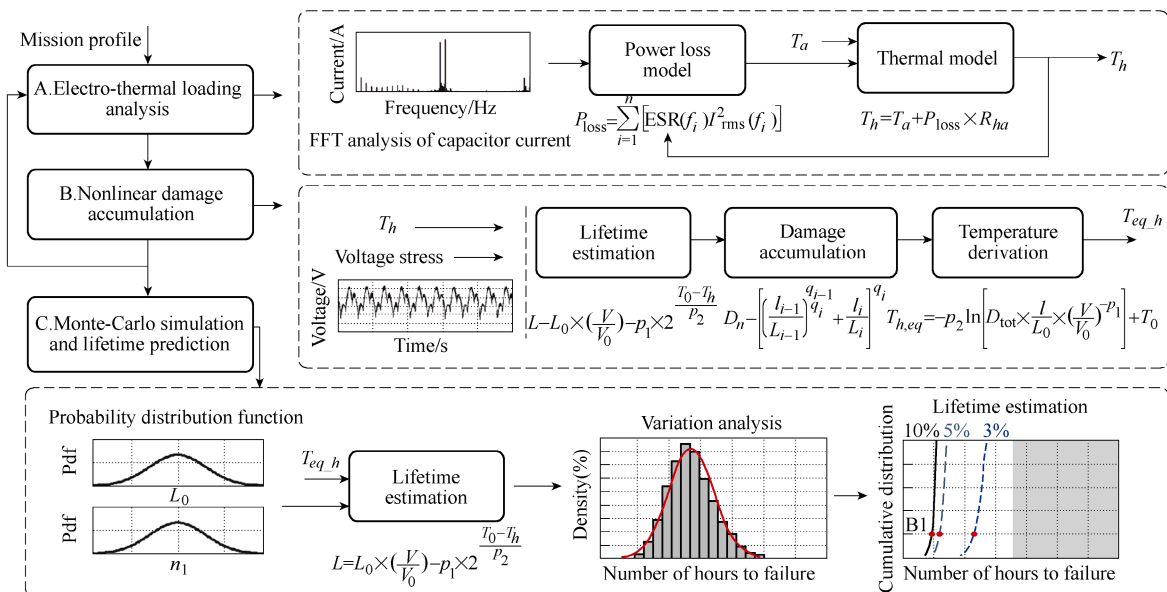


Fig.2 Mission profile based lifetime prediction procedure<sup>[11]</sup>

major steps: electro-thermal loading analysis, damage accumulation, and Monte-carlo simulation based variation analysis. A mission profile (i.e., ambient temperature, loading condition) is applied as the input. The output is the lifetime of the capacitor with a certain confidence level (e.g., 90 %).

### 2.2.1 Electro-thermal loading analysis

Thermal stress is critical to capacitor wear out. The ripple current and ambient temperatures are the contributors to the capacitor hot-spot temperature. For electrolytic capacitors, the dominant degradation mechanisms are electrochemical reaction in the oxide layer and the electrolyte vaporization<sup>[40-41]</sup>. The thermal stress leads to an increase of Equivalent Series Resistor (ESR) over time. In particular, the increase of capacitor power loss causes a higher operating temperature inside the capacitor. The hot-spot temperature of the capacitor, which is effected by the current stress and ambient temperature, is presented by [11]

$$T_h = T_a + R_{ha} \times \sum_{i=1}^n \left[ \text{ESR}(f_i) \times I_{\text{rms}}^2(f_i) \right] \quad (2)$$

where  $T_h$  is the hot-spot temperature,  $T_a$  is the ambient temperature,  $R_{ha}$  is the equivalent thermal resistance from hotspot to ambient,  $\text{ESR}(f_i)$  is the equivalent series resistance at frequency  $f_i$ ,  $I_{\text{rms}}(f_i)$  is the RMS value of the ripple current at frequency  $f_i$ .

### 2.2.2 Damage accumulation

The linear and nonlinear accumulated damage model is developed to describe the real damage progress<sup>[11,13]</sup>. The wear out of the capacitor is indicated by an increase of ESR. Damage is then defined as the ratio of instantaneous to final ESR growth. As an example, the formulated nonlinear model that accounts for the effects of these processes, but without a specific identification and is represented by

$$D_n = \left[ \left( \frac{l_{i-1}}{L_{i-1}} \right)^{q_i} + \frac{l_i}{L_i} \right]^{q_i} \quad (3)$$

$q$  is a function of lifetime  $L$  and material constants.  $l_i$  and  $L_i$  are the instantaneous equivalent operating time and total lifetime under the same loading condition, respectively. By accumulating the damage, the dynamical stresses are converted into static values for each type of temperature stress. Taking the accumulated damage into the lifetime model, the equivalent hot-spot temperature can be derived.

### 2.2.3 Monte-Carlo analysis and lifetime prediction

The application of the lifetime model results in a fixed accumulated damage. It is far from reality since the capacitor parameter variations and the statistical properties of the lifetime model are ignored. In field operations, the time to end-of-life for the capacitors could vary within a range due to the tolerance in physical parameters and the difference in the experienced stresses.

Therefore, a statistical approach based on Monte-carlo simulation is applied<sup>[8-11]</sup>. The sensitivity of the lifetime to temperature tolerance-related parameters can be evaluated individually or collectively. Finally, the distribution of the end-of-life of the capacitors can be obtained, allowing a lifetime analysis with a specified confidence level.

### 2.2.4 Closed-loop modelling process

Along with the damage accumulation, the capacitance reduction and ESR increase lead to an increasing of DC-link voltage ripple and changing of DC-link current, which accelerate the degradation process of the capacitor. A feedback loop is considered in the lifetime prediction procedure to represent the accelerated degradation.

## 3 Advanced passive DC links-reliability oriented design for capacitor banks

For the applications where single capacitor cannot fulfill the voltage rating or capacitance requirements, capacitor bank is always used as the energy buffer by connecting several capacitors in parallel for larger capacitance, or in series for higher voltage rating. In the ultra-compact converters with cost constraints, there are some design challenges for the capacitor banks: ① Uneven temperature distribution among the capacitors inside the bank due to thermal coupling and uneven boundary conditions, which leads to a part of capacitors severity aging<sup>[17-19]</sup>. The temperature estimation based on a single capacitor becomes over-simplified; ② Long-lifetime series of capacitors can be used to improve the reliability of the capacitor bank, however, at the expense of compromised performance in cost, power density, etc.<sup>[40-41]</sup>.

At the beginning of reliability-oriented design, thermal loading distribution of the capacitor bank needs to be predicted, so as to acquire the lifetime of individual capacitor. Considering the self-heating and thermal coupling effects, the lumped thermal model of the capacitor bank can be written in the matrix form as<sup>[18]</sup>

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_m \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \dots & Z_{1n} \\ Z_{21} & Z_{22} & \dots & Z_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ Z_{m1} & Z_{m2} & \dots & Z_{mn} \end{bmatrix} \begin{bmatrix} P_{\text{loss},1} \\ P_{\text{loss},2} \\ \vdots \\ P_{\text{loss},n} \end{bmatrix} + \begin{bmatrix} T_{a,1} \\ T_{a,2} \\ \vdots \\ T_{a,m} \end{bmatrix} \quad (4)$$

where  $T_i$  ( $i=1,2,\dots,m$ ) is the monitoring point temperature,  $P_{\text{loss},j}$  with ( $j=1,2,\dots,n$ ) is the power losses of each capacitor,  $T_{a,i}$  ( $i=1,2,\dots,m$ ) is the ambient reference temperature at the monitoring points, and  $Z_{i,j}$  ( $i=1,2,\dots,m$  and  $j=1,2,\dots,n$ ) is the coupling thermal impedance between the monitoring point and the reference point. In particular,  $Z_{i,i}$  ( $i=j$ ) is the self-heating thermal impedance.

From the lifetime model shown in (1), it can be seen that the rated lifetime, voltage stress and thermal stress are the key factors affecting the capacitor lifetime. Worth being noted is that if the voltage stress is under the rated voltage, it will introduce negligible effect on the lifetime. Therefore, design variables considered in

this paper are the rated lifetime and thermal stress of each capacitor<sup>[18]</sup>.

### 3.1 Lifetime matching of individual capacitors

Capacitor manufactures provide products with different classes of rated lifetime. The useful lifetime of capacitors is dependent on both its rated lifetime and the actual stress conditions. In a capacitor bank with multiple capacitors, the thermal coupling among the capacitors varies with physical location. The electro-thermal stresses among individual capacitors may be different, thereby. One way to match the lifetime of the individual capacitors is by selecting capacitors with different rated lifetime to configure the capacitor bank. The optimized variables are the rated lifetime of individual capacitor  $L_{rated,1}$ ,  $L_{rated,2}$ , ...,  $L_{rated,m}$ , and the optimization target is to minimize the lifetime difference among capacitor cells, where the mathematical model are shown below<sup>[18]</sup>:

$$\begin{cases} \min. \{X\} \\ X = \frac{[L_1(L_{rated,1}) - \bar{L}]^2 + [L_2(L_{rated,2}) - \bar{L}]^2 + \dots + [L_m(L_{rated,m}) - \bar{L}]^2}{m} \\ \bar{L} = \frac{L_1(L_{rated,1}) + L_2(L_{rated,2}) + \dots + L_m(L_{rated,m})}{m} \\ \min. \{L_m\} \geq L_{Target} \end{cases} \quad (5)$$

$X$  is the temperature variance.  $L_m$  and  $L_{rated,m}$  are the lifetime and the rated lifetime of the individual capacitor  $m$ , respectively.  $L_{Target}$  is the lifetime target of the capacitor bank.

A capacitor bank with nine electrolytic capacitors connected in parallel is used as a case study<sup>[18]</sup>. For conventional solution, 2000 hours rated lifetime series products are used for all individual capacitors. Based on the lifetime prediction shown in section 2.1, the lifetime of individual capacitor can be obtained, where the shortened lifetime of capacitor is a 4.7 year lifetime only at the middle of the capacitor bank, which cannot reach the 5 year lifetime target as shown in Fig.3. Based on the lifetime matching method, 3000 hours rated lifetime series product is used for the middle capacitor in the hybrid bank. Therefore, all the capacitors can satisfy the 5 year lifetime target with a slight rise in cost.

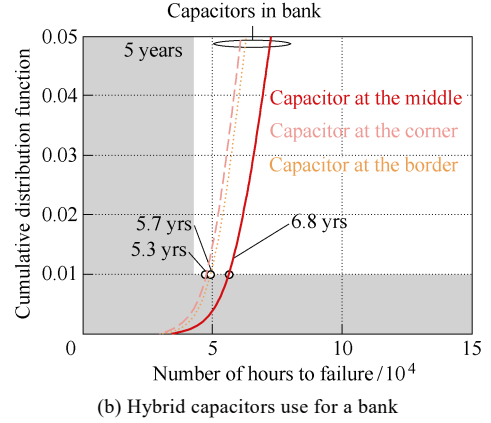
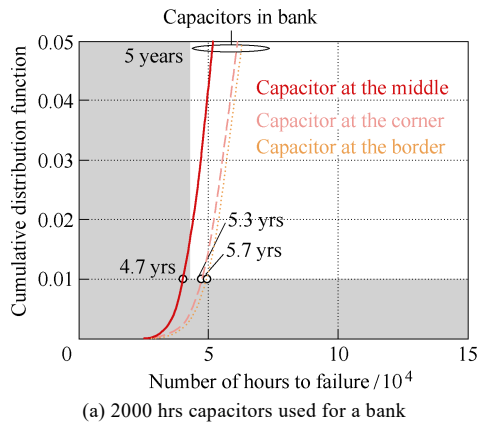


Fig.3 Lifetime estimation results with conventional design and hybrid design capacitor banks

In Fig.3(a),conventional design: individual capacitor uses 2000hours rated lifetime product, so that the capacitor at the middle has a 4.7 year lifetime which is lower than the 5 year. In Fig.3(b), hybrid design: partial capacitors use a 3000 hours series product for the middle capacitor and the others use 2000 hours series product, so that all the capacitor can reach 5 years lifetime target<sup>[18]</sup>.

### 3.2 Thermal stress matching

Power loss is the source for the thermal stress, which is determined by the current spectrum and the ESR of each capacitor. The current spectrum at low-frequency bandwidth depends on the capacitance (or impedance at specified frequency) of the capacitor, because of current sharing among capacitors. The specified capacitor current can be obtained as

$$i_{C_k} = i_{Bank} \times \frac{C_k}{C_1 + C_2 + \dots + C_n} \quad (6)$$

where  $n$  is the number of capacitors in a bank,  $k$  is the  $k$ -th capacitor in the bank,  $C_n$  is the capacitance, and  $i_{Bank}$  is the total current of the capacitor bank. ESR is also related to the capacitance, which is given by [40]

$$ESR = \frac{1}{C_k s} \times \tan \delta_k \quad (7)$$

where  $\tan \delta$  is the Dissipation Factor(DF) and  $\delta$  is the loss angle. Based on (7) and (8), the power loss of the  $k$ -th capacitor can be derived as

$$P_{loss} = i_{C_k}^2 ESR = C_k \times \frac{\tan \delta \times i_{Bank}^2}{(C_1 + C_2 + \dots + C_n)^2 s} \quad (8)$$

It can be seen that the power loss of the capacitor is linear with capacitance. Therefore, the hot-spot temperature can be obtained based on the power loss and the proposed lumped thermal model. Worth being noted, in the same series products, the size normally changed with the capacitance, which will further affect the thermal impedance because of the variation of the heat spread area. Therefore, the temperature redistribution method should hybrid different downsize series products, which series provides different capacitances for the same size for a capacitor bank. Therefore, the power loss is the

only variable corresponding to the hot-spot temperature as well as the lifetime of individual capacitor. The optimization model is defined as

$$\min. \{X\}$$

$$\left\{ \begin{array}{l} X = \frac{[T_1(C_1, C_2, \dots, C_m) - \bar{T}]^2 + [T_2(C_1, C_2, \dots, C_m) - \bar{T}]^2 + \dots + [T_m(C_1, C_2, \dots, C_m) - \bar{T}]^2}{m} \\ \bar{T} = \frac{T_1(C_1, C_2, \dots, C_m) + T_2(C_1, C_2, \dots, C_m) + \dots + T_m(C_1, C_2, \dots, C_m)}{m} \\ C = C_1 + C_2 + \dots + C_m \end{array} \right. \quad (9)$$

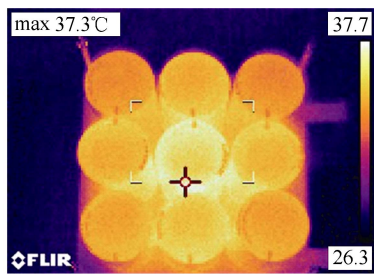
where the optimized variable is the capacitance for individual capacitor in the bank.

A case study is presented in Fig.4. With the same capacitance 470 $\mu$ F/450V for individual capacitor, the thermal loading distribution is uneven. Based on the proposed thermal stress matching method, the capacitance for individual capacitor can be optimized to balance the temperature, where four 750 $\mu$ F/450V, four 620 $\mu$ F/450V and one 390 $\mu$ F/450V capacitors are used. The total capacitance of the optimized solution is the same as with the design target and the cost keeps at a comparative level.

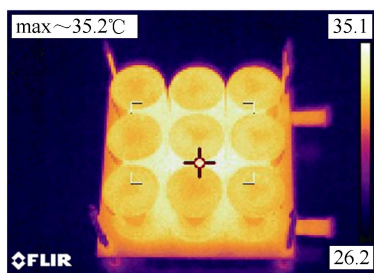
## 4 Advanced active DC links-two-terminal active capacitor

### 4.1 Overview of active DC links

To exceed the limits of power density, capacitance, voltage rating, reliability, and cost, various new capacitor concepts with the aid of active switching circuits have been proposed. The majority of the applications are for DC links, i.e., active DC links. Active DC links are achieved by switching devices



(a) With same capacitance design for each cell



(b) With thermal loading re-distribution

Fig.4 Experimental results of a capacitor bank without and with thermal stress matching solution

and significantly reduced passive components (e.g., capacitors, inductors, or both)<sup>[20-35]</sup>. Its performance depends largely on the active switching circuits and less on the dielectric materials and manufacturing constraints as the passive capacitors. It provides a new perspective to optimize the reliability, cost, or power density less compromised constraints compared to conventional passive capacitor bank design.

The typical active DC link configurations are shown in Fig.5<sup>[25]</sup>.  $AB$  is the DC terminal of the main circuit and  $CD$  is the AC terminal.  $A_{aux}B_{aux}$  is the input terminal of the auxiliary circuit and  $C_{aux}D_{aux}$  is the output terminal. An energy storage element is connected with the output terminal to balance the instantaneous power. Because the buffer capacitor is not directly connected with the DC link having a voltage-ripple constraint, the buffer capacitor can be reduced to allow large voltage ripple. Figs.5(a)~(c) show the solutions connected in series with the main circuit on the DC side. When there is ripple current flowing through the DC-link capacitor, the auxiliary circuit will generate a voltage ripple in order to minimize the DC-link voltage ripple ratio for system specification. Fig.5(d) shows the auxiliary circuit connected in parallel with the main circuit on the DC side. If there is ripple current on the DC link, the auxiliary circuit can be implemented as a current source to compensate the current directly. Therefore, no current and voltage ripple can be observed on the DC link ideally. Figs.5(e) and 5(f) present the auxiliary circuit connected with the main circuit in series and parallel on the AC side. The instantaneous power can be compensated directly on the AC side by instantaneous power calculation, mitigating the ripple on the DC side.

Following the topology derivation method in [25], different topologies with active DC links can be obtained based on the general structures in Fig.5.

### 4.2 A two-terminal active capacitor

Although many active DC links have been proposed in recent decades, they are rarely used in commercial products because of issues with cost, efficiency, and complexity. In order to make an active DC link more practical, a two-terminal active capacitor is proposed with the same level of convenience in use as passive capacitors and the feasibility in achieving better performance in cost, reliability, and/or power density<sup>[23]</sup>.

The two-terminal active capacitor has the following features: ① Has two terminals only without any additional connection because of the proposed control method and the applied self-power circuit, making it possible to be packaged as a conventional capacitor from the end-user's perspective, and ② Has impedance characteristics equivalent to a bulky capacitor or as a variable capacitor within a certain range of frequency depending on the control and switching frequency of its active switches for applications of interest.

In principle, there are various choices of the passive elements and active circuit architectures for the active capacitor. A cost benchmarking of different active DC-link solutions for a 2.2kW single-phase inverter application is presented in [25, 42-43]. The capacitors,

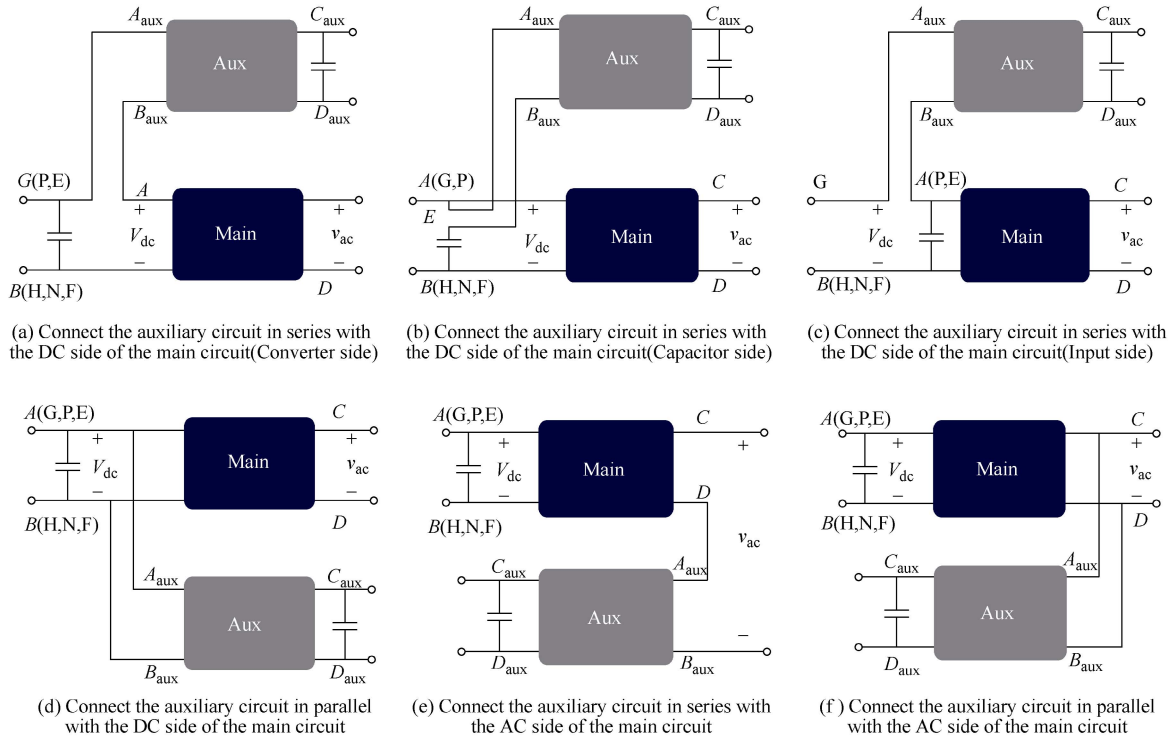


Fig.5 Typical structure diagrams of the active DC link (Aux) connected with the main circuit (Main)<sup>[23]</sup>

inductors, and semiconductor switches used in the inverter are sized with the same design margins and to system-level specifications (e.g., lifetime, output current total harmonic distortions). The results reveal that a few types of active DC links can achieve lower inverter design cost compared to a passive DC link in the scenario of a relatively high reliability requirement, which is relevant to many industry applications. In particular, solutions having a series-connected auxiliary circuit<sup>[45]</sup>, and [46] are the most cost-effective ones. The methods presented in [45] and [46] enable lowest design cost since the auxiliary circuit processes the ripple voltage of the capacitor connected in series to it, and the ripple current of the DC link only. However, none of the active capacitive DC links can be used as a plug-and-play active capacitor, since they have more terminals than a conventional capacitor, e.g., connections to an external power source for gate drivers and controller, and/or external feedback signals from the main circuits.

The circuit diagram of the two-terminal active capacitor is shown in Fig.6.  $v_{AB}$  and  $i_{AB}$  are the voltage and ripple current of the active capacitor, respectively. It consists of active switches, passive elements, a sampling and conditioning circuit, and self-powered controller and gate drivers. There are two power terminals A and B only, making it as convenient as a conventional passive capacitor from application point of view. As shown in Fig.6, the full-bridge circuit processes the ripple voltage and ripple current of  $C_1$  only, implying a low VA rating. A voltage control strategy is proposed based on internal voltage signals  $v_{C1}$  and  $v_{C2}$  only, as shown in Fig.6, which does not require any current information from external circuits. Therefore, it enables fully independent operation of the active capacitor without any feedback signals from external circuits. The control objective is to shape the impedance seen from AB terminals to be that

of an equivalent passive capacitor of interest. The experimental prototype of the two-terminal active capacitor is shown in Fig.7. Based on the specification of the case study, the impedance curves of the active capacitor and the comparable passive capacitor are shown in Fig.8. For a frequency at 120Hz or above, the impedance of the active capacitor is equivalent or lower than a passive capacitor with 34.4J rated energy storage. It implies that the active capacitor can achieve the same or even better harmonic filtering with 16.9% energy storage compared to a passive capacitor.

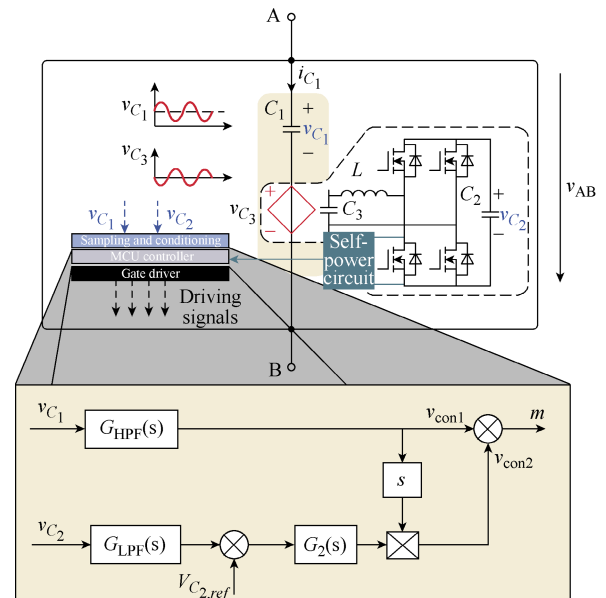


Fig.6 An implementation of the two-terminal active capacitor with a voltage control strategy<sup>[23]</sup> ( $v_{C1}$ ,  $v_{C2}$  and  $v_{C3}$  are capacitor voltages.  $G_{HPF}(s)$  and  $G_{LPF}(s)$  is the high pass filter(HPF) and low pass filter(LPF), respectively.  $G_2(s)$  is the voltage controller for stabilizing  $v_{C2}$ )

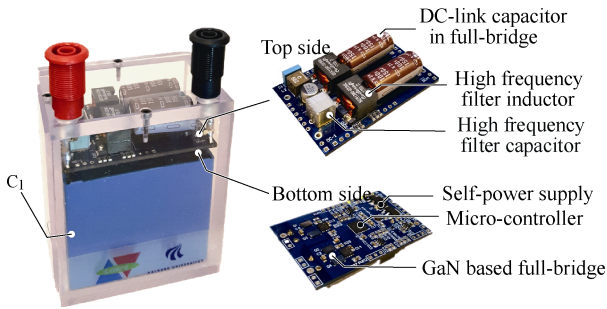


Fig.7 Prototype of the two-terminal active capacitor

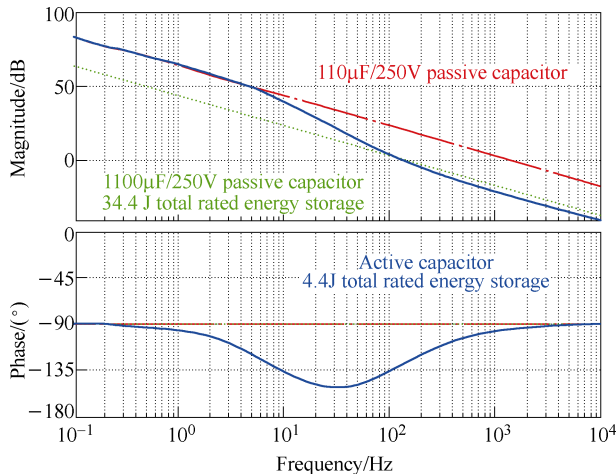


Fig.8 Bode diagram of the impedance of the active capacitor in the DC-link application<sup>[23]</sup>

## 5 Conclusions

The scientific challenges and existing studies on capacitive DC links are discussed in this paper. Among others things, the reliability aspect is especially addressed. Electro-thermal and lifetime modeling of capacitors to support model-based sizing and optimization of capacitor banks are presented. Two ways for useful lifetime matching of individual capacitors in a bank are briefly introduced with a case study. Besides passive solutions, the concepts and corresponding implementations of active capacitors are reviewed. A DC link with a two-terminal active capacitor is demonstrated by a case study, which represents the state-of-the-art active capacitive DC link solutions. From the authors' perspective, further research is needed to address the following scientific challenges in the topic discussed in this paper:

(1) Better mission profile data is needed to have better analysis of the actual stress levels of capacitors in power electronic applications. While extensive research has been done on the modeling of ripple current stress and internal temperature rise of capacitors, little study has been done on the modeling of the capacitor ambient temperature, which is affected by the heat dissipation of adjacent components, cooling system, and enclosure design, besides the environmental conditions. The capacitor bank thermal modeling discussed in this paper is an example of this effort. System-level thermal modeling and long-term mission profile data are essential to the capacitor ambient temperature profile analysis.

(2) There is still a lack of study on the impact of humidity and mechanical stresses on the wear out of capacitors, and on the catastrophic failure of capacitors due to single-event extreme stress. Besides the thermal-related failure mechanisms presented in this paper, an understanding of the above failure mechanism will help to have a more comprehensive reliability analysis of capacitors.

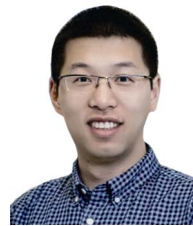
(3) Solid proof of the reliability performance of active capacitive DC links is absent in literature, even though theoretical analysis shows the potential benefits. The two-terminal active capacitor concept enables not only the same level of convenience in use as passive capacitors, but also can be used to perform the accelerated degradation testing, which provides an opportunity for an experimentally comparative study on the reliability performance of active DC links and passive DC links.

## References

- [1] H. Wang, and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters-an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569-3578, Sep. 2014.
- [2] F. Zare, H. Soltani, D. Kumar, P. Davari, H. A. M. Delpino, and F. Blaabjerg, "Harmonic emissions of three-phase diode rectifiers in distribution networks," *IEEE Access*, vol. 5, pp. 2819-2833, 2017.
- [3] X. Pei, W. Zhou, and Y. Kang, "Analysis and calculation of DC-link current and voltage ripples for three-phase inverter with unbalanced load," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5401-5412, Oct. 2015.
- [4] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-compact power pulsation buffer for single-phase DC/ac converter systems," *Proc. IEEE ECCE Asia*, May 2016, pp. 2732-2741.
- [5] G. Zhu, S. C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 779-792, Feb 2013.
- [6] W. Liu, K. Wang, H. S. H. Chung, and S. T. H. Chuang, "Modeling and design of series voltage compensator for reduction of DC-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534-2548, May 2015.
- [7] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Select. Topics Power Electron.*, vol. 2, no. 1, pp. 97-114, March 2014.
- [8] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of DC/DC converters for a backup power application," *IEEE Trans. on Power Electron.*, vol. 33, no. 9, pp. 8030-8039, Sept. 2018.
- [9] H. S. H. Chung, H. Wang, F. Blaabjerg, and M. Pecht, *Reliability of Power Electronic Converter Systems*. IET, 2015.
- [10] H. Wang, Y. Yang, and F. Blaabjerg, "Reliability-oriented design and analysis of input capacitors in single-phase transformerless photovoltaic inverters," *Proc. IEEE APEC*, pp. 2929-2933, Mar. 2013.
- [11] H. Wang P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of DC-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Trans. Power Electron.*, in press.
- [12] B. Sun, X. Fan, C. Qian, and G. Zhang, "Pof-simulation-assisted reliability prediction for electrolytic capacitor in LED drivers," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6726-6735, Nov. 2016.
- [13] A. Fatemi, and L. Yang, "Cumulative fatigue damage and life prediction theories: a survey of the state of the art for homogeneous materials," *International Journal of Fatigue*, vol. 20, no. 1, pp. 9-34, 1998.
- [14] S. G. Parler, "Deriving lifet multipliers for electrolytic capacitors," *IEEE Power Electronics Society Newsletter*, vol. 16, no. 1, Feb.



- 2004, pp. 11-12.
- [15] K. Lee, T. M. Jahns, G. Venkataramanan, and W. E. Berkopec, "DC-bus electrolytic capacitor stress in adjustable-speed drives under input voltage unbalance and sag conditions," *IEEE Trans. Ind. Appl.*, vol. 43, no. 2, pp. 495-504, Mar. 2007.
- [16] J. Rajmond, and P. Dan, "Thermal modeling of through hole capacitors," *Proc. IEEE SIITME*, pp. 227-232, Oct. 2012.
- [17] M. L. Gasperi, and N. Gollhardt, "Heat transfer model for capacitor banks," *Proc. IEEE Industry Applications Conference*, vol. 2, pp. 1199-1204, Oct. 1998.
- [18] H. Wang, and H. Wang, "Reliability evaluation and optimization of capacitor bank," *Proc. IEEE ECCE*, in press.
- [19] P. Pelletier, J. M. Guichon, J. L. Schanen, and D. Frey, "Optimization of a DC capacitor tank," *IEEE Trans. Ind. App.*, vol. 45, no. 2, pp. 880-886, Mar. 2009.
- [20] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711-2726, June 2013.
- [21] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778-4794, July 2016.
- [22] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Correa, "Low-frequency power decoupling in single-phase applications: a comprehensive overview," *IEEE Tran. Power Electron.*, vol. 32, no. 4, pp. 2892-2912, April 2017.
- [23] H. Wang, and H. Wang, "A two-terminal active capacitor," *IEEE Trans. on Power Electron.*, vol. 32, no. 8, pp. 5893-5896, Aug. 2017.
- [24] H. Wang, and H. Wang, "A two-terminal active inductor with minimum apparent power for the auxiliary circuit," *IEEE Trans. on Power Electron.*, in press.
- [25] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "A generic topology derivation method for single-phase converters with active capacitive DC-links," *Proc. IEEE ECCE*, pp. 1-8, 2016.
- [26] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos, and D. Boroyevich, "Study of energy storage capacitor reduction for single phase PWM rectifier," *Proc. IEEE APEC*, Feb 2009, pp. 1177-1183.
- [27] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," *Proc. IEEE EPE*, Sept 2007, pp. 1-10.
- [28] X. Cao, Q. C. Zhong, and W. L. Ming, "Analysis and control of ripple eliminators in DC systems," *Proc. IEEE Green Tech. Conf.*, April 2014, pp. 29-36.
- [29] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308-1319, March 2013.
- [30] Y. Xia, J. Roy, and R. Ayyanar, "A high performance T-type single phase double grounded transformer-less photovoltaic inverter with active power decoupling," *Proc. IEEE ECCE*, pp. 1-7, Sept 2016.
- [31] W. Qi, S. Li, Siew-Chong-Tan, and S. Y. R. Hui, "A two-switch buck-boost PFC rectifier with automatic ac power decoupling capability," *Proc. IEEE ECCE*, pp. 1-7, 18, Sept 2016.
- [32] S. Li, W. Qi, S. C. Tan, S. Y. R. Hui, and C. Tse, "A general approach to programmable and reconfigurable emulation of power impedances," *IEEE Tran. Power Electron.*, vol. 33, no. 1, pp. 259-271, Jan. 2018.
- [33] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690-4698, Nov 2012.
- [34] M. Chen, K. K. Afridi, and D. J. Perreault, "Stacked switched capacitor energy buffer architecture," *Proc. IEEE APEC*, pp. 1404-1413, Feb 2012.
- [35] G. Zhu, H. Wang, B. Liang, S. Tan, and J. Jiang, "Enhanced single-phase full-bridge inverter with minimal low-frequency current ripple," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 937-943, Feb. 2016.
- [36] W. J. Minford, "Accelerated life testing and reliability of high K multilayer ceramic capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. CHMT-5, no. 3, pp. 297-300, Sep. 1982.
- [37] C. Hillman, Uprating of Ceramic Capacitors. DfR Solution white paper.
- [38] N. Kubodera, T. Oguni, M. Matsuda, H. Wada, N. Inoue, and T. Nakamura, "Study of the long term reliability for MLCCs," *Proceedings of CARTS International*, pp. 1-9, 2012.
- [39] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of igbts in a pv inverter under a long-term operation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7171-7182, Oct. 2016.
- [40] CDE Cornell Dubilier, Aluminum Electrolytic Capacitors Application Guide.
- [41] Nippon-Chemi-con, "Aluminum capacitors group chart," Available: <https://www.chemi-con.co.jp/e/catalog/pdf/al-e/al-sepa-e/001-guide/al-groupchart-e-171001.pdf>, 2017.
- [42] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "Cost assessment of three power decoupling methods in a single-phase power converter with a reliability oriented design procedure," *Proc. IEEE ECCE Asia*, pp. 3818-3825, May 2016.
- [43] R. Burkart, and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," *Proc. IEEE ECCE*, pp. 2139-2146, Sept 2013.
- [44] A. Anurag, Y. Yang, and F. Blaabjerg, "Thermal performance and reliability analysis of single-phase PV inverters with reactive power injection outside feed-in operating hours," *IEEE J. of Emerg. and Select. Topics in Power Electron.*, vol. 3, no. 4, pp. 870-880, Dec 2015.
- [45] T. Tanaka, and S. Funabiki, "A new method of damping harmonic resonance at the DC-link of a large-capacity rectifier-inverter system," *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, Apr. 1999, vol. 2, pp. 888-893.
- [46] S. Qin, Y. Lei, C. Barth, W. C. Liu, and R. Pilawa-Podgurski, "A high power density series-stacked energy buffer for power pulsation decoupling in single-phase converters," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4905-4924, Jun. 2017.



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