Comparison of DSCC and SDBC Modular Multilevel Converters for STATCOM Application During Negative Sequence Compensation

Cupertino, A. F.; Farias, J. V. M.; Pereira, H. A.; Seleme, S. I.; Teodorescu, R.

Published in:
IEEE Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2018.2811361

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

Comparison of DSCC and SDBC Modular Multilevel Converters for STATCOM application during negative sequence compensation

Allan F. Cupertino, *Member*, João V. M. Farias, Heverton A. Pereira, *Member*, Seleme I. Seleme Junior, and Remus Teodorescu, *Fellow Member*

***Abstract*—Among the various topologies proposed in literature, the Modular Multilevel Converter (MMC) is considered the next generation of converters for medium and high voltage applications. This paper presents a comparison between two variants of modular multilevel converters for STATCOM applications: The Double-Star Chopper Cell (DSCC-MMC) and the Single-Delta Bridge Cell (SDBC-MMC). These converter topologies are compared and benchmarked during positive and negative sequence compensation. The comparisons are supported by analytical results regarding minimum effective dc-link voltage, number of cells, current rating, energy storage requirements and operation during unbalanced conditions. The dynamic behavior, power losses and cost of both solutions are evaluated through simulation model of a 15 MVA MMC STATCOM.**

***Index Terms*—Modular Multilevel Converter, STATCOM, Positive and negative sequence injection, Power losses, Costs.**

I. Introduction

NOWADAYS, the large number of nonlinear/unbalanced loads in the medium voltage (MV) systems (arc furnaces, MV electric drives, etc) and the massive penetration of renewable energy systems have driven the interest in MV STATCOMs applications. Once MV levels must be reached with standard rated semiconductor devices, multilevel converter structures are employed [1]. Among the various topologies proposed in literature, the Modular Multilevel Converter (MMC) is considered the next generation of converters for medium and high voltage applications. The MMC topology is based on cascaded connection of many smaller voltage cells (or submodules - SMs), in order to reach the required voltage.

The MMC family is usually classified into four topologies [2]: Single-Star Bridge Cell (SSBC), Single-Delta Bridge Cell (SDBC), Double-Star Chopper Cell (DSCC) and Double-Star Bridge Cell (DSBC). The circuit diagrams of these topologies are presented in Fig. 1. Generally, the DSBC topology is unsuitable for STATCOM applications, due to its higher number of power devices in comparison with the other topologies. Moreover, the SSBC-MMC topology does not have circulating current [2]. Thereby, the capacitor voltage balancing in SSBC topology must be performed through zero sequence voltage. For this reason, the capacitor voltage balancing during negative sequence injection and power unbalances is limited by the voltage rating of the converter, as mentioned in references [3], [4].

Since SDBC and DSCC topologies present circulating current [2], [5], they are the most attractive for STATCOM applications [2], [5]. Therefore, many works in literature propose control algorithms and design methodologies regarding these topologies [1], [3], [6]–[8].

Nevertheless, few works in literature present a comparison between SDBC and DSCC topologies for STATCOM applications. Reference [2] only discusses the differences in terms of the number of SMs. Additionally, reference [5] compares the losses and costs of SDBC and DSCC topologies for STATCOM application based on a 100 MVA case study. However, the SM capacitances are designed using different approaches and the comparisons are not presented analytically. Finally, it is not presented any comparison related with the energy storage requirements. Also, in terms of converter losses, it only includes the power semiconductor device contributions.

In fact, a fair comparison between SDBC and DSCC topologies regarding STATCOM applications cannot be found in literature. This work aimed to fill this void, by means of the following contributions:

- Comparison of topologies, considering the number of SMs, effective dc-link voltage, circulating current behavior and current rating. These comparisons are supported by analytical results;
- Definition and comparison of the energy storage requirements of both topologies when negative sequence

Manuscript received Month xx, 2xxx; revised Month xx, xxxx; accepted Month x, xxxx. This work was supported by the Brazilian agencies CAPES, CNPq and FAPEMIG.

A. F. Cupertino and S. I. Seleme Junior are with the Graduate Program in Electrical Engineering, Federal University of Minas Gerais, Belo Horizonte, MG, 31270-901 Brazil. A. F. Cupertino is also with the Department of Materials Engineering, Federal Center for Technological Education of Minas Gerais, Belo Horizonte, MG, 30421-169 Brazil (e-mails: afcupertino@ieee.org; seleme@cpdee.ufmg.br).

J. V. M. Farias and H. A. Pereira are with the Department of Electrical Engineering, Universidade Federal de Viçosa, Viçosa, MG, 36570-900 Brazil (e-mail: joao.farias@ufv.br; heverton.pereira@ufv.br).

R. Teodorescu is with the Department of Energy Technology, Aalborg University 9220 Aalborg, Denmark, and also with the Department of Energy and Environment, Division of Electric Power Engineering, Chalmers University of Technology, SE 41296 Gothenburg, Sweden (e-mail: ret@et.aau.dk).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2811361, IEEE Transactions on Industrial Electronics

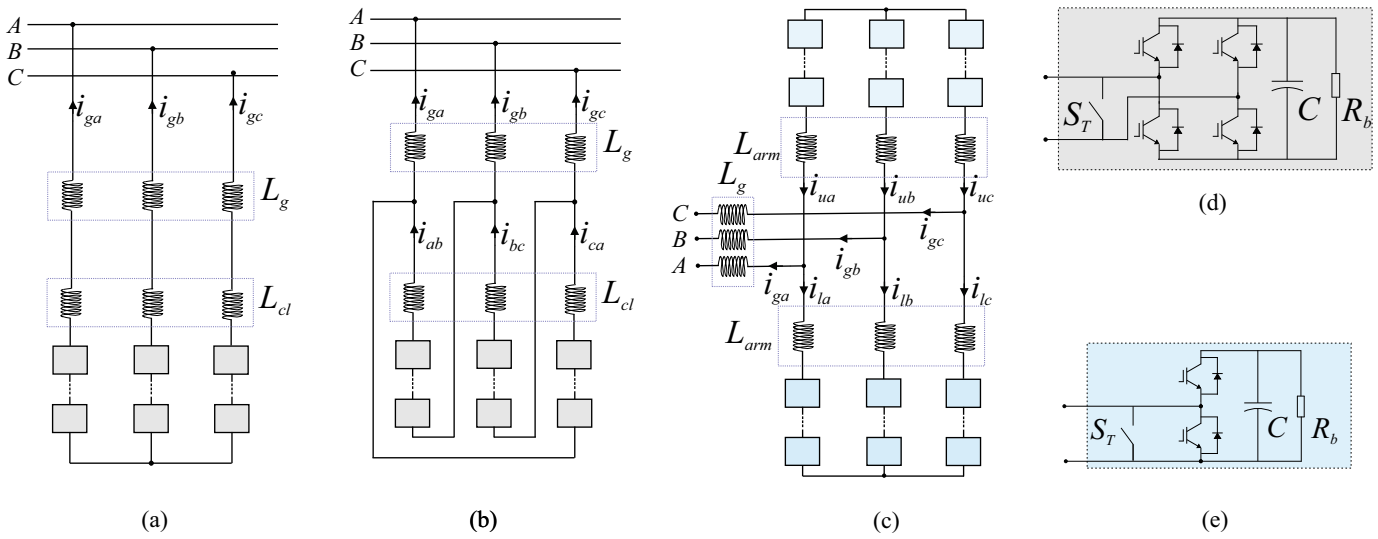

Fig. 1. Classification of MMC topologies: (a) SSBC topology; (b) SDBC topology; (c) DSCC or DSBC topology (dependent on the SM employed); (d) Full-bridge SM employed in SSBC, SDBC and DSBC topologies; (e) Half-bridge SM employed in DSCC topology.

currents are compensated;
- Evaluation of dynamic behavior, power losses and cost, considering a 15 MVA case study.

This work is outlined as follows. Section II presents the structure and control strategy for a MMC STATCOM, considering the DSCC and SDBC topologies. The design of both topologies is described in section III. Section IV presents the case study and the parameters employed in the simulations. Section V provides the results obtained and the comparison regarding dynamic behavior, circulating current requirements, losses and costs. Section VI presents the discussion of the results. The conclusions are stated in section VII.

II. MMC STATCOM Topologies

The SDBC MMC STATCOM is illustrated in Fig. 1 (b) while the DSCC MMC STATCOM is illustrated in Fig. 1 (c). In order to employ different nomenclature, it is considered that the DSCC topology presents 6 arms, while the SDBC topology presents 3 clusters. The inductances L_{arm} and L_{cl} are responsible to reduce the high order harmonics in the circulating current and to limit the currents during faults [2], [9]. The converters are connected to the main grid through a three-phase transformer with inductance L_g. The DSCC topology presents N_{2Y} SMs per arm, while the SDBC topology presents N_{Δ} SMs per cluster.

Figs. 1 (d) and (e) illustrate the SM employed in each topology. Generally there is a permanent by-pass switch S_T (usually a thyristor) in parallel with each SM, which is responsible for bypassing it in case of failures [10]. R_b represents the bleeder resistor, responsible to discharge the SM capacitor when the converter is turned off. C is the capacitance of each SM.

Since this work is focused in the STATCOM application, the control strategy needs to work during unbalanced conditions. Therefore, the grid voltage is assumed given by:

$$v_g = \widehat{V}^+ \cos(\omega_n t + \delta^+ + \theta_v) + \widehat{V}^- \cos(\omega_n t + \delta^- - \theta_v), \quad (1)$$

where $\widehat{V}^+$ and $\widehat{V}^-$ are the amplitudes of positive and negative sequence components of line voltage, respectively. Additionally, δ^+ and δ^- are the positive and negative sequence voltage angles, respectively. Finally, $\theta_v \in \{-\frac{2\pi}{3}, 0, \frac{2\pi}{3}\}$ refers to the phase angle of each phase and ω_n is the grid frequency.

Furthermore, the grid currents are given by:

$$i_g = \widehat{I}^+ cos(\omega_n t + \phi^+ + \theta_v) + \widehat{I}^- cos(\omega_n t + \phi^- - \theta_v), \quad (2)$$

where $\widehat{I}^+$ and $\widehat{I}^-$ are the amplitudes of positive and negative sequence currents, respectively. Finally, ϕ^+ and ϕ^- are the positive and negative sequence current angles, respectively.

The grid current control strategy is presented in Fig. 2 (a). This strategy is employed for both DSCC and SDBC. The external loop controls the square of the average voltage v_{avg} of all SMs of the converter. This loop calculates the amount of active power P^* which needs to flow to the converter. The average voltage is computed by:

$$v_{avg} = \frac{1}{N_T} \sum_{i=1}^{N_T} v_{sm,i}, \quad (3)$$

where $v_{sm,i}$ is the ith SM voltage. N_T is the total number of operating SMs in the MMC.

The internal loops control the currents injected into the grid. The structure is implemented in stationary reference frame ($\alpha\beta$) based on proportional resonant controllers. Feed-forward actions of the grid voltage are included in order to improve the dynamic behavior. The current reference is computed by:

$$\begin{bmatrix} i^*_{g\alpha} \\ i^*_{g\beta} \end{bmatrix} = \frac{1}{(v^+_{g\alpha})^2 + (v^+_{g\beta})^2} \begin{bmatrix} v^+_{g\alpha} & v^+_{g\beta} \\ v^+_{g\beta} & -v^+_{g\alpha} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix} + \begin{bmatrix} i^-_{g\alpha} \\ i^-_{g\beta} \end{bmatrix}, \quad (4)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2811361, IEEE Transactions on Industrial Electronics

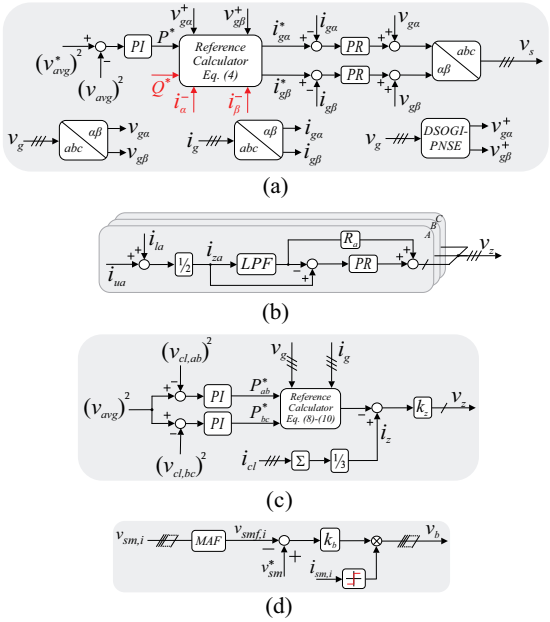

Fig. 2. Control Strategies of MMC STATCOM topologies: (a) Grid current control - DSCC and SDBC; (b) Circulating current control - DSCC; (c) Circulating current control - SDBC; (d) Individual balancing control - DSCC and SDBC.

where $v_{g\alpha}^{+}$ and $v_{g\beta}^{+}$ are the positive sequence components of grid voltage represented in stationary reference frame. These components are obtained through a positive and negative sequence extractor based on the double second-order generalized integrator (DSOGI-PNSE), proposed by [11]. The references Q^*, $i_{g\alpha}^{-}$ and $i_{g\beta}^{-}$ are dependent on the application. For example, in the case of reactive power and unbalance compensation of local loads, these values are obtained from the load current [12]. In the case of voltage support or low-voltage ride-through (LVRT) operation, these variables will be obtained through droop controllers [13]. Nevertheless, the obtainment of these variables exceeds the scope of this work, and the references are directly given to the controllers.

Regarding the DSCC topology, the circulating current per phase is given by:

$$i_z = \frac{i_u + i_l}{2}, \tag{5}$$

where i_u and i_l are the currents in the upper and lower arms, respectively. The circulating current control for DSCC topology is presented in Fig. 2 (b). As stated in [9], the circulating current dynamics is stable. However, it presents a small damping related to the arm inductor resistance R_a. Therefore, a circulating current loop based on a proportional resonant controller is implemented in order to increase the damping and compensate the second order harmonic that appears during negative sequence compensation [8].

On the other hand, the circulating current of the SDBC topology is given by:

$$i_z = \frac{1}{3}\left(i_{ab} + i_{bc} + i_{ca}\right). \tag{6}$$

As observed, the circulating current in SDBC topology is the zero sequence current. The circulating current control employed in this work, as proposed by [3], is presented in Fig. 2 (c). The cluster voltage balancing control calculates the reference value of the circulating current. The cluster voltages are calculated by:

$$v_{cl} = \frac{1}{N_\Delta}\sum_{j=1}^{N_\Delta} v_{sm,j}, \tag{7}$$

The square value of the cluster voltages are controlled. In this case, the outputs of the PI controllers are the power disturbances in the clusters, denoted by P_{ab}^* and P_{bc}^*. According to [3], the circulating current reference can be calculated by:

$$i_z = \widehat{I}^z \cos\left(\omega_n t + \varphi^z\right), \tag{8}$$

where:

$$I^z = \frac{P_{ab}^* - A}{X_1\cos(\varphi^z) + X_2\sin(\varphi^z)} = \frac{P_{bc}^* - B}{X_3\cos(\varphi^z) + X_4\sin(\varphi^z)},$$
$$\tan(\varphi^z) = \frac{(P_{bc}^* - B)X_1 - (P_{ab}^* - A)X_3}{(P_{ab}^* - A)X_4 - (P_{bc}^* - B)X_2}, \tag{9}$$

and

$$A = \frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \phi^- + \frac{\pi}{3}) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(\delta^- - \phi^+ - \frac{\pi}{3}),$$
$$B = \frac{\widehat{V}^+\widehat{I}^-}{2}\cos(\delta^+ - \phi^- - \pi) + \frac{\widehat{V}^-\widehat{I}^+}{2}\cos(\delta^- - \phi^+ + \pi),$$
$$X_1 = \frac{\sqrt{3}}{2}\widehat{V}^+\cos(\delta^+ + \frac{\pi}{6}) + \frac{\sqrt{3}}{2}\widehat{V}^-\cos(\delta^- - \frac{\pi}{6}),$$
$$X_2 = \frac{\sqrt{3}}{2}\widehat{V}^+\sin(\delta^+ + \frac{\pi}{6}) + \frac{\sqrt{3}}{2}\widehat{V}^-\sin(\delta^- - \frac{\pi}{6}),$$
$$X_3 = \frac{\sqrt{3}}{2}\widehat{V}^+\cos(\delta^+ - \frac{\pi}{2}) + \frac{\sqrt{3}}{2}\widehat{V}^-\cos(\delta^- + \frac{\pi}{2}),$$
$$X_4 = \frac{\sqrt{3}}{2}\widehat{V}^+\sin(\delta^+ - \frac{\pi}{2}) + \frac{\sqrt{3}}{2}\widehat{V}^-\sin(\delta^- + \frac{\pi}{2}). \tag{10}$$

A proportional controller is employed in this case to follow the reference of circulating current, as suggested by references [3], [7]. Therefore, the voltage command v_z is obtained.

The reference voltages v_s and v_z are inputs of the modulation strategy. For both topologies, the phase-shift pulse width modulation (PS-PWM) is considered. For DSCC topology, the addition of $1/6$ of third harmonic in the phase voltages is considered [14]. When the PS-PWM method is employed, an extra individual balancing control loop is necessary to maintain the capacitor voltages following the reference v_{sm}^* [15], as illustrated in Fig. 2 (d). Since the ac component included in v_{sm} is a disturbance, it should be eliminated by a moving-average filter [16]. A proportional controller k_b is employed.

The design of the studied topologies is presented in the next section. The approach is based on the steady-state conditions. Thus, the control strategy discussed in this section does not result in loss of generality and other control strategies can also be addressed.

III. Design methodology

This section presents the design of both DSCC and SDBC topologies. The case study considers a 15 MVA STATCOM connected to a 13.8 kV system. The design methodology is focused in applications where positive and negative sequence reactive power compensations are necessary, as in grid voltage regulation and renewable energy systems.

A. Effective dc-link voltage and number of SMs

Despite the absence of physical dc-link in SDBC MMC-STATCOM, the effective dc-link voltage is an important parameter to avoid overmodulation [1]. According to [5], the minimum value of the effective dc-link voltage is given by:

$$V_{dc,2Y} = \frac{2\sqrt{2}}{\sqrt{3}(1 - E_{dc} - \Delta V_{dc})} \frac{V_s}{\lambda_{2Y} m_{max}}, \tag{11}$$

$$V_{dc,\Delta} = \frac{\sqrt{2}}{(1 - E_{dc} - \Delta V_{dc})} \frac{V_s}{\lambda_{\Delta} m_{max}}, \tag{12}$$

where $\Delta V_{dc}(\%)$ is the dc-link voltage ripple in the worst case and $E_{dc}(\%)$ is the error in the average value in steady-state. Furthermore, the maximum modulation index m_{max} is determined according to the carrier frequency f_c and the minimum IGBTs on-time and dead-time T_d [1]. The modulation gain λ is included in order to extend the analysis to different modulation strategies.

The minimum line-to-line voltage (rms) synthesized by the converter V_s is calculated according to the grid voltage V_g and the maximum per unit value of the output impedance x_{eq}. Perceptual variations in these variables are assumed. Therefore, V_s is given by:

$$V_s = [(1 + \Delta V_g) + x_{eq}(1 + \Delta x_{eq})]V_g, \tag{13}$$

The number of SMs is determined according to the effective dc-link voltage V_{dc} by:

$$N_{2Y} = \frac{1}{f_{us}} \frac{V_{dc,2Y}}{V_{svc}}, \tag{14}$$

$$N_{\Delta} = \frac{1}{f_{us}} \frac{V_{dc,\Delta}}{V_{svc}}, \tag{15}$$

where f_{us} is defined by the ratio between the reference voltage of SMs v^*_{sm} and semiconductor device voltage class V_{svc}. Manufactures suggest that semiconductor devices cannot operate with voltages above 60 % of V_{svc} [17].

In fact, the ratio between the SM number of SDBC and DSCC topologies K_N can be expressed by:

$$K_N = \frac{N_{\Delta}}{N_{2Y}} = \frac{V_{dc,\Delta}}{V_{dc,2Y}} = \frac{\sqrt{3}}{2} \frac{\lambda_{2Y}}{\lambda_{\Delta}}. \tag{16}$$

As observed, if the same modulation gain is employed for both topologies, $K_N \approx 0.87$ and the SDBC topology presents 13% less SMs. Regarding the modulation strategies, reference [18] shows that when zero sequence voltage components are employed, the dc-link voltage utilization is improved and the zero sequence signal is canceled in the line voltages. This study was originally proposed in 2-level converters, however, it can be extended for other topologies which also does not have path for zero sequence current flow. Therefore, the use of zero sequence signals can be approached for DSCC-MMC topology. On the other hand, the sinusoidal modulation is more suitable for SDBC-MMC topology since it presents a path for zero sequence current flow.

Considering the modulation with injection of $1/6$ of third harmonic for DSCC, $\lambda_{2Y} = 1.15$. In this work, $\Delta V_g = \Delta X_{eq} = 0.05$, $X_{eq} = 0.15$, $\Delta V_{dc} = 0.1$, $E_{dc} = 0.03$ and $T_d = 1.5\mu s$. In such conditions, $V_s \approx 16.7kV$. Therefore, the approximate value of the effective dc-link voltage is $V_{dc,2Y} = 28kV$. For SDBC, considering the sinusoidal modulation, $\lambda_{\Delta} = 1$. Therefore, the approximate value for the effective dc-link voltage is $V_{dc,\Delta} = 28kV$. Thereby, considering semiconductors with voltage class of 3.3 kV and $f_{us} = 0.5$, $N_{2Y} = N_{\Delta} = 17$.

Finally, the total number of semiconductor switches is given by:

$$N_s = 12N_{2Y,\Delta}. \tag{17}$$

Therefore, if $N_{2Y} = N_{\Delta}$, the topologies will present the same number of semiconductor switches.

B. Arm and Cluster Currents

Considering that the harmonic components in the circulating current are suppressed, the circulating current for DSCC topology can be expressed by [12]:

$$i_{z,2Y} = \frac{\widehat{V}^+}{2V_{dc,2Y}} \left[\widehat{I}^+ cos(\delta^+ - \phi^+) + \widehat{I}^- cos(\delta^+ - \phi^- - \theta_v)\right] + \frac{\widehat{V}^-}{2V_{dc,2Y}} \left[\widehat{I}^+ cos(\delta^- - \phi^+ + \theta_v) + \widehat{I}^- cos(\delta^- - \phi^-)\right]. \tag{18}$$

The maximum value of the upper arm current is given by [8]:

$$\max(i_u) = \max(i_z) + \frac{1}{2}\max(i_g). \tag{19}$$

In this first analysis, for simplification, the grid voltage is assumed balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. Therefore, $\widehat{V}^- \approx 0$. Thus, the peak value of arm current is given by:

$$\max(i_u) = \widehat{I}_n \left(\frac{1}{2} + \frac{\lambda_{2Y} m_{max}}{4}\right) \approx \frac{3}{4}\widehat{I}_n, \tag{20}$$

where

$$\widehat{I}_n = \frac{\sqrt{2}}{\sqrt{3}} \frac{S_n}{V_g}, \tag{21}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2811361, IEEE Transactions on Industrial Electronics

and S_n is the STATCOM nominal power.

For SDBC, the maximum value of cluster currents can be expressed as [7]:

$$\max(i_{cl}) = \frac{2}{\sqrt{3}}\widehat{I}_n. \tag{22}$$

Thereby, the topologies can be compared through the current ratio K_I, given by:

$$K_I = \frac{\max(i_u)}{\max(i_{cl})} \approx \frac{3\sqrt{3}}{8}, \tag{23}$$

As observed, the SDBC current rating is 54 % larger than the DSCC topology.

C. SM capacitance

The SM capacitance can be designed based on the converter energy storage requirements. According to [14], the minimum SM capacitance for DSCC topology is given by:

$$C_{2Y} = \frac{2N_{2Y}E_{2Y}}{V_{dc,2Y}^2}. \tag{24}$$

E_{2Y} is the minimum value of the nominal energy storage per arm. Considering only the upper arm due to symmetry, E_{2Y} is given by [14]:

$$E_{2Y} = \frac{\Delta E_{2Y}}{k_{max}^2 - \max(\frac{n_u^2 - e_{u,v}k_{max}^2}{1-e_{u,v}})}, \tag{25}$$

where k_{max} defines the upper limit of the capacitor voltages. Typically, $k_{max} = 1.1$ is employed. Finally:

$$n_u = \frac{v_u}{V_{dc,2Y}}, \tag{26}$$

$$e_{u,v} = \frac{e_u}{\Delta E_{2Y}}. \tag{27}$$

where $\Delta E_{2Y} = max(e_u)$ is the maximum energy variation and v_u is the upper arm inserted voltage. For SDBC, similar relations can be derived where e_u is substituted by e_{cl}.

As observed, the energy variations e_u and e_{cl} must be known in order to complete the design methodology. These energy variations can be obtained from:

$$\begin{aligned} e_u &= \int p_u dt = \int v_u i_u dt, \\ e_{cl} &= \int p_{cl} dt = \int v_{cl} i_{cl} dt. \end{aligned} \tag{28}$$

Therefore, expressions for the instantaneous power are derived. The analysis is accomplished per phase and the most stressed one is considered in the design. For the sake of simplification, the grid voltage is assumed balanced and the negative sequence voltage synthesized by the converter is considered much smaller than the synthesized positive sequence. For DSCC topology, assuming the injection of $1/6$ of third harmonic component, the upper arm inserted voltages can be expressed as [14]:

$$v_u = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} m\cos(\omega_n t + \theta_v) + \frac{V_{dc}}{12} m\cos(3\omega_n t). \tag{29}$$

Furthermore, the upper arm current for DSCC topology is given by [8]:

$$i_u = i_z + \frac{i_g}{2}. \tag{30}$$

The energy variation in the upper arm can be obtained by performing the integration. Accordingly:

$$e_u = \frac{S_n}{12\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2u}\right] + \frac{S_n}{12m\omega_n}\left[\frac{\widehat{I}^+}{\widehat{I}_n} f_{3u} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{4u}\right] \tag{31}$$

where

$$\begin{aligned} f_{1u} &= \frac{m}{9}\cos(\varphi^+)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^+ - \theta_v) \\ &\quad + \frac{1}{12}\sin(4\omega_n t + \varphi^+ + \theta_v), \\ f_{2u} &= \frac{m}{9}\cos(\varphi^- - \theta_v)\sin(3\omega_n t) + \frac{1}{6}\sin(2\omega_n t - \varphi^- + \theta_v) \\ &\quad + \frac{1}{12}\sin(4\omega_n t + \varphi^- - \theta_v), \\ f_{3u} &= -2m^2\cos(\varphi^+)\sin(\omega_n t + \theta_v) \\ &\quad -m\sin(2\omega_n t + \varphi^+ + 2\theta_v) + 4\sin(\omega_n t + \varphi^+ + \theta_v), \\ f_{4u} &= -2m^2\cos(\varphi^- - \theta_v)\sin(\omega_n t + \theta_v) \\ &\quad -m\sin(2\omega_n t + \varphi^-) + 4\sin(\omega_n t + \varphi^- - \theta_v). \end{aligned} \tag{32}$$

Once ΔE_{2Y} and E_{2Y} are proportional to the converter rated power, the converter energy storage requirements can be expressed by:

$$W_{2Y} = \frac{6}{S_n} E_{nom}, \tag{33}$$

where W_{2Y} is the required energy storage per MVA.

For SDBC, the inserted voltages are given by [7]:

$$v_{cl} = mV_{dc}\cos(\omega_n t + \theta_v + \frac{\pi}{6}). \tag{34}$$

Therefore, the energy storage variation per cluster is given by:

$$e_{cl} = \frac{S_n}{6m\omega_n}\Big[\frac{\widehat{I}^+}{\widehat{I}_n} f_{1cl} + \frac{\widehat{I}^-}{\widehat{I}_n} f_{2cl}\Big], \tag{35}$$

where

$$\begin{aligned} f_{1cl} &= m\sin(2\omega_n t - \varphi^+ - \theta_v + \frac{\pi}{3}), \\ f_{2cl} &= -m\sin(2\omega_n t + \varphi^- + \theta_v - \frac{\pi}{3}) + m\sin(2\omega_n t - \varphi^-). \end{aligned} \tag{36}$$

Therefore, the energy storage requirements for SDBC topology can be expressed by:

$$W_\Delta = \frac{3}{S_n} E_\Delta. \tag{37}$$

As mentioned in [8], the worst case for DSCC topology in terms of energy requirements corresponds to $\varphi^+ = \varphi^- = \pi/2$. Similar conclusions can be obtained for SDBC topology. Therefore, the energy storage requirements W_{2Y} and W_Δ can be obtained considering $\widehat{I}^+$ and $\widehat{I}^-$, ranging from 0 to

1 pu, $k_{max} = 1.1$ and $\varphi^+ = \varphi^- = \pi/2$. The obtained surface is plotted in Fig. 3 (a) and (b). It can be observed that energy storage requirements increase with the current processed by the converter. Furthermore, W_Δ is more sensible to the negative sequence current, due to the characteristic of the circulating current.

Nevertheless, the positive and negative sequence components cannot be chosen arbitrarily, since the converter rated current cannot be exceeded. Actually, since $\varphi^+ = \varphi^- = \pi/2$, the capability curve of MMC is defined by the equation:

$$\widehat{I}^+ + \widehat{I}^- = \widehat{I}_n. \tag{38}$$

Taking into account the capability surface, the maximum required value of W_{2Y} is approximately 39 kJ/MVA, as observed in Fig. 3 (a). Similarly, W_Δ is 20 kJ/MVA, as observed in Fig. 3 (b).

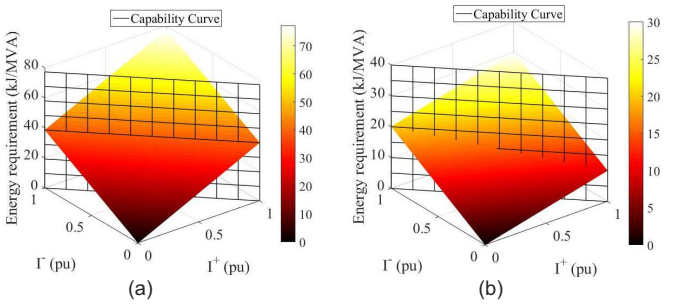

Fig. 3. Energy storage requirements according to the positive and negative sequence current components: (a) DSCC topology; (b) SDBC topology.

In order to compare the energy storage requirements of both topologies, the energy ratio K_e is defined as:

$$K_e = \frac{W_{2Y}}{W_\Delta}. \tag{39}$$

Considering the design point, $K_e \approx 2$. This means that DSCC topology energy storage requirement is twice the amount of SDBC. Additionally, the ratio of the SM capacitance of each topology is given by:

$$K_c = \frac{C_\Delta}{C_{2Y}} = \frac{\sqrt{3}}{K_e}\frac{\lambda_{2Y}}{\lambda_\Delta}. \tag{40}$$

For the considered modulation strategies $K_c \approx 1$ and $C_\Delta \approx C_{2Y}$. Using the effective dc-link voltage and the number of SMs, $C_\Delta = C_{2Y} = 4.5$ mF is obtained.

At this point, two important issues must be mentioned regarding the energy storage requirements derived in this work. Firstly, some works in literature propose the insertion of zero sequence components and/or harmonics in the circulating current in order to change the shape of the capacitor voltage waveform [19]–[21]. In such conditions, the energy storage requirements can be reduced. Nevertheless, these strategies tend to increase the circulating current rms value, increasing the power losses and affecting the overall efficiency [22]. For this reason, these strategies are not approached in this work.

Secondly, the energy storage requirements obtained in this section considers a STATCOM applied for grid voltage support or renewable energy systems. When flicker compensation of arc furnaces is considered, the mitigation of low-frequency oscillations are as important as the negative sequence compensation [7]. In such conditions, the low frequency components will affect the energy variation and consequently higher energy storage requirements are expected in such conditions. Nevertheless, the study of this phenomenon is beyond the scope of this work and it can be discussed in future works.

D. Arm and Cluster Inductances

The arm inductance is responsible for improving the circulating current characteristic and limiting fault currents. Furthermore, there is a resonant frequency resultant from the interaction of SM capacitances and arm inductances that must be avoided. For DSCC topology, the product of the arm inductor and the SM capacitance have to satisfy the following relation [23]:

$$L_{arm}C > \frac{5N}{48\omega_n^2}. \tag{41}$$

Moreover, taking the most critical fault into consideration, a short circuit fault is applied between the positive and negative dc-buses. To limit the fault current, the arm inductance should satisfy [24]:

$$L_{arm} = \frac{V_{dc}}{2\alpha}, \tag{42}$$

where α (kA/s) is the maximum current rise rate. According to (42), if the maximum current rise rate is $\alpha = 0.1(kA/\mu s)$ [25], the minimum value of arm inductance is 0.14 mH (0.004 pu), by applying (41), $L_{arm} > 2.9mH(\approx 0.09pu)$. Typically, the per unit (pu) arm inductance values for grid connected converters are limited at the range of 0.3 pu for both DSCC and SDBC topologies. This work employs $0.15pu$ for both topologies. Thus, $L_{arm} = L_{cl} = 5.1mH$.

IV. Comparison of MMC STATCOM Topologies

The comparisons of MMC STATCOM topologies are accomplished in terms of dynamic behavior, operation during unbalanced voltages, power losses and cost. The losses in the power semiconductors, arm and cluster inductors and SM capacitors are taken into account. The parameters of both converters are presented in Table I.

The case study considers three operational conditions:

- Case 1: $0 \leq t \leq 0.2$ seconds: 1 pu of positive sequence reactive power is injected into the power grid;
- Case 2: $0.2 < t \leq 0.8$ seconds: 0.5 pu of positive sequence reactive power and 0.5 pu of negative sequence reactive power are injected into the power grid;
- Case 3: $0.8 < t \leq 1.2$ seconds: 1 pu of negative sequence reactive power is injected into the power grid.

All simulations are performed in PLECS environment aiming to validate the design methodology proposed. Power losses in the semiconductors are estimated through the model

TABLE I
PARAMETERS OF THE MMC TOPOLOGIES.

Parameter	Value
Grid voltage (V_g)	13.8 kV
Line frequency (f_n)	60 Hz
Effective dc voltage ($V_{dc,2Y}, V_{dc,Delta}$)	28 kV
Rated power (S_n)	15 MVA
Transformer inductance (L_g)	1.35 mH
Transformer X/R ratio	18
Arm,Cluster inductances (L_{arm}, L_{cl})	5.1 mH
Arm inductor X/R ratio	15.1
Cluster inductor X/R ratio	19.8
SM capacitance (C_{2Y}, C_{Δ})	4.5 mF
Nominal SM voltage ($v^*_{sm,n}$)	1.56 kV
Carrier frequency (f_c)	210 Hz
Number of SMs (N_{2Y}, N_{Δ})	17

proposed by [26], [27]. The conduction, switching losses and thermal impedance are obtained from look-up tables based on the data provided in datasheets [26]. DSCC topology employs an IGBT part number 5SND 0500N330300 while SDBC topology employs an IGBT part number 5SNA 0800N330100. Both power modules are manufactured by ABB. Different IGBTs are employed once DSCC and SDBC topologies present different current rating.

In order to evaluate the inductor losses, the powder cores and the windings are designed according to the guidelines presented in [28]. The inputs of the design procedure are the desired inductance and the peak current. Based on these variables, the maximum energy storage in the inductor is computed. Using this energy, the core can be selected. Afterwards, an iterative process is used to determine the number of turns. The winding is based on Litz wire in order to mitigate the skin effect.

The winding losses are calculated by simulations using the inductor resistance. For simplification, the contributions of proximity and skin effects are disregarded, as suggested in [29]. Additionally, the magnetic losses are estimated through the improved generalized Steinmetz equation method (iGSE) [30], since the flux density waveforms are not sinusoidal.

The power losses of the SM capacitors include the ohmic loss in the ESR and the dielectric losses. These losses were estimated following the methodology proposed by [31]. High density Electronicon film capacitors are considered.

The costs are evaluated according to the methodology presented in [32]. According to this reference, the cost of the capacitors employed in the SMs are 150 €/kJ. Furthermore, the cost of the magnetic devices K_{mag} in euros can be estimated by [32], [33]:

$$K_{mag} = 4000 N_{mag} + 723000 A_p, \tag{43}$$

where N_{mag} is the number of inductors. For DSCC, $N_{mag} = 6$ is assumed while $N_{mag} = 3$ is assumed for SDBC topology. A_p is the product of the winding window area A_w and the cross section area A_c of the magnetic core, known as area product.

Finally, the additional costs (power modules, cabinets, control, etc) can be approximated by 3.5 €/kVA of the installed switching power P_{sw}, which is given by [33]:

$$P_{sw} = N_s V_{svc} I_{svc}, \tag{44}$$

where I_{svc} is the device rated current, respectively. The parameters employed in the losses and cost evaluation are presented in Tab II.

TABLE II
PARAMETERS EMPLOYED IN THE LOSSES AND COST EVALUATION.

Parameter	DSCC	SDBC
Inductor resistance	127.1 $m\Omega$	96.9 $m\Omega$
Capacitor ESR	0.417 $m\Omega$	0.417 $m\Omega$
Total Storage Energy	622.6 kJ	311.3 kJ
Area product	2.73 10^{-3} m^4	6.47 10^{-3} m^4
Installed Switching Power	336.6 MVA	538.6 MVA

V. RESULTS

A. Dynamic Behavior Analysis

Fig. 4 illustrates the results for DSCC topology. All results are presented in per unit (pu) where the base power is S_n while the base current is $\widehat{I_n}$. Fig. 4 (a) presents the instantaneous active and reactive power injected into the grid. At $t = 0.2s$, the STATCOM injects 0.5 pu of negative sequence added to 0.5 pu of positive sequence. Therefore, the instantaneous active and reactive power present oscillatory components at the doubled line frequency (120 Hz). The instantaneous active power presents an average value, which represents the amount of power responsible for supplying the converter power losses. At $t = 0.6s$, the STATCOM injects 1 pu of negative sequence current. In this case, the amplitude of the oscillations in active and reactive power reaches 1 pu. Regarding the time response, the system reaches the steady-state approximately 300 ms after the reference step.

The instantaneous power references affect directly the circulating currents, as presented in Fig. 4 (b). For case 1 the circulating currents are null, since only reactive power is injected. For cases 2 and 3, the circulating currents at arms B and C present a dc value. As observed, the second harmonic component is almost fully compensated by the control strategy employed. The time response of circulating currents is around 250 ms.

Fig. 4 (c) presents the arm currents. For case 1, the currents are balanced and similar stresses are observed in each phase of the converter. Nevertheless, when the converter processes both sequences, the currents are clearly unbalanced and the stresses in the phase components are different. For case 3, the currents are not balanced due to the amount of absorbed positive sequence resulting due to the converter power losses.

The average value of SM capacitor voltages is shown in Fig. 4 (d). Due to symmetry, only upper arms are presented. As observed, the SM voltage ripple depends on the values of positive and negative sequences. Different ripples are observed in each phase. Phase A is the most stressed one, since its

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2018.2811361, IEEE Transactions on Industrial Electronics

current is always close to 1 pu (Fig. 4 (c)). The dashed lines indicate the 10 % range adopted in the design methodology. The transient value reaches 1.18 pu in the worst case. As observed, the designed capacitance value guarantees that the maximum ripple in steady-state, since the most stressed phase is within the 10 % range. Regarding the time response of the control strategy, the SM voltages reach the steady-state in approximately 370 ms.

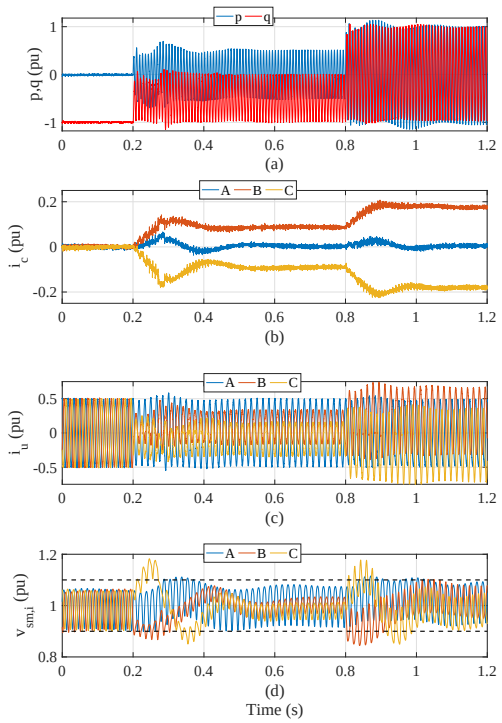

Fig. 4. Dynamic behavior of DSCC topology: (a) Instantaneous active and reactive power; (b) Circulating current; (c) Upper arm currents (d) Upper arm average SM capacitor voltages.

The results for SDBC topology are illustrated in Fig. 5. Similar behavior is observed in terms of instantaneous active and reactive power, as observed in Fig. 5 (a). Regarding the time response, the system reaches the steady-state approximately 200 ms after the reference step.

The dynamics of circulating current is presented in Fig. 5 (b). The circulating current is directly related with negative sequence injected into de grid, as provided by the theoretical results. This circulating current affects the amplitude of the cluster currents, as observed in Fig. 5 (c). For case 1, the cluster currents are balanced and similar stresses are observed in each phase of the converter. Nevertheless, when the converter processes both sequences, the currents are clearly unbalanced and therefore the stresses in the phase components are different. For case 3 the cluster current reaches a value above 1 pu, due to the circulating current.

The average value of the SDBC capacitor voltages is shown in Fig. 5 (d). As observed, the SM voltage ripple depends on the values of positive and negative sequences. During the injection of 1 pu of positive sequence, the ripples are very small, since the energy storage requirements at this condition are reduced. As observed, the designed capacitance value guarantees that the maximum ripple in steady-state for the most stressed phase is below the 10 % range when the converter injects 1 pu of negative sequence current into the grid. The transient value reaches 1.19 pu in the worst case. Regarding the time response, the SM voltages reach the steady-state in approximately 250 ms.

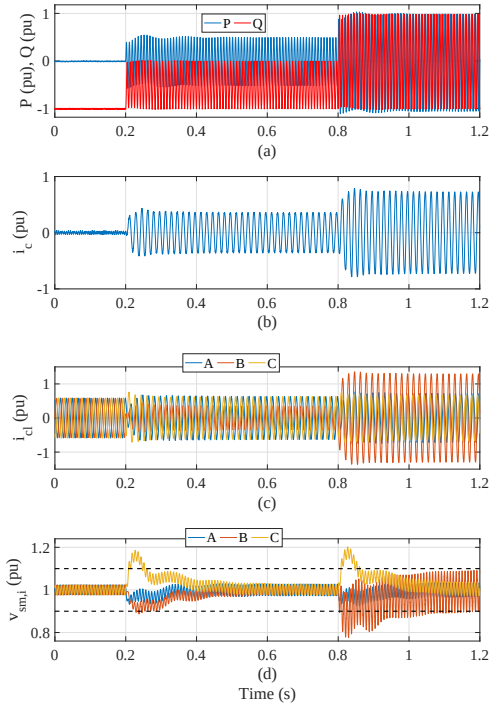

Fig. 5. Dynamic behavior of SDBC topology: (a) Instantaneous active and reactive power; (b) Circulating current; (c) Cluster currents; (d) SM capacitor voltages.

B. Circulating Current during unbalanced conditions

During unbalanced voltage conditions, the circulating current plays an important role in the power exchange between the arms/clusters of the MMC. Relations (8)-(10) and (24) show that the circulating current value for both topologies depends on the amplitude $\widehat{V}^-$ and phase δ^- of negative sequence voltage. Moreover, reference [3] shows that the SDBC topology has a singular operation point that requires an infinity circulating current to reach the capacitor voltage balancing. This operating point happens when the amplitudes of positive and negative sequence voltages are equal:

$$K_v = \frac{\widehat{V}^-}{\widehat{V}^+} = 1, \tag{45}$$

where K_v is the voltage unbalance factor. In order to compare the topologies, $\delta^+ = 0$ is assumed and 1 p.u. of positive sequence reactive power is injected into the grid. In this case, the per unit value of the circulating current is calculated according to K_v and δ^-. The results obtained are shown in Fig. 6. The unbalance factor is limited to 0.5. As observed, the circulating current amplitude increases with K_v. The SDBC topology presents higher values of circulating current

for the same operating conditions. Therefore, depending on the PCC voltage characteristics, the SDBC topology will be disconnected from the grid.

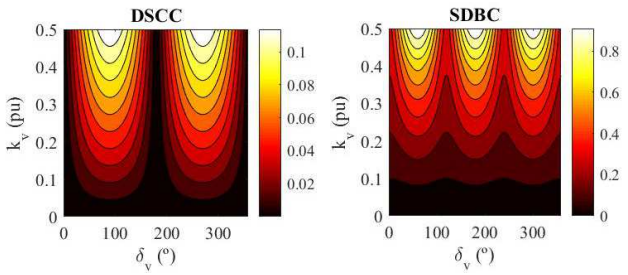

Fig. 6. Effect of negative sequence voltage on the MMC circulating current: (a) DSCC topology (phase A); (b) SDBC topology.

C. Power Losses and Cost Analysis

Considering the three operation scenarios aforementioned, the power losses for the MMC STATCOM were evaluated. For power semiconductors, the heatsink temperature is considered constant and equal to 70 $^{\circ}C$. The results obtained are presented in Table III.

As observed, once a low switching frequency is employed, the conduction losses are more significant than switching losses. The copper losses in the magnetic devices are considerable for both topologies while the core losses and ohmic losses in capacitors are negligible. For case 2 the total losses present the smaller value for both topologies. This fact happens because the arm and cluster currents presents smaller magnitude at this condition, as shown in Figs. 4 (c) and 5 (c).

Considering the case 1, the losses in SDBC are 28 % lower than DSCC topology. Nevertheless, for case 2 the losses in SDBC are 17 % higher than the losses in DSCC topology. For case 3 the cluster currents increase considerably due to the circulating current and the power losses in SDBC topology are 34 % higher than DSCC topology.

Finally, the specific cost (cost per kVA of rated power) of both topologies is presented in Table IV. Due to the higher current requirements of SDBC during negative sequence compensation, the cost of power electronics is approximately 60 % higher. In terms of SM capacitors, the SDBC topology presets lower storage energy requirements and lower cost. For the magnetic devices, the SDBC cluster inductors present a larger current rating. However, the DSCC topology presents the double of magnetic devices and the cost of magnetic devices is more expressive in this topology. Regarding the total cost, the SDBC is 50 % more expensive than DSCC.

TABLE III
POWER LOSSES IN THE MMC-STATCOM FOR THE TOPOLOGIES STUDIED.

Losses (kW)	Type	Case 1	Case 2	Case 3
Conduction losses	Δ	54.74	50.22	102.51
	2Y	61.50	38.10	68.55
Switching losses	Δ	15.07	13.94	22.75
	2Y	13.20	9.75	13.95
Core losses	Δ	0.39	0.35	1.14
	2Y	0.62	0.30	0.65
Copper losses	Δ	38.33	34.72	101.16
	2Y	75.12	40.63	87.02
Capacitor losses	Δ	0.06	0.06	0.26
	2Y	0.21	0.10	0.17
Total	**Δ**	**108.59**	**99.29**	**227.82**
	2Y	**150.65**	**88.88**	**170.34**

TABLE IV
SPECIFIC COST OF THE STUDIED TOPOLOGIES.

Costs	DSCC	SDBC
Power Electronics	78.54 €/kVA	125.66 €/kVA
Capacitors	6.22 €/kVA	3.11 €/kVA
Magnetics	1.73 €/kVA	1.11 €/kVA
Total	**86.49 €/kVA**	**129.88 €/kVA**

VI. DISCUSSION

An important question may be asked: Which is better, the DSCC or the SDBC for STATCOM application? This is not a trivial task, since requires multidisciplinary analysis. The idea of this work is to help the design engineer to find this answer.

As observed in the previous analysis, depending of the value of negative sequence component, the power losses in SDBC topology can be lower or higher than DSCC topology. Therefore, the mission profile of the application has an important role in the overall efficiency and must be evaluated. For example, if only positive sequence is considered, the energy losses in SDBC will be lower and the operational cost of the converter (in terms of energy losses) will be lower. Depending of the energy tariff value, the initial extra cost of SDBC topology can be paid by the smaller value of power losses.

The real cost of the converter will be also influenced by engineering costs, market conditions and exchange rates. Therefore, the cost metric is doubly challenging and few technical papers in literature includes this figure of merit. The values employed in this work are approximations implemented by references [32], [33], which compare the costs of dual-active bridge, three-phase modular multilevel converters and NPC converters. This analysis is in some degree limited and will not result in the exact cost of the converter. Nevertheless, this approach can be used as an initial comparison and also can be useful in the decision making procedure.

Finally, the grid conditions are an important issue. As observed, when unbalanced voltage conditions are considered, SDBC presents high values of circulating current and it can be disconnected from the grid if high values of unbalance factor are taken into account. Therefore, when weak grids are considered, DSCC topology presents advantages which can justify its application.

VII. Conclusion

This paper discussed two promise topologies of modular multilevel converters for STATCOM applications. The design methodology is focused in applications where positive and negative sequence reactive power compensation are necessary, as in grid voltage regulation and renewable energy systems. The comparison presented are supported by analytical results. The dynamic behavior, power losses and costs of both topologies were estimated based on a 15 MVA case study.

As observed, the SDBC topology presents smaller energy storage requirements than the DSCC topology. Additionally, smaller power losses were observed during positive sequence compensation. Nevertheless, when negative sequence components are compensated, the current rating and losses of SDBC topology increases considerably and DSCC topology presented a superior performance. Finally, SDBC topology is more susceptible to unbalanced voltage conditions and it is not recommended in such conditions.

References

[1] K. Fujii, U. Schwarzer, and R. W. D. Doncker, "Comparison of hard-switched multi-level inverter topologies for statcom by loss-implemented simulation and cost estimation," in *36th PESC*, pp. 340–346, Jun. 2005.

[2] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *IEEE Trans. Power Electronics*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[3] E. Behrouzian and M. Bongiorno, "Investigation of negative-sequence injection capability of cascaded h-bridge converters in star and delta configuration," *IEEE Trans. Power Electronics*, vol. 32, no. 2, pp. 1675–1683, Feb. 2017.

[4] P. Sochor and H. Akagi, "Theoretical comparison in energy-balancing capability between star- and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems," *IEEE Trans. Power Electronics*, vol. 31, no. 3, pp. 1980–1992, Mar. 2016.

[5] G. Tsolaridis, H. A. Pereira, A. F. Cupertino, R. Teodorescu, and M. Bongiorno, "Losses and cost comparison of ds-hb and sd-fb mmc based large utility grade statcom," in *16th EEEIC*, pp. 1–6, Jun. 2016.

[6] X. Liu, A. Lindemann, and H. Amiri, "Theoretical and experimental comparison of different control strategies for modular multilevel converters," in *15th COMPEL*, pp. 1–9, Jun. 2014.

[7] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-sequence reactive-power control by a pwm statcom based on a modular multilevel cascade converter (mmcc-sdbc)," *IEEE Trans. Industry Applications*, vol. 48, no. 2, pp. 720–729, Mar. 2012.

[8] J. V. Farias, A. F. Cupertino, H. Pereira, S. Seleme, and R. Teodorescu, "On the redundancy strategies of modular multilevel converters," *IEEE Trans. Power Delivery*, vol. PP, no. 99, pp. 1–1, 2017.

[9] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H. P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Industrial Electronics*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[10] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel vsc technologies for power transmission," in *IEEE/PES T&D*, pp. 1–16, Apr. 2008.

[11] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre, and F. Blaabjerg, "New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions," in *37th PESC*, pp. 1–7, Jun. 2006.

[12] Y. Yue, F. Ma, A. Luo, Q. Xu, and L. Xie, "A circulating current suppressing method of mmc based statcom for negative-sequence compensation," in *8th IPEMC*, pp. 3566–3572, May. 2016.

[13] K. Sharifabadi, L. Harnefors, H. Nee, S. Norrga, and R. Teodorescu, *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems*, ch. 2, pp. 214–216. John Wiley & Sons, 2016.

[14] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electronics*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[15] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electronics*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[16] F. Sasongko, K. Sekiguchi, K. Oguma, M. Hagiwara, and H. Akagi, "Theory and experiment on an optimal carrier frequency of a modular multilevel cascade converter with phase-shifted pwm," *IEEE Trans. Power Electronics*, vol. 31, no. 5, pp. 3456–3471, May. 2016.

[17] "Application note 5sya 2051: Voltage ratings of high power semiconductors," ABB, Tech. Rep., 2017.

[18] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based pwm-vsi drives," *IEEE Trans. Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[19] M. A. Perez and S. Bernet, "Capacitor voltage ripple minimization in modular multilevel converters," in *2015 IEEE ICIT*, pp. 3022–3027, Mar. 2015.

[20] R. Picas, J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. G. Agelidis, "Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization," in *2013 IEEE ECCE Asia*, pp. 318–324, Jun. 2013.

[21] R. Picas, J. Pou, S. Ceballos, V. G. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," in *2012 IECON*, pp. 4985–4991, Oct. 2012.

[22] B. Li, Z. Xu, S. Shi, D. Xu, and W. Wang, "Comparative study of the active and passive circulating current suppression methods for modular multilevel converters," *IEEE Trans. Power Electronics*, vol. 33, no. 3, pp. 1878–1883, Mar. 2018.

[23] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Trans. Power Electronics*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[24] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based hvdc," in *ICPST*, pp. 1–6, Oct. 2010.

[25] Z. Xu, H. Xiao, and Z. Zhang, "Selection methods of main circuit parameters for modular multilevel converters," *IET Renewable Power Generation*, vol. 10, no. 6, pp. 788–797, 2016.

[26] A. Sangwongwanich, L. Mathe, R. Teodorescu, C. Lascu, and L. Harnefors, "Two-dimension sorting and selection algorithm featuring thermal balancing control for modular multilevel converters," in *18th EPE*, pp. 1–10, Sep. 2016.

[27] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," in *IEEE Power and Energy Society General Meeting*, pp. 1–7, Jul. 2011.

[28] *Powder Cores*, Magnetics International Pittsburg P A Catalog, 10 2006.

[29] A. P. L. Cota, R. C. Abrantes, P. C. Cortizo, R. A. S. Santana, and W. C. Padrao, "Comparison of three 3-phase converter topologies for ups applications," in *13th COBEP/SPEC*, pp. 1–6, Nov. 2015.

[30] J. Muhlethaler, J. W. Kolar, and A. Ecklebe, "Loss modeling of inductive components employed in power electronic systems," in *8th ECCE Asia*, pp. 945–952, May. 2011.

[31] *Application notes and selection guide*, Electronicon, 10 2013.

[32] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. D. Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in hvdc and mvdc grids," *IEEE Trans. on Power Electronics*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[33] H. A. B. Siddique, A. R. Lakshminarasimhan, C. I. Odeh, and R. W. D. Doncker, "Comparison of modular multilevel and neutral-point-clamped converters for medium-voltage grid-connected applications," in *ICRERA*, pp. 297–304, Nov. 2016.

Allan Fagner Cupertino (M'15) received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV) in 2013 receiving the President Bernardes Silver Medal. He received the M.S. degree in Electrical Engineering from the Federal University of Minas Gerais (UFMG). Since 2014 he has been with the Materials Engineering Department at the Federal Center of Technological Education of Minas Gerais (CEFET), teaching in the area of electric machines. Currently, he is working toward the Ph.D. project about the use of modular multilevel converters in STATCOM applications. His main research interests include renewable power generation systems, multifunctional inverters, modular multilevel converters and reliability of power electronic converters.

João Victor Matos Farias is currently an undergraduate student in electrical engineering at the Federal University of Viçosa (UFV). His main research interests include modular multilevel converters, HVDC and STATCOM applications, electric drives and reliability of power converters.

Heverton Augusto Pereira (M'12) received the B.S. degree in electrical engineering from the Federal University of Viçosa (UFV), Brazil, in 2007, the M.Sc. degree in electrical engineering from the University of Campinas (UNICAMP), Brazil, in 2009 and the Ph.D. degree from the Federal University of Minas Gerais (UFMG), Brazil, in 2015. He was a guest Ph.D. from the Department of Energy Technology, Aalborg University, Denmark in 2014. He has been Adjunct Professor at the Electric Engineering Department, UFV, Brazil, since 2009. His main research interests includes: grid-connected converters for photovoltaic and wind power systems, HVDC/FACTS based on MMC.

Seleme Isaac Seleme Junior received the B.S. degree in electrical engineering from the Escola Politecnica (USP), São Paulo, Brazil, in 1977, the M.S. degree in electrical engineering from the Federal University of Santa Catarina, Florianópolis, Brazil, in 1985, and the Ph.D. degree in control and automation from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, in 1994. He spent a sabatical leave with the Power Electronics Group, Univesity of California, Berkeley, in 2002. In 2015, he spent a sabatical leave with the Institut National Polytechnique de Toulouse, INP, France where he developed researches about decentralized control and capacitor voltage estimation techniques for modular multilevel converters. He is currently an Associate Professor with the Department of Electronic Engineering, Federal University of Minas Gerais, Belo Horizonte, Brazil. His main research interests include renewable energy systems, modular multilevel converters and nonlinear control applied in power converters.

Remus Teodorescu (F'12) received the Dipl.Ing. degree in electrical engineering from the Polytechnical University of Bucharest, Bucharest, Romania, in 1989, and the Ph.D. degree in power electronics from the University of Galati, Romania, in 1994. In 1998, he joined the Power Electronics Section, Department of Energy Technology, Aalborg University, Aalborg, Denmark, where he is currently a Full Professor. Since 2013, he has been a Visiting Professor with Chalmers University. His research interests include design and control of grid-connected converters for photovoltaic and wind power systems, HVDC/FACTS based on modular multilevel converters (MMC) and storage systems based on Li-ion battery technology including modular converters and active BMS.