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High-frequency resonant operation of an integrated medium-voltage SiC MOSFET power module

Asger Bjørn Jørgensen[1*], *Thore Stig Aunsborg*[1], *Szymon Bęczkowski*[1], *Christian Uhrenfeldt*[1], *Stig Munk-Nielsen*[1]

[1] *Department of Energy Technology, Aalborg University, Pontoppidanstraede 111, Aalborg, Denmark*
[*] *E-mail: abj@et.aau.dk*

Abstract: Industrial processes which use induction and dielectric heating are still relying on resonant converters based on vacuum tubes. New emerging medium voltage silicon carbide semiconductor power devices have a potential to replace vacuum tubes and allow for more efficient and compact converters in the high frequency range. High voltage packages have been proposed in the literature that are suitable for the 10 kV silicon carbide MOSFETs, and its fast voltage switching capabilities in hard-switched applications have been demonstrated. However, no packaging is presented which allows the high frequency operation of a 10 kV silicon carbide MOSFET die. This paper proposes the design of a power module for MHz resonant operation of a 10 kV silicon carbide MOSFET. At high switching frequencies the gate losses become substantial, thus the gate driver is included inside the power module package to ensure a low inductive and high thermally conductive design as seen from the gate driver. The inductance of the proposed power module layout structure is evaluated using ANSYS Q3D Extractor. The thermal performance of the integrated gate driver circuitry is experimentally verified. Finally, the resonant operation of a medium voltage silicon carbide MOSFET power module is demonstrated experimentally at 1 MHz.

1 Introduction

Resonant converters operating at high voltages and high frequencies, are used in various industrial processes employing induction and dielectric heating. Applications include melting/annealing of metals [1], drying of wood/glue/textiles [2–4] and for food processing [5]. The industries require converters operating at hundreds of kHz to tens of MHz at voltages of typically 2-3 kV and are currently using vacuum tubes in their designs. The conventional silicon (Si) power devices are not capable of operating at the high switching frequencies and high voltages that are required for these applications. However, converters based on vacuum tubes suffer from low efficiencies and are bulky in size. In comparison, typical low voltage resonant converters realised with solid state devices are smaller, cheaper and reach efficiencies > 90% [6, 7].

Emerging wide band gap semiconductor devices, such as silicon carbide (SiC) MOSFETs, have increased voltage breakdown strength, higher thermal conductivity and reduced on state resistance when compared with similar Si devices [8–10]. As a result the chip area of a SiC MOSFET is smaller when compared with a Si MOSFET device of similar voltage and current ratings. Therefore, SiC devices have reduced gate charge requirements which potentially allows them to be operated at higher frequencies [11, 12]. Resonant converters using SiC devices have already been employed, proving its high efficiency and results in very clean waveforms during zero voltage switching (ZVS) at frequencies of several MHz [13–16]. All these converters have been built using SiC MOSFETs with voltage ratings of 1200 V or lower. SiC MOSFETs are currently commercially available up to voltages of 1200 and 1700 V [17, 18], which is not high enough to replace the vacuum tubes in the mentioned applications. Recently, 10 and 15 kV SiC MOSFETs from Wolfspeed have been released as engineering samples [19, 20] and are capable of reaching the targeted 2-3 kV voltage range or higher. These devices are only available in bare die form, and recent research has been focused on the development of high voltage packaging of such devices. Several research teams have investigated and demonstrated the fast switching capabilities of the 10 kV SiC MOSFETs mainly in hard-switched double-pulse tests [21–25], short-circuit characteristics [26–28], DC-DC converters [29–32] and inverter demonstrators with frequencies up to 40 kHz [33–37]. There has not yet been any documented attempts at operating 10-15 kV SiC devices in the MHz-range.

A challenge of operating a high voltage device at high frequency is identified when studying the on resistance of a MOSFET, given by

$$R_{\mathrm{on}} = \frac{4 \cdot V_{\mathrm{br}}^2}{\epsilon \cdot \mu \cdot E_{\mathrm{C}}^3 \cdot A} \tag{1}$$

where V_{br} is the breakdown voltage, ϵ is the dielectric constant of the semiconductor, μ is the electron mobility and E_{C} is the critical electric field for breakdown of the semiconductor material and A is the area. Part of the denominator ($\epsilon \cdot \mu \cdot E_{\mathrm{C}}^3$) is known as the Baliga figure of merit (BFOM) of a semiconductor material [38]. From (1) it is seen that increasing the voltage breakdown of a device from its typical ~1 kV to 10 kV, would result in the resistance to increase by 100 times. For Si this would result in a too high on resistance or impractical die area. However, by using the advantageous properties of SiC to yield a higher BFOM, a 10 kV 350 mΩ SiC MOSFET die has been designed by Wolfspeed with an area of 8.1 x 8.1 mm [39]. For high frequency operation, the on resistance should not be reduced by carelessly increasing the die area. Increasing the die area results in a larger input capacitance of the die, which increases the required power to be delivered from the gate driver circuit to charge and discharge the input capacitance of the SiC MOSFET die. The compromise between on resistance and input capacitance is found in the Baliga high frequency figure of merit (BHFFOM) [11], given by

$$\mathrm{BHFFOM} = \frac{1}{R_{\mathrm{on}} \cdot C_{\mathrm{in}}} \tag{2}$$

Thus, a careful design of the gate drive circuit is required to effectively deliver the necessary gate power and proper high voltage packaging must be developed to achieve high frequency operation of 10 kV SiC MOSFETs

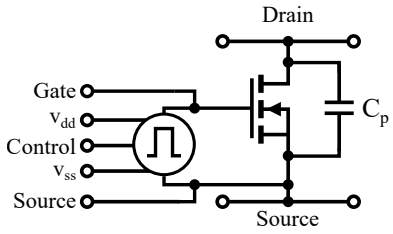

Fig. 1: Proposed module diagram.

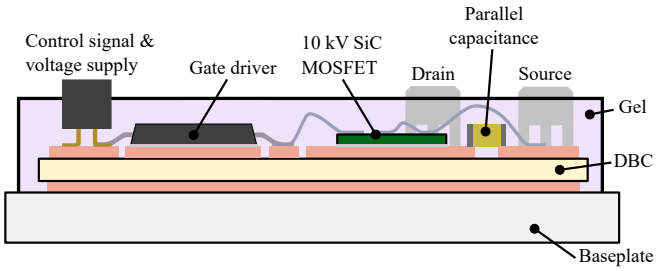

Fig. 2: Medium voltage SiC MOSFET power module structure.

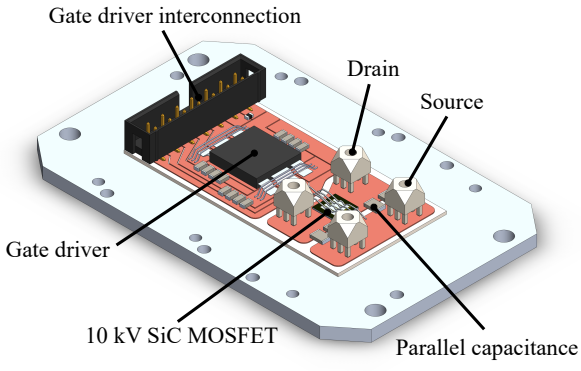

Fig. 3: Medium voltage SiC MOSFET power module design.

This paper is the first documented attempt of MHz operation of a 10 kV SiC MOSFET die, as a step in the process of turning vacuum tubes obsolete in some high voltage, high frequency applications. To address the gate driving challenge, this paper contributes with the design of an integrated package of high voltage semiconductor devices and proves the capability of high frequency resonant operation of a 10 kV SiC MOSFET. The power module structure, design and evaluation of its parasitics is presented in Section 2. In Section 3 the gate driver circuit itself is tested to ensure that the circuit can deliver the necessary power without overheating at high switching frequencies. The power module is characterized and its performance at high frequencies is experimentally tested in Section 4. The results are presented and some of the limitations of the power module are discussed. The paper is concluded in Section 5.

2 Power module design

A power module for a ZVS resonant circuit is designed, to test the feasibility of switching a 10 kV SiC MOSFET in the high frequency range. A schematic of components included in the power module is shown in Fig. 1. The parallel capacitance, C_p, ensures ZVS and this configuration is well-known from single switch resonant topologies such as the Class E, Class Φ_2 and ZVS resonant-switch converters. The parallel capacitance, C_p, should be placed as close to the SiC MOSFET die as possible. This is done to reduce the noise generated when current shifts from being conducted through the SiC MOSFET to parallel capacitance, and vice versa. A hard switched gate driver integrated circuit (IC) is chosen, due to its simplicity and flexibility. To ensure an undisturbed gate-source voltage of the SiC MOSFET a kelvin connection is used. The hard switched gate driver IC should be placed close to the SiC MOSFET to achieve fast switching speed without ringings, as described further in Section 2.1. Compared with a resonant gate driver, a hard switched gate driver IC has higher power density and allows for easier adjustment of the frequency and duty cycle without changing any components of the circuit [40, 41]. Its disadvantage is higher gate losses as the energy delivered to the gate is not recovered [42]. Operating at high frequencies requires a power module structure which allows both the SiC MOSFET die and the gate driver to dissipate the generated losses. The direct bonded copper (DBC) integrated power module structure, as shown in Fig. 2, enables both low inductive integrated design and high thermal conductivity and it has demonstrated great performance for lower voltage SiC MOSFETs [15, 16, 43]. A baseplate is used for mechanical stability and allows for mounting the power module onto a heat sink. The DBC is soldered to the baseplate, and ensures high voltage insulation capability while still maintaining low thermal resistance. The top side of the DBC is etched and populated with the components. All of the components are enclosed in an insulating silicone gel to allow high voltage operation.

Based on this power module structure, a medium voltage SiC MOSFET power module design is proposed, as shown in Fig. 3. The power module has both the 10 kV SiC MOSFET die, gate driver and the parallel capacitance soldered directly to the DBC. The ceramic capacitors making up the parallel capacitance, C_p, are of material class NP0 as they effectively maintain capacitance at increasing frequency and voltage bias. In contrast X7R, Y5V and X5R drop typically 10-20 % or more of their specified value, making it hard to maintain a desired capacitance regardless of frequency and voltage bias [44, 45]. The disadvantage of class NP0 is a low capacitance density, meaning that a high voltage capacitor with just a few hundred pF is not easily available in a small form factor. Surface mounted capacitors and a small form factor are requirements for integration of capacitors in the power module. Leaded capacitors introduce higher series inductance and could degrade the ZVS performance. For this paper four ceramic capacitors of 180 pF make up the parallel capacitance C_p, but are only rated for 3000 V. Surface mounted NP0 capacitors of higher voltage have not been available with the required capacitance value. This issue is to be solved for future power modules to further utilize the full 10 kV voltage rating of the SiC MOSFET dies, but is not necessary for this paper to demonstrate the ability to switch the module in the 2-3 kV range for the targeted applications. WACKER Silicone gel with a dielectric strength of 23 kV/mm [46] is used to ensure safe high voltage operation. The high voltage drain potential has a minimum clearance of 2 mm to all other planes of the power module. The DBC is 0.3 mm copper layers on either side of a 1 mm thick aluminium nitride layer. Aluminium nitride allows high voltage operation while still maintaining a low thermal resistance, as its thermal conductivity is 150-180 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ in comparison to the 24 $\frac{\mathrm{W}}{\mathrm{m \cdot K}}$ of conventional aluminium oxide ceramics [47].

Power terminals from Redcube are directly soldered to DBC for interfacing of drain and source potentials. A pin header socket located on the other side of the power module is used to interface the gate supply voltages, gate driver IC control signal and to allow measurement of the gate-source voltage between gate driver and the 10 kV SiC MOSFET die. The gate driver is a IXRFD630 from IXYS, which is capable of delivering high power. The expected rise and fall time is 5-7 ns [48], and it is rated at a peak output current of 30 A. This is used to ensure fast turn-on and turn-off speed of the 10 kV SiC MOSFET die and allow its operation into the MHz range. The $V_{ds} - I_{ds}$ characteristics of the 10 kV SiC MOSFET die, shown in Fig. 4, are obtained using a Keysight B1506A power device analyzer. It shows that the gate-source voltage should be maintained above 15 V to prevent saturation effects, which start to occur at currents of 7-8 A. From Fig. 4 the drain-source on resistance is determined to

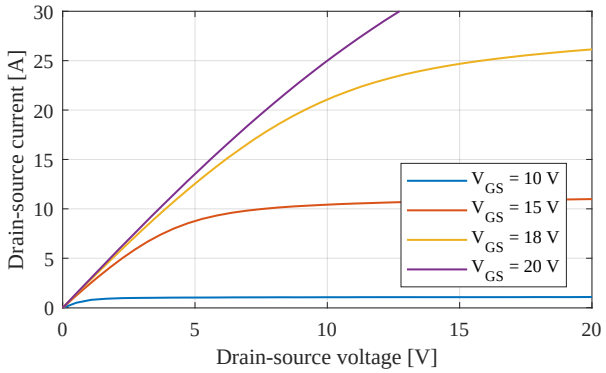

Fig. 4: Measured V_{ds}-I_{ds} characteristic of the 10 kV SiC MOSFET at different gate-source voltages, V_{GS}.

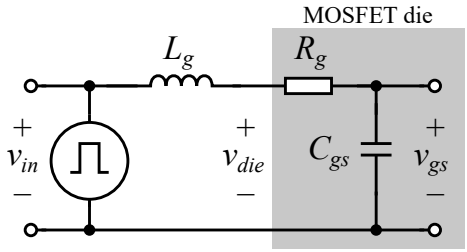

Fig. 5: Schematic used for gate drive design.

be 350 mΩ in its linear region. Also using the Keysight B1506A the gate-source threshold voltage is determined to be 4.3 V.

2.1 Gate driver design considerations

The layout of the power module is considered to reduce the influence of the unavoidable parasitics. A kelvin connection is employed to reduce influence from the power loop on the gate-source voltage. To turn the SiC MOSFET on/off as fast as possible no external gate resistance is inserted, which means that the gate-source loop has limited damping. A too high loop inductance results in an oscillating gate-source voltage which propagates as an undesirable high frequency component on the drain-source voltage [14]. The schematic of the gate driver used to determine its dynamics is shown in Fig. 5. Modelling the gate driver IC output, v_{in}, as an ideal step input, the dynamic response of gate-source voltage of the SiC MOSFET die, v_{gs}, is determined by [43, 49]

$$L_{\mathrm{g}} = \frac{C_{\mathrm{gs}} R_{\mathrm{g}}^2}{4\zeta^2} \tag{3}$$

where L_{g} is the gate-source loop inductance, C_{gs} is the gate-source capacitance of the SiC MOSFET, R_{g} is the gate resistance of the SiC MOSFET and ζ is the damping of the circuit [43].

By selecting a critically damped case ($\zeta = 1$), and using the preliminary datasheet of the 10 kV SiC MOSFET die, the maximum allowable gate-source loop inductance becomes

$$L_{\mathrm{g}} = \frac{5.8\mathrm{nF} \cdot (3.7\Omega)^2}{4 \cdot 1^2} = 20\mathrm{nH} \tag{4}$$

This value or anything below ensures that there will be no overshoot of the gate-source voltage of the SiC MOSFET. Designing a layout with the necessary inductance value is an iterative process where new designs are proposed which are then assessed using ANSYS Q3D Extractor as a design tool, as explained in Section 2.2.

2.2 Evaluation of design in ANSYS Q3D Extractor

The software package ANSYS Q3D Extractor is used to calculate the parasitic inductance of the proposed power module in Fig. 3. In

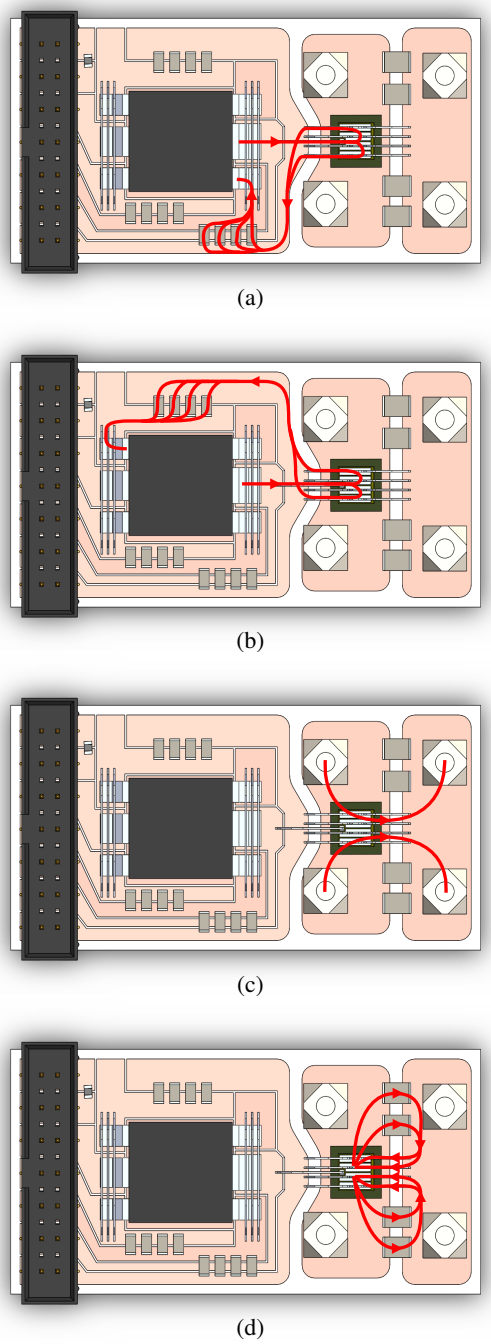

Fig. 6: (a) gate-source loop when clamped to negative voltage (b) gate-source loop when clamped to positive voltage (c) drain-source power loop (d) current path between SiC MOSFET and parallel capacitance.

ANSYS Q3D Extractor source and sink terminals (equivalently to an input and output) are defined on the 3D geometry, and by simulating the electromagnetic fields the inductance between these two terminals is calculated. The parasitics must be solved at a certain frequency. At very low frequencies ANSYS Q3D Extractor assumes there are no inductive effects and current is assumed to flow equally distributed across the conductor volume. At high frequencies the assumption is that inductive effects become pronounced, and due to skin effect the current density is increased at the surface. This paper is mainly concerned with the inductance during the fast switching instances which has components at various high frequencies [50]. Thus the inductance is solved as a surface problem.

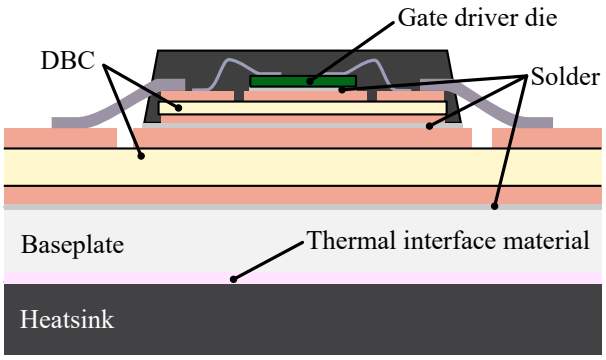

Fig. 7: Diagram of gate driver thermal structure.

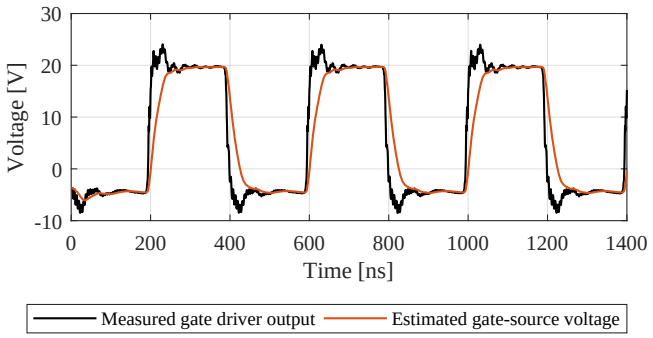

Fig. 8: Measured gate driver output and estimated gate-source voltage waveform.

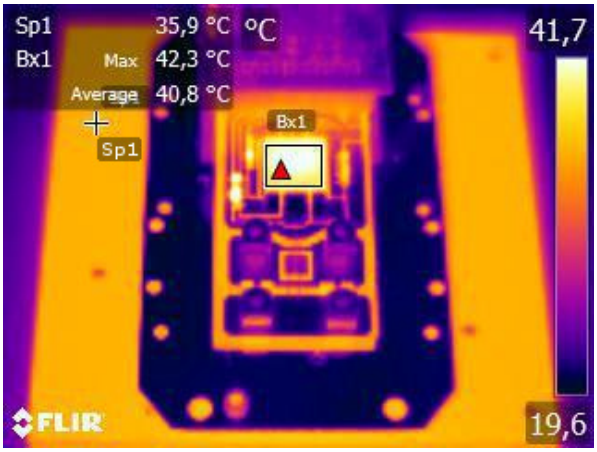

Fig. 9: Temperatures are logged using a FLIR E40 thermal camera.

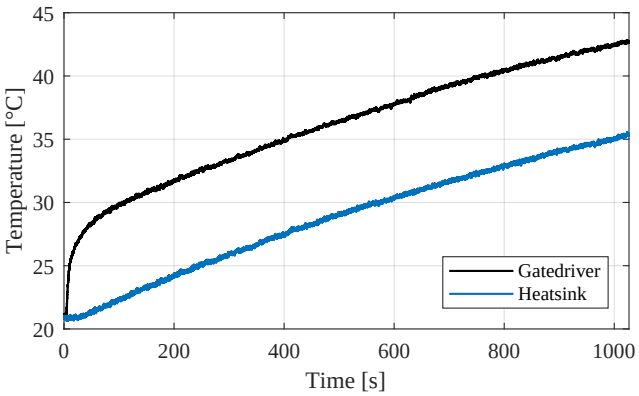

Fig. 10: Temperatures measured on the gate driver (Bx1.max in Fig. 9) and the heat sink (Sp1 in Fig. 9) during experiment.

The gate-source loop inductance when clamped to the negative voltage, shown in Fig. 6(a), is calculated as 10 nH. The loop when clamped to positive rail is shown in Fig. 6(b), and the extracted inductance is 12 nH. Both of these values are below the inductance calculated in (3), required for a critically damped response of the gate-source voltage on the SiC MOSFET. Thus, if Kelvin-source connections effectively mitigate the coupling between power and gate loops, limited oscillation is expected to the gate-source voltage. The drain-source power loop is defined from the drain to source terminals, shown in Fig. 6(c), and the inductance is calculated as 5.5 nH. When the SiC MOSFET turns off the current shifts to the distributed parallel capacitance placed inside the module. Thus, it is very important that this inductance is kept at a minimum. The loop inductance of the path between the SiC MOSFET and the parallel capacitors, as shown in Fig. 6(d), is calculated as 2.4 nH.

3 Performance of gate driver circuit

Before fully operating the power module, the gate driver IC and the gate structure of the 10 kV SiC MOSFET is tested. The purpose of the test is to ensure that the gate driver circuit is capable of delivering the necessary power without overheating. A diagram of the different layers as seen from the gate driver is shown in Fig. 7. The gate driver package contains its own DBC to ensure isolation, and bond wires connect the gate driver die to the external leads of the driver. When using this prepackaged gate driver the path from die junction to the heat sink includes a total of: two ceramic layers, four copper layers, three solder interfaces, a baseplate and thermal interface material between baseplate and heat sink. This highlights the necessity to experimentally verify that the gate driver IC is capable of dissipating its power losses when driving the SiC MOSFET at MHz frequencies. Furthermore, the test ensures that the 10 kV SiC MOSFET is capable of being driven at a high frequency. The resistance of the gate structure is relatively high, and it must be ensured that the physical structure of the device can handle the high frequency pulsing of power into the gate structure. O. Kreutzer *et al.* [49] demonstrated fusing of the gate-structure of a low voltage SiC MOSFET from excessive current pulsing, in an attempt to increase the switching speed.

The power module is mounted on a heat sink and an input signal of 2.5 MHz is given to the gate driver IC in the power module. The gate driver is supplied with a v_{dd} of +20 V for high output and v_{ss} of -5 V for low output. For the experiment it is not possible to measure the gate-source voltage inside the die, but only the voltage outside denoted v_{die} in Fig. 5. The measured output voltage from the gate driver is shown in Fig. 8. There is a spike on the measured output of the gate driver. Using a SPICE simulation the measured v_{die} is used as a voltage source input to the gate-resistance and gate-source capacitance, to estimate the gate-source voltage, v_{gs}, as shown in Fig. 8. This demonstrates the damped dynamic behavior as designed in Section 2.1.

The test is performed before the housing is mounted and the silicone gel is applied, which allows measuring surface temperature of the gate driver inside the power module using an thermographic camera. Temperatures of the gate driver IC and a reference temperature on a heat sink are measured using a FLIR E40 thermographic camera. The thermal image of the FLIR E40 during a test is shown in Fig. 9, and the surface temperatures are automatically logged at a frequency of 30 Hz during the experiment. Both the gate driver IC and the heat sink are covered in black paint, and an emissivity constant of 0.95 is used. No cooling fans are used to reduce the turbulence of the air around the power module. This is done to obtain conditions which are as close as to when the power module is encapsulated and limited power dissipation is possible through the top surface of the gate driver. Logged temperatures during 2.5 MHz operation of the gate driver are shown in Fig. 10.

As seen the gate driver temperature quickly increases to a level above the heat sink temperature, which then starts to slowly increase.

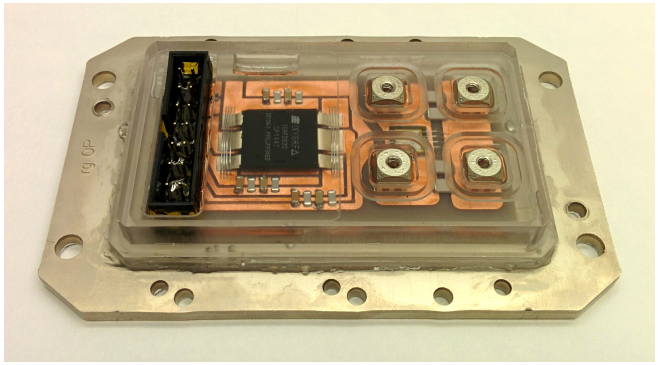

Fig. 11: Photograph of final power module.

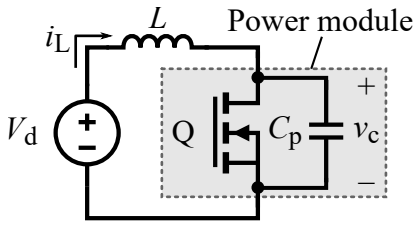

Fig. 12: LC circuit used to demonstrate resonant operation.

The absolute temperature difference then becomes constant for the rest of the test, while the temperature of the heat sink increases. Thus we can evaluate the thermal resistance from the gate driver IC to the heat sink, by

$$R_{\mathrm{gd}}(t) = \frac{T_{\mathrm{gd}}(t) - T_{\mathrm{hs}}(t)}{P_{\mathrm{gd}}} \tag{5}$$

where R_{gd} is the thermal resistance from gate driver IC to the heat sink, T_{gd} is the temperature of the gate driver, T_{hs} is the temperature of the heat sink and P_{gd} is the power dissipated in the gate driver IC. The DC power delivered to the gate driver circuit is measured as 17 W. From the LTSpice model of Fig. 5 the gate driver circuit, including gate resistance, input capacitance and loop inductances is developed. This predicts an energy consumption of 9.8 W in the SiC MOSFET gate resistance, meaning the remaining 7.2 W are assumed to be dissipated in the gate driver. This calculation does not account for the losses that might occur in the equivalent series resistance of the decoupling capacitors in the power module.

For the dataset shown in Fig. 10, the temperature difference between gate driver, T_{gd} and heat sink T_{hs} reaches a steady state of 7.5 °C after 100 seconds. Taking the value of the temperature difference in steady state and using the power dissipation of 7.2 W in (5), results in a thermal resistance from gate driver IC to heat sink, R_{gd}, of 1.04 $\frac{\mathrm{K}}{\mathrm{W}}$. The test demonstrates the capability of the 10 kV SiC MOSFET die to be driven at a frequency of minimum 2.5 MHz and that the gate driver can deliver the required power without overheating.

4 Experimental results of resonant operation

Following the verification of the gate driver circuit, the final power module is assembled. The housing is milled from a block of transparent acrylic plastic. After mounting of the housing, the power module is encapsulated in protective gel. The final power module is shown in Fig. 11.

A test setup is assembled to test the performance of the power module during resonant operation in high frequency range. An LC resonance oscillator as shown in Fig. 12 is used for this purpose.

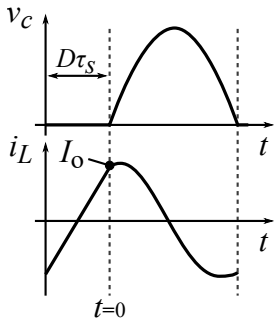

Fig. 13: Waveforms of LC resonant circuit.

The current in the inductor, L, is charged during the MOSFET on time by

$$\Delta i_{\mathrm{L}} = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{L} \tag{6}$$

where V_d is the DC-link voltage, L is the resonance inductance, D is the duty cycle and τ_s is the switching period. Because of the continuous resonant operation, the inductor current is centered around zero. Thus, geometrically from Fig. 13, the current which occurs at t = 0 is denoted I_0 and is calculated from

$$I_0 = \frac{D \cdot \tau_{\mathrm{s}} \cdot V_{\mathrm{d}}}{2 \cdot L} \tag{7}$$

At $t = 0$ the switch Q is turned off, and the energy charged in the inductor is released to the parallel drain-source capacitance C_p. The voltage across the capacitor, v_c following $t = 0$ is given by [51]

$$v_{\mathrm{c}} = V_{\mathrm{d}} - V_{\mathrm{d}} \cdot \cos(\omega t) + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \cdot \sin(\omega t) \tag{8}$$

To determine the maximum capacitor voltage (8) is differentiated

$$\frac{\mathrm{d}v_{\mathrm{c}}}{\mathrm{d}t} = V_{\mathrm{d}} \cdot \omega \cdot \sin(\omega t) + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \cdot \omega \cdot \cos(\omega t) \tag{9}$$

By equating (9) to zero and solving for t, its extremes occur at $t = \frac{\pi(2n-1)}{2\omega}$ for $n \in Z$. As the LC circuit is reset at every switching instance, we are mainly concerned with the initial peak, thus $n = 1$. Maximum capacitor voltage is found by inserting $t = \frac{\pi}{2\omega}$ to (8) which equals

$$V_{\mathrm{c}} = V_{\mathrm{d}} + \sqrt{\frac{L}{C_{\mathrm{p}}}} \cdot I_0 \tag{10}$$

The experimental results shown in this paper are done at an input DC link voltage, V_{d}, of 800 V. The capacitance is C_{p} = 890 pF, as shown in Fig. 14, which was obtained using a Keysight B1506A power device analyzer.

With the inductance, L, of 25 μH the resonance frequency becomes 1 MHz. Using these values, from (7) the build-up current I_0 becomes 5.0 A. Inserting this value to (8) the peak drain-source voltage is calculated as 1638 V.

The experimental results are shown in Fig 15. The drain-source voltage is measured using a high voltage Teledyne Lecroy PPE4kV passive probe, while the gate input voltage is measured using a Teledyne Lecroy ADP305 differential probe. The current is measured using a Teledyne Lecroy CP030 current probe. All probes are connected to a Teledyne Lecroy HDO4024A scope. A Magna XR2000-1.00/380NEG+LXi power supply is used to deliver the voltage, and is connected to a film capacitor bank of 1140 μF, ensuring a stable DC-link voltage up to a rating of 1500 V. To ensure the sinusoidal inductor current, the gate driver input signal is timed such that the duty cycle of the SiC MOSFET is $\frac{1}{\pi}$. However, the measured gate driver input signal is slightly below $\frac{1}{\pi}$ to account for non-equal delays during turn-on and turn-off.

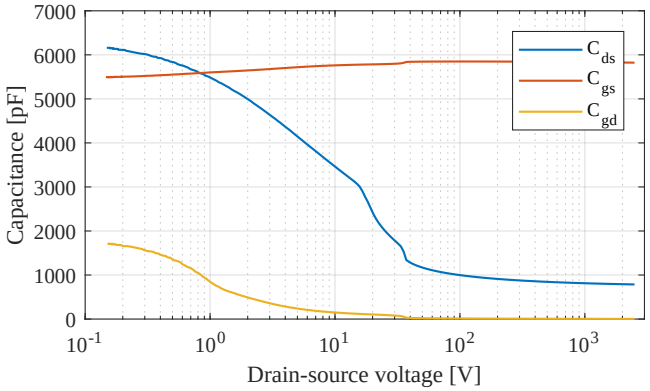

Fig. 14: Measured drain-source, C_{ds}, gate-source, C_{gs} and gate-drain C_{gd} capacitances of the power module.

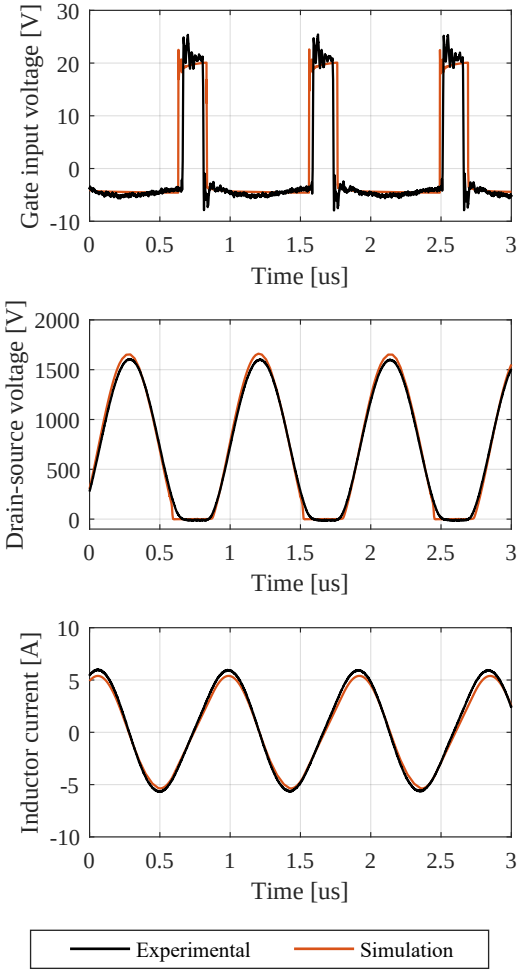

Fig. 15: Experimental and simulated waveforms during resonance operation of module.

The experimental results demonstrate the resonant operation of the medium voltage SiC MOSFET power module at 1 MHz. The measured peak drain-source voltage is 1597 V, which only deviates 2.4 % from the theoretically expected results. There are no higher frequency components of oscillation visible on the drain-source voltage. This indicates both the right damping of the gate-source loop and that the Kelvin connection mitigates coupling between the gate-source and power loop.

A SPICE simulation is made using the LC circuit model from Fig. 12, and adding the parasitic inductances calculated in Section 2.2. The SiC MOSFET device model is based on the static characteristics of $V_{\mathrm{ds}} - I_{\mathrm{ds}}$ in Fig. 4 and power module capacitances from Fig. 14. The SPICE simulation results are also shown in Fig. 15 and cohere with the experimental results. Some dynamics of the gate-source signal is not present in the simulation waveform, as not all loops of the gate-driver circuit or voltage supplies are modelled. Nevertheless, the simulation and theoretical calculations verify that in terms of drain-source voltage and inductor current the designed power module produces close to ideal LC oscillator circuit behavior.

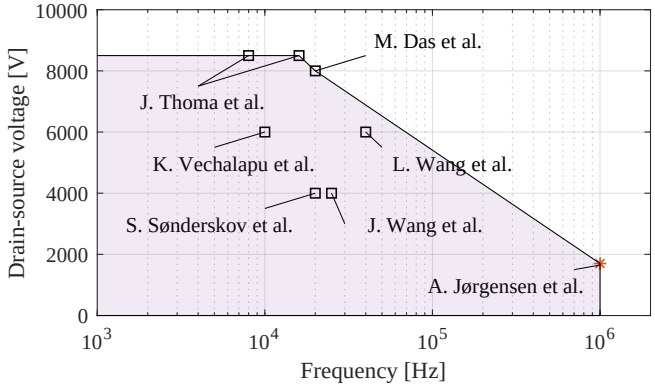

Fig. 16: Verified operation of 10 kV SiC MOSFETs at various drain-source voltages and frequencies. Boost converter demonstrators by K. Vechalapu *et al.* [29], J. Wang *et al.* [30] and J. Thomas *et al.* [31]. Inverter operation demonstrators by M. Das *et al.* [33], S. Sønderskov *et al.* [35], L. Wang *et al.* [36] and J. Thomas *et al.* [37]. The star point indicates the operating point for the experiment presented in this paper.

During the very first switching of the circuit, the full DC-link voltage is hard switched and results in a high $\mathrm{d}v/\mathrm{d}t$. The high $\mathrm{d}v/\mathrm{d}t$ of the drain copper plane of the DBC is capacitive coupled to the gate driver through the heat sink [52, 53]. The capacitive coupling between the two nodes causes flickering of the gate input signal preventing the circuit from entering its desired LC oscillation. For this reason successful resonance operation was not achieved above an input voltage level, V_d, of 800 V. To solve the root cause for future modules, the parasitic capacitance between the gate driver traces and the heat sink should be reduced. Recently, J. Shin *et al.* [54] proposed such a solution, by removing parts of the bottom-side copper of the DBC to reduce capacitive coupling, but only in places where effective heat transfer is not necessary. Additionally, a bare die gate driver could be used instead of the prepackaged version used for this paper, as this would result in a more compact layout and more flexibility in the routing. This would also reduce the thermal resistance of the gate driver, by removing some of the layers in its thermal path.

In summary, the chosen integrated power module structure is disadvantageous in terms of electromagnetic compatibility, as capacitive coupling to the heat sink links the high $\mathrm{d}v/\mathrm{d}t$ of the SiC MOSFET to the sensitive gate driver circuit. The advantages of the power module structure is its low inductive design and high voltage capability, which are important aspects used to demonstrate the 1 MHz resonant operation of a 10 kV SiC MOSFET.

Despite the observed issues of the designed power module, this paper has achieved an operating point in terms of drain-source voltage and switching frequency, which is beyond the range of previously published research on 10 kV SiC MOSFETs. The operating points published by other research teams and the results achieved in this paper are shown Fig. 16 for comparison.

5 Conclusion

The purpose of the paper is to prove the high frequency resonant operation of a 10 kV SiC MOSFET device. An integrated DBC power module structure is chosen, as it allows for low inductive design and allows both the semiconductor die and the gate driver to dissipate

its heat effectively. A power module design is proposed, and its layout is evaluated using the simulation software package ANSYS Q3D Extractor. The gate loop inductances are found as 10 nH and 12 nH when clamped to +20 and -5 V voltages, respectively. The drain-source inductance of the module is 5.5 nH, while loop inductance between SiC MOSFET die and parallel capacitance, C_p is 2.4 nH. The gate driver circuit was tested without any drain-source bias, to ensure that both gate driver and SiC MOSFET are capable of operating at high frequencies. A thermographic camera measured temperatures of both gate driver IC and the heat sink, and a thermal resistance of 1.04 $\frac{\mathrm{K}}{\mathrm{W}}$ from gate driver to heat sink is calculated. It was demonstrated that the gate driver was capable of driving the SiC MOSFET up to a frequency of minimum 2.5 MHz. A resonant LC circuit setup is used to verify the ZVS performance of the designed power module. By using L = 25 μH and a parallel capacitance, C_p = 890 pF, the case of a resonant frequency of 1 MHz is tested. The experimental waveforms show very clean switching at an input voltage of V_d = 800 V, at which a peak voltage of 1.6 kV is measured, and proves the capability of the 10 kV SiC MOSFET to operate at 1 MHz. At increasing DC link voltages the high $\mathrm{d}v/\mathrm{d}t$ causes flickering of the gate driver circuit, which limits tests at higher voltages. The proposed integrated medium voltage SiC MOSFET power module design is advantageous for its low inductive design, high voltage breakdown rating and its power dissipation capability of both SiC MOSFET and gate driver. Due to these properties the ZVS operation at 1 MHz was demonstrated of the 10 kV SiC MOSFET.

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