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Compact Sandwiched Press-Pack SiC Power Module with Low Stray Inductance and Balanced Thermal Stress

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***Abstract* - In this letter, a compact SiC power module featuring low stray inductance and balanced thermal resistance is proposed. To make full utilization of SiC devices in high-frequency and high-power-density applications, the laminated busbar and double-sided cooling heatsinks are directly packed as parts of SiC power module. To balance the mechanical and thermal stress on the chips, a press-pack-like package technology is adopted. The electrical and thermal experiments of the prototype are evaluated to validate the design of low inductance and balanced thermal distribution.**

I. Introduction

Silicon-Carbide (SiC)-based power devices can offer higher blocking voltage, higher operating temperature, faster switching frequency, and smaller conduction resistance compared with Si ones [1]. However, one of the hurdles hindering the progress of SiC devices towards practical applications is wire-bond technology with single-sided cooling structure, which is originally developed for Si. The parasitic inductance of the bonding wires limits the SiC devices at high switching-frequency applications [2]. At the same time, the failure mechanisms such as bond-wire lift-off and soldering joint crack have a serious effect on the operation reliability [3]. Moreover, the employment of single-sided cooling structure also challenges the thermal management for high power modules.

To fully exploit the potentialities of SiC devices in high-frequency and high-power-density applications, a package technology with less parasitic inductance and optimized thermal performance is highly demanded. A 3D-package concept of planar SiC power modules integrated with double-sided cooling configuration has been already developed in the past [4-5], showing great reduction in parasitic electrical impedance and thermal resistance. In both the above cases, though, the bonding wires and solder joints are still used, therefore a lift off may take place anyway. To completely get rid of bonding wires, a press-pack technology, such as StakPak from ABB [6] or press-pack from Westcode [7], is needed. A press-pack SiC MOSFET has also been presented in [8], which combines the advantages of both press-pack package and SiC devices. However, due to the heatsinks included in the power loop, the total parasitic inductance is inevitably higher than 10 nH and the volume of power module is larger than SiC power modules [8].

In this letter, a more compact and cost-effective package technology is presented for the first time, by utilizing the laminated copper busbar as the electrical terminal. The chips are directly embedded into the busbar structure. No bond wires nor solder joints and ceramic layers are present anymore, hence both the overall inductance and thermal resistance are greatly reduced. The busbar and SiC dies form a sandwiched power module, where thermal dissipation occurs through both sides. To clamp the mechanical assembly and guarantee the electrical insulation, polyether-ether-ketone (PEEK) bolts have been used. To achieve good and uniform electrical and thermal contact, bolts are placed symmetrically around the chips. The effects of the mechanical stress on the thermal distribution of the chips is evaluated by experiments.

II. Configuration of Proposed Press-Pack SiC Module

The exploded view of the proposed press-pack power module is reported in Fig. 1. The chips are embedded inside recesses made in the Cu-busbar elements.

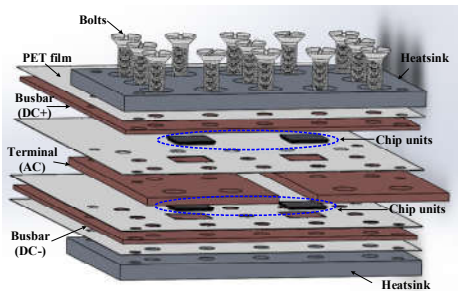

Fig. 1. Explosion view of proposed SiC module.

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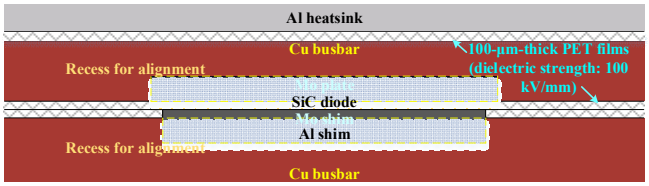
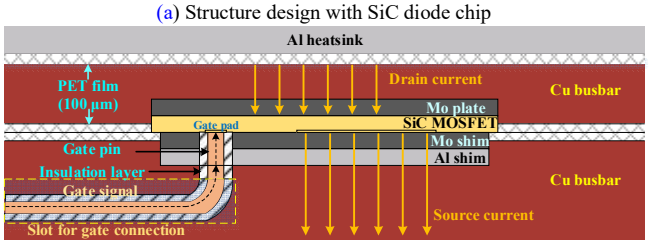
The 100-micrometer-thick polyethylene terephthalate (PET) films provided by Mylar® of DuPont Teijin Films [9], are inserted inside the power module. The dielectric strength of this PET film is more than 100 kV/mm. Consequently, the voltage blocking capability could be guaranteed. The electrical topology is a full bridge, where SiC diodes are used as initial step, therefore the structure operates as single-phase rectifier.

The cross sectional view of the chip unit is shown in Fig. 2(a). A molybdenum (Mo) square plate is placed between the copper (Cu) busbar and SiC chip (VS-H2257H12A6x) to match the coefficients of thermal expansion (CTE). An aluminum (Al) shim and a Mo shim are placed between the chip and the other side of copper busbar. The Al shim is used to uniformly distribute the pressure. Under high-current conditions, the Mo shim and Al shim can form the eutectic alloys with the chip to avoid short circuit. On all the internal surfaces of Cu busbar elements, a recess is made for positioning and aligning the chips. Around the chip, the PET film is used to fill the space between different layers of busbar.



(a) Structure design with SiC diode chip



(b) Structure design with SiC MOSFET chip

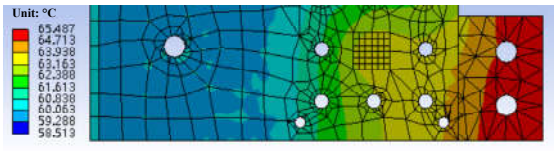
Fig. 2. Sandwiched configuration of press-pack chip unit.

As for SiC MOSFET chips, the structure design for press-pack MOSFET chips is illustrated in Fig. 2(b) (SiC MOSFET CPM2-1200-0080B is taken as an example). A slot is made inside the Cu pad and press-pack unit meanwhile the insulation layer is covered on the surface of the slot to avoid short-circuit between source and gate pad. To connect the gate pad with the copper inside the slot, a gate pin is inserted inside the press-pack chip unit. It is adopted from the internal construction of IXYS press-pack IGBT module [7] [10]. Correspondingly, the effects of gate connection on the thermal stress has been investigated on Fig. 3.

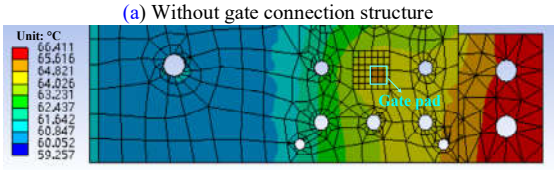
The thermal model is analyzed with finite-element-method (FEM). Due to the symmetrical layout of the module, only half part is simulated. When one chip is heated with a power injection of 10 W and the ambient temperature is set as 25 °C, without gate connection the maximum temperature is about 65.5 °C in Fig. 3 (a). If the SiC MOSFET chip is applied and the sandwiched configuration is adjusted as shown in Fig. 2(b), the insulation layer of gate connection structure will lead to higher thermal resistance for heat dissipation. The simulation result in Fig. 3(b) presents the thermal stress distribution on the chip with gate connection design. The temperature of the gate pad is only about 1 °C higher than other part of the chip.

Because the sandwiched structure has been preserved and the relative positions of chips, DC busbar and AC terminals have not been changed, the gate connection structures have little impact on the parasitic inductance of power loop within the power module. And the thermal distribution of the power module is not affected as well because of the same distributed press-pack packaging approach. Hence, it can be concluded that gate connection structure does not change the thermal stress and thermal distribution of the chips too much.

However, to embed the gate slot inside the busbar and make sure the gate pin correctly contacts the gate pad under a proper pressure, a higher demand is put forward on the fabrication of busbar with gate connection. The spring contact through the source busbar like the solution mentioned in [8] can be used to realize the gate connection to withstand the pressure. At same time the printed contact solution may be applied to print and curve a gate trace whose inductance is too small to have any impact on the circuit performance [11]. But both of them make it more expensive and difficult to achieve the mechanical assembly. Since this letter is aimed at the packaging technology of higher power density, lower cost and balanced thermal distribution, SiC diode chips are integrated in the prototype as an initial step to analyze the feasibility of proposed packaging concept.



(a) Without gate connection structure



(b) With gate connection structure

Fig. 3. Thermal dissipation when one chip is heated.

The fabrication process of the prototype with SiC diode chips is introduced in Fig. 4 and is described as follows.

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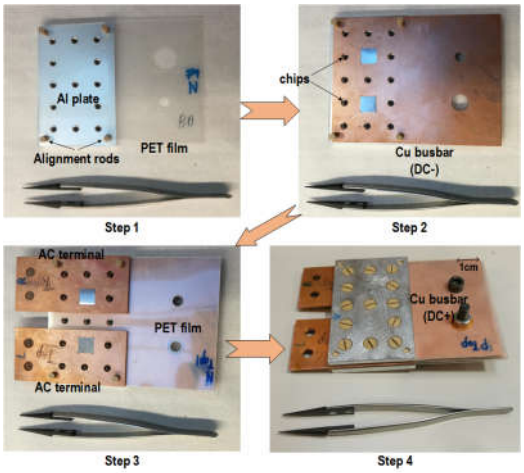

Fig. 4. Process flow of fabrication.

Step 1: alignment rods are used to align holes of the Al cold-plate with threads and put the PET film under the Al cold-plate.

Step 2: DC– Cu busbar and PET insulation layer along the alignment rods. And then mount the chips and the related shims on the recesses of the busbar.

Step 3: Add another PET layer and put the two AC terminals along the rods. Mount the chips and other shims on the recesses.

Step 4: Mount the PET film, Cu busbar (DC+) and another cold-plate. And fasten the assembly with the PEEK bolts.

Fig. 4 presents the picture of the full-bridge prototype of SiC power module. A tweezers is placed next to the prototype to illustrate the size of assembled prototype and the specific dimensions of the prototype is displayed. The compact and integrated press-pack based structure indicates a high-power-density package design.

III. Electro-magnetic Characteristics

Since the heatsinks are isolated by the PET films and the bolts are made of PEEK, the heatsinks and the bolts can be safely excluded in electro-magnetic analysis. The power loop inside the full-bridge rectifier is displayed in Fig. 5.

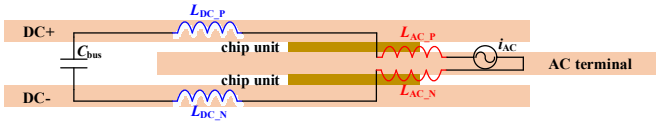

Fig. 5. Power loop configuration of proposed layout and equivalent circuit of parasitic parameters.

The power loop contains DC current path and AC current path. The DC current i_{DC} represents the output average current flowing through the DC terminals while the AC component i_{AC} is circulating inside AC terminals and SiC chip units. To extract the stray inductance of the power loop, the prototype without heatsinks and bolts is modeled and the stray inductance is analyzed in Ansys Q3D. To measure the stray inductance, the DC terminals are short-circuited and the AC terminals are injected with the excitation current i_{AC}.

The stray inductance is measured by the impedance analyzer Keysight E4990A with the power loop configured as Fig. 5. The results comparison is listed in Table I. The parasitic inductance of Q3D is averagely simulated as 7.3 nH while the measurement results are about 8.7 nH. The difference might be caused by the internal parasitic inductance of analyzer.

TABLE I. Parasitic inductances under variable frequencies.

Frequency (Hz)	100	1k	10k	100k
Simulation result (nH)	7.0	7.3	7.3	7.4
Measurement result (nH)	8.5	8.7	8.7	8.8

IV. Balanced Thermal Distribution

A. Distributed press-pack package approach

The thermal management remains a key challenge to the package design of power module in high-power-density applications. Among the chips inside the press-pack power modules, the thermal stresses are not uniformly distributed because the mechanical stresses are not balanced among paralleling chips and the thermal resistance is negatively correlated with the mechanical stress on the chips [12]. According to [13], the pressure on the silicon chips at the edge of the press-pack power module is extremely low during clamping process compared to the silicon chips located in the center. Hence the unbalanced thermal stress will be introduced and junction temperature of the chips at the edge or corner of press-pack power module is higher than those in the middle.

The root reason of unevenly distributed stress for the pressed chips is illustrated in Fig. 6. σ_a and σ_b are the mechanical stress distributed on the pressed chips. The clamping force P is usually applied in a lumped way through the clamping pad. The mechanical stress would decay along with the angle increasing from α to β.

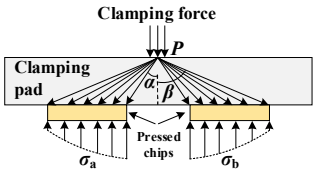

Fig. 6. Distribution of stress on the pressed chips.

This can be proved in the mechanical FEM simulation model in Fig. 7. The equivalent mechanical stress (Von-Mises stress) of the chip is mainly distributed at the edge close to the location of the clamping force, of which the value is about 10 MPa. However, at the edge which is far from the clamping force, the mechanical stress is only 1 MPa. The effective area where the pressure is beyond 10 MPa for optimal thermal contact and electrical contact is less than 20 % of the whole chip.

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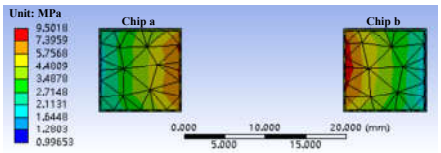


Fig. 7. Simulation results of equivalent (Von-Mises) stress distribution on chips under lumped clamping condition.

In order to balance the mechanical and thermal stress of the pressed chips, a distributed press-pack solution instead of the lumped pressure contact approach is applied in the prototype. It can be seen from Fig. 8 that the bolts are placed evenly around the chip. The clamping force of the stud bolts are equal to each other and controlled by the torque spanner. Moreover, to ensure the insulation capability and the mechanical strength, the material of the bolts is chosen as PEEK and the size is customized as M5 * 0.7 (diameter of bolts is 5 mm and the pitch of threads is 0.7 mm).

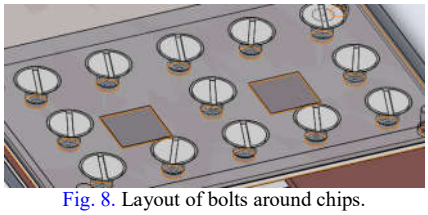


Fig. 8. Layout of bolts around chips.

Because of the bolts fastened around the chips, one more control degree of freedom (DoF) is introduced to optimize the thermal distribution of the SiC power module. And thanks to the symmetrical structure of the prototype, the thermal stress distributed along the vertical direction of the chips is balanced as well. By applying the given pressure of 10 MPa on every bolt, the mechanical distribution of the chips in FEM model is exhibited in Fig. 9. Over 80 % of the chip has the pressure between 10 MPa and 20 MPa, and the pressure is distributed evenly on the chip.

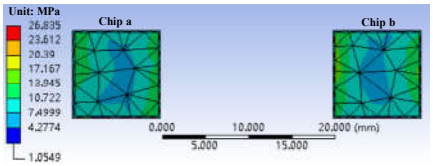


Fig. 9. Equivalent (Von-Mises) stress distribution on chips under distributed press-pack condition.

B. Experiment verifications of thermal distribution

In order to validate the thermal distribution of the assembled prototype, the thermal experiment is carried out with the DC current source. The current flows through the DC+ and DC- terminals hence all the chips are heated. Since the metal parts like Al heatsinks and Cu AC terminals has inefficient emissivity and IR camera is not able to read their temperature, Kapton tape, which is thermally stable and thin enough, is utilized to cover the surface of heatsinks and AC terminals and act as a high-emissivity target to help the IR camera obtain an accurate measurement. The real prototype under thermal test is shown in Fig. 10 and the thermal imagery is shown in Fig. 11. The ambient temperature is stayed at 25 °C. The total of power of 20 W and the prototype is cooled by natural air convection. Since the extreme torsional strength is 1.28 N·m [14], the initiative fastening torque of bolts is set as 0.8 N·m to ensure a safe and tight assembly.

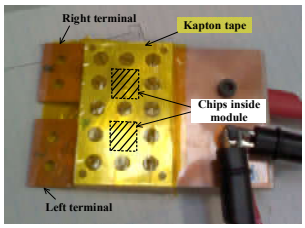
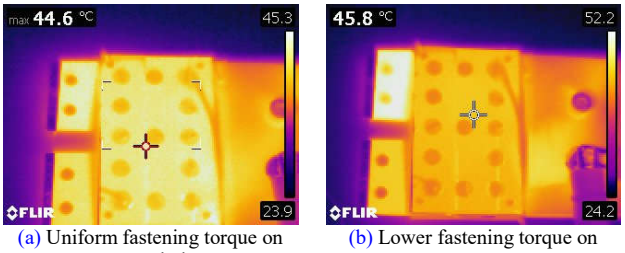


Fig. 10. Configuration of prototype under thermal test.

The chips are directly pressed with the AC terminals so the temperature of the AC terminals can be viewed as the junction temperature of the chips. And it is also the maximum temperature of the prototype when the chips are heated. From Fig. 11(a), it can be seen that the temperature gap between the terminals is within 1 °C. Because the prototype is pressed evenly, the thermal resistance for all the chips are balanced distribution and lead to uniform thermal stress.



(a) Uniform fastening torque on every bolt

(b) Lower fastening torque on bolts of right terminal

Fig. 11. Overall thermal imagery of whole prototype when 4 chips heated.

However, when the fastening torque on the bolts of the right terminal shown in Fig. 11(b) is adjusted as 0.4 N·m, the thermal resistance of corresponding chips and the pressed components increases. The temperature of the loosened chip is 52.2 °C and is 7 °C higher than the fastened chip which is 45.3 °C. It has verified the effect of the pressure distribution on the thermal stress distribution. The feasibility of distributed press-pack package approach has also been validated.

V. Conclusion

In this letter, a compact sandwiched press-pack based package concept has been investigated and explored. By integrating the busbar and the SiC chips directly, the low inductive design was achieved and the total parasitic inductance of the prototype was measured as 8.7 nH. By means of the distributed press-pack package approach, the mechanical and thermal stress was balanced and the cost was also saved by simplifying the implementation procedure. The experiments were conducted to verify the feasibility of distributed press-pack package technology. By removing the fragile parts in convention package of power modules, the

proposed package technology with SiC devices has been characterized by higher level of integration, which can also improve the power modules' reliability in long-term operation.

REFERENCES

[1] X. She, A. Q. Huang, Ó. Lucía and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193-8205, Oct. 2017.

[2] A. S. Bahman, F. Blaabjerg, A. Dutta and A. Mantooth, "Electrical parasitics and thermal modeling for optimized layout design of high power SiC modules," *in Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2016, pp. 3012-3019.

[3] M. A. Eleffendi, C. M. Johnson, "In-Service Diagnostics for Wire-Bond Lift-off and Solder Fatigue of Power Semiconductor Packages," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7187-7198, Sept. 2017.

[4] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," *in Proc. IEEE Energy Convers. Congr. Expo.*, Montreal, QC, Canada, 2015, pp. 4907-4912.

[5] M. Barrière, A. Guédon-Gracia, E. Woirgard, S. Bontemps, F. Le Henaff, "Innovative conception of SiC MOSFET-Schottky 3D power inverter module with double side cooling and stacking using silver sintering," *Microelectron. Reliab.*, vol. 76-77, pp. 431-437, 2017.

[6] http://new.abb.com/semiconductors/stakpak.

[7] http://www.westcode.com/igbt1.html.

[8] N. Zhu, H. A. Mantooth, D. Xu, M. Chen, and M. D. Glover, "A solution to press-pack packaging of SiC MOSFETS," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp 8224-8234, Oct. 2017.

[9] DuPont Teijin Films. [Online]. Available: http://europe.dupontteijinfilms.com/media/2431/info-mylar-a-electrical-properties.pdf.

[10] Press-pack IGBT, towards the next generation of super switch. [Online]. Available: https://fhi.nl/app/uploads/sites/38/2014/01/KWx-IXYS-UK-IGBT-june14.pdf.

[11] X. Lan et al., "Direct On-Chip 3-D Aerosol Jet Printing with High Reliability," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 7, no. 8, pp. 1369-1376, Aug. 2017.

[12] W. Lai, H. Li, M. Chen, S. Kang, H. Ren, R. Yao, and et al, "Investigation on the Effects of Unbalanced Clamping Force on Multi-chip Press Pack IGBT Modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, Early Access, 2018.

[13] E. Deng, Z. Zhao, Z. Lin, R. Han, and Y. Huang, "Influence of Temperature on the Pressure Distribution within Press Pack IGBTs," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6048 - 6059, July, 2018.

[14] http://www.sarltsf.com/products/chemis/peek.html.