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# A Cascaded H-bridge with Integrated Boosting Circuit

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*Abstract*—**This letter proposes a multilevel inverter (MLI), which can be considered to be belonging to the cascaded H-bridge (CHB) family. In the proposed MLI, some of the H-bridges are connected to dc-sources, while most of the H-bridges are connected to only floating capacitors. A boosting circuit is integrated in the CHB, which permits charging the floating capacitors, enabling a higher voltage at the inverter's output with respect to the dc-sources total one. This boosting feature is essential in some applications like photovoltaic and fuel cell systems. Compared to the popular solutions in the literature, the proposal still offers a high boosting ratio with fewer employed components. A prototype of the proposed MLI has been built, and the results confirming its validity are shown in this letter. Efficiency analysis and evaluation with respect to one of the conventional solutions is also presented, where it is demonstrated that the proposal shows an improvement of 3.94% according to the European efficiency.**

*Index Terms*—**CHB, Efficiency, Fuel-cell, Grid-connected, Photovoltaic.**

## I. INTRODUCTION

CASCADED H-bridge (CHB) is one of the types of multilevel inverters, which benefits from less diodes compared to the neutral-point-clamped (NPC) inverter, and less capacitors compared to the flying capacitors (FC) inverter. In some applications, like photovoltaic (PV) or fuel cell systems, boosting the voltage is, usually, a must, especially in grid-connected applications, since these technologies generate power under low voltage. Accordingly, a boosting stage is added at the dc-link of each H-bridge [1], which affects the price, efficiency, volume, and weight of the overall power converter negatively. In some configurations, it is suggested to employ Z-source or qZ-source-based power cells instead of H-bridge ones [2], [3]. Although these two topologies offer one stage conversion, the efficiency of the system is still degraded, and a high components count is needed. As it is reported in [4], in a CHB, one of the H-bridges can be connected to only a floating capacitor, which is charged during low output voltage levels and discharged during the high level ones; consequent-

ly, the total output voltage would be higher than the dc-source's. Since this solution does not require any additional components with respect to the previous mentioned ones, it is cheaper and more efficient. However, its limitation lies on the voltage boosting ratio, which is approximately 1.5 only. The capacitor voltage can not be charged above this limit since it discharges faster than it charges, i.e. the capacitor charges under low voltage level where the current flowing in the converter is low; but, it discharges under high voltage level where the current flowing in the converter is high. Accordingly, some solutions for this problem have been proposed, where the voltage in the floating capacitor can be boosted further [5]-[7]. In [5], the authors employed multioutput boost (MOB) stage on an NPC with floating capacitors. This MOB offers flexibility since it charges the floating capacitors under high current, which is independent on the current delivered to the grid/load. Similar concept has been applied in [6]; but, the MLI there is CHB-based, as shown in Fig. 1(a). Pump Charge stage instead of MOB has been used in [7] to charge the floating capacitors of CHB. It is noteworthy that, these configurations not only offer the boosting feature; but also are suitable for the case of not having isolated dc-sources, since
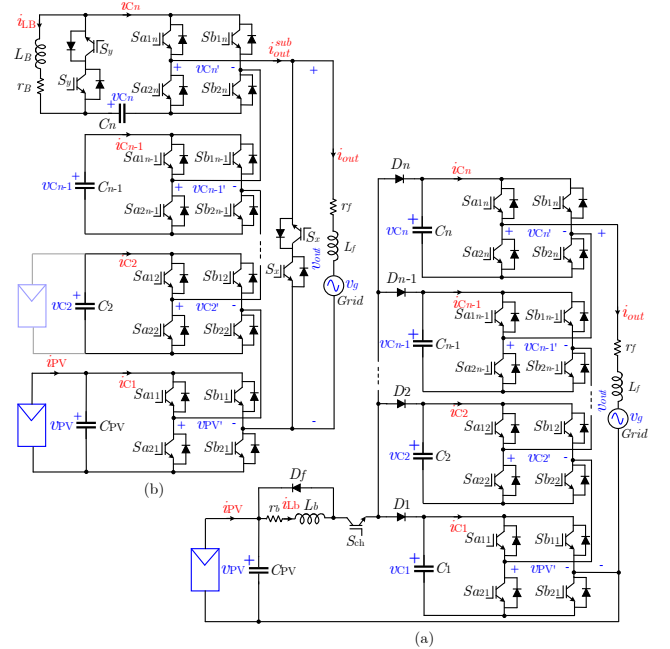


Fig. 1. (a) The conventional MLI fed by a PV system through a MOB stage [6]; (b) The proposed CHB-IB for PV applications.

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the latter are installed in only one cell. Although all these solutions offer the granular boosting ratio, they require high power switches count. Moreover, the count of the active switches, as well as employed inductors increase proportionally with that of the H-bridges with dc-sources.

In this letter, a CHB with integrated boosting stage (CHB-IB) is proposed, wherein the floating capacitors are charged under high boosting current, which permits attaining a high boosting ratio. In the proposed CHB-IB, only one inductor and two bidirectional switches, regardless of the H-bridges with dc-sources count and levels, are added compared to the CHB. It, therefore, uses fewer semi-conductors compared to the other mentioned solutions.

## II. PROPOSED CHB WITH INTEGRATED BOOSTING CIRCUIT

### A. Inverter Description

The proposed CHB-IB is a CHB with few additional components, as depicted in Fig. 1(b), along which the resulted topology boosts the input dc source's voltage. Compared to the conventional CHB, this topology employs a minimum of one dc source, or PV array as considered in this letter, while the other H-bridges are connected to floating capacitors, as shown in Fig. 1(b). It should be emphasized that, many H-bridges can be also connected to PV arrays, as shown by the PV array in faded color in Fig. 1(b), where only one inductor and two bidirectional switches are still employed. However, it is expected to always have H-bridges with floating capacitors more than the ones connected to PV arrays as this topology offers boost capability. The added components are an inductor and two bidirectional switches, where the inductor and one of those switches are installed at the input of one of the H-bridges that are connected to floating capacitors (this power cell is referred to as CELB thereafter). The other bidirectional switch is paralleled to the output of the inverter.

### B. Operation Principle and Modulation

In the remaining of this letter, it is assumed that $n$, which is the total cells count, equals three, and that the floating capacitor power cells' nominal voltage is half that of the PV array. Accordingly, the targeted boost ratio is 2 (a higher one can be still attainted as will be explained later).

In order to decrease the switching loss, the PV power cell is switched only once during each grid's half-cycle, while the floating capacitor cells are switched at the inverter switching frequency ($f_{sw}$). Fig. 2 shows the modulator carriers in the proposed CHB-IB, as well as the output voltage of each cell together with the total resulted one. The floating capacitor cells are controlled through phase-shifted level-shifted pulse width modulation (PS-LS-PWM). The levels near zero (i.e. in the middle) are for charging the capacitors, while the far ones from zero are for discharging them.

### 1) CELB is inserted & Switching function below 0.5 p.u.

In this case, the floating capacitors are inserted according to shifted carriers, one carrier for each floating capacitor, where the shift between two adjacent carriers is $2\pi/(n-1)$. The latter insertion should be opposed to the PV cell's output voltage in order to charge those floating capacitors. This case its self can
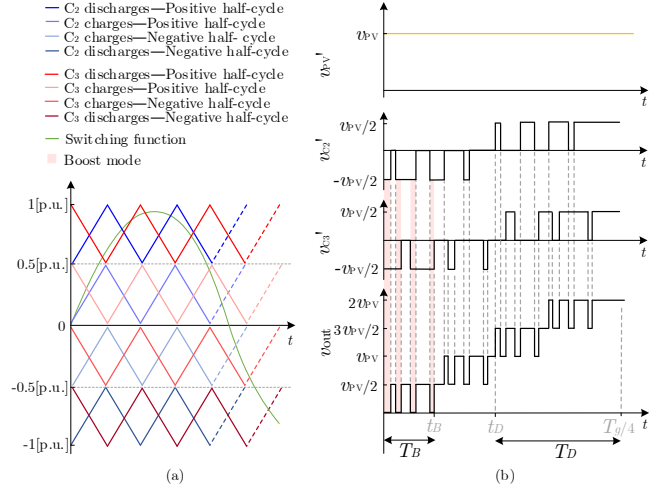


Fig. 2. (a) The employed carriers in the proposed CHB-IB, and (b) the cells and total output voltages.
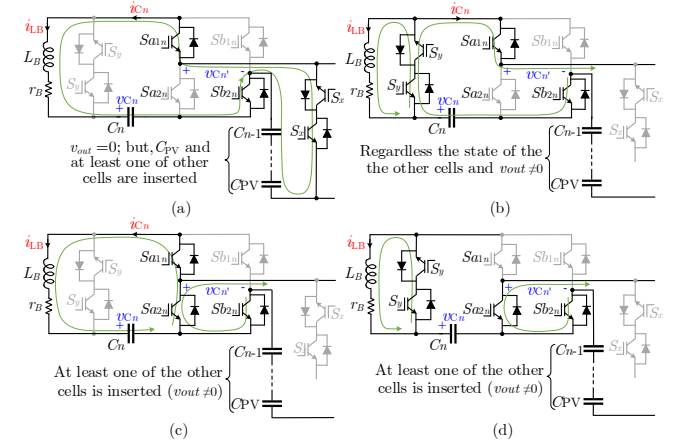


Fig. 3. Different states of CELB, considering the grid's positive half-cycle: (a) the capacitor and inductor are inserted to boost the energy of the latter; (b) inserted while the inductor is free-wheeled; (c) bypassed while the inductor is discharging in capacitor; and (d) bypassed while the inductor is free-wheeled.

be divided into two subcases, where the first subcase is when the total output voltage ($v_{out}$) is at the zero level. In this subcase, $L_B$ is inserted when at least one of the floating capacitors is in boost mode, as shown in Fig. 3(a). The inductor $L_B$ is employed to keep the charging current at a high level and also to limit the inrush current from the PV capacitor to the floating ones. The inductor is inserted by blocking the switch $S_y$, and conducting $S_x$. These time intervals are highlighted by pink bars in Fig. 2(b). $S_x$ plays another role, which is AC-type decoupling when it is turned-on during the zero-voltage vector, achieving a decoupling between the PV panels and the grid. The second subcase is when $v_{out}$ is at least one level far from the zero equivalent. In this situation, the floating capacitors also charge since they are inserted with opposed polarity with respect to the PV one; but, the inductor current $i_{LB}$ is freewheeled, as shown in Fig. 3(b).

### 2) CELB is inserted & switching function is above 0.5 p.u.

In this case, the floating capacitors are inserted according to shifted carriers, one carrier for each floating capacitor, where

the shift between two adjacent carriers is $2\pi/(n\text{-}1)$. These carriers compared to the ones described in the previous subsection are one level shifted, as shown in Fig. 2(a). This insertion should generate voltages in the same polarity as the PV cell's output one in order to obtain a total output voltage level higher than the PV equivalent.

*3) CELB is Bypassed*

When CELB is in the zero state, the extra inductor energy (i.e. when the inductor current goes higher than its reference) is released in the capacitor by short-circuiting the left bridge's leg and blocking the bidirectional switch $S_y$, as shown in Fig. 3(c). If the inductor current is below its reference, the inductor current is freewheeled using $S_y$, as depicted in Fig. 3(d).

*C. Boost ratio*

According to the operation principle explained, the boost ratio is dependent upon, i) the voltage of the floating capacitor cells with respect to the PV ones, ii) the total number of the floating capacitor cells with respect to the PV ones, and iii) number of adopted levels ($l$). This latter affects the time during which the converter boosts the voltage ($T_B$) negatively. The converter boosts the voltage when

$$M \sin(\omega_g t) \leq \frac{2n}{l-1} \qquad (1)$$

From which the time when the converter stops boosting ($t_B$) can be obtained as

$$t_B = \frac{1}{\omega_g} \arcsin \frac{2n}{M(l-1)} \qquad (2)$$

such as $\omega_g$ and $M$ are the grid angular frequency and modulation index, respectively. Note that, for the analysis in this subsection a quarter grid cycle is considered for simplification. The $i$th capacitor's energy ($E_i$) is quadratically proportional to its charge ($Q_i$) as follows

$$E_i = \frac{1}{2C_i} Q_i^2 \qquad (3)$$

The charge as function of the current can be expressed as

$$Q = \int I \, dt \qquad (4)$$

The capacitor's charge change during its discharging can be found by substituting the grid current ($i_{out}$) as follows

$$Q_i^D = \int_{t_D}^{T_g/4} I_\phi \sin(\omega_g t) \, dt = \frac{I_\phi}{\omega_g} \cos(\omega_g t_D) \qquad (5)$$

where $t_D$, $I_\phi$, and $T_g$, are, respectively, the instant at which the $i$th capacitor starts discharging (see Fig. 2(b)), grid current peak, and grid period. As for the charging, two cases are regarded for analysis:

*1) Charging classically (through the grid current)* [4]: In this case, the capacitor's charge change can be estimated as

$$Q_i^B = \int_0^{t_B} I_\phi \sin(\omega_g t) \, dt = -\frac{I_\phi}{\omega_g} \Big[ \cos(\omega_g t_B) - 1 \Big] \quad (6)$$
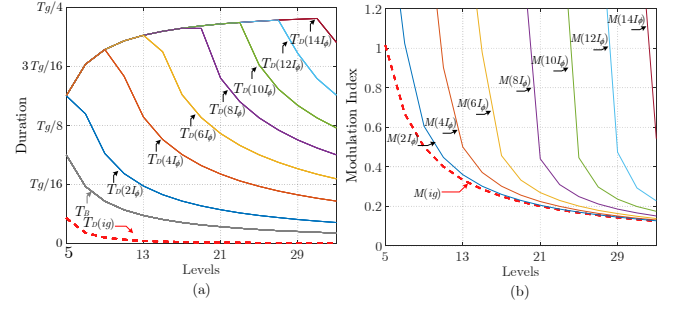


Fig. 4. (a) The boost and discharge durations, as well as (b) the modulation index, both considering different inductor boosting current and level numbers.

In order for the capacitor voltage to be maintained at the desired level, its charge change during the charging $Q_i^B$ and the discharging $Q_i^D$ need to be equal. Hence, from (6) and (5),

$$\cos(\omega_g t_B) + \cos(\omega_g t_D) = 1 \qquad (7)$$

The above equation (7) indicates that, for the charge balance, the times $t_D$ and $t_B$ are trigonometrically complimentary, which with coordination with Fig. 2(a) also means that the discharging duration $T_D$ is always less than the charging one $T_B$, as shown by the red dashed line as well as the grey one in Fig. 4(a). On the other hand, with the increase of levels, the modulation index decreases, as shown in Fig. 4(b), meaning that not all the cells can be inserted simultaneously, which in turn, implies that the boost ratio of the converter's is degraded.

*2) Charging using the proposed approach:*
In the proposed approach, the floating capacitors are charged under relatively higher boosting current. By assuming that the latter is constant, the capacitor's charge change during the charging can be estimated as

$$Q_i^B = \int_0^{t_B} i_{LB} \, dt = i_{LB} t_B \qquad (8)$$

By equalizing (8) and (5), $t_D$ can be assessed as

$$t_D = \frac{\arccos(i_{LB} t_B \omega_g \, / \, I_\phi)}{\omega_g} \qquad (9)$$

The latter equation indicates that, contrary to the case of charging under the grid current, $t_D$ is flexible here, which can be decreased by increasing the inductor boosting current, i.e. the discharging duration $T_D$ can be increased by increasing the inductor boosting current, as shown in Fig. 4(a). This also allows attaining high modulation indices even when employing high levels count, as shown in Fig. 4(b), which eventually makes it possible to insert all the cells simultaneously, reaching a high boost ratio,

$$v_{out} = v_{PV}\Big(S_{a11} - S_{b11}\Big) + \sum_{i=2}^{n} v_{Ci}\Big(S_{a1i} - S_{b1i}\Big) \quad (10)$$

It is worth to note that $v_{Ci}$ is limited to half $v_{PV}$, which is not the case in [6]. From Fig. 3(a), and by considering $\Delta i_{LB}$ as the desired current ripple in the inductor over a maximum zero states duration $\Delta T_{max}$ gives,
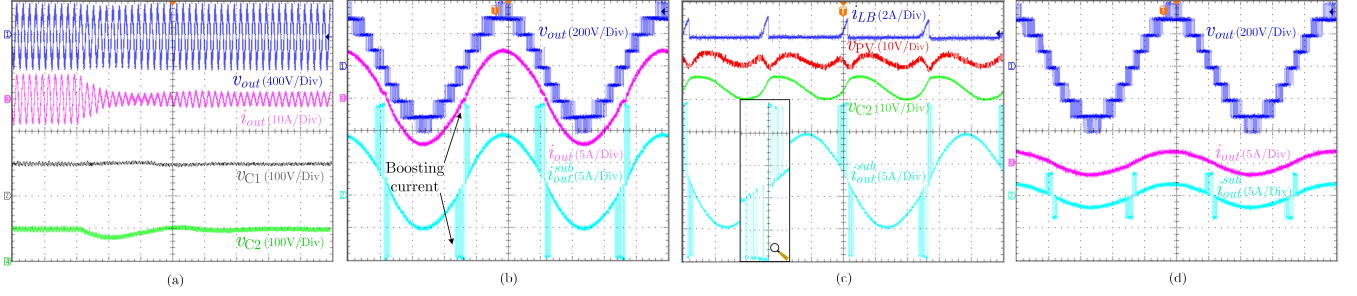
Fig. 5. The obtained experimental results during (a) the STC followed by partial shading. (b) and (c) zoom-in views during STC. (d) a zoom-in view during partial shading. **Note that, the plots in (c) are with offsets for a clearer reading.
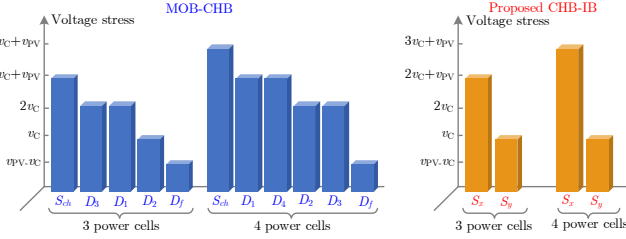


Fig. 6. A comparison between the MOB-CHB and proposed inverter.

$$L_B = \frac{\Delta T_{\max}}{\Delta i_{LB}}\left(v_{\mathrm{PV}} - \sum_{i=2}^{n} v_{Cn}\right) \qquad (11)$$

## III. COMPARATIVE ANALYSIS

The chart in Fig. 6 shows a comparison between the CHB-MOB and proposed CHB-IB, in terms of components count and voltage stress. As it can be seen from this chart, the CHB-IB uses three and four fewer semiconductor devices in, respectively, the cases of using three and four power cells. Moreover, the MOB-CHB operates two diodes under two cells voltage in case of three power cells, and the voltage stress of the diodes keeps increasing with the level increase. In the CHB-IB, however, only the voltage in $Sx$ keeps increasing with the total output voltage, as shown in Fig. 6.

## IV. EXPERIMENTAL VALIDATION

### A. System Description

In order to confirm the feasibility of the proposed inverter, an experimental prototype has been built, which has the following specifications. The built 2kW inverter consists on one PV cell, one cell with floating capacitor, and CELB, where the voltage of the PV cell is 200V, while the other cells operate at half of that, each. Two E4360A Agilent PV simulators have been used, emulating the behavior of five serially connected Soltech 1STH-325-WH PV arrays, which are characterized by $v_{\mathrm{OC}}$=49V, $i_{\mathrm{SC}}$=8.70A, $v_{\mathrm{MPP}}$=40.6V, and $i_{\mathrm{MPP}}$=8A. All capacitors have been selected as 2m$F$. The boosting inductor has been selected as 1.8mH, while the filtering one has been set as 6mH. The carriers and output frequencies were, respectively, 3kHz and 50Hz.

### B. Test Results

The system has been tested during two-time intervals, emulating different weather conditions. During the first time-interval, the system operates under the standard test conditions (STC), and after a while, the solar irradiance decreases suddenly by 70%, considering it as a second time-interval.

Fig. 5(a) shows the obtained results during the aforementioned time intervals, where the output voltage, output current, capacitor voltages are considered. As it can be seen from this figure, the proposed converter conserved the same output voltage, despite the solar irradiance decrease. Accordingly, it kept delivering the harvested power during both test time intervals. As it can be observed from the same figure, capacitor $C_2$ voltage has been slightly affected by the solar decrease; however, it was just a transient, as the output current of the inverter is regulated from CELB. Capacitor $C_1$ voltage was unnoticeably affected.

A zoom-in view of the first time-interval is shown in Fig. 5(b). As it can be seen from this figure, the proposed inverter provides a nine-level stair-case like output voltage, where the output current is close to sinusoidal. Fig. 5(c) shows a zoom-in view of the same time-interval; but considering the inductor boosting current, PV voltage, and $C_2$ voltage. As it can be seen from this figure, $C_2$ charges during the converter zero states, causing $i_{\mathrm{LB}}$ to increase, which is at the expense of $C_{\mathrm{PV}}$ charge. The latter capacitor charges again soon after the zero states, and discharges a second time when the output current increases. Since $C_{\mathrm{PV}}$ discharges three times during each half cycle, i.e. in the floating capacitors, in the inverter output, then in the floating capacitors again, it suffers from lower ripple than the floating ones, as shown in the same figure.

Fig. 5(d) shows the obtained results during the second time-interval. As it can be seen from this figure, the output current has been decreased due to the partial shading; however, it was kept close to sinusoidal waveform. It can be also noted from the same figure that, $i_{out}^{sub}$ peak also decreased, which is due to the decrease of $i_{\mathrm{LB}}$. This latter was decreased by the controller intentionally to limit from the power loss dissipated in CELB since the output current decreased and the capacitors charge in shorter time now.

### C. Efficiency Evaluation

In order to evaluate the efficiency of the proposed inverter, it has been thermally modeled and compared to one of the
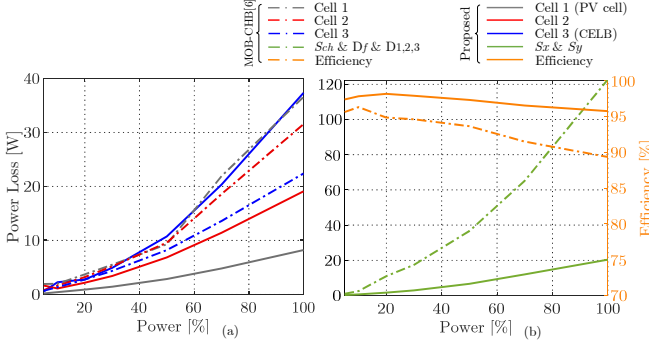
Fig. 7. The power loss and efficiency in both topologies under evaluation.

conventional solutions, namely MOB-CHB. In order to have a fair comparison, the same IGBTs were employed in the CHB parts of both inverters, and they were IRG6B330UD. Due to the different ratings in the remaining power switches, different ones have been used, where for the MOB-CHB diodes, IDP45E60 were used, while for $S_x$ and $S_{ch}$, STGW40V60DF were the used ones.

Fig. 7 shows the obtained loss in each power cell of both proposed topology and MOB-CHB, where the conduction and switching loss are combined. Note that the obtained efficiencies of both inverters are shown in the same figure.

Starting by MOB-CHB, it can be seen that cell 1 has more loss compared to cell 2, and the latter has more loss compared to cell 3. This is due to the fact that the boost can be applied in the specific cell when it and cells below it are in zero state. In the proposed topology the power loss are lower in the PV cell since it switches only once per grid half-cycle. The power loss are higher in cell 2, as it switches according to $f_{sw}$. Furthermore, CELB suffers from the highest power loss as it switches at $f_{sw}$ and also has higher current stress on the switches due to the current passing through $L_B$. By comparing MOB-CHB with the proposal it can be seen that, they each have one cell with similar loss, while considering the other two cells, the power loss are lower in the proposal.

Regarding the added switches, i.e. $S_{ch}$ & $D_f$ & $D_{1,2,3}$ in MOB-CHB and $S_x$ & $S_y$ in the proposal, it is clear that the MOB-CHB again suffers from more power loss, as shown by Fig. 7(b). This lies on the fact that, the MOB-CHB employs higher components count. Moreover, $S_{ch}$ operates under $2v_C+v_{PV}$, $D_1$ and $D_3$ operate under $2v_C$. Whereas in the proposed topology, only $S_x$ operates under $2v_C+v_{PV}$, and all the remaining power switches operate under $v_C$. Accordingly, the proposed topology has reached higher total conversion efficiency in the whole power range, as shown in Fig. 7(b), resulting to an improvement of $3.94\%$ according to the European efficiency.

## V. CONCLUSION

A CHB-IB has been proposed in this letter, in which some of the H-bridges are connected to dc-sources, while the rest of them are connected to only floating capacitors. The voltage can be boosted from the dc-sources "or PV panels as considered in this letter" to the floating capacitors through the integrated boosting circuit, which consists on only two bidirectional switches and an inductor. The CHB-IB,

therefore, employs fewer semiconductor devices with respect to its counterparts. Moreover, the CHB-IB still employs the same components count, even when the level and/or dc-sources count increase. The obtained results by the built experimental prototype confirm the feasibility of the proposal. Last but not least, the CHB-IB has been compared to the MOB-CHB in terms of power loss and efficiency, where it was shown that the proposal suffers from lower loss due to the fewer employed semiconductor devices, as well as due the lower voltage stress in some devices.

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