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Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2019.2938224

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):
Khan, M. N. H., Siwakoti, Y., Li, L., & Blaabjerg, F. (2020). H-Bridge zero-voltage switch-controlled rectifier transformerless midpoint-clamped inverter for photovoltaic applications. *I E E E Journal of Emerging and Selected Topics in Power Electronics*, *8*(4), 4382-4394. Article 8819964. https://doi.org/10.1109/JESTPE.2019.2938224

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H-Bridge Zero-Voltage Switch Controlled Rectifier (HB-ZVSCR) Transformerless Mid-Point-Clamped Inverter for Photovoltaic Applications

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Abstract- A single-phase transformerless mid-point clamped H-bridge zero-voltage switch-controlled rectifier inverter topology is proposed in this paper for photovoltaic (PV) systems to address the issue of common mode (CM) voltage and leakage currents. Apart from the full H-bridge inverter, the proposed voltage clamping circuit consists of two switches and a full-bridge diode which clamps the AC terminal to the DC midpoint (consisting of two DC-link capacitors) during the freewheeling period. As a result, the common mode voltage is held constant which makes it suitable for the grid-connected PV system. The operating principle and CM effect of the proposed topology are analysed and compared with the conventional topologies. This is followed by the thermal analysis and loss calculation, which shows that the proposed circuit is more efficient over the conventional topologies. Validation is carried out using MATLAB-Simulink using the PLECS toolbox followed by a scale down prototype of 1.5 kW. It is shown that the proposed inverter has the 98±1% efficiency over a wide range of loads with a peak efficiency of 98.96%, and the total harmonic distortion of the output current relatively low (≤1.8 %). The leakage current (i_{cm}) is measured for different values of parasitic capacitance that reaches a maximum of 16.65 mA for 330 nF capacitor under consideration which is well below the limit set by different safety standards.

Index Terms— Common mode voltage (CMV), leakage current, mid-point clamping, photovoltaic system.

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I. INTRODUCTION

Due to the growing demand for clean energy, renewable energy sources are becoming popular. Especially solar photovoltaic (PV) systems are of prime interest because of their low maintenance cost and ease of installation compared to other renewable sources. Therefore, the deployment of PV system is rapid in both small (rooftop type) and large utility-scale solar farm applications. According to the annual report of the International Energy Agency-Photovoltaic Power Systems Program, the global installed PV capacity is estimated to be roughly 531.3 GW by the end of 2018 [1] [2]. It is expected that the PV would reach the terawatt production capacity level in 2022 [3]. The major driving force behind this development is the reduction in the cost of PV panels continuously and generous subsidy from the government of different countries to promote the clean energy [2]-[3].

For a grid-connected PV system, a transformer is often used to provide galvanic isolation between the PV panels and the grid and to provide voltage ratio transformation. However, these conventional iron and copper-based transformers increase the weight/size and cost of the inverter while reducing the efficiency and power density [4]-[8]. It is therefore desirable to avoid using transformers in the inverter; however, the additional care must be taken to avoid safety hazards such as ground fault currents and leakage currents, e.g. via the parasitic capacitance between the PV panel and/or its frame and the ground as shown in Fig. 1. Consequently, grid-connected transformerless PV inverters must comply with strict safety standards such as DIN VDE V 0-126-1-1, and IEC 62109-2, where the leakage current limit is both set to be less than 300 mA [9].

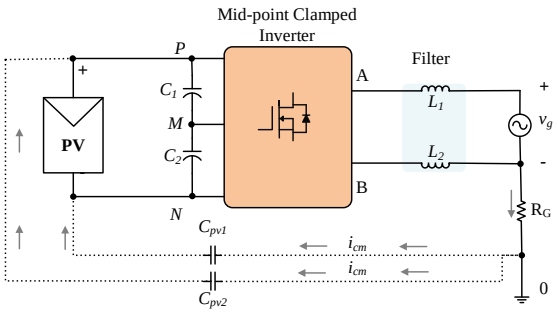

Fig. 1. The general layout of a mid-point clamped type single-phase transformerless inverter.

To eliminate the common mode (CM) leakage current during the freewheeling period, many transformerless topologies are proposed in the literature such as DC bypass topologies (i.e., H5, Hybrid, and H6), and AC bypass topologies (i.e., HERIC) [9]-[12]. Nevertheless, the leakage current cannot be simply eliminated by galvanic isolation and modulation techniques, due to the presence of switches' junction capacitances and resonant circuit effects. During the freewheeling time, the DC-bypass or AC-bypass switches disconnect the DC-link from the grid. Therefore, the voltage across point A to neutral (N) and point B to neutral (N) is floating with respect to the DC-link. The switching state does not determine the common mode voltage (CMV) during this

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period, but instead, oscillates with an amplitude depending on the parasitic parameters and the switches' junction capacitances of the corresponding circuit. Therefore, the leakage current can still flow during the freewheeling period [11]-[12].

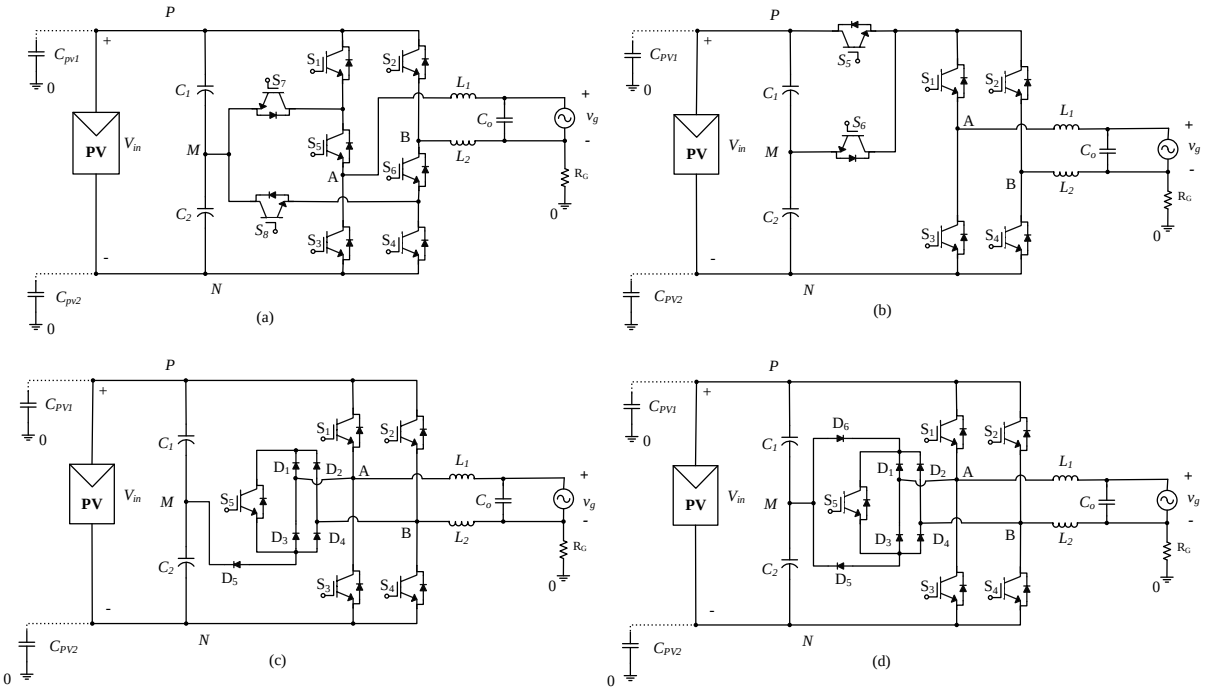

Fig. 2. Existing mid-point clamping topologies; (a) PN-NPC [14], (b) oH5 [15], (c) HB-ZVR [16] and (d) HB-ZVR-D [17].

In order to generate a constant CMV, a mid-point clamping branch is introduced in [13]-[17] using a capacitor divider as shown in Fig. 2 to make sure that the freewheeling path is clamped to half of the DC-link voltage. Fig. 2(a) and Fig. 2(b) shows PN-NPC [14] and oH5 [15] mid-point clamping topologies respectively where both topologies use DC-decoupling method. In these topologies, two or more switches are active during the positive and negative states, which results in higher conduction losses and lower efficiency. Meanwhile, there is a short period of time (during the dead-time, between the active vector and the zero state) when all switches are turned OFF and the freewheeling current of HB-ZVR topology (see Fig. 2(c)) [16] finds its path through the anti-parallel diodes to the input capacitor. It leads to higher losses. On the other hand, the clamping branch of HB-ZVR does not function optimally as it is only clamped well in one-half cycle when the freewheeling path voltage (V_{FP}) is greater than half of the DC link voltage (V_{PN}) ($V_{FP} > \frac{V_{PN}}{2}$), but CMV is fluctuated with high frequency when the freewheeling path voltage is less than half of the DC link voltage ($V_{FP} < \frac{V_{PN}}{2}$). It happens owing to the limitation of the clamping branch. This problem is mitigated in HB-ZVR-D (see Fig. 2(d)) [17] by adding a fast recovery diode. The combination of diodes D_5 and D_6 with switch S_5 forms a clamping branch for the freewheeling path, but the additional loss in the switch and diodes reduces the overall efficiency of the system.

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Considering all these aspects, a modified H-bridge clamped transformerless inverter is presented in this paper to obtain high efficiency and low leakage current with constant CMV compared with the topologies mentioned above.

This paper is organized as follows: Section II presents the proposed topology with its conversion structure, operating principles, modulation strategies, CM effect, and component selection guidelines. Further, a comparative thermal analysis is presented in Section III to show the losses in the proposed topology and some selected existing single-phase mid-point clamped transformerless inverter topologies. This is followed by the simulation and experimental results both for a 1.5 kW prototype in Section IV. Finally, a conclusion is made in Section V to summarize the findings and results.

II. PROPOSED HB-ZVSCR TOPOLOGY

a) Description of the proposed HB-ZVSCR circuit

A new topology called H-bridge zero-voltage switch-controlled rectifier (HB-ZVSCR) is proposed as shown in Fig. 3. The circuit consists of two switches and a full-bridge rectifier which clamps the AC terminal to the DC midpoint (consisting of two DC-link capacitors C_1 and C_2) during the freewheeling period. This topology is a modified topology of both HB-ZVR [16] and HB-ZVR-D [17]. The proposed topology replaces two diodes of the HB-ZVR-D with two extra switches and eliminates the bidirectional switches to alleviate the loss. The freewheeling path is created by the bridge rectifier and extra switches (S_5 and S_6), where during the zero-voltage vector the mid-point of the DC-link is clamped to the AC terminals which bypass the flow of leakage current to the grid.

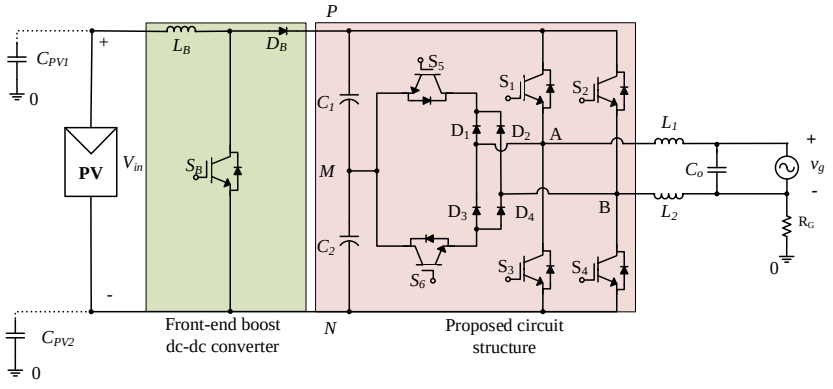

Fig. 3. The proposed transformerless inverter circuit.

b) *Operating principle*

According to the operating principle of the proposed HB-ZVSCR topology, there are four operating modes. Mode 1 and Mode 3 operate in the positive half-period of the grid voltage, while Mode 2 and Mode 4 operate in the negative half of the grid voltage. Fig. 4(a) shows Mode 1. S_1 and S_4 are ON while S_2 and S_3 are OFF. The current increases and flows through S_1, S_4 and load where the positive DC-link voltage ($+V_{PN}$) appears across the

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filter capacitor. In Mode 2, S_2 and S_3 are active while S_1 and S_4 are OFF (see Fig. 4(b)). The output voltage is equal to the negative DC-link voltage ($-V_{PN}$). Mode 3 shows the freewheeling path for positive half-period (see Fig. 4(c)) and Mode 4 demonstrates the freewheeling path for negative half-period (Fig. 4(d)). In the positive freewheeling time, switches S_5 and S_6 are ON with diodes D_2 and D_3 and in the negative half cycle freewheeling path, where the output current goes through D_1, D_4 and the switches S_5 and S_6.

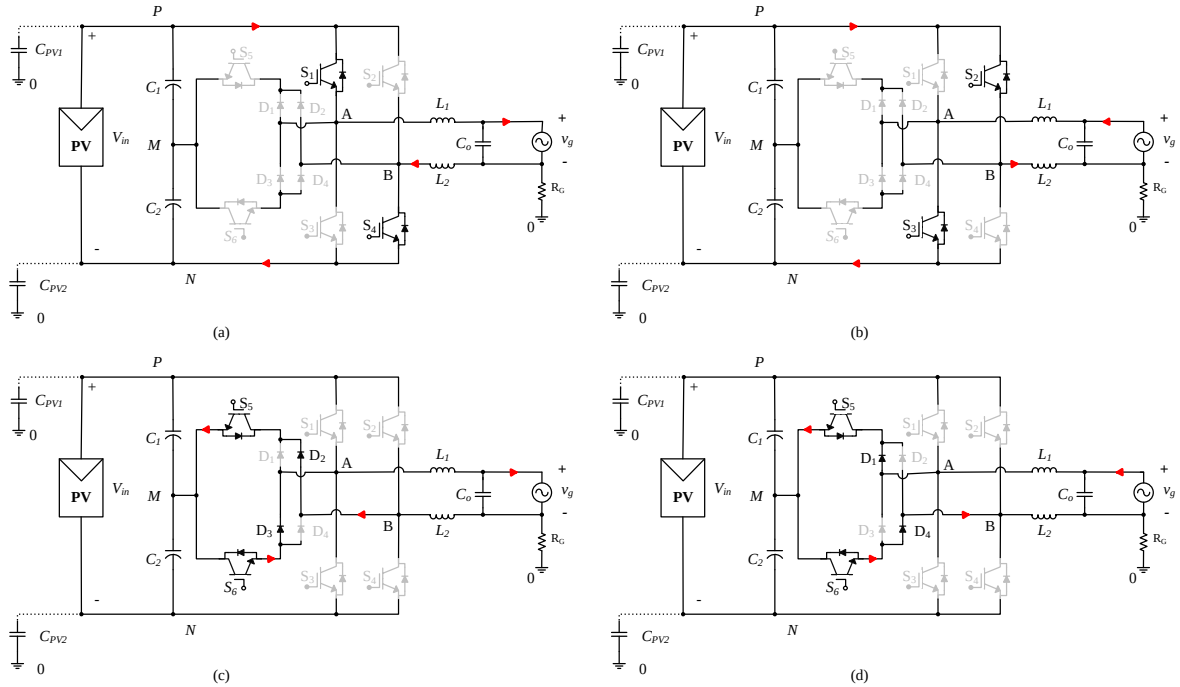

Fig. 4. Operating modes of HB-ZVSCR inverter, (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

c) Modulation strategy

A unipolar sinusoidal pulse width modulation (SPWM) technique is employed in the proposed HB-ZVSCR topology as shown in Fig. 5.

The modulation signal can be written as follows,

$$R_{Sig} = A \sin \omega_s t \tag{1}$$

where A is the maximum amplitude value of the reference waveform, ω_s is the angular frequency.

The maximum amplitude of a carrier signal (n) is 1 and the modulation index as defined in (2) is:

$$M = \frac{A}{n} < 1. \tag{2}$$

The reference signal is compared with the triangular carrier signal. In the positive half-period, S_1 and S_4 have the same driving signals, and S_5 and S_6 have the opposite driving signals. In the negative half-period, S_2 and S_3 have the same driving signals, and S_5 and S_6 have the opposite driving signals.

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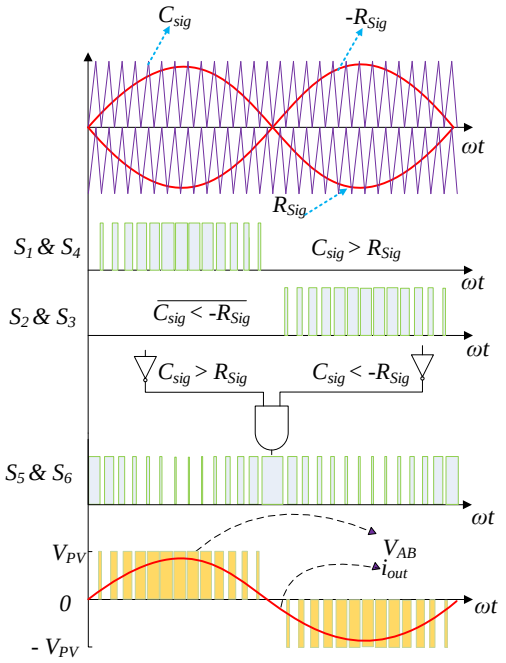

Fig. 5. Pulse width modulation for the proposed topology.

d) Common mode effect

In order to investigate the ground leakage current (i_{cm}), the equivalent CM circuit is presented in Fig. 6 where M represents the combination of the mid-point clamping point, the filter inductors L_1 & L_2, and the parasitic capacitor C_{PV}. The power circuit can be replaced with phase voltages of the inverter V_{AN} and V_{BN} which are equal to the potential of A and B points relative to the point N [14]-[19].

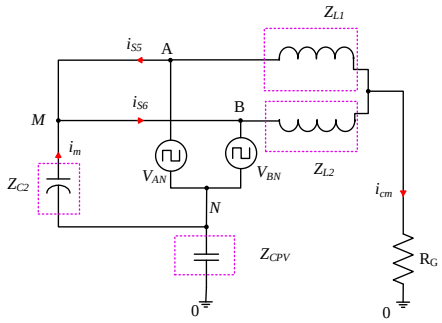

Fig. 6. Common-mode equivalent circuit of the proposed PV inverter.

The CMV and differential-mode voltage (DMV) can be written based on the phase voltages as follows:

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \tag{3}$$

$$V_{DMV} = V_{AN} - V_{BN} \tag{4}$$

Moreover, the phase voltages can be expressed based on V_{CMV} and V_{DMV} as mentioned in (5) and (6).

$$V_{AN} = V_{CMV} + \frac{V_{DMV}}{2} \tag{5}$$

$$V_{BN} = V_{CMV} - \frac{V_{DMV}}{2} \tag{6}$$

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The voltage at point "B" relative to "N" and "A" relative to "N" is zero for the proposed topology at the positive and negative half cycle respectively, so the CMV is equal to half of the DC-link voltage (see (7)-(9)).

$$V_{CMV}(\text{positive half cycle}) = \frac{V_{PN} + 0}{2} = \frac{V_{PN}}{2} \tag{7}$$

$$V_{CMV}(\text{negative half cycle}) = \frac{0 + V_{PN}}{2} = \frac{V_{PN}}{2} \tag{8}$$

$$V_{CMV}(\text{zero Vector states}) = \frac{\frac{V_{PN}}{2} + \frac{V_{PN}}{2}}{2} = \frac{V_{PN}}{2} \tag{9}$$

The equivalent CMV (V_{ECMV}), and leakage current (i_{cm}) shown in Fig. 6 and Fig. 7 are obtained as

$$V_{ECMV} = V_{CMV} + \frac{V_{DMV}}{2} \times \frac{L_2 - L_1}{L_1 + L_2} \tag{10}$$

$$i_{cm} = \frac{V_{ECMV}}{Z_{EQU}} = \frac{V_{ECMV}}{Z_{C2} + (Z_{CPV}) + (Z_{L1} // Z_{L2}) + R_G} \sim i_m \tag{11}$$

$$i_m = i_{S6} - i_{S5} \tag{12}$$

where $Z_{CPV} = (Z_{CPV1} // Z_{CPV2})$.

The maximum leakage current flows during the freewheeling time due to non-separation between PV panel and grid at the freewheeling time. Hence, the mid-point clamping connection helps to get the current path (see Fig. 6 and Fig. 7). This circuit can be demonstrated in the *s*-domain to analyse the frequency and magnitude of the created resonant circuit (see Fig. 7(c)). Letting $L_1 = L_2$ in (10) for the topologies with symmetrical structure (e.g. H-bridge), the equivalent CMV can be replaced with $\mathrm{V_{CMV}}$. The transfer function from i_{cm} to CMV created by the converter through the resonant circuit can be expressed as (13) and (14).

$$V_{ECMV}(s) - \left(L_f s + \frac{1}{sC_{PV}}\right) i_{cm}(s) = 0 \tag{13}$$

$$H(s) = \frac{i_{cm}(s)}{V_{ECMV}(s)} = \frac{s}{L_f s^2 + \frac{1}{C_{PV}}} \tag{14}$$

In (13) and (14), $L_f = (L_1 L_2)/(L_1 + L_2)$. Fig. 8 illustrates the Bode plot of the transfer function in (14) considering $L_1 = L_2 = 2.6$ mH and $\mathrm{C_{PV}}$ =68 to 330 nF. It shows the changing resonant frequency values based on C_{PV}, while the magnitude remains almost same.

It is evident that the resonant frequency varies from 7.68×10^3 to 16.9×10^3 Hz for different parasitic capacitor from 68 to 330 nF. Moreover, as the filter inductor and parasitic capacitor forms a typical LC resonant circuit, its resonant frequency can be calculated theoretically using (15). Both the simulation and analytical results show the equal resonant frequency, with which a large CM current i_{cm} flows into the system.

$$f_r = \frac{1}{2\pi\sqrt{L_f C_{PV}}} \tag{15}$$

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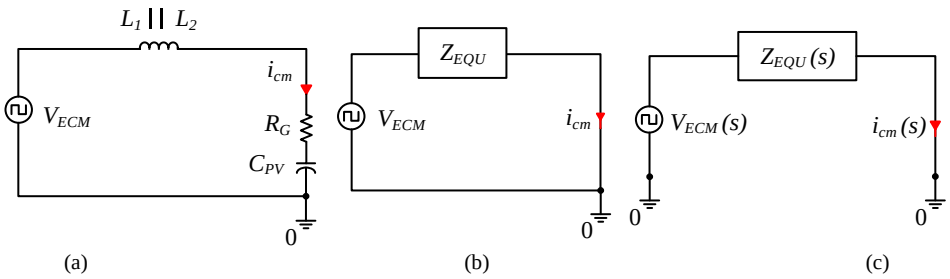

Fig. 7. Simplified single loop CM model, (a) considering the series connection of components, (b) the equivalent impedance circuit, and (c) the *s*-domain equivalent circuit.

Without galvanic isolation, the potential between the PV array and the ground (V_{ECMV}) fluctuates, which charges and discharge the parasitic capacitor (C_{PV}). This fluctuating CMV activates the resonant circuit as discussed above and may lead to higher ground leakage current. However, the resonant frequency is not fixed, as it depends on the parasitic capacitance together with the DC-link that connects the PV array to the inverter. It also depends on the size of the PV array and the environmental conditions. All these conditions make the elimination of leakage current more difficult in practice.

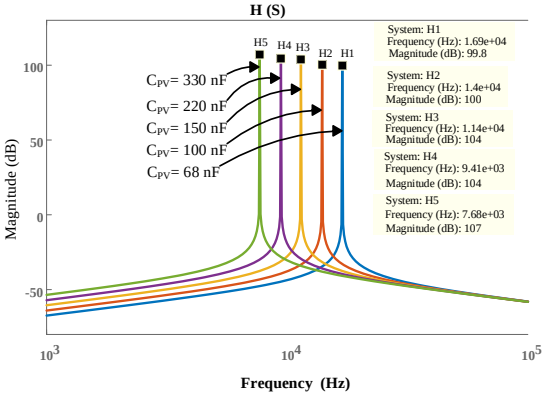

Fig. 8. Bode plot of the resonant circuit model in Fig. 7.

e) Component selection guidelines

A component selection guideline at the end is helpful in estimation and selection of the parameters for the practical design. First of all, the voltage and current rating of the active switches and diodes must be selected just above the safety margin. Even though the input DC-link capacitor helps to maintain a constant voltage at the DC-link, there are some small spikes in practice across the semiconductor devices. As a result, the voltage and current rating of the selected semiconductor devices are 650 V and above 50 A accordingly.

To select the components of the proposed inverter, a few more things need to be calculated such as DC-link capacitors (C_1 or C_2), and the output filter (L_1 or L_2, and C_o).

The following parameters are considered for the practical design: the switching frequency (f_{sw}) of the inverter is 25 kHz, the input voltage (V_{in}) is 173.5 V, the forward voltage (V_D) of the diode (C5D50065D) is 1.8

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V, the modulation index (M) is 0.90, the DC-link voltage (V_{PN}) is 364 V, and the maximum input current ripple and voltage ripple are selected as 40% of the input value respectively.

The boost inductor can be calculated using (16) which depends on the input current ripple (ΔI_{in}), input voltage (V_{in}) and output voltage of the boost converter. Using (16), the calculated value of the inductor is 0.4 mH.

$$L_{Bmin} = \frac{V_{in} \times (V_{out} + V_D - V_{in})}{\Delta I_{in} \times f_{sw} \times (V_{out} + V_D)} \tag{16}$$

The DC-link capacitors C_1 and C_2 can be calculated by (17) which is dependent on the maximum output load current ($i_{g,max}$) and the permissible voltage ripple across the applied input voltage (ΔV_{in}) of the system. More specific selection can be done by duty ratio (D_b) which is selected 0.5 as a boost converter is used at the front side. As a result, the calculated minimum capacitor value is around 650 µF.

$$C_{1min} \; or \; C_{2min} \geq \frac{i_{g,max} \times D_b \times (1 - D_b) \times 1000}{\Delta V_{in} \times f_{sw}} \tag{17}$$

The selection criteria mentioned here is for voltage source type inverters that only need filter inductor at the output to provide filtering for the output waveform. However, to reduce the inductor size, usually a capacitor is used in parallel with the load, and hence, the solution here would be similar to the use of a low pass LC filter. The required filter inductor depends on output current ripple which is recommended to choose a value between 20% and 40 % of the rated output inductor current (i_{L_f}) [20]. Moreover, the filter inductor value depends on the modulation type, and switching conditions [20], [21]. Thus, the maximum ripple factor (ΔI_{factor}) is given in (18). Fig. 9 shows the waveform of ΔI_{factor} for a selected modulation index (M) to obtain the maximum ripple factor which helps to calculate the filter inductor value by (19). The highlighted maximum ripple factor is approximately 0.25 which, applied in (19) together with a ripple across the inductor of 40%, results in a minimum inductance value of approximately 2.5 mH.

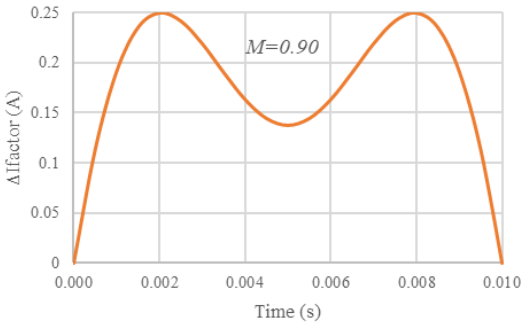

Fig. 9. ΔI_{factor} waveform to highlight the maximum ripple factor.

$$\Delta I_{Factor} = M \; sin \; (2\pi f_m t) - M^2 \; sin^2 \; (2\pi f_m t) \tag{18}$$

where f_m is the fundamental frequency.

$$L_{1min} \text{ or } L_{2min} = \frac{v_g \times \Delta I_{Factor}}{f_{sw} \times \Delta I_{Lf}} \tag{19}$$

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On the other hand, the filter capacitor (C_o) can be calculated by (20) where the cut-off frequency (f_c) is set to be 10% of f_{sw} [19] and the calculated value is approximately 2.2 µF.

$$C_o = \frac{1}{4 \times \pi^2 \times {f_c}^2 \times L_1} \tag{20}$$

III. COMPARISON WITH EXISTING TOPOLOGIES

The following section systematically compares the proposed topology with conventional mid-point clamped transformerless inverter topologies. Table I presents a detailed comparison list of the proposed topology with selected mid-point clamped topologies considering the required input voltage, output voltage, the number of active and passive components to design the inverter, output filter type and its value, CM effect, reactive power capabilities, power factor, total harmonic distortion (THD), cost, and efficiency.

TABLE I. COMPARATIVE SUMMARY OF PROPOSED TOPOLOGY WITH CONVENTIONAL MID-POINT CLAMPED TRANSFORMERLESS INVERTER TOPOLOGIES

Topologies	No. of semiconductor devices		Passive component		Output filter type			Common mode effect		RPC	Reported φ_{pf}	Reported THD	Cost / size*	Reported η (%)
	S	D	L	C	L_1 (mH)	L_2 (mH)	C_f (µF)	i_{cm} (mA)	CMV (V)					
PN-NPC [14]	8	0	0	2	3	3	0.47	< 20	constant	Yes	Unity	N/A	++++	97.2 @ 1 kW
oH5 [15]	6	0	0	2	4	4	6.6	< 20	constant	Yes	Unity	N/A	++	N/A
[13]	7	0	0	2	0.85	0.85	--	< 20	constant	Yes	Unity	1.7%	++++	97 @ 2 kW
HB-ZVR [16]	5	5	0	2	1.8	1.8	2	> 20	constant	Yes	Unity	N/A	+++	94.88 @ 2.8 kW
HB-ZVR-D [17]	5	6	0	2	3	3	6	> 20	constant	Yes	Unity	N/A	+++	95.03 @ 1 kW
H5-D [22]	5	1	0	2	1	1	10	>20	constant	Yes	Unity	N/A	++	95.8 @ 630 W
[23]	9	1	1	2	0.9	0.9	--	< 20	constant	Yes	Unity	4.2%	++++	96.13 @ 220 W
[24]	8	2	2	4	N/A	N/A	N/A	N/A	constant	NR	Unity	N/A	++++	97 @ 1 kW
[25]	8	0	0	2	5	5	5	< 20	N/A	Yes	Unity	4.35%	++++	96.02 @ 1 kW
[26]	7	4	0	2	3	3	4	< 20	constant	Yes	Unity	1.6%	++++	97.65 @ 1 kW
Proposed topology	6	4	0	2	2.6	2.6	2.2	< 20	constant	Yes	Unity	1.8%	+++	98.14 @ 1.5 kW
Proposed topology	6	4	0	2	2.6	2.6	2.2	< 20	constant	Yes	0.86	1.72%	+++	98.441 @ 1.5 kW

* More "+" represents the higher cost/size: "+" ≡ low, "++" ≡ medium, "+++" ≡ high, and "++++" ≡ extremely high.
In the above table, "S" represents switch, "D" represents diode, "C" represents a capacitor, "L" represents inductor, "η" represents efficiency, "i_{cm}" represents leakage current, "CMV" common-mode voltage, "RPC" reactive power capability, "φ_{pf}" power factor, "THD" total harmonic distortion, "NR" not recommended, "N/A" not available.

It can be seen that the proposed topology requires the least semiconductor devices with low CM effect. Moreover, as seen in Table I, other conventional topologies were reported only with a unity power factor and the information about the reactive power capability is not available; on the othe hand, the proposed topology has reactive power capability as demonstrated by 0.86 power factor where the THD reduces to 1.72%. The prototype cost and size depend on the number of components required in the system design. A careful analysis and comparison of the cost of the mentioned topologies and the proposed topology reveal that the cost and size of the

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proposed topology are reasonably less [19], just a little larger than oH5 [14] and H5-D [22]. Moreover, the proposed topology beats all other topologies in terms of efficiency (98.8 % at a 1.5 kW full load condition).

TABLE II. VOLTAGE STRESS COMPARISON OF SELECTED MID-POINT CLAMPING TOPOLOGIES.

Topologies	Voltage stress	No. of semiconductors in the current path		No. of high-frequency switches
		positive	negative	
HB-ZVR [16]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{PN}$	2	2	4 (f_{sw} for half-cycle only) 2(f_{sw} for full-cycle)
HB-ZVR-D [17]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{PN}$	2	2	4 (f_{sw} for half-cycle only) 2(f_{sw} for full-cycle)
PN-NPC [14]	$V_{S2} = V_{S3} = V_{PN}, V_{S1} = V_{S4} = V_{S5} = V_{S6} = V_{S7} = V_{S8} = \frac{V_{PN}}{2}$	4	2	4 (f_{sw} for half-cycle only) 4 (f_m for half-cycle only)
oH5 [15]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{DC}, V_{S5} = V_{S6} = \frac{V_{PN}}{2}$	3	3	4 (f_{sw} for half-cycle only) 2(f_{sw} for a full cycle)
Proposed	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{DC}$, $V_{S5} = V_{S6} = \frac{V_{PN}}{2}$	2	2	4 (f_{sw} for half-cycle only) 2(f_{sw} for full-cycle)

Table II lists the voltage stress and the number of required high-frequency switches. For the proposed topology, the voltage stress of four switches (S_1-S_4) is equal to the DC-link voltage, and the voltage stress of the other two switches (S_5, and S_6) is half of the DC-link voltage which is later verified by the simulation and experiment. The PN-NPC requires four switches operating at the grid frequency (low switching loss), however, it requires a higher number of semiconductor switches (higher conduction loss). As a result, the overall loss is comparatively higher than the mentioned topologies.

TABLE III. COMPARISON OF THE CALCULATED POWER LOSSES OF EXISTING MID-POINT CLAMPING SINGLE-PHASE TRANSFORMERLESS INVERTER TOPOLOGIES WITH THE PROPOSED TOPOLOGY

Topologies	Output Power (W)					
	100	300	500	1000	1500	Losses
HB-ZVR	6.22	11.5	11.1	13.25	29.26	C_{Loss}
	0.63	1.5	2.33	3.83	5.3	S_{Loss}
HB-ZVR-D	6.05	7.2	7.86	9.05	24.7	C_{Loss}
	0.64	1.7	2.6325	4.64	4.6	S_{Loss}
PN-NPC	9.48	11.4	13.15	16.38	38.3	C_{Loss}
	1.5	1.8	2.23	3	4.8	S_{Loss}
oH5	6.7	10.16	10.3	13.46	33.5	C_{Loss}
	1.01	1.1	1.12	2.8	3.71	S_{Loss}
Proposed	4.66	6.96	7.68	8.66	24.8	C_{Loss}
	0.8	0.8	1.02	1.8	3.98	S_{Loss}

Note: C_{Loss} = Conduction loss, S_{Loss} = Switching loss.

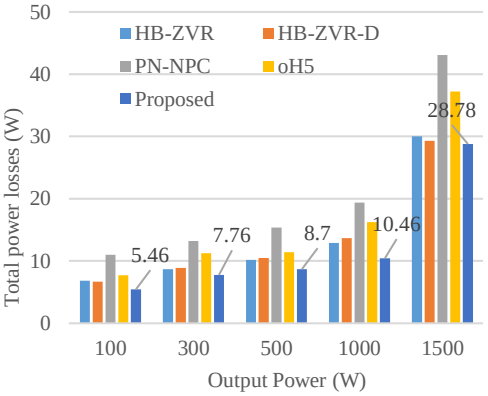

Fig. 10. Total loss comparison under different load conditions.

To have a feeling of the loss distribution in different components of the mid-point clamping inverter topologies, simulations have been carried out using PLECS models. Similar parameters and switches (SCT3022ALGC11 for active switches and C5D50065D for diodes) covered by the heat sink are considered for the thermal modelling. Their thermal impedances with conduction and switching (turn-ON/OFF) loss characteristics are imported from the datasheet of the devices. Passive component losses in the filters and capacitors are also modelled appropriately considering the magnetic property of the inductor core and equivalent series resistance (ESR) of the filter capacitor.

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Table III illustrates the loss breakdown (conduction and switching) of the mid-point clamped topologies and Fig. 10 shows the total losses for the selected topologies. It is evident that the proposed topology exhibits minimal losses over a wide range of loads (100-1500 W). Fig. 11(a) shows the losses on each power device compared with conventional topologies. Fig. 11(b) illustrates the loss distribution in a different part of the proposed inverter, where the semiconductor losses are on the top as expected. In addition, the losses related to the forward voltage drop in the bridge diodes are considerable. In contrast, the losses in the passive components are considerably low.

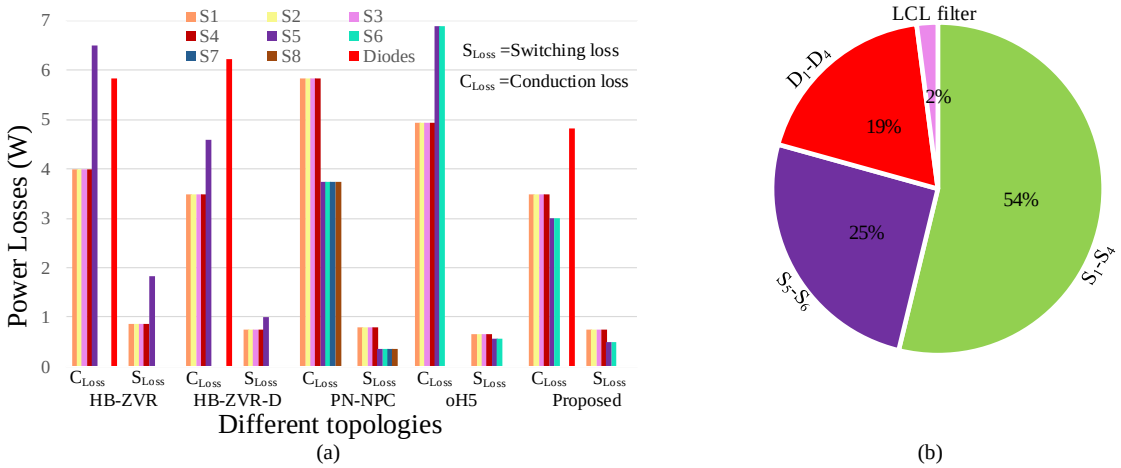

Fig. 11. Loss analysis: (a) loss comparison of each power devices, and (b) losses at full load condition.

Since one of the main concerns of the transformerless inverter topology is the leakage current that flows through the parasitic capacitor. Here the leakage current (i_{cm}) is also analysed for the different circuits (HB-ZVR, HB-ZVR-D, PN-NPC and oH5) with different parasitic capacitance (68 µF-330 µF) and filter inductance (1 mH-5 mH) values (see Fig. 12).

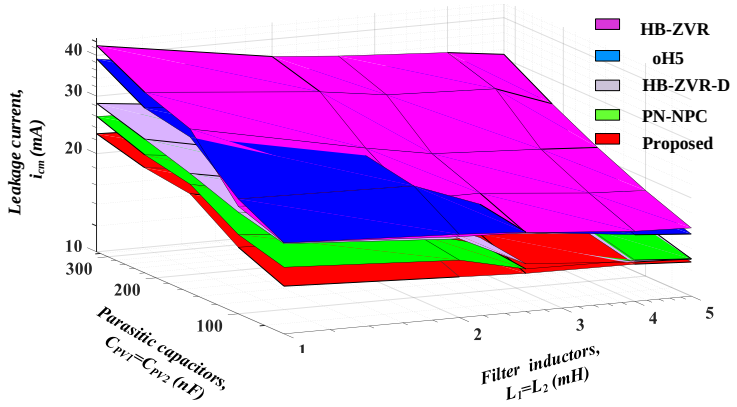

Fig. 12. Leakage current comparison in terms of varying parasitic capacitance and the filter inductance values.

Among all the topologies, the proposed topology shows excellent performance. The leakage current (i_{cm}) is increased with reducing the filter inductor values. HB-ZVR topology has the maximum i_{cm} (pink colour), whereas the proposed (red colour) and PN-NPC (green colour) have the low amount of leakage current. Moreover,

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the leakage current analysis for the proposed topology is verified through the simulation and experiment in the next section for 2.6 mH filter inductors. For 2.6 mH filter inductors, the leakage current (i_{cm}) of the proposed topology reaches the maximum 22.02 mA with the 330 nF parasitic capacitance ($C_{PV1} = C_{PV2}$), and the minimum 13.08 mA with the 68 nF parasitic capacitance ($C_{PV1} = C_{PV2}$). However, for the same filter inductor values, i_{cm} reaches the maximum 34 mA, and 31 mA for HB-ZVR, and oH5 topologies respectively, whereas i_{cm} of PN-NPC and HB-ZVR-D topologies remains low comparatively.

IV. SIMULATION AND MEASUREMENT RESULTS

Simulation of the proposed topology is carried out in Matlab-Simulink using the PLECS blockset and then is verified experimentally with a 1.5 kW laboratory prototype. Both the simulation and experiment use the same parameters as listed in Table IV.

A simple boost converter is interfaced at the front stage of the proposed inverter for boosting the PV voltage (173.5 V) to the required DC-link voltage (364 V) which is the required DC-link voltage of the inverter for 230 V AC output.

TABLE IV. PARAMETERS FOR SIMULATION AND MEASUREMENTS

Description	Values/Parameters
Input Voltage (V_{in})	173.5 V
DC-link Voltage (V_{PN})	364 V
Output Voltage (v_g)	230 V
Rated Power (P_o)	1.5 kW
Switching Frequency (f_{SW})	25 kHz
Line Frequency (f_m)	50 Hz
Modulation Index (M)	0.90
Boost Diode (D_B)	C5D50065D (650 V, 50A)
DC-link-Capacitors (C_1 and C_2)	0.68 mF (LLS2E681MELA)
Switches (S_B, $S_1 - S_6$)	SCT3022ALGC11 (650 V, 93 A, 22 mΩ)
Boost Inductor (L_B)	0.4 mH, 0.01 Ω
Filter Inductor ($L_1 = L_2$)	2.6 mH, 0.01 Ω
Filter Capacitor (C_O)	2.2 µF
Parasitic Capacitors ($C_{PV1,}$and C_{PV2})	220 nF
Ground Resistor, (R_G)	10 Ω
Resistive Load	51.8 Ω
Resistive-Inductive Load	46.8 Ω, 70 mH
Power Factor	0.86
Controller	sb-RIO GPIC
Gate Drive Circuit (GDC_{SB}, $GDC_{S1} - GDC_{S6}$)	
Optocoupler IC	ACPL-P343
DC/DC Converter	RP1212D
Resistor	10 Ω, 47 kΩ
Capacitor	1 µF, 100 µF

Fig. 13(a) shows the test bench of the experiment work with the layout of the loads and equipment used. Zoomed-in views of the top and bottom part of the circuit board are shown in Fig. 13(b) and Fig. 13(c) respectively. To turn ON the MOSFET with a proper voltage level, the gate drive circuit generates 18 V from an isolated DC/DC

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converter, and the voltage isolation between the control board and the power circuit is achieved by the optocoupler. The gate driver circuit for the MOSFETs of the proposed inverter prototype can be found on the bottom side of the PCB (see Fig. 13(c)). Fig. 13(d) shows the 1.5 kW load arrangement.

The controller sb-RIO GPIC is interfaced with LabVIEW software and operates the switching pulses through the LabVIEW software. The PWM gate pulses for all the active switching devices generated by the sb-RIO GPIC are illustrated in Fig. 14.

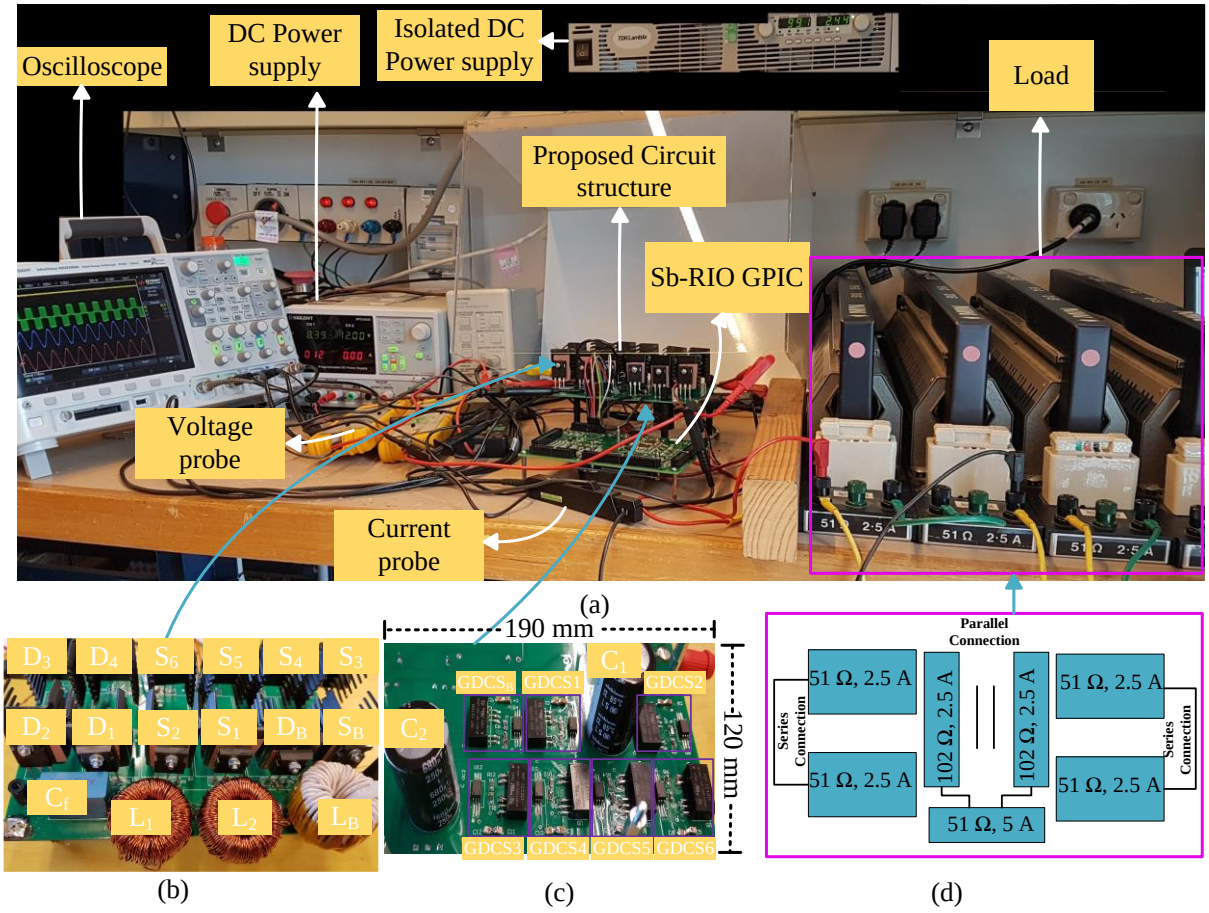

Fig. 13. Experimental setup of the HB-ZVSCR transformerless inverter topology (a) test bench, (b) top view of the proposed circuit structure, and (c) bottom view of the proposed circuit structure, (d) load connection for 1.5 kW prototype test.

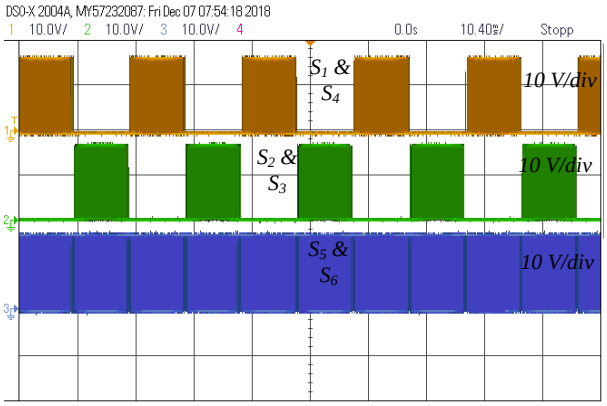

Fig. 14. Switching gate signals for S_1-S_6.

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Simulations and experiment results of the proposed topology are shown in Fig. 15 - Fig. 23 using the parameters listed in Table IV. Fig. 15(a) and Fig. 15(b) show the voltage stress waveforms of the power switches ($S_1 - S_6$) in the simulation and experiment respectively. On the other hand, the voltage stress waveforms of H-bridge diode rectifiers are shown in Fig. 16.

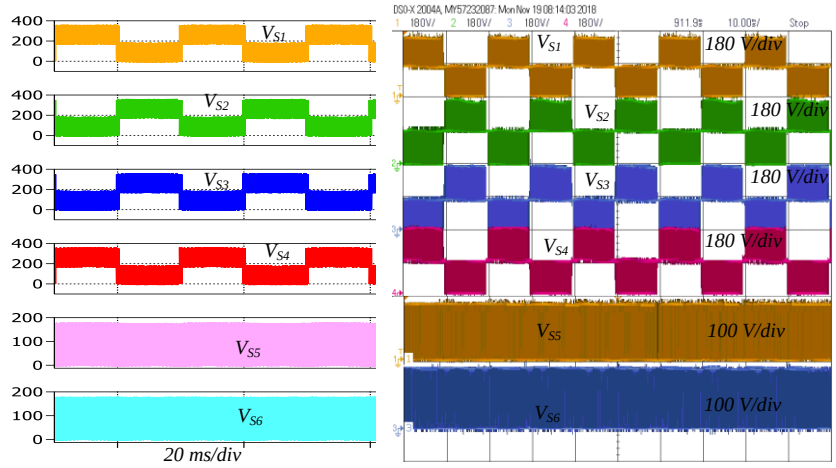

Fig. 15. Voltage stress of the power switches; (a) simulation waveforms, (b) experimental waveforms.

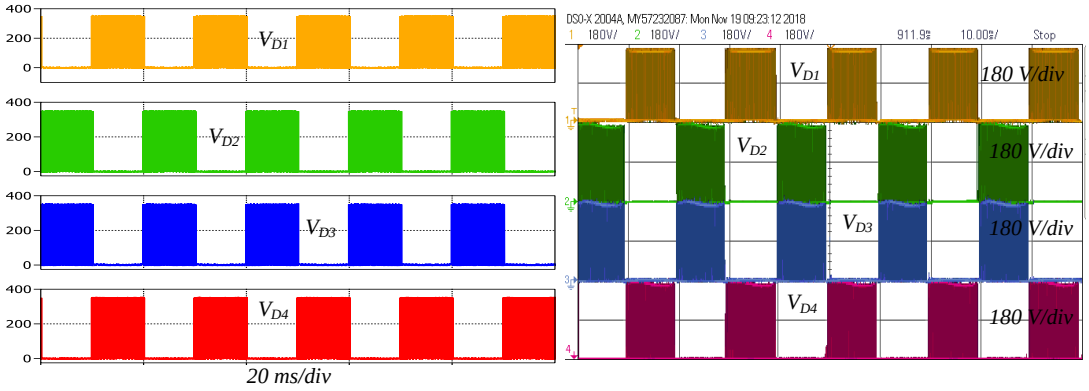

Fig. 16. Voltage stress on the bridge diodes; a) simulation waveforms, (b) experimental waveforms.

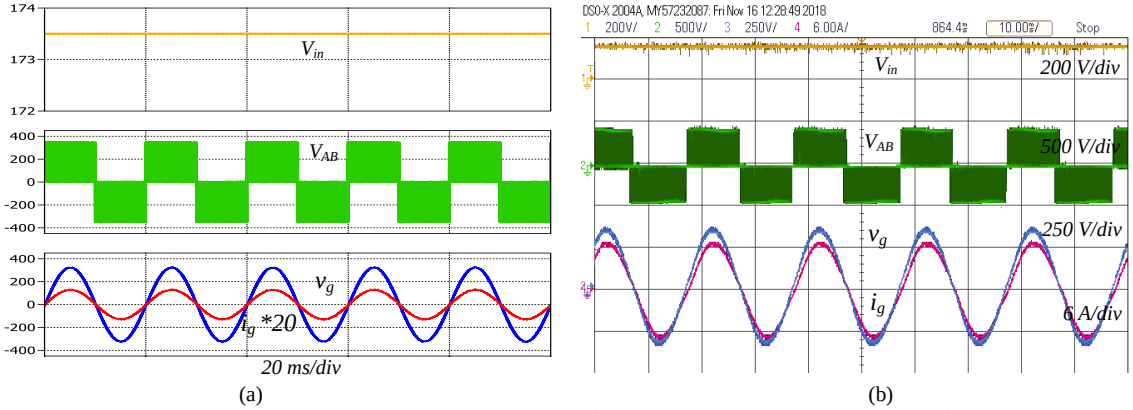

Fig. 17. The input voltage, inverter output, output voltage and current for resistive (R) load (a) simulation waveforms, (b) experimental waveforms.

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The input voltage (V_{in}), DMV (V_{AB}), output voltage (v_g), and output current (i_g) for the resistive and resistive-inductive loads are displayed in Fig. 17 and Fig. 18, respectively. The input voltage is 173.5 V, the DC-link voltage is boosted to 364 V.

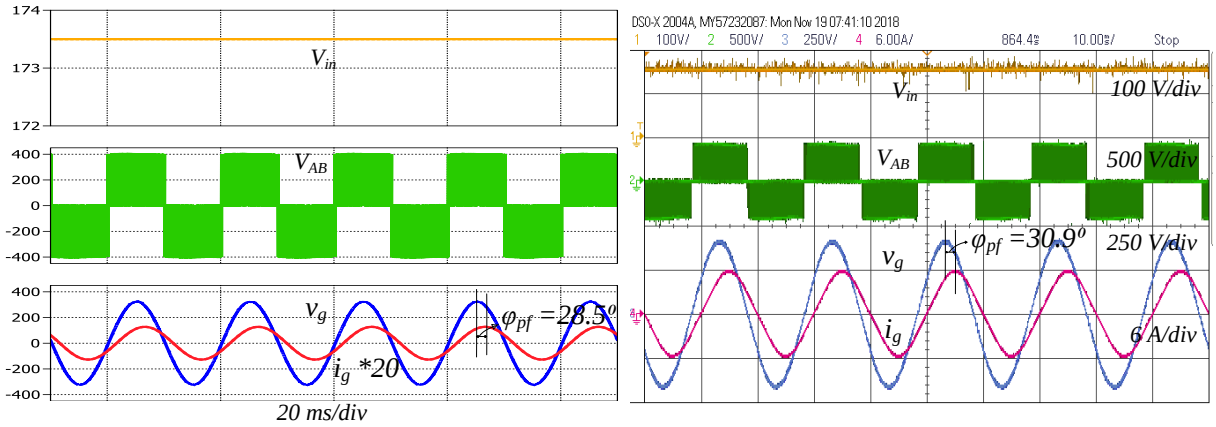

Fig. 18. The input voltage, inverter output, output voltage and current for resistive−inductive (R−L) load (a) simulation waveforms, (b) experimental waveforms.

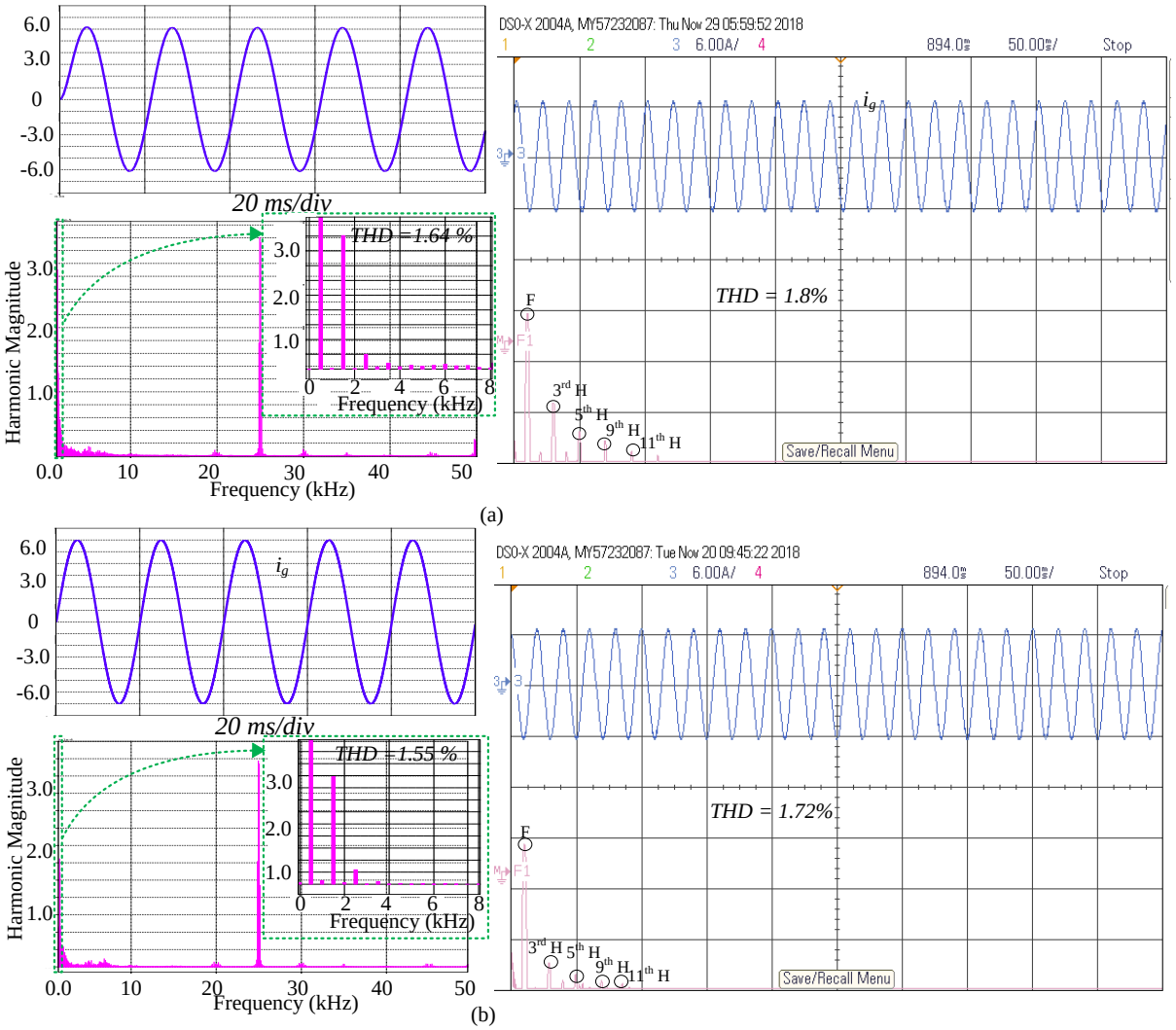

Fig. 19. Harmonic spectrum of the output current; (a) resistive (R) load, (b) resistive−inductive (R−L) load.

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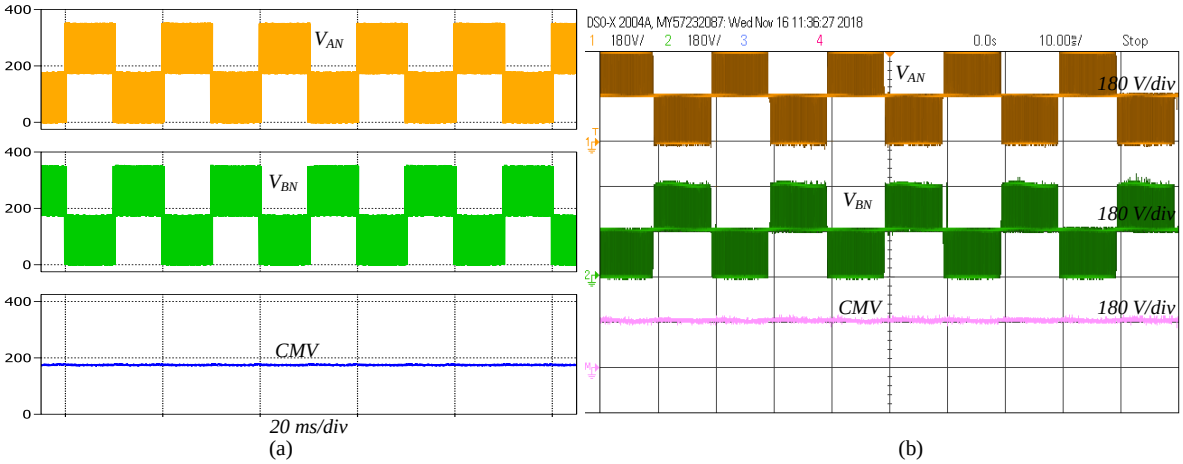
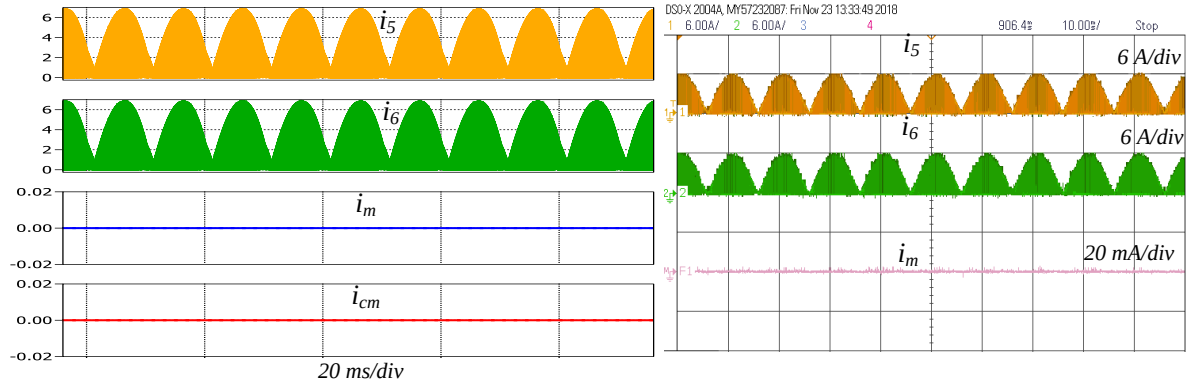
The RMS value of the output voltage is 228.4 V which is in phase with the corresponding load current of 4.45 A for a 51.8 Ω resistive load. Moreover, the THD of the output voltage and current waveforms are measured, which is 1.6 %, and 1.8 % respectively.

The capacity of delivering reactive power to the grid is also successfully demonstrated in the simulation (see Fig. 18(a)) and experiment (see Fig. 18(b)) with cos φ = 0.87 (φ = 28.5° lagging current), and cos φ = 0.86 (φ = 30.8° lagging current) respectively. Fig. 18 displays the harmonic spectrum of the output current to show the THD in the resistive load (see Fig. 19(a)) and resistive-inductive load (see Fig. 19(b)). Hence, it is evident that the THD of the output current is less than 1.8 %.



(a) (b)

Fig. 20. The voltage across point A to neutral, voltage across the point B to neutral, and CMV (a) simulation waveform, (b) experimental waveform.



(a) (b)

Fig. 21. Effect of the parasitic capacitor when $C_{PV1} = C_{PV2} = 0$; (a) simulation waveform, (b) experimental waveform.

The waveforms of the voltage V_{AN}, V_{BN} and CMV ($\frac{V_{AN}+V_{BN}}{2}$) (using the math function of the oscilloscope) are shown in Fig. 20 where in both the simulation (see Fig. 20 (a)) and experiment (see Fig. 20 (b)), the CMV is kept constant. It is shown in Section II-d that the current difference between switch S_5 and S_6 is almost equal to the leakage current, that is, $i_m = (i_5 - i_6) \sim i_{cm}$. In addition, the influence of dead time on the CM voltage and current is also studied for different dead-time between switches. The dead-time is varied from 10 ns to 300 ns, (10 ns, 100 ns, and 300 ns) whilst keeping all the other parameters constant. The analysis reaveals that the variation of leakage

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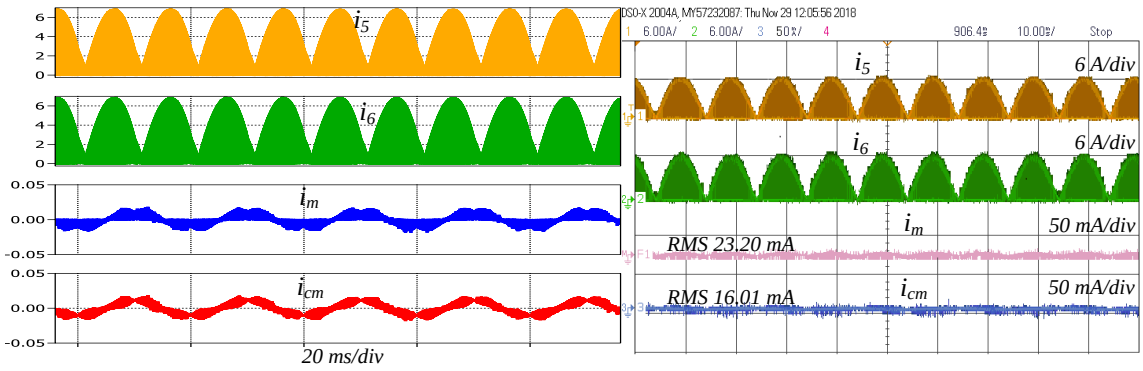
current is negligiblely small over the wide range of plausible dead-times between the switches (14.56 mA @ 10 ns, 14.68 mA @ 100 ns, and 15.50 mA @ 300 ns).



(a) (b)

Fig. 22. Effect of the parasitic capacitor when $C_{PV1} = C_{PV2} = 220$ nF; (a) simulation waveform, (b) experimental waveform.

Fig. 21 and Fig. 22 show the the simulation and experimental waveforms of the current through the switches S_5 and S_6, and the difference between these switches (i_m), and i_{cm} at the 100 ns dead-time. When $C_{PV1} = C_{PV2} = 0$ nF, there is no path to flow any ground current, and as a result, $i_5 = i_6$. On the other hand, after applying the parasitic effect ($C_{PV1} = C_{PV2} = 220$ nF), the currents of the switches S_5 and S_6 are different ($i_5 \neq i_6$); i_{cm} reaches 16.01 mA (RMS) and i_m is equal to 23.20 mA (RMS). Fig. 23 shows the leakage current with different values of parasitic capacitances at the 25 kHz switching frequency. It can be seen that the leakage current gradually increases with the increasing value of $C_{PV1} = C_{PV2}$. For example, when $C_{PV1} = C_{PV2} = 68$ nF, i_{cm} reaches 12.55 mA. Moreover, more examples are shown in Fig. 22 where the maximum leakage current is 16.65 mA for 330 nF parasitic capacitances.

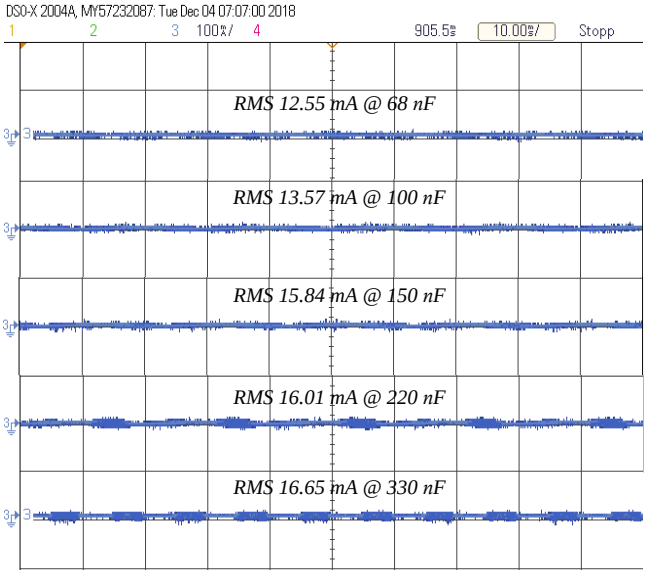


Fig. 23. Experimental waveforms of the leakage current with different values of parasitic capacitance (68 nF-330 nF).

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Table V demonstrates the measured value of both i_{cm} and i_m at 25 kHz with different values of parasitic capacitance. With varying the values of parasitic capacitance, the leakage current i_{cm} range is 12.55 mA - 16.65 mA, and i_m range is 19 mA - 24.20 mA.

The overall efficiency curve under different resistive load conditions in both the simulation and experiment of the proposed inverter is illustrated in Fig. 24, measured by a FLUKE 345 power quality clamp meter. It has the 98±1% efficiency over a wide range of loads with a peak efficiency of 98.96% at the full load condition.

TABLEV. MEASURED RMS VALUE OF THE LEAKAGE CURRENT AT DIFFERENT PARASITIC VALUES C_{PV})

$C_{PV1} = C_{PV2}$ (nF)	i_{cm} (mA)	i_m (mA)
68	12.55	19
100	13.57	20.50
150	15.84	22.20
220	16.01	23.20
330	16.65	24.20

The formula for calculating the overall efficiencies are given in (21) and (22) which stand for European (EU) and California Energy Commission (CEC) weighted efficiencies respectively.

$$\eta_{EU} = 0.03.\ \eta_{5\%} + 0.06.\ \eta_{10\%} + 0.13.\ \eta_{20\%} + 0.10.\ \eta_{30\%} + 0.48.\ \eta_{50\%} + 0.20.\ \eta_{100\%} \quad (21)$$

$$\eta_{CEC} = 0.04.\ \eta_{10\%} + 0.05.\ \eta_{20\%} + 0.12.\ \eta_{30\%} + 0.21.\ \eta_{50\%} + 0.53.\ \eta_{75\%} + 0.05.\ \eta_{100\%} \quad (22)$$

TABLE VI. EFFICIENCY COMPARISON FOR 1.5 KW RATED POWER OF DIFFERENT MID-POINT CLAMPING EXISTING TOPOLOGIES

Topologies	**Output power (W)**						
	~100	**~200**	**~300**	**~500**	**~750**	**~1000**	**~1500**
HB-ZVR [16]			89 %	90.4 %	91.6%	92.8%	93.8%
HB-ZVR-D [17]	89 %	90.8 %	93.2%	95.2 %	96.1 %	96.1 %	N/A
PN-NPC[14]	96%	97.7 %	97.7 %	97.5 %	97.3 %	97.1%	N/A
oH5 [14]	95.6 %	97 %	97.4 %	97.2 %	97 %	96.8 %	N/A
Proposed	94.1 %	96.76 %	97.22 %	97.74 %	98 .32%	98.8 %	98. 441%

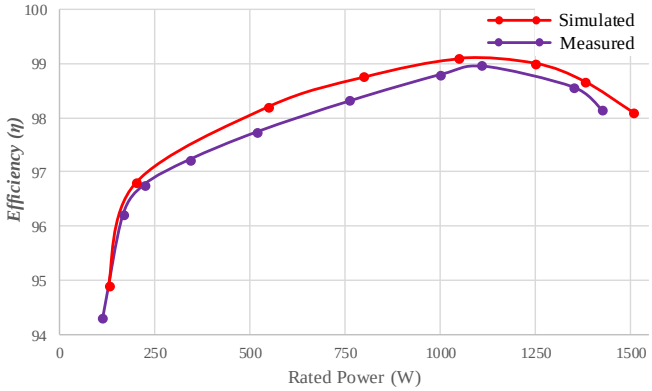

Fig. 24. A plot of power vs efficiency of the proposed inverter.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2019.2938224, IEEE Journal of Emerging and Selected Topics in Power Electronics

Table VI displays the efficiency under different load conditions for the selected topologies. In the proposed topology, the voltage stress of the freewheeling switches are half of the DC-link voltage, and the inductor current flows through two switches during the whole time period. As a result, the switching losses and conduction losses are reduced considerably.

According to the given formulas, the calculated efficiencies are 98.1 %, and 97.84 % when selecting CEC, and EU respectively. Note that, the efficiency is measured without the front stage boost DC-DC converter and it covers the total power device losses and the output filter losses, but it does not include the losses for the control circuit.

V. CONCLUSION

In this paper, a new single-phase transformerless mid-point claimed PV inverter has been presented. The proposed topology exhibits constant CMV during the whole time period (positive, negative, and zero states). As a result, the leakage current is well mitigated. This is demonstrated by measuring the leakage current at different parasitic capacitance values and switching frequencies, where the maximum leakage current is 16.65 mA with 330 nF capacitor at 25 kHz switching frequency. The proposed topology reduces the output current ripples, and as a result, THD is relatively low ($\leq$1.8 %). Moreover, only two switches are in series during the active state, which helps in reducing the conduction loss in the system. Finally, the measured efficiency is 98±1% over a wide range of loads for a 1.5 kW prototype with the peak efficiency of 98.96 % which is higher than the conventional mid-point clamped topologies. With all these advantages, the proposed topology provides a good choice for single-phase transformerless PV inverters.

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