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Xu, Tao; Gao, Feng; Zhou, Kangjia; Blaabjerg, Frede

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Optimized Design for AC Filter and Switching Frequency of Parallel-Connected Inverters with Global Synchronous Pulse Width Modulation

Tao Xu, Member, IEEE, Feng Gao, Senior Member, IEEE, Kangjia Zhou, Frede Blaabjerg, IEEE Fellow

Abstract—This paper proposes a new optimized design method for AC filter and switching frequency of parallelconnected inverters with global synchronous pulse width modulation (GSPWM) to improve the efficiency or reduce the cost. Being different from the traditional design methods that only focus on the individual inverter itself, the quantity of parallel-connected inverters and the operational principles of GSPWM are involved as the key considerations for designing the proper ac filter values and switching frequencies. In specific, the general principles and the realization details are comprehensively elaborated. Experimental results are presented to verify the proposed theoretical findings.

Keywords—Global synchronous pulse width modulation; optimized parameter; parallel-connected inverters; switching frequency; AC filter

NOMENCLATURE

N	Quantity of total parallel-connected inverters.			
N_{NS}	Quantity of running inverters.			
X	Quantity of quitting parallel-connected			
	inverters.			
Y	Quantity of restarting parallel-connected			
	inverters.			
М	Serial number of inverter ($M=1,,N$).			
<i>i</i> _{sum}	Total grid-side current.			
$\dot{l}_{ m sum,h}$	Total grid-side current harmonics.			
$I_{\rm sum,h}$	RMS values of $i_{sum,h}$.			
$I_{\rm sum,h,No}$	RMS values of <i>i</i> _{sum,h} without GSPWM.			
$I_{\rm sum,h,GS}$	RMS values of <i>i</i> _{sum,h} with GSPWM.			
I _{sum,h,No,max}	Maximum value of $I_{\text{sum,h,No}}$.			
Isum,h,GS ,max	Maximum value of $I_{\text{sum,h,GS}}$.			
I _{h,Limit}	Grid-side current harmonic limitation.			
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Corresponding author: Feng Gao.

T. Xu, F. Gao and K. Zhou are with the Key Lab of Power System Intelligent Dispatch and Control of Ministry of Education, Shandong University, Jinan 250061, China. (email: txu@sdu.edu.cn, fgao@sdu.edu.cn, 17865192711@163.com, fbl@et.aau.dk)

F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Denmark.

$f_{ m s}$	Switching frequency.	
L	Inverter-side inductance.	
$f_{ m s,limit}$	Lower limitation of $f_{\rm s}$.	
L_{limit}	Lower limitation of <i>L</i> .	
$ch_{ m M}$	Operation state of inverter M.	
T_{GS}	Period of calculation part in GSPWM.	
$\varphi_{M,PWM}$	Phase shift angle between PWM_M and PWM_1 .	
$\varphi_{M,PWMb}$	Optimal phase shift angle.	
$\Delta \varphi_{M,Err}$	Phase fluctuation around $\varphi_{M,PWMb}$.	
$\lambda_{ ext{sum,h,min}}$	Boundary of feasible region.	

I. INTRODUCTION

Nowadays, plenty of photovoltaic (PV) stations and wind farms have been successfully built in rural areas driven by the environmental issues, economic factors, and social interests [1-4]. In practice, a large number of grid-tied inverters are parallel connected to the point of common coupling (PCC) to integrate the large-scale renewable energy sources as shown in Fig. 1, where every inverter will obey with the power quality standards in traditional [5-6]. In principle, the harmonic performance of grid-tied inverters under steady state is mainly determined by the output filter and switching frequency, both of which are offline designed prior to the implementation.

Actually, the grid-side current harmonics generated from parallel connected inverters do not simply accumulate at PCC, but can be attenuated among inverters [7-8]. The centralized carrier interleaving methods can attenuate the current harmonics but are not adaptive to the distributed inverters [9-11]. Some decentralized methods can realize the carrier interleaving without using central controller but can only be used in DC converters [12-14]. Aiming to reduce the high-frequency harmonics at PCC, the recently proposed global synchronous pulse width modulation (GSPWM) method [7] provided a feasible operation scheme by coordinating the PWM sequences among parallel-connected inverters. Besides, references [15-16] proposed a decentralized phase-locked-loop based carrier synchronization (PLL-CS) method for GSPWM, which significantly improves the operational adaptivity because it makes the GSPWM not rely on the low-latency communication system.

Quite intuitively, when assuming GSPWM for parallel connected inverters, the output filter value and the switching frequency of individual inverter can be reduced to some extent as long as the power quality of PCC keeps qualified. However, the operational status of single inverter is variable. The reduction of filter value and switching frequency cannot be simply realized the same as the multi-leg inverter [17-18]. So

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far, reference [19] has proposed a method to design the parallelconnected inverters by only considering N-1 (one inverter quits) and N+1 (one inverter restarts) operation. While, the principles and details of optimized design method for parallel-connected inverters need to be further improved.

This paper therefore fully investigates the design principle for output filter and switching frequency of grid-tied parallelconnected inverters under the GSPWM operation. Regardless of the specific optimization techniques for individual inverters, e.g. the employment of wide-bandgap devices [20-21], multilevel topologies [22-23], high order filter [24-25], the proposed method mainly considers the accumulated harmonic performance at PCC under various operation scenarios and then derives the general principle for designing the output filter value and switching frequency when assuming the GSPWM operation because the electric utility company only evaluates the power quality of PCC but not the power quality of individual equipment connected to the PCC. Experimental results verified the proposed theoretical findings.

II. BASIC PRINCIPLE AND PROCEDURES OF PROPOSED METHOD

In this section, the basic principle of the proposed method is introduced with the brief analysis of GSPWM. After that, the main procedures and corresponding issues are presented.

A. Basic Principle

When many inverters are connected to the same PCC, their grid-side high order current harmonics will randomly accumulate at PCC because the phase shift angles of PWM sequences among multiple inverters change along with the time progress. The original purpose of GSPWM is to fix the phase shift angles of triangular carriers around their optimal values, so that the RMS value of the total current harmonics indicated by $I_{\text{sum,h}}$ can be minimized [7]. When using the GSPWM, the main challenges are the carrier synchronization and optimal phase shift angle calculation. The PLL based carrier synchronization method (PLL-CS), which is a distributed method, can be used to synchronize the carriers [15-16]. And the method proposed in [26] could help realize the distributed calculation in digital controllers of parallel-connected inverters. It is noted that the realization techniques of GSPWM will not bring challenges on hardware design.

In the following, $I_{\text{sum,h,No}}$ and $I_{\text{sum,h,GS}}$ are defined as $I_{\text{sum,h}}$ without and with GSPWM, respectively. It is obvious that the maximum value of $I_{\text{sum,h,GS}}(t)$ can be much smaller than that of $I_{\text{sum,h,No}}(t)$, which is given as:

$$I_{\text{sum,h,GS,max}} \ll I_{\text{sum,h,No,max}} \tag{1}$$

According to (1), there is room left for reducing switching frequencies and filter values.

Traditionally, the switching frequencies and filter values are designed according to the operational requirements of individual inverter, which means the parameter values are irrelevant to the quantity N of parallel-connected inverters [7]. While, the optimized switching frequencies and filter values can relate to N once assuming the GSPWM operation. The ideal relationship is illustrated in Fig. 2, where f_s and L can be dramatically reduced with the increasing of N. The real relationship between optimized switching frequencies, filter values and N in practice should be carefully calculated as elaborated below.

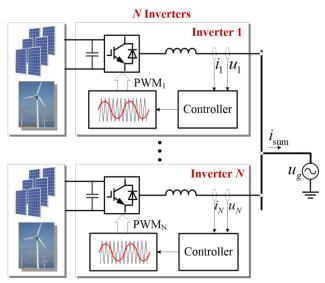


Fig. 1. Illustration of parallel-connected inverter.

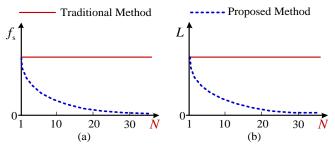


Fig. 2. Comparative illustration of (a) switching frequency and (b) filter value variation trend with the proposed design method.

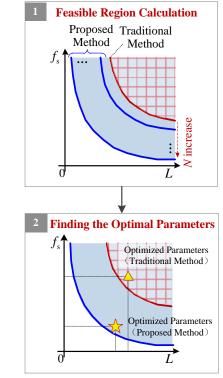


Fig. 3. Main procedures of the proposed method.

B. Main Procedures

During the design procedures, what extent the parameters can be reduced but not worsen the power quality is quite important. So, the feasible region of parameters should be

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calculated firstly by considering the operational principles of GSPWM and limitation of current harmonics. After that, choosing the optimized parameters from the feasible region should consider the practical issues, e.g. power losses, cost and etc. The main implementation procedures of the proposed method are shown in Fig. 3, where the traditional method refers to the design method for individual inverter while the proposed method represents the optimized design method for parallel-connected inverters with GSPWM.

When calculating the boundaries of the feasible region, *N* and GSPWM operation principles are considered. Compared with multi-leg inverter, the parallel-connected inverters can change their states (on/off) individually. That means, the operation states of whole parallel-connected inverters are much more complicated. Moreover, the elimination of current harmonics is realized by using GSPWM instead of the traditional phase-shifted PWM generated from one controller, which means the operation. Additionally, the optimized design should take into account all the possible operation scenarios of both inverters and GSPWM. Therefore, these issues make the feasible region calculation much more difficult compared with those in multi-leg inverter.

III. REALIZATION DETAILS OF THE PROPOSED METHOD

Two procedures of the proposed method have been briefly presented in the last section. In this section, the realization details of these two procedures are comprehensively elaborated.

A. Feasible Region Calculation

The GSPWM mainly contains the *Calculation part* and the *Synchronization part* [7]. The *Calculation part* in Global Synchronization Unit (GSU) can calculate the optimal phase shift angles according to the received operational parameters of inverters and the *Synchronization part* can fix the phase shift angles of carriers with limited fluctuation among distributed inverters by using the phase-locked-loop based carrier synchronization (PLL-CS) method, respectively.

Although the details of GSPWM have been presented in [7, 15], it has never been analyzed from the point of calculating feasible region of AC filter and switching frequency. For the convenience of analysis, the GSPWM is simplified as shown in Fig. 4, where only the necessary parameters for calculating feasible region are reserved.

The total quantity of inverters is defined as N and the serial number of inverters is defined as M, where M=1,...,N. Considering that some inverters may quit during the operation, $N_{\rm NS}$ is used to indicate the number of inverters that are operating, where $N_{\rm NS} \le N$. The operation state of inverter M is indicated by $ch_{\rm M}$, and matrix **ch** indicates the operation states of parallel-connected inverters, which is given as:

$$\mathbf{ch}(t) = \begin{bmatrix} ch_1(t) & \cdots & ch_N(t) \end{bmatrix} \quad ch_M = 0 \text{ or } 1 \qquad (2)$$

Where, $ch_M=1$ means that inverter M is producing power while $ch_M=0$ means that inverter M has stopped producing power. $ch_M=0$ may indicate the fault of inverter or the normal shutdown which could happen when the DC input power is insufficient. So, **ch**(t) is assumed as the totally random value and ch_M can change between 0 and 1 at any time. Meanwhile, the GSU can only receive **ch**(kT_{GS}) at T_{GS} , which is defined as the *GSPWM period* referring to the time interval between two

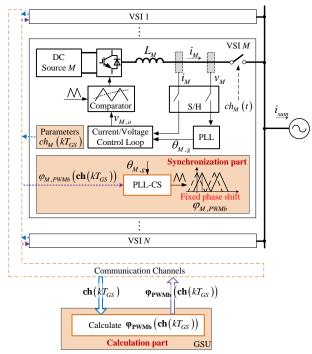


Fig. 4. Illustration of distributed parallel-connected inverters with GSPWM.

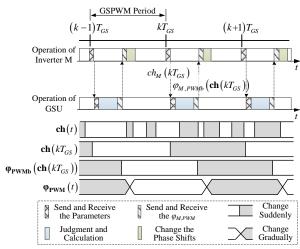


Fig. 5. Time sequences and change of variables of Calculation Part.

adjacent GSPWM operations as shown in Fig. 5. Other parameters, such as the topology, rated power, dc-link voltage, modulation strategy etc., are determined by the specific application scenario. So, these parameters are assumed as the pre-known values in this paper.

 $PWM_{\rm M}$ and $PWM_{\rm 1}$ refer to the PWM sequences of inverter M and inverter 1, respectively. $\varphi_{M,PWM}$ indicates the phase shift angle between $PWM_{\rm M}$ and $PWM_{\rm 1}$. When assuming GSPWM, $\varphi_{M,PWM}$ is not a random value but will track $\varphi_{M,PWM}$ gradually within a limited fluctuation range, which is given as:

Where, $\Delta \varphi_{Err}$ refers to the matrix of the phase fluctuations. For inverter M, $\Delta \varphi_{M,Err}$ is the phase fluctuation around $\varphi_{M,PWMb}$. $\Delta \varphi_{M,Err_max}$ is the maximum range of fluctuation which is mainly determined by the synchronization strategy in *Synchronization part* [15] and can be assumed as a pre-known value in this paper. φ_{PWMb} indicates the matrix of

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calculated optimal phase shift angles among inverters:

$$\boldsymbol{\varphi}_{\mathbf{PWMb}}\left(\mathbf{ch}\left(kT_{GS}\right)\right) = \begin{bmatrix} \varphi_{1,PWMb}\left(\mathbf{ch}\left(kT_{GS}\right)\right) \\ \cdots \\ \varphi_{N,PWMb}\left(\mathbf{ch}\left(kT_{GS}\right)\right) \end{bmatrix}$$
(4)

Where, $\varphi_{M,PWMb}$ is calculated in *Calculation part* and mainly determined by $ch(kT_{GS})$ because other parameters are assumed to be the fixed values.

After defining all the variables of GSPWM, the RMS of total current harmonics using GSPWM is given as:

$$I_{\text{sum,h}}\left(f_{s}, L, \mathbf{ch}(t), \varphi_{\text{PWMb}}\left(\mathbf{ch}(kT_{GS})\right) + \Delta\varphi_{\text{Err}}\right)$$

$$= \sqrt{\sum_{f=f_{0}+1}^{\infty} \left|\sum_{M=1}^{N} \eta \cdot ch_{M}\left(kT_{GS}\right) \cdot I_{M,\text{hf}}\left(f_{s}, L\right) \cdot e^{j\varphi_{M,M}\left(\frac{\varphi_{M}, PWMb}{(+\Delta\varphi_{M,Err}}\left(\mathbf{ch}(kT_{GS})\right)\right)}\right|^{2}}$$

$$(5)$$

 $\varphi_{\mathrm{M,hf}}\left[\varphi_{M,PWMb}\left(\mathbf{ch}\left(kT_{GS}\right)\right)\right]=n\cdot\varphi_{M,PWMb}\left(\mathbf{ch}\left(kT_{GS}\right)\right)$

Where, $I_{M,hf}(f_s,L)$ indicates the RMS of current harmonics when the switching frequency and filter parameter are f_s and L, which can be obtained using Double Fourier Method. η indicates the amplitude/phase coefficient of harmonics caused by different topologies or different modulation methods, e.g., single-phase, three-phase, DPWM, SPWM, etc. Additionally, when the grid voltage contains low-order harmonics, the modulation waveforms will produce the corresponding distortion and consequently influence the high frequency current harmonics. In this case, the one-dimensional method can be employed to calculate the switching harmonics of the arbitrary modulated wave [27].

The L-filtered inverter is firstly considered when calculating the feasible region. $I_{\text{sum,h}}$ is expressed as: $(\mathbf{1}(1\pi))$

 $\left(c + 1 \right)$

$$I_{\text{sum,h}}\left(f_{s}, L, \operatorname{ch}(t), \varphi_{\text{PWMb}}\left(\operatorname{ch}(kI_{GS})\right) + \Delta\varphi_{\text{Err}}\right)$$

$$= \frac{1}{f_{s} \cdot L} \cdot \sqrt{\sum_{f=f_{0}+1}^{\infty} \left|\sum_{M=1}^{N} \eta \cdot ch_{M}(t) \cdot I_{\text{M,hf}}(1,1) \cdot e^{j\varphi_{\text{M,hf}}\left(\frac{\varphi_{M,PWMb}\left(\operatorname{ch}(kT_{GS})\right)}{+\Delta\varphi_{M,Er}}\right)\right|^{2}}$$

$$= \frac{1}{f_{s} \cdot L} \cdot g_{\text{sum,h}}\left(\operatorname{ch}(t), \varphi_{\text{PWMb}}\left(\operatorname{ch}(kT_{GS})\right) + \Delta\varphi_{\text{Err}}\right)$$

$$= \frac{1}{\lambda_{\text{sum,h}}} \cdot g_{\text{sum,h}}\left(\operatorname{ch}(t), \varphi_{\text{PWMb}}\left(\operatorname{ch}(kT_{GS})\right) + \Delta\varphi_{\text{Err}}\right)$$

$$L = \kappa L_{\text{ind}}$$
(6)

Where, $\lambda_{sum,h}$ indicates the product of f_s and L. $g_{sum,h}$ includes all the other variables except of f_s and L when calculating $I_{\text{sum,h}}$. $I_{\text{M,hf}}$ and η are constant value for specific topology and modulation method, so they are involved in $g_{sum,h}$ as constant coefficient. In order to consider the mismatch of filter parameters in practice, κ is added in (6) to indicate the coefficient between the real L and the claimed inductance L_{ind} . The minimum value of κ which reflects the worst mismatch can be checked in the datasheet. After obtaining the boundary of Lwhich is $\lambda_{sum,h}$ with the proposed method, the boundary for choosing the real inductance is $\lambda_{\text{sum,h}}/\kappa$. Doing so, the real current harmonics can still meet the grid requirement even the worst mismatch occurs. In the following analysis, κ is assuming as 1 in the following.

In practice, f_s and L cannot be too small, otherwise $I_{sum,h}$ will exceed the grid harmonic limit which is indicated by I_{h,limit}. So, in order to get the boundaries of f_s and L, the largest $g_{sum,h}$ should be found. $g_{\text{sum,h}}$ is determined by the value of ch(t), $ch(kT_{GS})$,

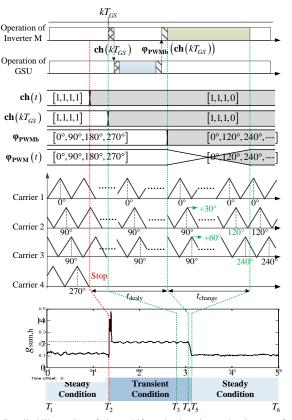


Fig. 6. Detailed illustration of phase shift angle changing and trajectory of $g_{sum,h}$ in 4-1 condition.

 $\Delta \phi_{\mathrm{Err}}$. The model for calculating $g_{\mathrm{sum,h,max}}$ is expressed as:

$$\max g_{\text{sum,h}} \left(\mathbf{ch}(t), \boldsymbol{\varphi}_{\text{PWMb}} \left(\mathbf{ch}(kT_{GS}) \right) + \Delta \boldsymbol{\varphi}_{\text{Err}} \right)$$
s.t $ch_{M}(t) = 0 \text{ or } 1; \quad ch_{M}(kT_{GS}) = 0 \text{ or } 1$

$$- \Delta \varphi_{M, Err_{-} \max} \leq \Delta \varphi_{M, Err} \leq \Delta \varphi_{M, Err_{-} \max}$$

$$(7)$$

Where, $\phi_{M,PWMb}(ch(kT_{GS}))$ is the dependent variable which is obtained from the following model:

min
$$g_{\text{sum,h}}\left(\mathbf{ch}\left(kT_{GS}\right), \boldsymbol{\varphi}_{\mathbf{PWM}}\left(t\right)\right)$$

s.t $0^{\circ} \leq \varphi_{M,PWM} \leq 360^{\circ}$ (8)

After obtaining $g_{sum,h,max}$, the boundary of f_s and L which is indicated as $\lambda_{sum,h,min}$ can be calculated as:

$$\lambda_{\text{sum,h,min}} = \frac{g_{\text{sum,h,max}}}{I_{\text{h limit}}} \tag{9}$$

And the feasible region is given as:

S

$$f_s \cdot L \ge \lambda_{\text{sum,h,min}} \tag{10}$$

Eq. (7)-(9) are general formula which can also be employed when the parameters of inverters are different. But it will cost much time to find $g_{\text{sum,h,max}}$ directly because there are so many combinations of ch(t), $ch(kT_{GS})$ and $\Delta \varphi_{Err}$. So, (7) should be further simplified by deeply analyzing the principles of GSPWM.

Considering that the Calculation part leads to infinite operation combination of ch(t) and $ch(kT_{GS})$, while the Synchronization part leads to the synchronization fluctuation $\Delta \phi_{\rm Err}$, the following two steps are employed to simplify eq. (7), which are to find the worst operation combination by involving the influence of Calculation Part and find the worst synchronization fluctuation by involving the influence of Synchronization Part. In the following, these two steps are presented in details.

(a) Finding the Worst Operation Combination

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According to the operation principles of *Calculation Part* and (7), both ch(t) and $ch(kT_{GS})$ can change between 0 and 1 separately. The goal of (7) is to find $g_{\text{sum,h,max}}$. So, some combination of ch(t) and $ch(kT_{GS})$ which will not lead to $g_{\text{sum,h,max}}$ can be ignored by analyzing the *Calculation Part*.

For the convenience of analysis, the steady state conditions and transient state conditions are defined. The steady state conditions mean that $\mathbf{ch}(t)$ is equal to $\mathbf{ch}(kT_{GS})$, while transient state conditions mean that $\mathbf{ch}(t)$ is not equal to $\mathbf{ch}(kT_{GS})$. For example, N_{NS} -X condition means X inverters stop operating while N_{NS} +Y condition means Y inverters begin operating. Two simple examples: 4-1 and 3+1 conditions are analyzed in the following to reveal phenomena of N_{NS} -X and N_{NS} +Y conditions. After analyzing N_{NS} -X and N_{NS} +Y conditions, the conclusions which can help to ignore many combinations are drawn. In these two examples, f_s and L are assumed as 10kHz and 3.5 mH, respectively.

The 4-1 condition is firstly analyzed in order to clearly introduce the details of transient state conditions. Fig. 6 shows the zoomed illustration of ch(t), $ch(kT_{GS})$, $\phi_{M,PWMb}(ch(kT_{GS}))$, $\varphi_{\text{PWM}}(t)$, carriers in 4 inverters and I_{sumh} (from top to bottom) within one GSPWM period. In specific, Fig. 6 contains two steady state conditions ($[T_1, T_2]$ and $[T_5, T_6]$) and one transient state condition ($[T_2, T_5]$). At T_2 , inverter 4 stops producing power and ch(t) changes from [1,1,1,1] to [1,1,1,0] suddenly. The states of inverters may change at any time. But GSU can only detect this change at T_3 . At T_3 , the new **ch**(kT_{GS}) is transmitted to GSU and $ch(kT_{GS})$ will change from [1,1,1,1] to [1,1,1,0]. Then the GSU calculates the new $\phi_{M,PWMb}(ch(kT_{GS}))$ according to the received $ch(kT_{GS})$ and transmits $\varphi_{M,PWMb}(ch(kT_{GS}))$ to each inverter at T_4 . $\varphi_{PWM}(t)$ will track $\varphi_{M,PWMb}(\mathbf{ch}(kT_{GS}))$ and change to the new values gradually during $[T_4, T_5]$. After T_5 , the system is back to steady state condition. Ignoring the sudden jump of $g_{\text{sum,h}}$ at T_2 , which is mainly caused by the sudden change of fundamental current, the trajectory of $g_{sum,h}$ can be divided into 4 parts which are defined as $g_{\text{sum,h}}([T_1,T_2])$, $g_{\text{sum,h}}([T_2,T_4]), g_{\text{sum,h}}([T_4,T_5]), g_{\text{sum,h}}([T_5,T_6]). g_{\text{sum,h}}([T_1,T_2])$ and $g_{\text{sum,h}}([T_5,T_6])$ are $g_{\text{sum,h}}$ under steady state conditions and $g_{\text{sum,h}}([T_2,T_4])$ is $g_{\text{sum,h}}$ under transient state condition. $g_{\text{sum,h}}([T_4, T_5])$ indicates the transition from $g_{\text{sum,h}}([T_2, T_4])$ to $g_{\text{sum,h}}([T_5,T_6])$. It can be concluded that $g_{\text{sum,h}}([T_5,T_6])$ is always smaller than $g_{\text{sum,h}}([T_2, T_4])$ because $\phi_{M,PWMb}(\mathbf{ch}(kT_{GS}))$ has been updated to further minimize $g_{sum,h}$ according to the new **ch**(kT_{GS}). This conclusion is applied to every $N_{\rm NS}$ -X condition even when the parameters of inverters are totally different. That means, for each steady state condition, there will always be $N_{\rm NS}$ -X transient state conditions that have comparatively large $g_{sum,h}$.

Under transient state condition, t_{delay} indicates the time interval from the transient state condition happening to updating $\phi_{M,PWMb}(ch(kT_{GS}))$. t_{delay} is smaller than one GSPWM period T_{GS} . t_{change} indicates the tracking time of $\phi_{PWM}(t)$ and is determined by DSP and tracking strategy. For most inverters, t_{change} is smaller than 1 second [7].

Next, the 3+1 operation condition as shown in Fig. 7 is analyzed in order to introduce the relation between $N_{\rm NS}$ +Y condition and $N_{\rm NS}$ -X condition. In the $N_{\rm NS}$ -X condition introduced above, $ch_{\rm M}$ can change from 1 to 0 at any time. But, $ch_{\rm M}$ can only change from 0 to 1 after the inverter receives the command sent from GSU. Fig. 7 shows the zoomed illustration of operation procedures and the trajectory of $g_{\rm sum,h}$ under 3+1 condition. At T_2 , inverter 4 will send its requirement to the GSU

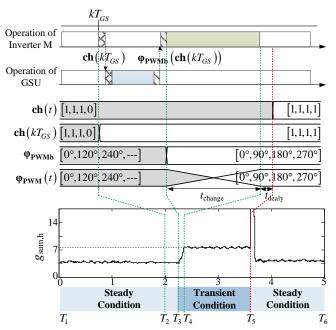


Fig. 7. Detailed illustration of phase shift angle changing and trajectory of $g_{sum,h}$ in 3+1 condition.

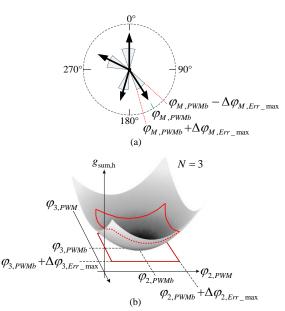


Fig. 8. Illustration of synchronization fluctuation. (a) The fluctuation of $\varphi_{M,PWM}$; (b) The fluctuation of g_{sumh} caused by the fluctuation of $\varphi_{M,PWM}$

and $\mathbf{ch}(kT_{GS})$ will change from [1,1,1,0] to [1,1,1,1]. Then from T_2 to T_4 , $\mathbf{\phi}_{M,PWMb}(\mathbf{ch}(kT_{GS}))$ is updated and sent back to inverters. At T_5 , inverter 4 will begin to produce power and $\mathbf{ch}(t)$ changes from [1,1,1,0] to [1,1,1,1]. Comparing $g_{\text{sum,h}}$ in Fig. 6 and Fig. 7, it can be seen that 3+1 condition is the reverse process of 4-1 condition from the harmonic performance point of view. Generally, N_{NS} +Y is the reverse process of $(N_{\text{NS}}$ +Y)-Y, which is just another N_{NS} -X condition by replacing N_{NS} by N_{NS} +Y.

In the above two examples, only the simplest conditions are introduced. But it can be seen that: 1) $g_{\text{sum,h}}$ under N_{NS} -X transient state condition is larger than $g_{\text{sum,h}}$ under steady state conditions. 2) $g_{\text{sum,h}}$ under N_{NS} -Y transient state condition is the same as that under N_{NS} -X transient state condition. In practice, **ch**(*t*) may change several times in one GSPWM period. But the operation conditions can still be separated into N_{NS} -X or N_{NS} +Y conditions. According to the conclusions above, the harmonic performance of all transient conditions can be covered by the

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harmonic performance of $N_{\rm NS}$ -X conditions.

By only considering the N_{NS} -X conditions, $g_{\text{sum,h}}$ can be found through the following model:

$$\max g_{\text{sum,h}} \left(\mathbf{ch}(t), \boldsymbol{\varphi}_{\text{PWMb}} \left(\mathbf{ch}(kT_{GS}) \right) + \Delta \boldsymbol{\varphi}_{\text{Err}} \right)$$

s.t $ch_M \left(kT_{GS} \right) = 0 \text{ or } 1;$ $\sum_{M=1}^N ch_M \left(kT_{GS} \right) \ge 2$
 $ch_M \left(t \right) = \left(0 \text{ or } 1 \right) \times ch_M \left(kT_{GS} \right);$ $\Delta \boldsymbol{\varphi}_{M, Err} = 0$

$$(11)$$

Doing so, the calculation burden is dramatically reduced.

(b) Finding the Worst Synchronization Fluctuation

After finding the worst operation condition, the influence of synchronization fluctuation is added. In practice, PWM signals cannot be synchronized without any fluctuation as shown in Fig. 8(a). According to [15], the maximum phase fluctuation can be controlled within the limited range. The maximum fluctuation is indicated by $\Delta \varphi_{M,Err_{max}}$. As shown in Fig. 8(b), the fluctuation of φ_{PWM} will make $g_{sum,h}$ fluctuate. So, the rise of $g_{sum,h}$ caused by the phase fluctuation should be considered. Assuming that the worst condition calculated by (11) is $ch(t)=ch_{w1}$ and $ch(kT_{GS})=ch_{w2}$, ch_{w1} and ch_{w2} are substituted into the following model:

$$\max g_{\text{sum,h}} \left(\mathbf{ch}_{\mathbf{w}} \mathbf{u}, \mathbf{\phi}_{\mathbf{PWMb}} \left(\mathbf{ch}_{\mathbf{w}} \mathbf{u} \right) + \Delta \boldsymbol{\phi}_{\mathbf{Err}} \right)$$

s.t
$$\Delta \boldsymbol{\phi}_{\mathbf{Err}} = \left[\Delta \varphi_{1, Err}, \dots, \Delta \varphi_{N, Err} \right] \qquad (12)$$
$$- \Delta \varphi_{M, Err_{-} \max} \leq \Delta \varphi_{M, Err} \leq \Delta \varphi_{M, Err_{-} \max}$$

Where, only $\Delta \varphi_{\text{Err}}$ are variables in this model. After solving (12), the value of $g_{\text{sum,h,max}}$ can be obtained.

To be noted, for scenarios where the parameters of inverters are exactly the same, the model expressed in (11) and (12) can be further simplified. In these scenarios, the optimal phase shift is only influenced by N_{NS} , so the equation to calculate $\varphi_{M,PWMb}$ is given as:

$$\varphi_{M,PWMb}\left(M,N_{NS}\right) = 360^{\circ} \times \frac{M-1}{N_{NS}}$$
(13)

The worst operation combination can be expressed as:

$$\max g_{\text{sum,h}} = \sqrt{\sum_{f=f_0+1}^{\infty} \left| \sum_{M=1}^{N_{NS}-X} I_{\text{M,hf}}(1,1) e^{j\varphi_{\text{M,hf}}(\varphi_{M,PWMb}(M,N_{NS}))} \right|^2}$$

s.t $N_{NS} = 1, 2, \dots, N$ $X = 0, 1, \dots, N_{NS} - 1$ (14)

The solution of (14) is assumed to be N_{NS_W} and X_W . Being similar to (12), when considering the phase fluctuation, $g_{\text{sum,h,max}}$ can be expressed as:

$$\max g_{\text{sum,h}} = \sqrt{\sum_{f=f_0+1}^{\infty} \left| \sum_{M=1}^{N_{NS_w}-X_W} I_{M,\text{hf}}(1,1) e^{j\varphi_{M,\text{hf}}\left(\frac{\varphi_{M,PWMb}(M,N_{NS_w})}{+\Delta\varphi_{M,Err}}\right)} \right|^2}$$

s.t $-\Delta\varphi_{M,Err_max} \leq \Delta\varphi_{M,Err} \leq \Delta\varphi_{M,Err_max}$ (15)

Although (14) and (15) are complicated, most of variables except N can be obtained according to the known parameters.

B. Choosing Optimized Parameters

The above calculation mainly considers the limitation of total current harmonics. In practice, the reduction of switching frequency and filter value will influence the inverter stability.

On the one hand, the switching frequency cannot be too small, or the time delay caused by the sampling and PWM updating can reduce the controller bandwidth [28]. On the other hand, if the filter value of inverter is reduced, the stability margin will be reduced simultaneously under the same grid impedance [29]. So, the minimum switching frequency and filter inductance should be considered as the boundaries of feasible region either. In this paper, they are assumed as pre-known value and indicated by $f_{s,limit}$ and L_{limit} , respectively. For case, where only one inverter is left to produce the output power, its generated current harmonics can be easily determined upon knowing the selected L and f_s . Therefore, as long as the defined boundary of $f_{s,limit}$ and L_{limit} could make current harmonics from one inverter smaller than $I_{h,limit}$, the above proposed method can satisfy the operation of such extreme condition, otherwise, $f_{s,limit}$ and L_{limit} should be adjusted.

After obtaining the feasible region, the optimized parameters will be selected in the feasible region according to the specific purpose, such as power loss minimization as shown in the following model:

$$\min P_{loss}(f_s, L) = \sum_{M=1}^{N} P_{M, total}(f_s, L)$$

$$s.t. \quad f_s \cdot L \ge \lambda_{sum.h.min}(N) \quad f_s \ge f_{s.limit} \quad L \ge L_{limit}$$
(16)

where, $P_{M,total}(f_{s},L)$ is the sum of the losses $P_{M,loss}(f_{s},L)$ from every inverter. The main power losses consist of semiconductor loss and inductor loss. The semiconductor loss contains switching loss P_{SW} and conduction loss P_{ON} , while the inductor loss contains iron loss P_{Fe} and copper loss P_{Cu} . Then, $P_{M,loss}(f_{s},L)$ can be expressed as:

$$P_{\text{M,loss}}\left(f_{s},L\right) = P_{\text{SW}}\left(f_{s},L\right) + P_{\text{ON}}\left(f_{s},L\right) + P_{\text{Fe}}\left(f_{s},L\right) + P_{\text{Cu}}\left(f_{s},L\right)$$
(17)

The mathematic model of (16) can be solved using Particle Swarm Optimization (PSO) method, which is widely used and will not be introduced here. After solving (16), the final optimized parameters could be obtained.

To be noted, the proposed method can also be employed for LCL-filtered inverter. Comparing LCL filter and L filter, the total inductance of LCL-filter is about 1/2 of the inductance selected for L-filter in traditional [30]. When using the proposed method, the inductance of L-filter can be half of the inductance designed by the traditional method when N is larger than 2 according to Fig. 9 in next section. So, with the proposed method, the inductance of redesigned L-filter is close to the inductance of LCL-filter. Then the LCL filter can be replaced by L filter when many inverters are connected in parallel. Additionally, the resonance problem of parallel-connected LCL filter inverters [31-33] can be avoided by using the simplified L filter.

After reducing the filter value, the multi-sampling method can be used to detect fault current and the improved control loop can compensate the effect of additional fault current contributed from reduced value filter.

In implementation, few of the redesigned inverters can be grouped as one unit as long as it can fulfill the operational limits. When increasing the scale of PV station or battery energy storage system, at least one group should be assumed. Doing so, it is not necessary to change the filter values and the switching frequencies of already installed inverters.

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Table I Parameters of inverters				
	Parameter	Value		
	$V_{\rm M,dc}$	350 V		
Basic parameters of inverter	$V_{ m ac}$	110 V		
	P_{M}	1 kW		
	f_1	50 Hz		
	$I_{\mathrm{M},1}$	3A		
	$V_{\rm stress}$	350 V		
	Istress	1.27 A		
Parameters of switch	$t_{ m don}$	0.13 us		
(IGBT	$t_{ m doff}$	0.3 us		
FF100R12RT4)	$t_{ m f}$	0.03 us		
	$V_{\rm CE(sat)}$	$\approx 1 V$		
	$f_{ m s}$	<20kHz		
	L	3.5 mH		
	C_{Feh}	0.193*10-6		
	Mh	1.29		
Parameters of inductor (Fe-Si-Al:	Nh	2.01		
Kool Mu 77192)	$B_{ m mh0}$	0.1		
	G_0	86 cm ³		
	$I_{ m h0}$	5.2 A		
	$R_{ m Cu0}$	0.02 Ω		

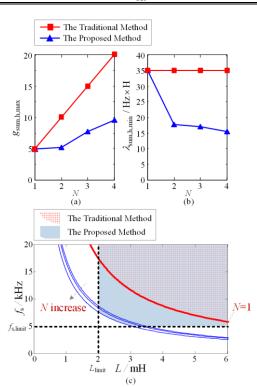


Fig. 9. Results of feasible region calculation by using traditional method and the proposed method. (a) $g_{\text{sum,h,max}}$; (b) $\lambda_{\text{sum,h,min}}$; (c) The feasible region.

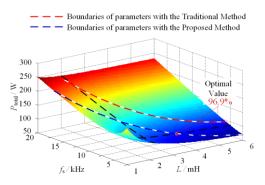


Fig. 10. Calculated power losses and efficiency with different inductance values and switching frequencies when *N*=4.

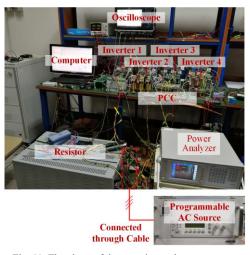


Fig. 11. The photo of the experimental prototype.

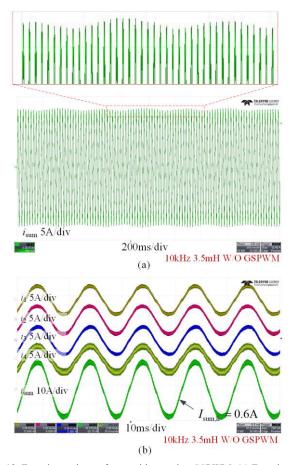


Fig. 12. Experimental waveforms without using GSPWM. (a) Experimental waveform and zoomed view of $I_{sum,h}$; (b) Current waveforms when the maximum value of $I_{sum,h}$ appears.

IV. EXPERIMENTAL VERIFICATION

The whole procedures of the proposed method have been introduced in details. In this section, a prototype with four inverters is employed to verify the effectiveness of the proposed design method. These four distributed inverters have their own independent DC sources, three-phase circuits, output L filters and digital controllers. The inverter parameters are listed in Table I. All inverters are connected to an emulated grid using a programmable AC source AMETEK-CI-4500LS, whose RMS value of output voltage is 110V and output frequency is 50Hz. The power losses are measured by the power analyzer VOLTECH PM6000.

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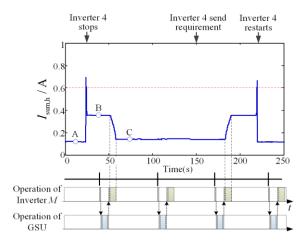


Fig. 13. Experimental trajectory of I_{sum,h} during 4-1, 3+1 conditions.

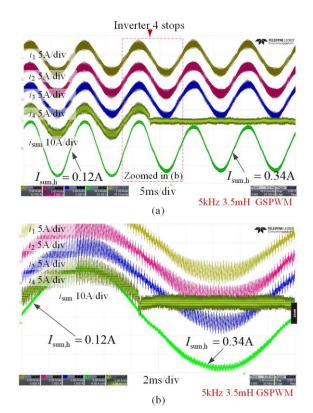


Fig. 14. Experimental waveforms of i_1 , i_2 , i_3 , i_4 and i_{sum} during 4-1 conditions. (a) The transient waveform during 4-1 condition; (b) Zoomed view of (a).

Following the procedures in Section III-A, $g_{\text{sum,h,max}}$ is calculated by fully considering the influence of *Calculation Part* and *Synchronization Part*. In specific, $g_{\text{sum,h,max}}$ with different N is illustrated in Fig. 9(a).

Assuming that the RMS value of output current for each inverter is 3A, $I_{h,limit}$ in this experiment is given as:

$$I_{\rm h,limit} = 5\% \times 3A \times N = 0.15N \text{ A}$$
(17)

Then according to (9), $\lambda_{\text{sum},h,\text{min}}$ is obtained from $g_{\text{sum},h,\text{max}}$ and $I_{h,\text{Limit}}$ as shown in Fig. 9(b).

Finally, the boundaries of f_s and L can be drawn in Fig. 9(c) using the following formula:

$$\sup_{sum,h,\min} = f_s \times L$$
 (18)

In this example, $f_{s,\text{limit}}$ and L_{limit} which are assumed as 5kHz and 2mH are also drawn in Fig. 9(c).

According to Fig. 9, the traditional method can be seen as a special application of the proposed method when N=1. When N>1, the feasible region obtained by the traditional method is unchanged while the feasible region obtained by the proposed

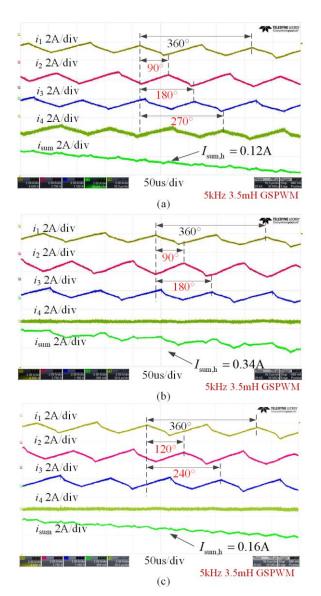


Fig. 15. Zoomed view of current waveforms at different moment. (a) Current waveforms at moment A; (a) Current waveforms at moment B; (c) Current waveforms at moment C.

method becomes larger. There are 4 inverters in this prototype, so the feasible region for 4 inverters is used in the following verification.

Next, the switching frequency and ac filter inductance are chosen by optimizing the specific goals. In this case, the goal is to minimize the power losses. The relationship between power losses, f_s and L is shown in Fig. 10. By considering the boundaries, the optimized combination of f_s and L can be calculated, which refers to 5kHz and 3.5mH. Compared with the parameters designed by the traditional method which are 10kHz and 3.5mH, f_s becomes much smaller.

After choosing the AC filter and the switching frequency, the total current harmonics and the power losses using the proposed method and traditional method are measured and compared as elaborated below. The experimental prototype is shown in Fig. 11.

A. Current Harmonics Measurement of Traditional Method

When using the traditional method, f_s and L are 10kHz and 3.5mH, respectively. Additionally, GSPWM is not employed. The i_{sum} is shown in Fig. 12(a), where $I_{sum,h}$ will change with the time progress. Fig. 12(b) shows the experimental waveforms

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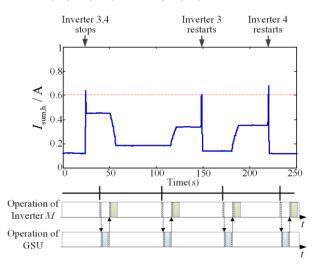


Fig. 16. Experimental trajectory of I_{sum,h} during 4-2, 2+1 and 3+1 conditions.

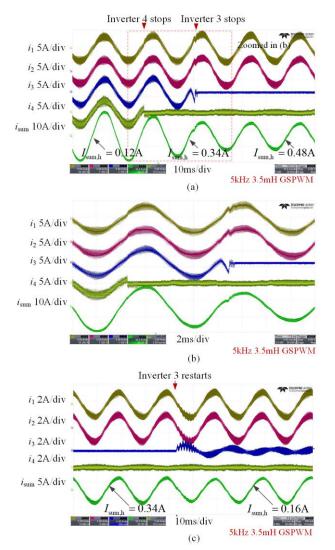


Fig. 17. Experimental waveforms of *i*₁, *i*₂, *i*₃, *i*₄ and *i*_{sum}. (a) The transient waveform during 4-2 condition; (b) Zoomed view of (a); (c) The transient waveform during 2+1 condition.

when the maximum value of $I_{\text{sum,h}}$ appears, where $I_{\text{sum,h}}$ is 0.6A.

B. Current Harmonics Measurement of the Proposed Method

The total current harmonics are measured in this subsection to verify that the chosen parameters can still make the current harmonics meet the grid requirement.

Firstly, the 4-1 and 3+1 conditions are tested. 4-1 and 3+1

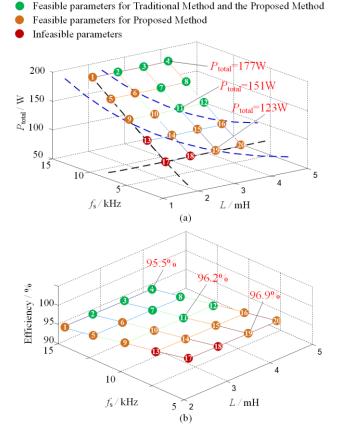


Fig. 18. Experimental (a) power losses and (b) efficiency with different switching frequencies and filter values.

conditions are not the worst conditions but they can show the operation details of $N_{\rm NS}$ -X and $N_{\rm NS}$ +Y conditions when GSPWM is employed. Fig. 13 shows Isum,h and the operation modes in 250 seconds. In this experiment, the inverter 4 quits at 25 seconds and I_{sum,h} rises from 0.12 A to 0.34 A suddenly, because the phase shift angles of the remaining inverters have not been changed. The current waveforms around 25 seconds and their zoomed view are shown in Fig. 14(a) and (b), respectively. Further, the switching harmonics at moment A, B, C which are identified in Fig. 13 are shown in Fig. 15. When all inverters are operating, the phase shift values are 0° , 90° , 180° , 270° while $I_{\text{sum,h}}$ is 0.12 A. When inverter quits, the phase shifts of other inverters have not been updated. So, Isum,h will rise to 0.34 A. At 50 seconds, the GSU sends the updated phase shift values to inverter 1, 2 and 3 to change their phase shift angles from 0° , 90° , 180° to 0° , 120°, 240°. So, I_{sum.h} will reduce gradually from 0.34 A to 0.16 A. So far, the 4-1 condition has been tested. Next, inverter 4 sends its requirement of restarting to GSU at 150 s. The GSU will calculate the new optimal phase shift and send them back to all inverters. Then the phase shifts of inverter 1, 2 and 3 will change from 0°, 120°, 240° to 0°, 90°, 180°. $I_{\text{sum,h}}$ rises from 0.16 A to 0.34 A. After the restarting of inverter 4, $I_{\text{sum,h}}$ reduces from 0.34 A to 0.12 A gradually. The experimental results verified that the 3+1 condition is the reverse process of (3+1)-1condition, which consequently verifies that $N_{\rm NS}$ +Y condition is the reverse process of $N_{\rm NS}$ -X condition as analyzed in this paper.

Secondly, the worst condition is tested to verify whether $I_{\text{sum,h}}$ is always smaller than $I_{\text{h,limit}}$. When inverter 3 and inverter 4 stop, $I_{\text{sum,h}}$ rises from 0.12 A to 0.48 A, whose trajectory is shown in Fig. 16. As a consequence, Inverter 1 and inverter 2 need to change their phase shifts to minimize $I_{\text{sum,h}}$. After a while,

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inverter 3 and inverter 4 restart respectively. Fig. 17(a) shows the waveforms during 4-2 operation, where $I_{\text{sum,h}}$ is 0.48 A while the calculated $I_{\text{h,limit}}$ is 0.6 A because the calculations take the maximum phase shift fluctuations into consideration. So, $I_{\text{sum,h}}$ can always be smaller than $I_{\text{h,limit}}$ even when the worst condition occurs. That means the proposed design method can completely guarantee that the harmonic performance is qualified.

In a word, the experimental results have verified that $I_{\text{sum,h}}$ can always meet the requirement in every possible condition, which means the proposed method can well design the parallelconnected inverters without influencing the current quality.

C. Power Losses Comparison

After measuring the total current harmonics, the power losses with different parameters are measured to verify that the proposed method can improve the efficiency. Limited by the available inductors in lab, the power losses at some selected operation points were measured. The selected inductor values are 2.1mH, 2.8mH, 3.5mH, 4.2mH, while the selected switching frequencies are 5kHz, 7.5kHz, 10kHz, 12.5kHz, 15kHz, respectively. The power losses with different f_s and L are measured as shown in Fig. 18, where 20 operation points can be divided into three groups. The green points mean the feasible solutions for the traditional method and the proposed method. The yellow points mean the feasible solutions only for the proposed method. The red points mean the infeasible solutions. If the traditional method is employed, the optimized solution is point 11. When the proposed method is employed, the optimized solution is point 19. The proposed method can minimize the power losses and the inverter efficiency reaches 96.9%. To be noted, the efficiency is lower than the commercial inverter because the experimental prototype is not fully optimized in terms of semiconductor devices, inductors, wiring and etc. But the experimental results can still verify the advantage of the proposed method.

V. CONCLUSION

This paper proposes an optimized design method for parallel-connected inverters with global synchronous pulse width modulation. Being different from the traditional design methods that focus on individual inverter, the main contribution of the proposed method is that the quantity of parallel-connected inverters and operational principles of GSPWM are fully considered when designing the filter values and switching frequencies. Doing so, filter values and switching frequencies can be reduced while keeping the total current harmonics still conform to standards.

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Tao Xu (S'16-M'19) received his B.Eng. degree and Ph.D degree in electrical engineering from Shandong University, Jinan, China, in 2014 and 2019. From September 2017 to September 2018, he was a Visiting Scholar at the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. Since 2019, he joined School of Electrical Engineering, Shandong University, where he is currently a postdoc. His research interests are parallel inverters, power quality and modulation methods.

Dr. Xu was the recipient of the IEEE Power Electronics Transactions Second Prize Paper Award in 2017 and the IEEE PELS Prize Ph.D. Thesis Talk in 2019.



Feng Gao (S'07-M'09-SM'18) received the B.Eng. and M.Eng. degrees in electrical engineering from Shandong University, Jinan, China, in 2002 and 2005, respectively, and the Ph.D. degree from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2009. From 2008 to 2009, he was a research fellow in Nanyang Technological University. Since 2010, he joined School of Electrical Engineering, Shandong University, where he is currently a professor. From September 2006 to February 2007, he was a Visiting

Scholar at the Institute of Energy Technology, Aalborg University, Aalborg, Denmark.

Dr. Gao was the recipient of the IEEE Industry Applications Society Industrial Power Converter Committee Prize for a paper published in 2006 and 2017 IEEE Power Electronics Transactions Second Prize Paper Award, and he is now serving as the Associate Editors of IEEE TRANSACTIONS ON

POWER ELECTRONICS and CPSS TRANSCATIONS ON POWER ELECTRONICS AND APPLICATIONS.



Kangjia Zhou (S'19) received his B.Eng. degree in electrical engineering from Shandong University, Jinan, China, in 2019, where he is currently working toward his master degree. His research interests are grid-connected converter and Internet of things.



Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 30 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

He is nominated in 2014-2018 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.