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A Six-Switch Seven-Level Triple-Boost Inverter

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***Abstract*—Multilevel inverters in renewable applications usually require a high-voltage DC link fed by a front-end DC-DC boost stage. Such a two-stage power conversion however increases the switch count, leading to higher costs and power losses. To lower the number of switches, this letter proposes a six-switch inverter, capable of generating a seven-level voltage and a triple-voltage boost. Both features are achieved with only four switches operating at a high frequency, while clamped by low-voltage capacitors. The remaining two switches must however endure higher voltage stresses, but fortunately operate at a much lower frequency. Overall switching losses of the inverter are thus significantly reduced. Besides, the inverter shares a common ground between its DC input and AC output, which theoretically helps to eliminate leakage current, if powered by photovoltaic sources. Operating principles of the inverter have been described and verified through experiments with an 800-W prototype.**

***Index Terms*—Boost multilevel inverter, low switch count, common-grounded structure, renewable applications.**

I. Introduction

Exploitation of renewable energy is important because of environmental concerns. Harvesting renewable energy requires a large number of power converters, among which, multilevel inverters (MLIs) are the most commonly used [1]. MLIs, including the neutral-point-clamped (NPC) and flying-capacitor (FC) inverters, have many advantages including high-quality output voltage, low dv/dt across switches and small output filter [2]. However, when used for photovoltaic (PV) generation, some forms of voltage boosting for grid connection are necessary, since the output voltages of most PV arrays are relatively low. One boost option is to cascade many PV modules as a high-voltage string [3], which presently has met many mismatch issues. Alternatively, a front-end DC-DC converter can be added to form a two-stage DC-AC power converter [4]. This power converter however uses more switches with accompanied higher costs and power losses. A third option involving the single-stage boost MLIs has therefore been deliberated [5]–[15].

One such attempt in [5] achieves its boosted output voltage from a multi-DC link formed by multiple switched-capacitor cells (SCCs) in series. Its number of switches (N_S) in each SCC is however still comparably high. That prompts [6] to introduce another multi-DC link, but like [5], its usage of a rear-end full bridge for generating the desired AC output remains a concern.

It should however be pointed out that reversal of the output-voltage polarity in each half fundamental cycle does not necessarily require a full bridge. On example is in [7], where an SCC-based five-level boost inverter with inherent polarity reversal has been proposed. That inverter however demands nine switches with at least four of them conducting simultaneously. The increases in switches are even more noticeable in [8] and [9] at a higher voltage level. It may therefore be more appealing to consider the variant in [10], where some switches and their gating circuits in [9] have been replaced by diodes. Despite that, both inverters must have their leakage currents suppressed before they can be suitable for PV applications.

Other MLIs use an active NPC structure to construct either a five- or a seven-level inverter [11]–[13], whose switch count can further increase if bidirectional switches are needed [12], [13]. Such an active NPC structure additionally has a low voltage conversion ratio due to its clamping of grounded neutral of its AC output to mid-point of its DC input [11]. Despite that, MLIs with a common-grounded (CG) connection can result in the minimization of leakage current, as also demonstrated by inverters from [14] and [15]. Another feature shared by the MLIs [11]–[15] is the switch count (N_S) of each inverter being always higher than the number of voltage levels (N_{VL}). Certainly, this is an achievement, but not as challenging as the rarely attained target of reducing switches per level (i.e., $N_S/N_{VL}<1$), while yet producing the desired high voltage boost.

The challenge has now been met in this letter through the proposal of a six-switch (6S) seven-level (7L) inverter with a triple boost (TB) in the output voltage. The three-phase schematic of the inverter is shown in Fig. 1, where it is powered by a single DC input and conditioned by a shared DC-link capacitor C_{dc}. Throughout the letter, the proposed inverter has been notated as 6S7LTBI and shown to have the following features:

- A very low switch-per-level ratio (≈0.86).
- Reduced losses achieved by only three switch pairs with one pair operating at the fundamental frequency.
- Common DC-input and AC-output ground and hence a very small leakage current.

These features are systematically explained by first describing operating states of the 6S7LTBI with a multicarrier pulse-width-modulation (PWM) scheme in Section II. Determination of its parameters and a comparison with other MLIs then follow in Section III. Last but importantly, experimental results are given in Section IV, before a conclusion is drawn in Section V.

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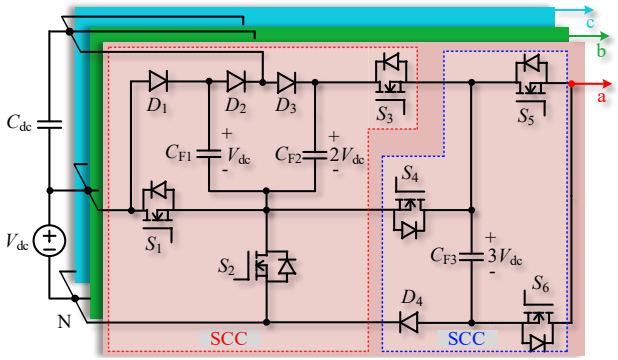

Fig. 1. The 6S7LTBI and its three-phase schematic (terminals a, b and c).

TABLE I
SWITCHING SIGNALS AND KEY VOLTAGES OF THE 6S7LTBI

States	S_1 ($\bar{S}_2$)	S_3 ($\bar{S}_4$)	S_5 ($\bar{S}_6$)	V_o	V_{CF1}	V_{CF2}	V_{CF3}
I	0	0	0	$-3V_{dc}$	Increase	/	Decrease
II	0	0	1	0	Increase	/	/
III	0	1	0	$-V_{dc}$	Increase	Increase	Decrease
IV	0	1	1	$2V_{dc}$	Increase	Increase	/
V	1	0	0	$-2V_{dc}$	Decrease	/	Decrease
VI	1	0	1	V_{dc}	Decrease	/	/
VII	1	1	0	0	Decrease	Decrease	Increase
VIII	1	1	1	$3V_{dc}$	Decrease	Decrease	Increase

0—switch-OFF; 1—switch-ON; /—No change.

II. OPERATION OF 6S7LTBI

A. Operating States

The 6S7LTBI consists of three floating capacitors C_{F1}–C_{F3} per phase, whose capacitances, and that of C_{dc}, can be assumed as large enough to keep their respective voltages constant. Among them, C_{F1} and C_{F2} with switches S_1–S_3 and diodes D_1–D_3 form the first SCC, while C_{F3} with switches S_4–S_6 and diode D_4 form the second SCC. Together, they produce eight switching states, as summarized in Table I and Fig. 2. These states, in turn, give rise to an output voltage with seven discrete levels notated as $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0, where V_{dc} represents the DC input voltage. Conceptually, $2V_{dc}$ and $3V_{dc}$ are boosted voltages respectively associated with C_{F2} in Fig. 2(d) and C_{F2} in series with the DC input in Fig. 2(h). Similarly, $-3V_{dc}$ is obtained by reversing C_{F3} in Fig. 2(a) and $-2V_{dc}$ is achieved by the reverse series connection of the DC input and C_{F3} in Fig. 2(e). These, together with other equivalent circuits in Fig. 2 for generating $\pm V_{dc}$ and 0, show the viability of obtaining seven voltage levels with only six switches.

In practice, the six switches must additionally create charging and discharging intervals for the three floating capacitors, which in Table I are indicated by their voltages increasing or decreasing. None of the floating capacitive voltages will hence drop to zero or increase indefinitely. In other words, average voltages of the floating capacitors can self-balance around their specified constant values. Likewise, the DC-link capacitor C_{dc} discharges when in states I–IV and charges when in states V–VIII to keep a steady voltage.

Further, in all states, neutral (N) of the AC output has been grounded to the negative terminal of the DC input. Variation of the terminal voltage of the DC source is therefore restricted, which in turn, eliminates leakage current. In addition, unlike the usual seven-level NPC structure, modulation strategy for the 6S7LTBI needs to create three pairs of complementary gating signals for its six switches, to be demonstrated next.

B. Multicarrier Pulse-Width Modulation (PWM)

Three triangular carriers (T_1–T_3) with the same frequency (f_s), amplitude (E_c) and phase for generating three preliminary independent gating signals are shown in Fig. 3(a). Also shown in the figure is a rectified sinusoidal reference (V_{ref}) with a peak of A_m. This, together with the amplitude of carriers, gives rise to a modulation index of M_a=A_m/(3E_c). Implementation of the state-selection logic is then given in Fig. 3(b), where the eventual gating signals for the switches (S_1, S_3, and S_5) in Fig. 3(a) are chosen from a lookup table. A notable feature observed with the signals is that the switches S_5 and S_6 are switched at the fundamental frequency to lower overall switching losses. Other switches however have to operate at a high frequency but are fortunately clamped by low-voltage capacitors as analyzed in the next section.

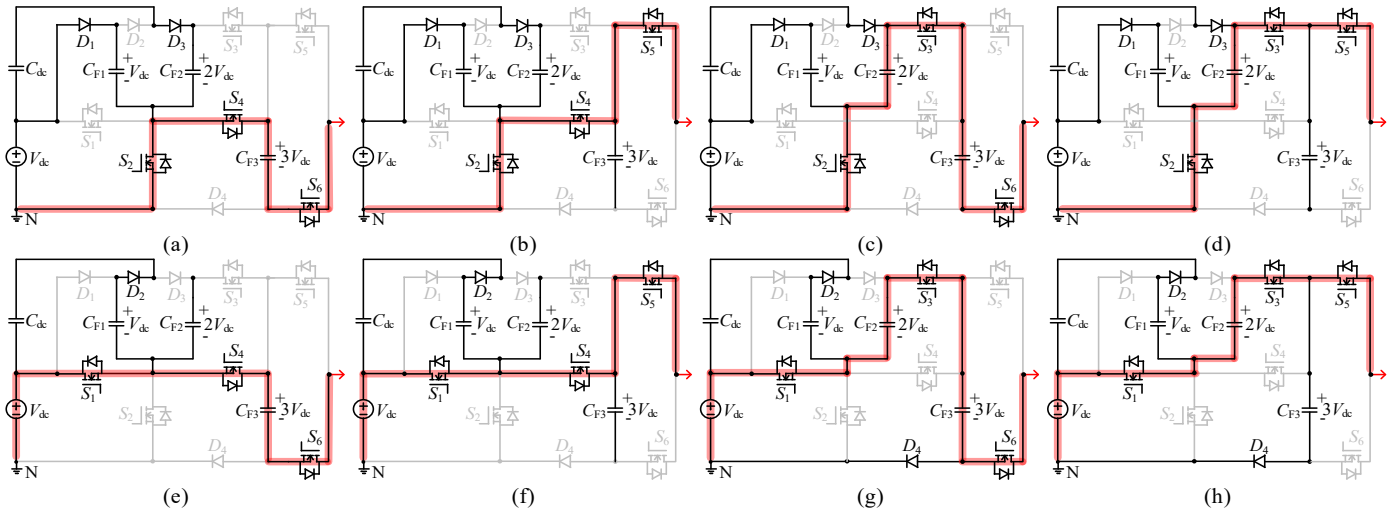

Fig. 2. Equivalent 6S7LTBI when in states I–VIII with output voltages of (a) $-3V_{dc}$, (b) 0, (c) $-V_{dc}$, (d) $2V_{dc}$, (e) $-2V_{dc}$, (f) V_{dc}, (g) 0, and (h) $3V_{dc}$.

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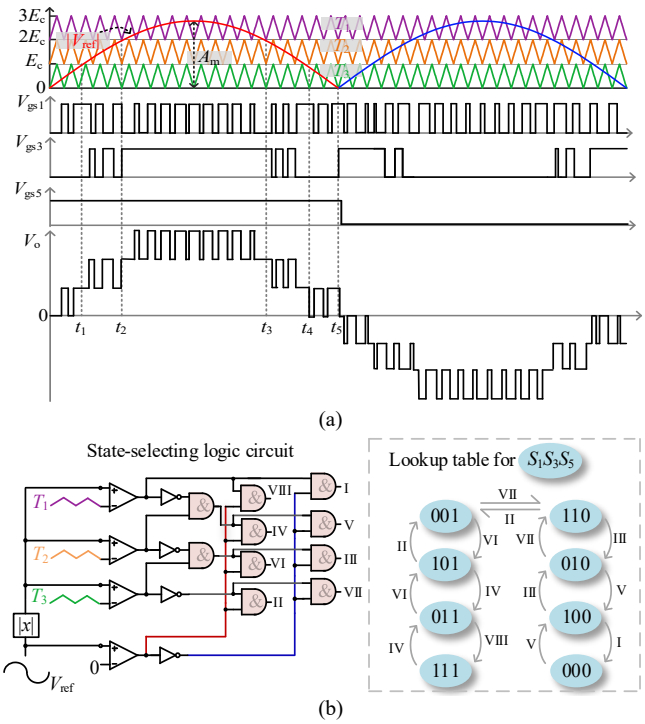


Fig. 3. Illustrations of (a) key PWM waveforms and (b) logics for generating gating signals V_{gs1}, V_{gs3}, and V_{gs5}.

III. Performance Indexes

A. Switch Voltage Stresses

From the eight states in Fig. 2, voltage stresses (V_{dsi}, i = 1 to 6) of the six switches are found as

$$V_{ds1} = V_{ds2} = \frac{1}{2}V_{ds3} = \frac{1}{2}V_{ds4} = \frac{1}{3}V_{ds5} = \frac{1}{3}V_{ds6} = V_{dc} \quad (1)$$

Including voltage stresses (V_{dj}, j = 1 to 4) of the diodes, the total standing voltage (*TSV*) of all semiconductors in per unit, after normalizing with the maximum output voltage $V_{o\text{-}max}$, is thus

$$TSV = (\sum_{i=1}^{6} V_{dsi} + \sum_{j=1}^{4} V_{dj})/(n_{vb}V_{dc}) = 6 \quad (2)$$

where n_{vb}=$V_{o\text{-}max}$/V_{dc} is the voltage-boost ratio.

B. Capacitor Voltage Ripples

The peak charging and discharging currents of the floating capacitors depend on voltage difference Δv_{CF} between two of them at their starting instant of parallel connection. It is therefore possible to reduce the two peak currents to acceptable values by keeping voltage ripples of the floating capacitors small. For C_{F1} and C_{F2}, this is not a major issue, since they do not discharge within two consecutive states. They can therefore replenish in each switching cycle to maintain a steady voltage with only a small voltage ripple ($\Delta v_{CF1,2}$). The same does not apply to C_{F3}, which continuously discharges to the output over the time span (t_4–t_1) in Fig. 3(a). Its voltage ripple is thus relatively large, expressed as

$$\Delta v_{CF3} = \frac{1}{2C_{F3}} \left| \int_{t_1}^{t_4} \sqrt{2} I_o \sin(\omega t) dt \right| \quad (3)$$

where ω and I_o are the angular frequency and rms value of the output current i_o, respectively.

Assuming a specification of $\Delta v_{CF3} \le 5\% V_{CF3}$, capacitance C_{F3} must hence have a relatively large value, and satisfy

$$C_{F3} \ge \frac{10}{3V_{dc}} \left| \int_{t_1}^{t_4} \sqrt{2} I_o \sin(\omega t) dt \right| \quad (4)$$

C. Loss Analyses

Efficiency of the 6S7LTBI mainly depends on the semiconductor losses caused by currents flowing through them. For that, diodes D_1 and D_3 are noted to conduct the input current (I_{in}) when in states I–IV. Their average currents I_{d1} and I_{d3} can thus be regarded as half of the input current. Similarly, the average current I_{d2} of diode D_2 in states V–VIII can be viewed as $1/2I_{in}$. Differences however occur with diode D_4, whose current in states VII and VIII is (I_{in}–i_o). Its average value can be approximated as I_{in}. The determined currents can then be used below to find the overall conduction losses of the diodes

$$P_d = \frac{V_F}{2}\left(\frac{I_{in}}{2} \times 3 + \frac{\overline{(I_{in}-i_o)}}{2}\right) \approx \frac{V_F}{2}\left(\frac{I_{in}}{2} \times 4\right) \quad (5)$$

where V_F is the forward voltage drop across each diode.

As for the switches, their conduction losses can be divided into three switch pairs, noting too that only three switches of the 6S7LTBI are conducting at any instant. The first switch pair {S_1, S_2} conducts (I_{in}–i_o) when in states I–IV and (I_{in}+I_{d2}) in states V–VIII. Conduction losses of its switches S_1 and S_2 can thus be computed using

$$P_{con1} = \frac{R_{on}}{2}\left({I_{in}}^2 + (I_{in} + I_{d2})^2\right) \quad (6)$$

where R_{on} represents the same on-state resistance for all switches.

The same applies to the other switch pairs {S_3, S_4} and {S_5, S_6}, whose conduction losses can be computed using

$$P_{con2} + P_{con3} = R_{on}({I_{in}}^2 + {I_o}^2) \quad (7)$$

In terms of the switching losses, only switches S_1–S_4 need to be considered since S_5 and S_6 are operating at the fundamental frequency. Moreover, for S_3 and S_4, they switch rapidly only over certain intervals, as depicted by Fig. 3(a). The maximum time that can be occupied by these intervals is half of a fundamental period, divided between the positive and negative half cycles. Therefore, the overall switching losses are calculated by

$$P_{sw} = \frac{(t_r + t_f) f_s}{2}\left(V_{dc}(I_{ds1} + I_{ds2}) + 2V_{dc}\frac{I_{ds3} + I_{ds4}}{2}\right) \quad (8)$$

where t_r and t_f are the turn-on and -off times of switches; and I_{ds1}–I_{ds4} are the average currents through S_1–S_4, respectively.

D. Comparison with Existing MLIs

The numbers of voltage levels, switches, diodes, and floating capacitors (N_{VL}, N_S, N_D, and N_{FC}) of the 6S7LTBI are compared with those of existing single-source MLIs in Table II. Other parameters compared in the same table are *TSV* and n_{vb} of the considered MLIs. Returning to N_{VL} and N_S, they particularly inform that the 6S7LTBI uses the least number of switches to produce an output voltage with seven levels or N_{VL} = 7, which is thus higher than those of [7], [14] and [15]. Its switch-per-level ratio is very low at around 0.86. Its *TSV* is not high either and, in fact, smaller than or equal to those of the seven-level

TABLE II
COMPARISONS WITH EXISTING SINGLE-SOURCE MLIS

MLIs	N_{VL}	N_S	N_D	N_{FC}	TSV	CF with α: 1	CF with α: 2	n_{vb}	I_{lk} (PV)	Total cost (USD)
[7]	5	9	0	1	4.5	21.25	23.25	2	High	62.29
[8]	9	11	0	2	5.5	26.75	29.5	2	High	75.43
[9]	9	12	0	2	5.25	27.31	28.63	4	High	81.17
[10]	9	8	3	3	5.75	23.44	24.88	4	High	66.30
[11]	7	8	2	2	6	26	32	1	Low (NPC)	65.13
[12]	7	10	0	2	7.33	26.89	31.77	1.5	Low (NPC)	81.69
[13]	7	10	0	1	6	25	29	1.5	Low (NPC)	73.67
[14]	5	7	0	2	5	21	26	1	Low (CG)	64.73
[15]	5	7	2	2	8.5	22.25	26.5	2	Low (CG)	72.21
6S7LTB	7	6	4	3	6	21	23	3	Low (CG)	64.72

The total cost is for a design example based on the devices in Table III.

Table III
DEVICES CHOSEN FOR STUDIED MLIS (VOLT-STR. ≡ VOLTAGE STRESS)

Volt-str.	Si MOSFETs ($)	Si diode ($)	Driver ($)	C0 ($)
$2V_{o\text{-}max}$	STW30N80K5 (6.38)	/	HCPL-3120 (3.86)	381LX102M400 (6.31)
$4V_{o\text{-}max}/3$	IPW60R125C6 (5.09)	/		
$V_{o\text{-}max}$	FQA30N40 (4.75)	STTH30R04 (3.55)		
$3V_{o\text{-}max}/4$ $2V_{o\text{-}max}/3$	IXFA26N30X3 (3.18)	APT30D30B (2.09)		
$V_{o\text{-}max}/2$ $V_{o\text{-}max}/3$	IRFP250NPBF (2.71)	FFPF30UP20S (1.37)		
$V_{o\text{-}max}/4$	IRLI2910PBF (1.91)	SDT30B100D1 (0.63)		

Unit price ($) from www.digikey.com and may vary with purchase quantities.

inverters [11]–[13]. It is however higher than those of the five-level inverters [7], [14], and nine-level inverters [8]–[10]. These compared MLIs nevertheless use more switches and hence more gating circuits. A way to consolidate all compared numbers for all the MLIs is thus necessary, which from [10], can be achieved using the following cost function (CF)

$$CF = N_{Dr} + N_S + N_D + N_{FC} + \alpha \cdot TSV/n_{vb} \quad (9)$$

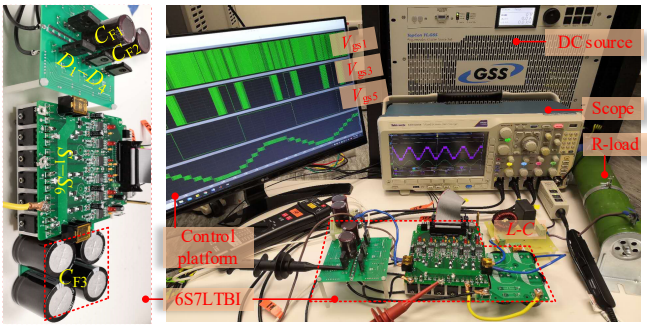
where N_{Dr} representing the number of gate drivers, is assumed to be equal to N_S.

Also included in (9) is coefficient α for tuning the weighted cost of selecting different semiconductors (materials such as Si, SiC or GaN, types such as IGBT or MOSFET, or ratings). With α then set to 1 and 2 for low- and high-cost semiconductors, respectively, CF of each MLI can be computed as tabulated in Table II. The numbers show that the inverter from [14] and 6S7LTBI have the lowest CF. The lowest CF has however not included influences from floating capacitances, their voltages (V_{CF}), voltage ripples, and power ratings, which in practice, may affect the total cost of the MLIs. To demonstrate, the monetary costs for all considered MLIs at 1-kW and with $V_{o\text{-}max}$ = 400 V are computed, after identifying appropriate semiconductors. For that, Table III lists eight voltage stresses that the switches/diodes of the considered MLIs must endure, followed by recommended parts and their unit costs. As for the floating capacitors, a quick estimate of their costs starts by choosing a base, which in Table III, is a 400-V, 1-mF capacitor (C0) with unit cost $\$_{C0}$. The estimated cost of each floating capacitor can then be expressed as $V_{CF}/V_{o\text{-}max} \times \$_{C0}$.

The eventual computed monetary costs are given in the last column of Table II, where the MLI from [7] has the lowest monetary cost, even though its CFs are slightly higher than those of the 6S7LTBI. The differences are due to more details accounted, when computing the more complex monetary costs. Both CF and monetary costs have however undisputedly projected the 6S7LTBI as a low-cost MLI that can produce seven-level switching with only six switches.

TABLE IV
COMPONENTS OF THE 800-W INVERTER PROTOTYPE

Voltage ratings	V_{dc}=100 V; $V_{o\text{-}max}$=300 V, 190 Vrms, 800 W
Capacitances	$C_{dc} = C_{F1} = C_{F2}$ = 220 μF; C_{F3} = 4000 μF
Switches / diodes	SCT3060AL × 6 / C3D20065 × 4



(a) (b)

Fig. 4. Photographs of the (a) inverter prototype and (b) testing setup.

Besides the cost, applicability as a renewable PV generator for all MLIs has been deliberated. Beginning with the criterion of n_{vb} larger than unity, MLIs from [11] and [14] are undoubtedly less suitable. Also, among MLIs capable of suppressing leakage current (I_{lk}) by either adopting the NPC or CG structure, the MLI from [15] produces a five-level output with a gain of two. This is less appealing than the seven-level output with a gain of three obtained from the 6S7LTBI. The 6S7LTBI is therefore suitable for interfacing with low-voltage PV modules while using low-profile output filters.

However, with only six switches, it does not have redundant states for replacing any unintentionally failed states. Also, like many SCC-based MLIs [9]–[15], voltage stresses experienced by its semiconductors are non-identical. Different switches and diodes may be necessary when optimizing its implementation. Lastly, its usage of electrolytic capacitors and diodes to form the SCC may affect efficiency when supplied by a low input voltage. The 6S7LTBI therefore does have some concerns, even though its advantages outweigh those concerns.

IV. EXPERIMENTAL RESULTS

An 800-W single-phase 6S7LTBI has been built using components from Table IV. Its PWM has a carrier frequency of 25 kHz and a modulation ratio of M_a=0.9, while its input has a capacitor added in parallel with the 100-V source (V_{dc}). An output L-C filter has then been added between the inverter and resistive load, as in Fig. 4. Fig. 5(a) shows the resulting steady-state output, which clearly has seven distinct voltage levels formed by voltages 100 V, 200 V and 300 V across C_{F1}–C_{F3}, respectively, as captured by Fig. 5(b). The highest output voltage level is thus 300 V or the achievable n_{vb} is 3, in accordance with the analysis. Concurrently, the capacitors have clamped voltages across the power switches, among which S_5

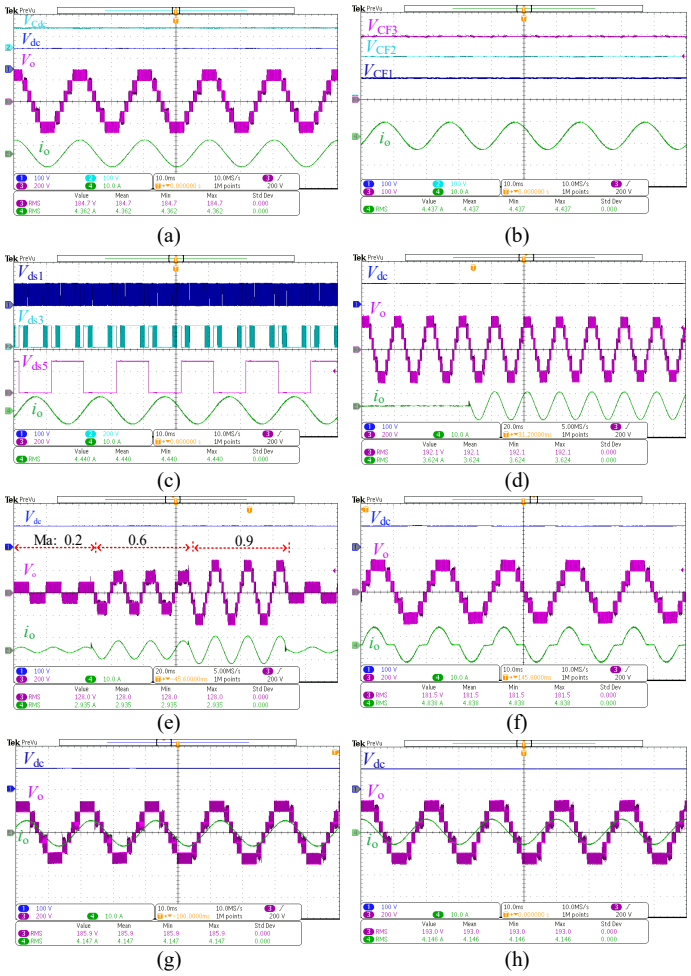


Fig. 5. Experimental results of the 800-W inverter prototype: (a) voltages of the DC input V_{dc} (100V/div), DC link capacitor V_{Cdc} (100V/div), AC output V_o (200V/div), rms 185 V, and AC output current I_o (10A/div), rms 4.4 A; (b) voltages of the floating capacitors V_{CF1}–V_{CF3} (100V/div); (c) voltages of the switches V_{ds1} (100V/div), V_{ds3} (200V/div), and V_{ds5} (200V/div); (d) step-change from no-load to full-load; (e) performance under a varied M_a; (f)–(h) operation under a nonlinear, inductive, or capacitive load.

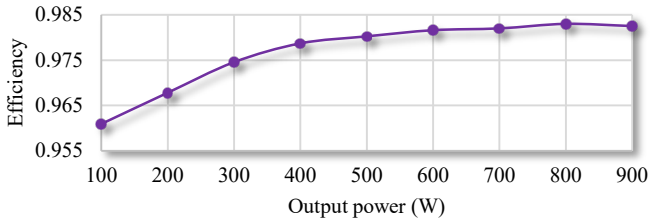


Fig. 6. Measured efficiencies with a 100-V DC input and a 190-Vrms AC output.

(and S_6) endures the highest clamped voltage, but is driven at the fundamental frequency, as seen from Fig. 5(c).

Other results showing the 6S7LTBI step-changing from no-load to full-load and from a modulation index M_a of 0.2 to 0.6 and then to 0.9 are given in Fig. 5(d) and (e), respectively. Together, they confirm stable dynamic operations of the 6S7LTBI. As for its ability to manage reactive power, Fig. 2 shows all its eight states having a bidirectional current path between its input and output. It can therefore operate with non-unity power factor, during which some small amount of energy will return to the source in case of a single-phase system. This expectation, together with supplying nonlinear load, has been confirmed by waveforms shown in Fig. 5(f)–(h).

Last but importantly, Fig. 6 shows efficiencies of the 6S7LTBI falling within 97% ± 1.3% at different output powers. Such high efficiencies are undoubtedly due to its low conduction and switching losses, earlier proven theoretically.

V. Conclusion

A seven-level inverter with the minimum number of switches has been proposed. Its features include offering a triple voltage-boost and a common-grounded connection for eliminating leakage current in a PV system. It also uses only a simple gate-driving pattern, designed to reduce conduction and switching losses. These features have collectively been compared with existing inverters and tested through experiments, which indeed record a high voltage gain and a high efficiency.

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