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Ensuring a Reliable Operation of Two-Level IGBT-Based Power Converters: A Review of Monitoring and Fault-Tolerant Approaches

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ABSTRACT Despite the emerging multi-phase and multi-level converters, two-level insulated gate bipolar transistor-based power converters are still widely used in industrial applications in nowadays. Thus, its reliability is of significant importance for ensuring industrial safety. In this paper, a review of the possibilities to ensure the reliable operation of these power converters is presented. The possible approaches are categorized into two groups: condition monitoring and fault-tolerant control. The former approach performs the monitoring methods of power converters, which enables the identification of device degradation to be realized. Accordingly, the mechanisms, indicators, and measuring methods of degradation are demonstrated in this paper to assist the design of condition-based maintenance. In contrast, the latter approach is a post-fault one, where power converters remain the operation by activating the fault-tolerant units after faults are identified. For this approach, fault detection, fault isolation, and tolerant strategies are essential. Finally, the performance and cost-effectiveness of the two categories are discussed in this paper.

INDEX TERMS Two-level power converter, reliability, condition Monitoring, fault tolerance, renewable energy application, insulated gate bipolar transistor.

I. INTRODUCTION

Insulated gate bipolar transistors (IGBTs)-based two-level converters are still widely adopted in today's industrial applications, e.g., wind turbine power systems [1], [2], photovoltaic (PV) systems [3], [4] and electrified vehicles [5]–[9]. In those applications, the power converters may face harsh conditions, which as a consequence, challenges the reliability, being the main lifetime-limiting component. For instance, according to the study in [10], power converters account for 34% of all the failures in electrified railway traction systems, as shown in Fig. 1. A similar conclusion has been revealed in [11] (see Fig. 2) that PV inverters contribute 37% of overall unscheduled maintenance events. The power converter failures lead to 59% of the total unplanned maintenance expenditure. Furthermore, based on an industry-based survey in [12], the most fragile components in power converters are semiconductor power devices, contributing to around 31% of all the converter failures.

There are two types of failures in IGBT power devices: 1) wear-out failures and 2) catastrophic failures [13]. The first category of failure is package-related, where the failure is a consequence of accumulated damage due to the temperature, vibration, and humidity stresses on the devices [12]. Among those stressors, the temperature, more specific, the junction temperature is considered the most critical failure-inducer in IGBT power devices, especially for the wear-out failure [14], [15]. This can be further demonstrated using the cross-section view of an IGBT device, as shown in Fig. 3, where the wear-out failure images and the coefficient of thermal expansion (CTE) of the materials of a wire-bonded IGBT can be observed [15]–[20]. Due to the

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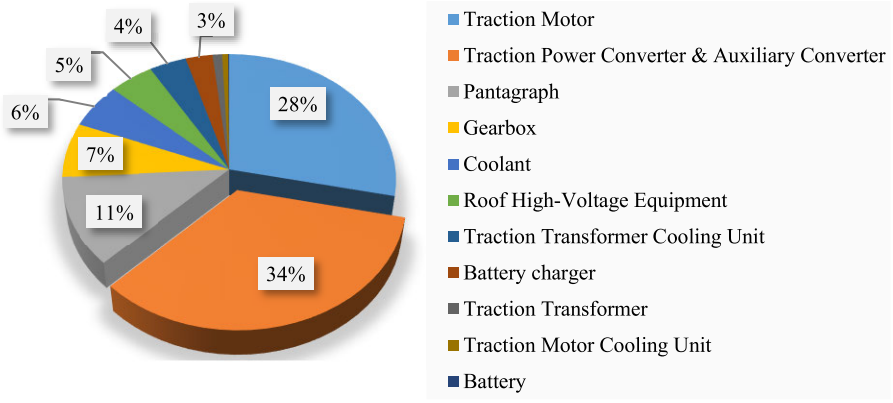

FIGURE 1. Failures of electrified railway traction drive systems from 2009 to 2013 [10].

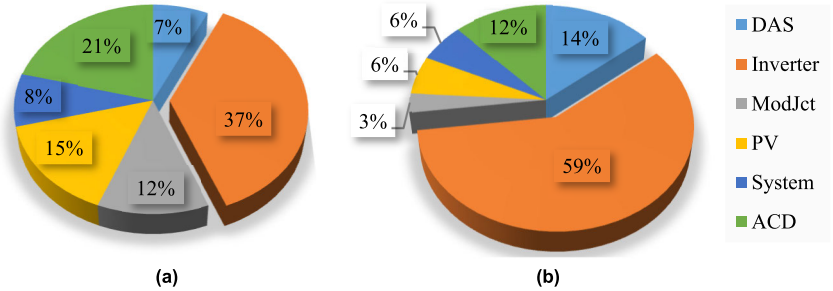

FIGURE 2. Five-year experience of failures in a commercial PV power plant in Arizona from 2001 to 2006 (DAS: Data Acquisition System, ACD: ac disconnects, ModJct: Module Junction Box, PV –PV arrays): (a) unscheduled maintenance events and (b) associated maintenance costs [11].

CTE mismatch between the adjacent layers, bond wires, solder joints, and metallization layers, thermo-mechanical stresses in the case of temperature swings can accelerate the degradation (i.e., wear-out), leading to various wear-out failures like the bond wire lift-off, bond wire cracking, and metallization reconstruction. On the contrary, the IGBT catastrophic failures are not accumulated failures but triggered by a single overheat, overvoltage or overcurrent event. They are categorized as open-circuit faults and short-circuit faults. Open-circuit faults may be caused by the failure of gate drivers or bond wires, while short-circuit faults may occur due to unclamped inductive switching, high-temperature latch-up, second breakdown, or energy shocks [13]. Therefore, ensuring reliable operation of power electronic converters is of importance to avoid unexpected downtime of the entire systems, and hence to lower the maintenance efforts.

Many attempts should be made to address the two failures. In the literature, there are two ways to cope with the above IGBT failures, and by doing so, the reliability of the entire power converters can be improved. The first approach is based on reliability assessment schemes, which provides information about the health status of the power devices. By evaluating the degradation level, the condition-based maintenance can be performed before the catastrophic failures take place, which could reduce the maintenance costs and potential loss. In contrast, the other approach attempts to improve reliability by increasing the system operation redundancy for the two-level converters. That is to say, it is a post-fault approach. When faults are identified, the power electronic converters can still operate by activating the redundant unit (e.g., reconfiguring the power converter system). Clearly, the fault-tolerant strategies inevitably require more power semiconductor devices as well as more sophisticated control schemes (i.e., fault identification, isolation, and reconfiguration). Consequently, costs are rising. Nevertheless, it is highly application-dependent to select a cost-effective approach to guarantee the reliable operation of power electronic converters.

In light of the above, this paper reviews the possibilities to enhance power converter reliability. The performance and cost of the methods are benchmarked considering different application conditions, where the selection criteria are also presented. The rest of this paper is organized as follows. An overview of the monitoring methods is given in Section II, including degradation mechanisms and indicator extraction methods. In Section III, fault detection, isolation, and tolerant strategies are discussed. A comparison of these approaches under different working conditions is presented in Section IV. Finally, concluding remarks and discussions are provided in Section V.

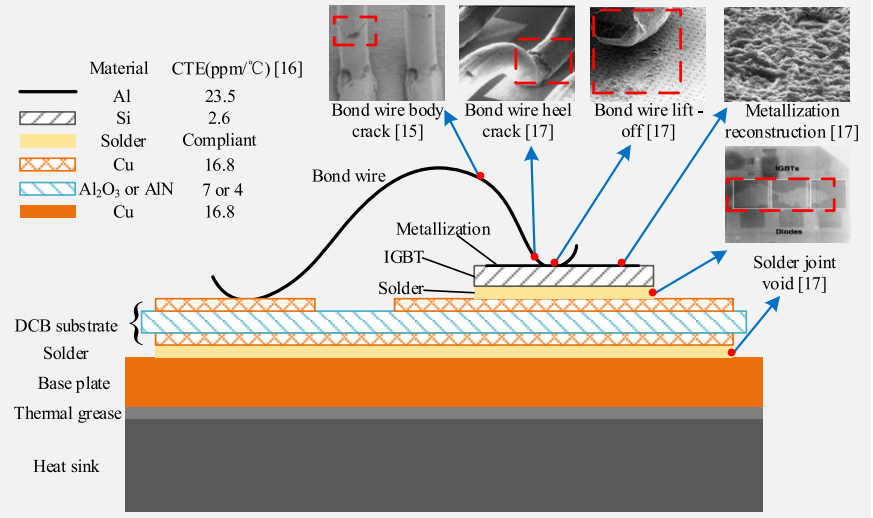

FIGURE 3. Cross-section view of a wire-bonded IGBT, where the possible wire-out failures are shown [15]–[17].

II. MONITORING OF DEGRADATIONS

In order to achieve the highly-reliable operation of power converters, an alternative is to evaluate the health state and then perform pre-fault schemes before the converter system fail. This strategy requires an understanding of how the converter will degrade and how degradation can be identified, which are demonstrated in part A and B, respectively.

A. WEAR-OUT MONITORING

IGBT power devices age over time, and in this case, some parameters will drift away from the initial values accordingly. Thus, the parametric changes can be the indicators of wear-out failures. If the monitored parameters exceed the thresholds, an early warning replacing the aged device will be provided. Depending on failure mechanisms, different monitoring techniques should be applied. Thus, the following firstly reviews the failure mechanisms, which is followed by the corresponding indicators.

1) BOND WIRE FATIGUE MECHANISM

Power chips are wire-bonded during packaging. The wire bonds suffer from severe temperature swings due to switching. As shown in Fig. 3, there is a significant CTE mismatch between the bond wires (aluminum-based) and chips (silicon-based), and thus the shear stress is introduced to the interface. This further imposes repeated flexures on the aluminium wires, i.e., fatigue [21]. The bond wire fatigue, leading to the bond wire lift-off and/or bond wire cracking, is one of the dominant failures in IGBT modules. The bond wire lift-off initiates from the fracture at the tail of the bond, and it propagates to the center. Eventually, the bond-wire is lift off and loses the electrical contact with the IGBT chip because of the spring effect of the aluminium wire loop [20]. For the bond wire cracking, according to [22], the heel of the bond wire suffers from larger stresses than other parts, and it becomes the most critical part in terms of cracking.

Nonetheless, the above two failures will contribute to an increase in the total resistance of the bond wires. Accordingly, the on-state collector-emitter voltage $V_{ce,on}$ will increase [15], [18], [23]–[28]. Hence, the voltage $V_{ce,on}$ can be an observable variable for bond-wire fatigue. For instance, an increase of 5 % [15, 18], 15% [25] and 20% [29] in the voltage $V_{ce,on}$ from the initial value are considered as the thresholds. In [30], the threshold was set as $1500/I_{Rated}$ with I_{Rated} being the rated current of the power device. Although the increase of the resistance leads to the on-state voltage increase, the change is sensitive and affected by various factors. First, the voltage $V_{ce,on}$ is a temperature-sensitive electrical parameter (TSEP) [31], and it changes with the junction temperature (T_j) during operation. For example, in [25], a sudden drop followed by a sudden increase in the voltage $V_{ce,on}$ was reported. It is because the solder fatigue occurs, the on-state voltage $V_{ce,on}$ decreases dramatically, when the IGBT operates in the negative thermal coefficient area. Then, if the bond wire fatigue happens, the on-state voltage $V_{ce,on}$ will increase. In order to eliminate the thermal effect, compensations should be applied. In [26], [32], the relationship between the on-state voltage $V_{ce,on}$ and the junction temperature T_j is determined through power cycling tests. Subsequently, the thermal effect can be compensated by subtracting the temperature -induced voltage changes. Additionally, variations of $V_{ce,on}$ are relatively small, compared to the original voltage, which requires high-resolution measurements of the voltage $V_{ce,on}$. This may increase the cost of the hardware system. Meanwhile, small variations may be hidden due to the load current or temperature changes under harsh operating conditions [33].

The bond wire crack and lift-off will affect the parasitic parameters. In return, the changes of the parasitic parameters

will inevitably affect the IGBT gate characteristics [34]. Therefore, the change of gate characteristics can be another indicator of the bond wire fatigue [16], [35]–[37]. More specifically, the bond wire lift-off will decrease the gate-emitter capacitance and increase the parasitic inductance. Hence, the voltage drop induced between the power emitter and auxiliary emitter V_{EE}' increases and the Miller-plateau duration t_{gp} declines [38], [39]. Meanwhile, the gate-emitter voltage V_{ge} and the collector-emitter voltage V_{ce} will rise faster during turn-on and turn-off, respectively, compared to the case without bond-wire fatigue [35]. In addition, the metallization reconstruction and solder fatigue take place simultaneously with the bond wire degradation. Fortunately, the change of gate characteristics caused by the bond wire fatigue is not significant [37]. However, the results are entirely different in [16] in terms of the gate-emitter voltage V_{ge}. There are no significant changes in the voltage V_{ge} until all the bond wires are lifted off, which is in contrast with the results in [35]. Consequently, more attempts should be made to explore how different degradations contribute to the changes in the gate (switching) characteristics, and how the characteristics correlate to early wear-out failures.

2) SOLDER FATIGUE MECHANISM

The solder fatigue is another dominant wear-out failure in IGBT modules. It is typically induced by the temperature wing and CTE mismatch. There are two solder layers in one IGBT device, as shown in Fig. 3: one between the chip and the substrate and one between the substrate and the baseplate. Due to the thermo-mechanical stress, delamination incidents, cracks and voids can occur in solder joints. Typically, cracks start from the edge of the joints, decrease the thermal dissipation path and increase the thermal resistance (R_{th}), which eventually leads to a higher junction temperature T_j. In the positive temperature coefficient area, the increased junction temperature results in more power losses and a further higher junction temperature. Hence, the positive feedback accelerates the failure of the IGBT device. To prevent this, the junction-to-case thermal resistance R_{thjc} (or junction-to-case thermal impedance) [40]–[42], and the junction temperature T_j [43], [44], are commonly used as indicators to monitor the solder fatigue in IGBT. Furthermore, considering the non-uniform distribution of the thermal resistance R_{th} on the case, due to the solder fatigue, the ratio of the junction-to-case-center resistance to the junction-to-case-edge thermal resistance can also be utilized as an indicator [45]. Besides, the chip solder degradation leads to the rise of the gate-collector capacitance and trans-conductance, decrease of the gate-emitter, which eventually cause the decline of voltage change rate $\mathrm{d}v_{ce}/\mathrm{d}t$ and increase of current change rate $\mathrm{d}I_c/\mathrm{d}t$ during turn-on [46], [47]. Additionally, because the junction temperature T_j influences the turn-off transient, low-order harmonics will be affected, when the solder fatigue occurs. Therefore, the 5th-order harmonic can also be used to monitor the solder fatigue incident [48].

3) METALLIZATION RECONSTRUCTION MECHANISM

The aluminium metallization layer is deposited on the chip, providing electrical connection between the power dies and the emitter. Meanwhile, it maintains off-state parasitic components, which are inherent to the structures of power components [49]. The CTE mismatch between the chip (Si) and the aluminium layer (Al) is the reason for the metallization reconstruction, as shown in Fig. 3. Subsequently, the huge thermo-mechanical stress may exceed the elastic limit of the thin aluminium film, which may cause plastic deformation at the grain boundaries, leading to the extrusion of aluminium grains or cavitation effects at the grain boundaries [50]. In this case, the active cross-section of the metallization is reduced and the sheet resistance R_{sheet} increases linearly [50]–[55]. Thus, the collector-emitter voltage $V_{ce,on}$ will have a linear increase, which can indicate the metallization reconstruction [45], [56].

4) GATE OXIDE DEGRADATION MECHANISM

The gate oxide degrades along with the above degradations. It is because the high temperature (e.g., a high electric filed) causes time-dependent dielectric breakdown or a high current causes hot electrons [57]. Due to the accumulated charges in the gate oxide, the capacitance-voltage characteristics will shift along with the gate voltage, and the threshold voltage (V_{th}) will increase, consequently [24]. In addition, the electron injection may degrade the quality of the oxide, and lead to an increase in the gate leakage current (I_{ges}) [37], [57]. Further, the accumulated charges and the gate oxide degradation increase the gate oxide capacitance and the Miller capacitance, which extends the t_{gp} [39], [58].

The major degradations in IGBT modules are discussed in the above and summarized in TABLE 1. The mechanisms of those degradations are also shown, where the observable variables to indicate the corresponding degradation have also been presented. The prior-art methods using those indicators to identify degradations can be found in the literature, which are also given in TABLE 1. The main problem of using the indicators to monitor the health state of the IGBT is that the indicators are influenced by more than one failure mechanisms. For example, t_{gp} is affected by both the bond wire lift-off and the gate oxide degradation, while their effects to t_{gp} are opposite. Furthermore, most of the indicators are temperature dependent, i.e., they cannot be able to reflect a correct health state unless they are measured at the same temperature. Thus, new indicators that dedicated to one failure mechanism or indicator combination that can effectively monitor the health state of the IGBT are expected in the future.

B. INDICATOR MEASUREMENT

The condition of the IGBTs can be monitored through the indicators. In this part, methods that are utilized to do so in the literature will be reviewed and compared.

TABLE 1. Mechanisms and indicators for different degradations in IGBT modules.

Degradations	Mechanisms	Indicators
Bond wire fatigue	Combination of CTE mismatch and temperature swing	$V_{ce,on}$ [15, 18, 23-28]
		V_{ce} during turn-on [16, 35-37]
		$V_{EE'}$ [38]
		t_{gp} [39]
Solder fatigue	Combination of CTE mismatch and temperature swing	R_{thjc} [40-42]
		T_j [43, 44]
		5th harmonic [48]
		dv_{ce}/dt [46]
		dI_c/dt [47]
Metallization reconstruction	Combination of CTE mismatch and temperature swing	Sheet resistance [50-55]
		$V_{ce,on}$ [45, 56]
		C-V plot [24]
Gate oxide degradation	High temperature (high electric filed sometimes)	V_{th} [24]
		I_{ges} [37,57]
		t_{gp} [39, 58]

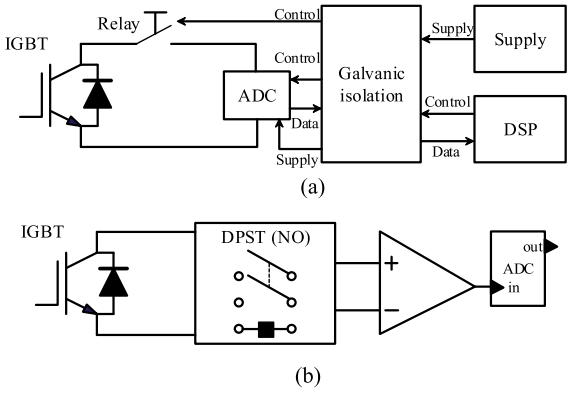

FIGURE 4. Relay-based Vce,on measurement circuits [28], [56].

of IGBT devices. In [56] (see Fig. 4(a)), the Analog-Digital Converter (ADC) is directly connected to the IGBT through a reed relay. When the power converter is operating, the relay is open to block the high voltage from the power electronic converter. Only when it stops or is forced to stop because of the measurement routine, a control signal will be generated to close the relay, and the ADC is then connected to the IGBT device, starting the measurement. Meanwhile, a simple current injection switching sequence is applied to turn on each IGBT. Thus, the on-state voltage $V_{ce,on}$ of each IGBT can be measured with high noise immunity and high resolution (2-3 mV), as reported. The method in [28] (Fig. 4(b)) is similar to that in [56]. The difference is that it uses an amplifier to extract $V_{ce,on}$. Nonetheless, the relay-based measurement is a relatively simple but offline approach.

1) MONITORING THE COLLECTOR-EMITTER ON-STATE VOLTAGE $V_{ce,on}$

The on-state voltage $V_{ce,on}$ can indicate the condition of the IGBT devices in terms of bond wire fatigue and metallization reconstruction. However, $V_{ce,on}$ does not vary significantly, and thus measurements of a high resolution are required. In addition, the high voltage from the DC-link should be isolated and blocked to protect the measurement circuit, when the IGBT is off. Relays [28], [56], MOSFETs [15[, [18], [33], diodes [28], [59], [60], and multiplexers [25] are common blocking devices, which can be seen in TABLE 2.

a: RELAY-BASED METHODS

All the relay-based extraction methods for $V_{ce,on}$ are offline schemes, since the response of relays is much longer than that

b: MOSFET-BASED METHODS

Since MOSFETs switches at a higher switching frequency than IGBTs, MOSFETs are also used to block the voltage as an online or quasi-online method to measure the voltage $V_{\mathrm{ce,on}}$. In [49] (Fig. 5(c)), when the IGBT is turned on, V_{ce} decreases, and the falling edge will be detected by the falling edge detector. Following, the monostable multivibrator triggers the MOSFET to measure $V_{ce,on}$. In [18], an online method to measure the voltage under high and low currents is proposed, as shown in Fig. 5(a). In this method, taking the upper switch as an example, for the measurement of $V_{ce,on}$ under a high current, AS_2 is turned off, and the following are obtained

$$V_{RC1} = V_{ce,on} - V_{ASC1} = V_{C1} - V_{SG1} \quad (1)$$

TABLE 2. Methods to measure the on-state voltage $V_{ce,on}$.

Topology	Blocking device	Additional hardware for each IGBT	Cost	Applicable condition
Fig. 4 (a) [56]	Relay	1 relay, 1 galvanic isolation	L	• Offline application
Fig. 4 (b) [28]	Relay	1 relay, 1 amplifier, 1 inductive isolation	L	• Offline application • Relatively high voltage • Noisy environment
Fig. 5 (c) [33]	MOSFET	2 amplifiers, 1 MOSFET, 1 capacitor, 1 multivibrator, 1 falling edge detector	H	• Online application • medium voltage • Online application
Fig. 5 (a) [18]	MOSFET	3 MOSFETs, 1 current source, 1 amplifier	H	• Low voltage • Noisy environment • High performance unrequired
Fig. 5 (b) [15]	MOSFET	1 MOSFET, 2 Schottky diodes, 1 zener diode	H	• Online application • Low voltage
Fig. 6 (a) [28]	Zener diode	1 Zener diode, 1 diode, 1 amplifier, 1 inductive isolation	M	• Online application • Low voltage • Noisy environment
Fig. 6 (b) [60]	diode	4 diodes; 1 current source; 1 amplifier	M	• Offline application • High voltage
Fig. 7 [25]	multiplexer	2 amplifiers; 1 multiplexer	H	• Online application • Low voltage

H-high; M-medium; L-low

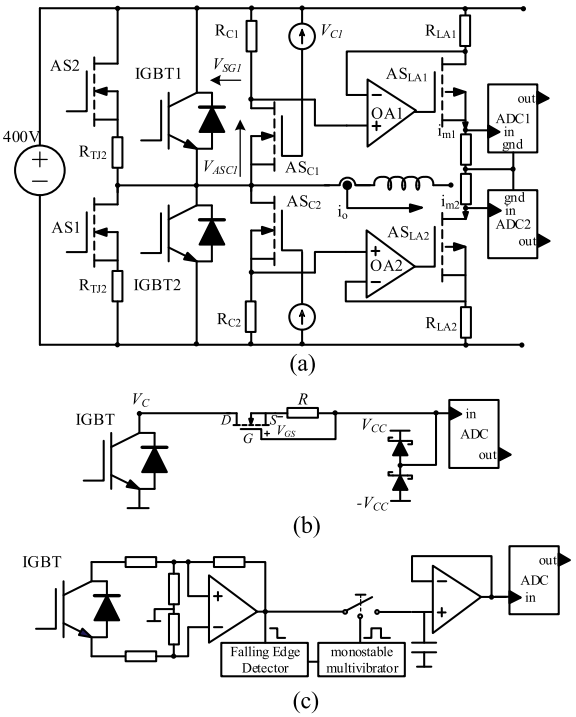

FIGURE 5. MOSFET-based Vce,on measurement circuits [15], [18], [33].

$$V_{SG1} = V_{C1} - V_{ce,on} + V_{ASC1} \tag{2}$$

where V_{RC1} is the voltage across R_{C1}, V_{ASC1} is the Drain-Source voltage of AS_{C1}, V_{C1} indicates the voltage of the current source and V_{SG1} represents the Source-Gate voltage of AS_{C1}. According to (2), when the power converter is operating and IGBT1 is on, AS_{C1} will turn on because $V_{ce,on}$ is small and V_{SG1} is larger than the threshold voltage of AS_{C1} (V_{SGTH1}). Then, it can be obtained from (1) that $V_{ce,on}$ is almost equal to V_{RC1}, as the on-state resistance of AS_{C1} is relatively small compared to R_{C1}. When IGBT1 is off, the collector-emitter voltage V_{ce} increases and V_{SG1} is smaller than V_{SGTH1}, and AS_{C1} is turned off. Consequently, the off-state high voltage is blocked. To measure the voltage $V_{ce,on}$ under a low current, AS_2 is turned on at the current zero-crossing, and R_{TJ2} is set to $0.1 \times V_{dc}$ to inject a current of 100 mA into IGBT1. Then, $V_{ce,on}$ can be measured as mentioned above. This needs a short period of zero load currents, which may affect the normal operation. Finally, V_{RC1} ($V_{ce,on}$) is generated on the resistor R_{LA1} by the amplifier, which gives a current i_{m1} equal to VR_{C1}/R_{LA1}, passing to the ADC through AS_{LA1}. This current can be a few dozens of milliamperes. Thus, a high-immunity transmission is guaranteed and the galvanic insulation is avoided.

In [15], a simple method to measure $V_{ce,on}$ is proposed, using a depletion-mode small-signal MOSFET with auxiliary components (see Fig. 5(b)). Notably, when the voltage V_{CC} is larger than the collector-emitter voltage $V_{ce,on}$, the input impedance of the measurement circuit becomes higher. When the upper switch T_{UH} is turned on, $V_C = V_{ce,on} < V_{CC}$. In addition to the high impedance, I_D cannot flow through the MOSFET, and $V_{GS} = 0$. Thus, the MOSFET is turned on and $V_{out} = V_{ce,on}$. When the upper switch T_{UH} is turned off, V_{ce} increases, and finally exceeds V_{CC}. Then, I_D flows through the MOSFET, and a voltage drop across R is produced, which makes V_{GS} smaller than the voltage threshold. Therefore, the MOSFET is turned off, the high voltage is blocked, and V_{out} is clamped to V_{CC}. However, because of the low voltage rating of the MOSFET, more MOSFETs will be required to block the DC-link voltage in high-voltage applications.

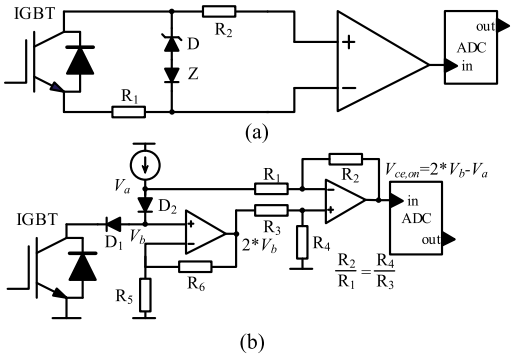

FIGURE 6. Diode-based Vce,on measurement circuits [28], [59], [60].

c: DIODE-BASED METHODS

Compared to the relay-based and MOSFET-based methods, measuring the voltage $V_{ce,on}$ with diodes is a cheaper solution, especially for higher voltage applications. Fig. 6(a) shows a Zener diode-based circuit that measures the collector-emitter voltage [28]. The off-stage voltage is clamped by the Zener diode, and another diode with low stray capacitance is connected in series to reduce the stray capacitance effect. When the IGBT is turned on, $V_{ce,on}$ can be measured by the amplifier. The resistors are used to limit currents and minimize the common-mode error. Nevertheless, when the IGBT is on, the clamped voltage on the resistance may induce variations, which may affect the operation of the power converter. In addition, limited by the rating of the Zener diode, this circuit in Fig. 6(a) is only effective and safe under 600-V off-stage voltages.

In [61], a measurement circuit for higher voltages is thus proposed (Fig. 6(b)), where D_1 and D_2 are forward-biased by the current source when the IGBT is turned off. Thus, the off-stage voltage is blocked. When the IGBT is turned on, $V_{ce,on} = V_b - V_{D1}$. Assuming that D_1 is identical to D_2, we have $V_{D1} = V_{D2}$. Therefore, $V_{ce,on} = V_b - V_{D2} = V_b - (V_a - V_b) = 2V_b - V_a$. This is realized with two amplifiers by setting $R_5 = R_6$ and $R_2/R_1 = R_4/R_3$. In this case, the difference between the two diodes may lead to measurement errors.

d: MULTIPLEXER-BASED METHODS

In [25], a two-to-one multiplexer circuit is used to filter out the off-state data. An amplifier is adopted to scale down the on-state voltage. When the gate signal is active, the scaled voltage $V_{ce,on}$ will be selected as the output. Otherwise, zero will be the output. Limited by the scaling circuit, this extractor cannot work under high voltage. The detailed circuit is given in Fig. 7.

The on-state voltage of IGBT measuring methods have been discussed above and concluded in TABLE 2. It can be a reference when selecting appropriate and cost-effective methods to measure or monitoring the collector-emitter voltage, through which the fatigue assessment in IGBT modules can be enabled. The relay-based methods are preferred for the

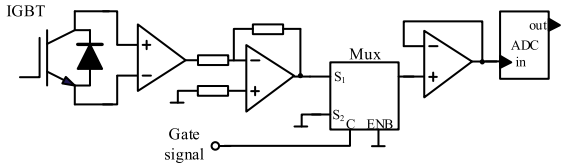

FIGURE 7. Multiplexer-based Vce,on measurement circuits [25].

offline conditions as they can fulfil the task with the lowest cost. However, the diode outperforms the other methods if both the cost and the online performance are taken into consideration.

Note that $V_{ce,on}$ depends on the temperature and current, which requires the measurement at the same working point and same temperature. To tackle this problem, [62] decomposes the voltage into three parts and gives the temperature and current dependent formula of each part. In this way, the degradation caused component can be estimated even the temperature or current varies. It should be noted that the accuracy will be limited by the precision of the formula. Besides, the so-called inflexion point where $V_{ce,on}$ almost keeps constant with different temperatures could be another solution to avoid the influence of the temperature [63].

2) MONITORING THE JUNCTION TEMPERATURE T_j

The junction temperature T_j can be measured by a thermocouple sensor or infrared camera directly, or by the thermosensitive electrical parameters (TSEPs) indirectly. In practice, however, it is impossible to perform the junction temperature measurement directly without modifying the package or housing (e.g., open the module and remove dielectric gel). As a result, the direct measurement is limited for temperature monitoring in practice. Although NTC thermistors are provided in most modules, the calibration between T_j and the thermistor is lacked. TSEPs, dependent on the junction temperature T_j, are therefore preferred to estimate the junction temperature, since they can be measured directly.

Methods by TSEPs include static and dynamic approaches. The first one uses the static electrical parameters to estimate T_j. The static parameters can be the collector-emitter voltage under high currents $V_{ce,Ihigh}$ [15], [64]–[67], collector-emitter voltage under low currents $V_{ce,Ilow}$ [31], [40], [67]–[70], gate internal resistance $R_{G,int}$ [71]–[73], saturation current I_{sat} [74]–[77], short circuit current I_{sc} [78], and gate-emitter voltage V_{ge} [79]. The other approach uses dynamic electrical parameters to estimate T_j. Such dynamic parameters include the threshold voltage V_{th} [31], [33], [80]–[83], Miller-plateau voltage V_{gp} [84], turn-on delay time t_{don} [85], maximum current slope of turn-on $dI/dt_{max,on}$ [85], turn-off time t_{off} [85], [86], turn-off delay time t_{doff} [87], the peak value of $V_{EE'max}$ during turn-off [88], [89] and the flatband voltage V_{fb} [90]. The following describes the above methods.

a: TEMPERATURE ESTIMATION BY $V_{ce,Ihigh}$

The relationship between $V_{ce,Ihigh}$ and T_j is not exactly linear. With an acceptable range of errors, the relationship can be

approximated as [65], [66]

$$V_{ce,Ihigh} = \underbrace{V_{ceo}}_{V_{ce}\ at\ T_{jo}} + \underbrace{\underbrace{k_{Vceo}\cdot\left(T_j - T_{jo}\right)}_{V_{ce}\ increse\ on\ the\ chip} + \underbrace{I_c\cdot[r_o + k_{ro}\cdot(T_r - T_{ro})]}_{V_{ce}\ increse\ on\ the\ series\ resistance}}_{V_{ce}\ increse\ due\ to\ temperature\ vatiation} - \underbrace{k_{ge}\cdot\Delta V_{ge}}_{V_{ce}\ increse\ due\ to\ V_{ge}\ variation} \quad (3)$$

where $V_{ce,Ihigh}$ is the measured collector-emitter voltage under high currents, T_{jo} denotes the base junction temperature, V_{ceo} is the on-state collector-emitter voltage at T_{jo}, T_r indicates the series resistance temperature, T_{ro} represents the series resistance base temperature, r_o is the series resistance at T_{jo}, k_{Vceo} and k_{ro} indicate the temperature coefficient of V_{ce} and r_o, repsectively, ΔV_{ge} is the gate-emitter voltage variation, k_{ge} denotes the coefficient of ΔV_{ge}, and I_c means the collector current.

Practically, it is difficult to measure V_{ce} from the module terminals because the chip is packaged inside the module. The measured voltage $V_{ce,Ihigh}$ consists of V_{ce} and the series packaging resistance voltage. In addition, $V_{ce,Ihigh}$ is affected by T_j, T_r and V_{ge}. However, V_{ge} can be treated as a constant in normal operation mode. Therefore, T_j can be estimated as

$$T_j = \frac{V_{ce,Ihigh} - V_{ceo} - I_c\cdot[r_o + k_{ro}\cdot(T_r - T_{ro})]}{k_{Vceo}} + T_{jo}. \quad (4)$$

In the literature, it is considered that T_r is equivalent to T_j. Assuming that the temperature distribution is homogeneous when the coefficients k_{ro} and k_{vceo} are identified by experiments. T_{j_est} is then obtained as

$$T_{j_est} = \frac{V_{ce,Ihigh} - \overbrace{(V_{ceo} + I_c\cdot r_o)}^{V_{ce}\ at\ base\ temperature\ (I_c)}}{k_{Vceo} + I_c\cdot k_{ro}} + T_{jo}. \quad (5)$$

However, it should be pointed out that T_r and T_j are not equal due to the non-uniform temperature distribution. In order to improve accuracy, T_r should be estimated as a prerequisite. According to [66], it gives

$$T_j - T_r = \alpha\cdot\left(T_{j_est} - T_H\right) \quad (6)$$

where T_H is the heatsink temperature and α is the scaling factor that is obtained by experiments. With (6), the temperature T_j can be estimated accurately as

$$T_{j_est} = \frac{V_{ce,Ihigh} - V_{ce,B} + \alpha\cdot k_{ro}\cdot I_c\left(T_{j_est} - T_H\right)}{k_{Vceo} + I_c\cdot k_{ro}} + T_{jo} \quad (7)$$

in which $V_{ce,B}$ is the voltage V_{ce} at the base temperature. It can be found in (7) that the estimated temperature T_j using $V_{ce,Ihigh}$ is sensitive to the coefficients k_{Vceo}, k_{ro}, and the collector current I_c. The sensitivity varies from 1 mV/°C (300 A) to 5 mV/°C (1000 A) [67]. In addition, the online junction temperature estimation requires measuring $V_{ce,Ihigh}$, I_c, and some predefined parameters.

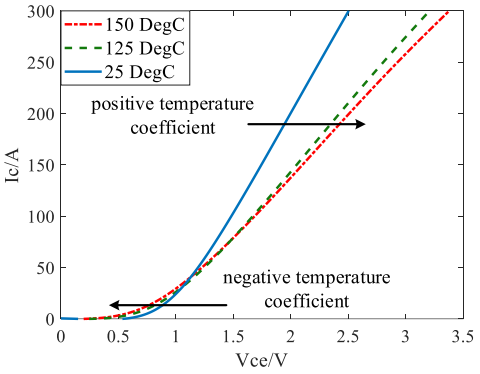

FIGURE 8. I-V characteristics of an IGBT.

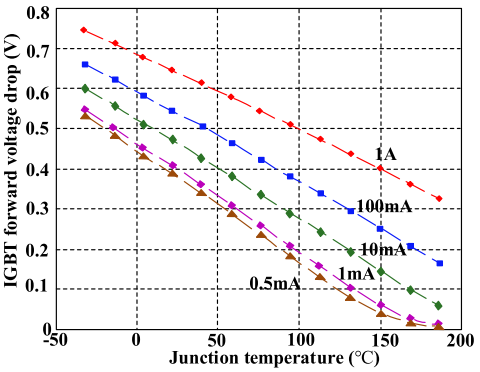

FIGURE 9. $V_{ce,Ilow}$ of an IGBT as a function of the junction temperature T_j for different low currents [31].

b: TEMPERATURE ESTIMATION BY $V_{ce,Ilow}$

Fig. 8 shows the typical I-V characteristics of an IGBT. Unlike the positive temperature coefficient for the high current, it can be seen that the temperature coefficient for the low current is negative. Compared to the method using $V_{ce,Ihigh}$, utilizing $V_{ce,Ilow}$ neglects the series packaging resistance because its voltage drop is relatively low. At the same time, the self-heating effect can be eliminated. Thus, it has higher accuracy and stronger linearity than the previous method (i.e., using $V_{ce,Ihigh}$). In this case, the relation can be expressed as

$$V_{ce,Ilow} = V_{ceo} + k'_{Vceo}\cdot\left(T_j - T_{jo}\right) \quad (8)$$

where k'_{Vceo} is the temperature coefficient for the low current.

Fig. 9 depicts the voltage $V_{ce,Ilow}$ of an IGBT as a function of the junction T_j under various low currents. It can be observed that the voltage change rate in respect to the junction temperature is within the range of −0.19 mV/°C to −0.28 mV/°C, where the current varies from 0.5 mA to 1 A. Although the injection of lower currents leads to a higher change rate (absolute value), it becomes non-linear at high temperatures, as shown in Fig. 9. In most applications, the load current is normally much higher than the currents in Fig. 9. In this case, the power converter should be stopped first to allow the low current injection to estimate the junction temperature. This may be not easy to implement. Nonetheless, online current injection and voltage

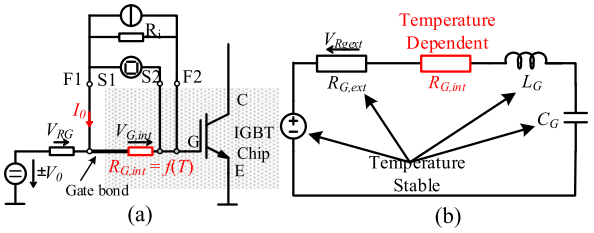

FIGURE 10. Temperature estimation using the resistance $R_{G,int}$: (a)$R_{G,int}$ measurement circuit [72] and (b) gate driver RLC network [71].

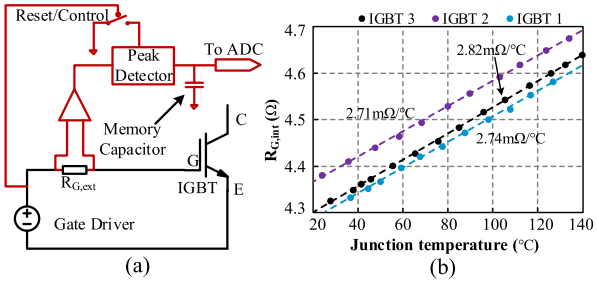

FIGURE 11. Temperature estimation using the resistance $R_{G,int}$: (a) gate peak voltage detection circuit and (b) calibration between$R_{G,int}$ andT_j [71].

drop measurement strategies have been proposed in [68], [70]. However, the injection and measurement window may decrease system performance. It should be noted that the low current should be injected to measure the voltage $V_{ce,Ilow}$ immediately, after the load current is suspended and the transient has passed. By doing so, the maximum error of the estimated junction temperature T_j caused by the cooling system can be reduced. The advantage of this method is that the self-heating effects can be avoided and the packaging degradation caused voltage drop is negligible.

c: TEMPERATURE ESTIMATION BY $R_{G,int}$

The thermo-sensitive resistance $R_{G,int}$ is a resistor in the center of the die. By calculating its temperature, the junction temperature T_j can be estimated. Nevertheless, it is almost impossible to implement the measurement during the converter operation without opening the module and adding measurement circuits, as shown in Fig. 10(a). To improve this, *Baker et al.* proposed a peak gate current method, where $R_{G,int}$ is considered as the equivalent series resistance (ESR) of both the gate-emitter capacitor C_{ge} and the gate-collector capacitor C_{gc}. Therefore, the gate driver *RLC* network can be depicted in Fig. 10(b) [71]. During the turn-on delay, both C_{ge} and C_{gc} are stable before the gate voltage reaches the threshold voltage V_{th}. The gate current I_g can be taken as a step response of the *RLC* network and the parasitic gate inductor should satisfy $R^2 > 4L/C$. Hence, the *RLC* network is overdamped, and I_g can be approximated by

$$I_g = \frac{V_{step}}{R_{G,int} + R_{ext}} e^{-\frac{t}{(R_{G,int}+R_{G,ext})C_g}}. \tag{9}$$

Given that the gate capacitance is stable, the gate inductor then has a negligible effect on the overdamped circuit. Assuming that the external resistor is not strongly dependent on the temperature, the resistance $R_{G,int}$ can be estimated by (10) when the peak gate current is detected.

$$R_{G,int} = \frac{V_{step}}{I_{peak}} - R_{G,ext} \tag{10}$$

It should be noted that the gate driver voltage is affected by the high dV_{ce}/dt and temperature. To create an exact step voltage, the difference between the gate voltage before ($V_{G,neg}$) and after turn-on ($V_{G,pos}$) is utilized. Considering that the voltage is easier to measure than the current, $V_{peak}/R_{G,ext}$ is used to calculate the peak current, where V_{peak} is the peak voltage on the external gate resistor. Fig. 11(a) shows the detection circuit for V_{peak} [71]. Finally, $R_{G,int}$ can be measured as

$$R_{G,int} = \frac{V_{G,neg} - V_{G,pos}}{\frac{V_{peak}}{R_{G,ext}}} - R_{G,ext}. \tag{11}$$

Then, with calibration, T_j can be estimated, as shown in Fig. 11 (b) [71]. There is a strong linear relationship between the resistance and the estimated temperature, as shown in Fig. 11(b). The advantage of this method is that it is immune to the load current and the measurement circuit can be integrated into the driver. Nevertheless, measurement errors may appear due to the assumptions.

d: TEMPERATURE ESTIMATION BY I_{sat}

If the self-heating effect is neglected, the IGBT saturation current can be calculated as [77]

$$I_{sat} = \left(1+\beta_{PNP}\left(T_j\right)\right) \frac{\mu_{ns}\left(T_j\right) C_{OX} Z_c}{2L_c} \cdot \left(V_{GS} - V_{th}\left(T_j\right)\right)^2 \tag{12}$$

where β_{PNP} indicates the PNP transistor current gain, μ_{ns} is the surface mobility of electron, C_{OX} denotes the oxide capacitance, Z_c is the channel width, and L_c is the channel length. It is nonlinear and there is the coupling with other thermo-sensitive parameters, as demonstrated in Fig. 12 [31]. Due to the nonlinearity and the coupling, it is not recommended to estimate T_j using the saturation current I_{sat}.

e: TEMPERATURE ESTIMATION BY I_{sc}

In [78], a short-circuit current-based estimation method is proposed. The short-circuit pulse is introduced by a bypass IGBT, as shown in Fig. 13(a). When the Device under Test (DUT) is on, the bypass IGBT will be triggered for a short time to create a short current pulse, whose amplitude is approximately linear in respect to the junction temperature T_j. By measuring the amplitude of the short-circuit current, T_j can be estimated, as exemplified in Fig. 13(b). This method has a relatively high sensitivity which is about −0.35 °C/A. Meanwhile, it is immune to the DC-link voltage. However, due to the risk of short-circuit, an additional protection scheme is required. Furthermore, additional control for the bypass IGBT and high-current sensor for the short-circuit pulse are needed to realize this.

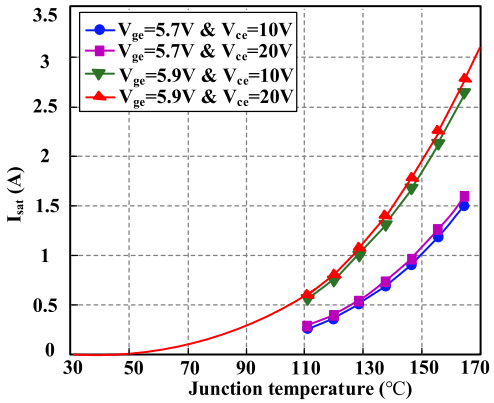

FIGURE 12. IGBT saturation current as a function of the temperature [31].

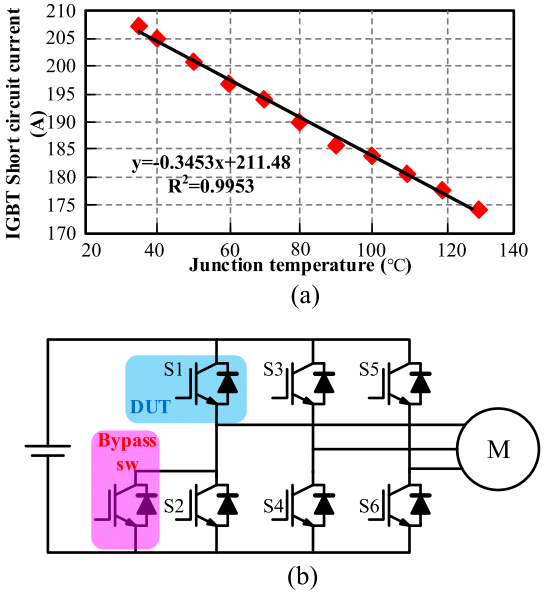

FIGURE 13. Junction temperature estimation using the short-circuit current Isc: (a) entire circuit diagram and (b) calibration between Isc and Tj [78].

f: TEMPERATURE ESTIMATION BY V_{ge}

The gate-emitter voltage V_{ge} is another TSEP for the junction temperature estimation. *Berning et al.* proposed a circuit to estimate T_j, as shown in Fig. 14(a) [91]. In order to eliminate the voltage spike induced by the oscillation-free gate resistor, the difference between the cathode voltage and the gate voltage is utilized. The results show good linearity and the sensitivity is within 11.6 mV/°C to 13 mV/°C, with the collector current being 1 A to 25 A., as shown in Fig. 14(b). However, this method is an offline approach, as the bias current source, consisting of a 62-V voltage source and a 75-kΩ resistor, will affect the normal conversion operation.

g: TEMPERATURE ESTIMATION BY V_{th}

The threshold voltage V_{th} of an IGBT is the gate-emitter voltage when the device begins to turn-on. According to [81],

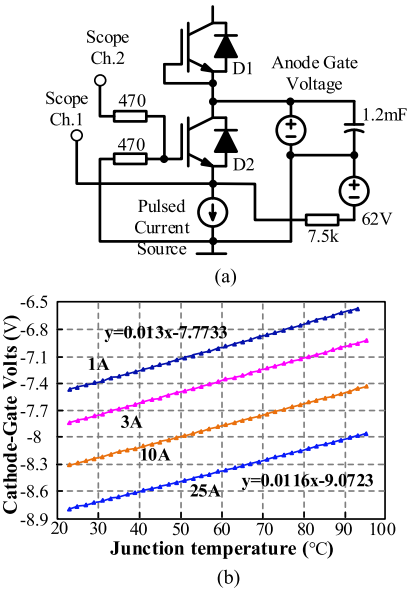

FIGURE 14. Temperature Estimation using the gate-emitter voltage V_{ge}: (a) cathode to gate voltage measurement circuit (b) calibration withT_j [91].

V_{th} can be described as

$$V_{th}\left(T_j\right) = \frac{\kappa}{q} \cdot \ln\left\{\frac{N_A}{N_D}\right\} \cdot T_j - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} + \frac{\sqrt{4 \cdot \varepsilon_{Si} \cdot N_A \cdot \kappa}}{C_{ox}} \cdot \sqrt{\ln\left\{\frac{N_A}{n_i\left(T_j\right)}\right\} \cdot T_j} \quad (13)$$

in which κ is the Boltzmann constant, q denotes the elementary charge, N_A indicates the concentration of acceptors, N_D implies concentration of donors, Q_f is the fixed oxide charge, Q_m is the charge of mobile ions, Q_{ot} indicates the intrinsic charge within the oxide, C_{ox} denotes area specific capacity of the oxide layer, ε_{Si} indicates permittivity of silicon, and n_i is intrinsic carrier density.

From (13), it can be found that V_{th} only depends on the junction temperature T_j, as all the other parameters are fixed. However, it is not strictly linear. Fortunately, in the range of operating temperatures, the relationship is nearly linear. In this case, V_{th} decreases linearly with the temperature due to the positive correlation between n_i and T_j. The sensitivity varies from −6 mV/°C to −9 mV/°C in different conditions [81], [92].

In order to measure V_{th} online, the parasitic inductance $L_{\sigma E}$ between the Kelvin and power emitter terminals is utilized, as discussed in [81], [82], [83] (see Fig. 15(b)). When the IGBT starts to turn-on and the current begins to flow through $L_{\sigma E}$, the parasitic voltage $V_{EE'}$ is induced. Then, by comparing $V_{EE'}$ with the reference voltage, the trigger pulse is produced. With NAND-gates and the driver output voltage, the measurement pulse is generated, which can enable the sample-and-hold (SH) gate to hold V_{th} and disable the SH when the freewheeling diode is on. This measurement circuit can be integrated into the gate driver due to the common ground reference. However, the reference voltage should be

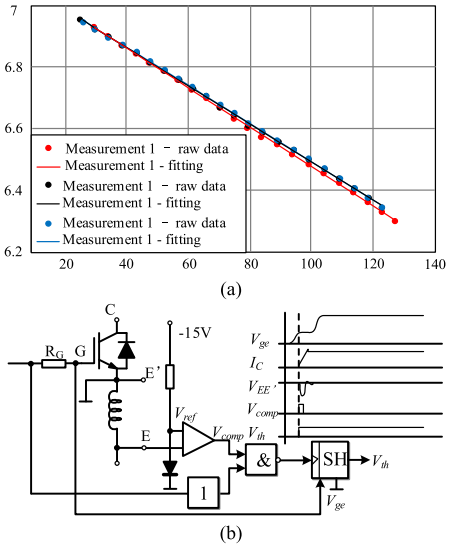

FIGURE 15. Temperature estimation using V_{th}: (a) calibration with T_j (b) measurement circuit [81], [82], [92].

set carefully. Otherwise, V_{th} may not be measured as the turn-on transient is also relevant to the junction temperature.

h: TEMPERATURE ESTIMATION BY V_{gp}

The Miller-plateau voltage V_{gp} can be calculated by (14) [84].

$$V_{gp}(T_j) = \sqrt{\frac{I_c}{g_m(T_j)}} + V_{th}(T_j) \tag{14}$$

where g_m is the trans-conductance. Since V_{th} decreases and g_m increases with the rise of the temperature, it can be concluded that V_{gp} decreases monotonically with the temperature rise. In practice, it is difficult to measure V_{gp} because $R_{G,int}$ is inaccessible. Thus, one has to estimate V_{gp} through V_{meas} by (15).

$$\begin{cases} V_{meas} = V_{gp} + \Delta V \\ \Delta V = (V_d - V_{gp}) \cdot \dfrac{x}{1+x} \text{ with } x = \dfrac{R_{G,int}}{R_{G,ext}} \end{cases} \tag{15}$$

Note that $R_{G,int}$ is temperature dependent, the compensation must be made before using it to estimate T_j. According to the sensitive and error analysis, the precise knowledge of g_m is crucial for the estimation. However, the small error of the current is acceptable which implies that the averaged phase current utilized in the control software is applicable here. The comparison between the prediction and the sensing results for a hybrid IGBT module FS800R07A2E3B13 is given in Fig. 16. The sensitivity is 1.5 to 7 mV/K over the entire operating range. Consider the fact that it is affected by the load current, the current dependency should be understood first. Otherwise, it must work at the same current, which limits its application.

i: TEMPERATURE ESTIMATION BY t_{don}

The turn-on delay t_{don} is the time between the start of the gate-emitter voltage V_{ge} rising and the beginning of the collect

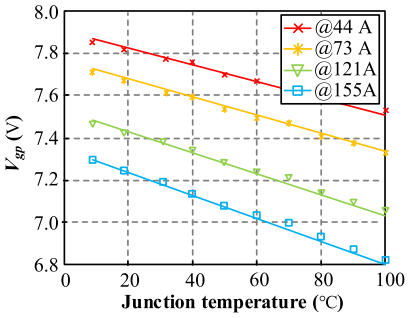

FIGURE 16. Comparison between the prediction and the sensing results of V_{gp} method [84].

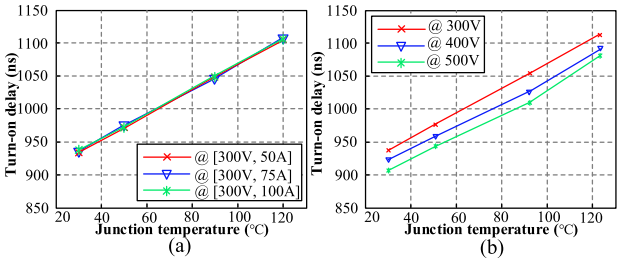

FIGURE 17. Temperature estimation using t_{don} under different: (a) currents and (b) voltages (same current) [85].

current I_c rising. It can be described as [85]

$$t_{don} = \left(R_{G,ext} + R_{G,int}\right) \cdot C_g \cdot ln\left(1 - \frac{V_{th}}{\Delta U}\right). \tag{16}$$

As aforementioned, $R_{G,int}$ increases and V_{th} decreases with the increase of the junction temperature T_j. As a result, t_{don} is sensitive to the junction temperature. More specifically, it increases with the rise of temperature when the temperature effect of C_g is neglected. When referring to the dependency, V_{th} only depends on T_j and $R_{G,int}$ is only affected by T_j. As for C_g, it consists of the oxide capacitance C_{ox} and depletion capacitance C_{dep}. C_{ox} can be seen as a constant, while C_{dep} is governed by

$$C_{dep} = A\sqrt{\frac{\varepsilon \cdot e_0}{2 \cdot V_{ce}} \cdot \frac{N_A \cdot N_D}{N_A + N_D}} \tag{17}$$

where A represents the surface area of the capacitor and e_0 indicates the unit charge. It is dependent on the DC-link voltage V_{dc} [85]. In addition, the intrinsic carrier concentration increases at higher temperatures, which indicates that C_{dep} increases along with the temperature increase. Therefore, t_{don} is monotonically temperature-dependent and it is affected by V_{dc}. However, it is immune to the load current. Consider that V_{dc} is almost kept constant, this method is more applicable than the current-dependent methods. The delay time t_{don} versus the junction temperature T_j is depicted in Fig. 17, and the sensitivity of T_j is about 2 ns/°C.

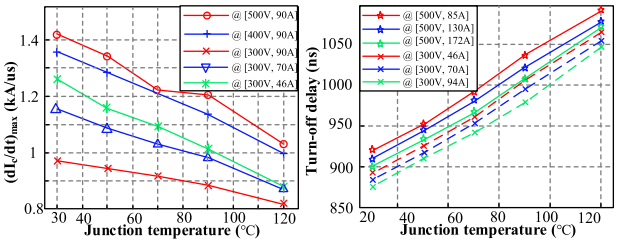

FIGURE 18. Temperature estimation using: (a)$dI_c/dt_{max,on}$and (b)t_{off} [85].

j: TEMPERATURE ESTIMATION BY $dI_c/dt_{max,on}$

The turn-on current slope is related to the gate-emitter voltage change rate as

$$\frac{dI_c/dt}{dV_{ge}/dt} = \underbrace{\left(\frac{1}{1-\alpha_{PNP}(T)}\right)}_{PNP\ transistor} \cdot \underbrace{\left[\mu\,(T)\cdot C_{ox}\cdot\frac{W}{L}\cdot\left(u_{ge}-V_{th}\,(T)\right)\right]}_{MOSFET} \quad (18)$$

where α_{PNP} is the gain of the inherent bipolar transistor, μ is the mobility, W is the width, and L is the length of the MOS channel. According to (16), the temperature-dependence caused by α_{PNP}, μ and V_{th} on $dI_c/dt_{max,on}$ can be obtained [85]. The correlation between $dI_c/dt_{max,on}$ and T_j under different currents and voltages is shown in Fig. 18(a). The relation is not as linear as the TSEPs above. As for the sensitivity, it is about 40 A/(μs·°C), which is affected by the DC-link voltage and load current.

k: TEMPERATURE ESTIMATION BY t_{off}

Equation (19) gives the description of the turn-off time t_{off} [82]. As it contains g_m and V_{th}– both decrease with the increase of the junction temperature T_j, the turn-off time t_{off} is also a TSEP. The correlation between t_{off} and T_j under different currents and voltages is shown in Fig. 18(b).

$$t_{off} = R_G \cdot C_{ISS} \cdot ln\left(\frac{I_C}{g_m\,(T)\,V_{th}\,(T)}+1\right) \quad (19)$$

where R represents the gate resistance and C_{ISS} is the input capacitance.

l: TEMPERATURE ESTIMATION BY t_{doff}

The turn-off delay t_{doff} can be divided into three parts, denoted as Δt_1, Δt_2, and Δt_3, which are shown in Fig. 19 and described as (20)∼(22) [87].

$$\Delta t_1 = R_G\,(T)\,C_{ge} + C_{gc} ln \frac{V_{gon}-V_{goff}}{V_{gp}\,(T)-V_{goff}} \quad (20)$$

$$\Delta t_2 = \frac{L_M q n_{ac}}{\Delta J_{ch}} \quad (21)$$

$$\Delta t_3 = \sqrt{\frac{2\cdot\varepsilon\cdot q\cdot V_{dc}}{N_B+\frac{J_c}{qv_{ce}}}}\cdot\frac{1}{\frac{\Delta J_{ch}}{qn_{drl}}} \quad (22)$$

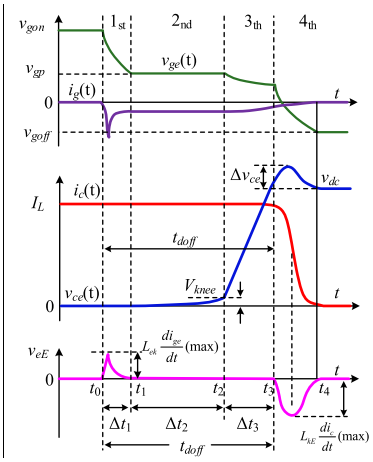

FIGURE 19. IGBT turn-off characteristics with module parasitic inductors [78].

where V_{gp} is the Miller-Plateau voltage, L_M presents the half physical length under gate region, n_{ac} denotes carrier concentration, J_c is the collector current density, and ΔJ_{ch} indicates the electron current density reduction in the MOS channel under the gate region.

As shown in (18), the first stage – Δt_1 is mainly affected by R_G and V_{gp}. Consider that both of them have positive temperature coefficients, R_G and V_{gp} increase with the rising junction temperature T_j, and similarly, Δt_1 increases. For Δt_2 and Δt_3, when T_j increases, α_{PNP} and n_{drl} increase at the same time [93], [94]. In addition, ΔJ_{ch} can be described as

$$\Delta J_{ch} = \frac{2\Delta V_{ge}\sqrt{(1-\alpha_{PNP})\,K_c I_c}}{A_c} = \frac{(1-\alpha_{PNP})\,g_m \Delta V_{ge}}{A_c} \quad (23)$$

implying that it decreases with the temperature rise. Therefore, Δt_2 and Δt_3 will increase when the junction temperature T_j rises.

Due to the reason that Δt_1, Δt_2 and Δt_3 increase with T_j, the turn-off delay t_{doff} increases monotonically, when T_j goes up. Further, it can be found from (18)∼(20) that t_{doff} is also affected by the load current and DC-link voltage. The correlation between t_{doff} and T_j under different load currents and voltages is shown in Fig. 20. It indicates that the sensitivity is about 4 ns/°C. However, it varies slightly according to the load currents and DC-link voltages. In Fig. 19, it can be found that there are voltage pulses across $L_{\sigma E}$ at the beginning and the end of the turn-off delay, both of which can be utilized to measure t_{doff}.

m: TEMPERATURE ESTIMATION BY $V_{EE'max}$

In the turn-off period, the negative voltage pulse across $L_{\sigma E}$ is induced by the drop of I_c, which can be described as [88]

$$V_{EE'} = -L_{\sigma E}\cdot\left.\frac{dI_c}{dt}\right|_{max} \quad (24)$$

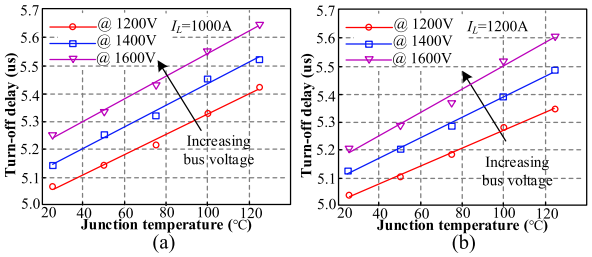

FIGURE 20. Correlation between t_{doff} and T_j under different voltages: (a) 1000-A load current and (b) 1200-A load current [87].

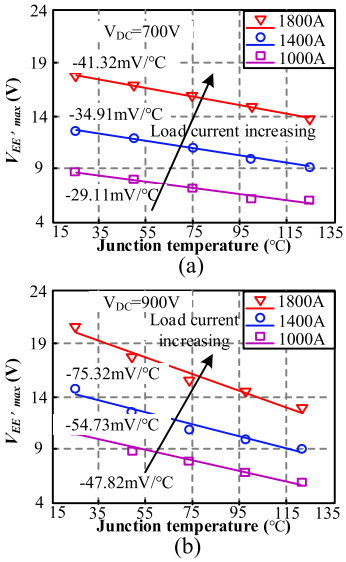

FIGURE 21. Correlation between $V_{EE',max}$ and T_j under different currents: (a)V_{dc} = 700 V and (b)V_{dc} = 900 V [88].

where $V_{EE'}$ is the voltage between the Kelvin emitter and power emitter.

Hence, instead of measuring $dI/dt_{max,on}$, the maximum voltage $V_{EE',max}$ can also be used to estimate the junction temperature. The correlation between $V_{EE',max}$ and T_j under different load currents and voltages is depicted in Fig. 21. The sensitivity varies from −29.11 mV/°C to −74.72 mV/°C, depending on the DC-link current and load current. In [89], T_j with respect to the $V_{EE',max}$ and I_c is modelled through least-squares fitting in the form of (25). Hence, it could be more practicable in the real-time T_j estimation.

$$T_j = \frac{1}{AI_c + B}\left(V_{EE',max} + C + D \cdot I_c + E \cdot I^2\right) \quad (25)$$

n: TEMPERATURE ESTIMATION BY V_{fb}

The temperature dependence of V_{fb} could be attributed to the ionic contaminants induced mobile oxide charges Q_{ox} which changes with temperature [90]. Thus, according to (26), V_{fb}

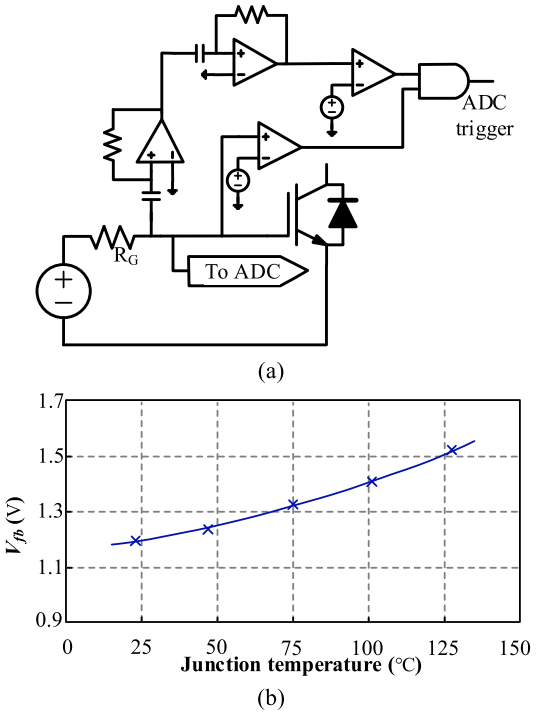

FIGURE 22. (a) Vfb measuring circuit (b) different values of Vfb at different temperature [90].

is a TSEP.

$$\Delta V_{fb} = \frac{\Delta Q_{ox}}{C_{ox}} \quad (26)$$

The measuring circuit and the different values of V_{fb} are given in Fig. 22(a) and Fig. 22(b), respectively [90]. The gate capacitance reduces sharply when the gate voltage reaches V_{fb} due to the depletion capacitor is added in series with the oxide capacitor. As a result, the gate voltage increases faster before it reaches V_{th}. Two differentiators and two comparators are utilized to capture this moment and trigger the ADC to sample V_{fb} at this time. The results of an Infineon FF1000R17IE4 module is given in Fig. 22(b) with the sensitivity at about 3.1 mV/°C. It turns out that the temperature dependency of V_{fb} is not strictly linear, which may limit the practical performance. Nevertheless, its advantage is that it is measured before the device conducting the load current, i.e., it can work well under different working condition.

The above methods to estimate T_j are further benchmarked in TABLE 3, in terms of online performance, selectivity, linearity, sensitivity, additional hardware, effects on converter performance, and integrability. The selectivity represents the factors that can affect TSEPs. Due to the DC-link voltage is kept as constant in most cases, the collector current is the main factor that influences the estimation performance. The accurate current measurement may require additional expensive current sensors, which increases the costs. In this sense, the $R_{G,int}$ and V_{fb} methods outperform the rest methods. The linearity shows the theoretical accuracy of the estimation

TABLE 3. Comparison of different junction temperature estimation methods.

Classification	TSEP	Online	Selectivity	Linearity	Sensitivity	Additional hardware For online measurement*	Effects on converter	Integrability
Static TSEPs	$V_{ce,Ihigh}$ [15, 64-67]	Yes	T_j, I_c	Medium	1 ~ 5 mV/°C	Same with $V_{ce,on}$ online methods	Maybe	No
	$V_{ce,Ilow}$ [31, 40, 67-70]	Yes	T_j	High	-0.19 ~ -0.28 mV/°C	Current source; V_{ce} measurement; Additional control	Yes	No
	$R_{G,int}$ [71-73]	Yes	T_j	High	0.9 ~ 2.8 mΩ/°C	Amplifier; Peak detector; reset switch	No	Yes
	I_{sat} [74-77]	Yes	T_j, V_{dc}	Not	——	Additional sensor	No	No
	I_{sc} [78]	Yes	T_j, V_{dc}	Medium	-0.35 °C/A	Additional protection circuit; Bypass IGBT; High current sensor;	Yes	No
	V_{ge} [79]	No	T_j, V_{dc}, I_c	High	11.6 ~ 13 mV/°C	——	——	No
Dynamic TSEPs	V_{th} [31, 49, 80-83]	Yes	T_j	High	-6 ~ -9 mV/°C	Amplifier; NAND-gates; Sample-and-hold gate	No	Yes
	V_{gp} [84]	Yes	T_j, I_c	Medium	1.5 ~ 7 mV/°C	Not mentioned	No	Yes
	V_{fb} [90]	Yes	T_j	Low	3.1 mV/°C	Differentiator; Comparator; AND gate	No	Yes
	t_{don} [85]	Yes	T_j, V_{dc}	High	2 ns/°C		No	Yes
	$dI/dt_{max,on}$ [85]	Yes	T_j, I_c, V_{dc}	Low	40 A/(μs·°C)	Not mentioned, but could be measured through parasitic inductance between the Kelvin and power emitter terminals	No	Yes
	t_{off} [85, 86]	Yes	T_j, I_c, V_{dc}	Medium	2 ns/°C		No	Yes
	t_{doff} [87]	Yes	T_j, I_c, V_{dc}	High	4 ns/°C		No	Yes
	$V_{EE'max}$ [88, 89]	Yes	T_j, I_c, V_{dc}	High	-29.11 ~ -74.72 mV/°C		No	Yes

* All methods require the ADC

method, where the higher linearity leads to higher accuracy. The sensitivity is a derivative of the TSEPs concerning T_j. A higher sensitivity indicates the larger variation of TSEPs with the same junction temperature rise, which can deal with noise and measurement errors. Additional hardware evaluates the cost of the corresponding estimation method. It can be concluded from TABLE 3 that the TSEPs measured through the gate or auxiliary terminals are much cheaper because they are free of the high voltage or current. Normally, they can be integrated into the gate driver at the same time. Thus, this kind of TESPs has greater potential in commercial products. The converter performance effect indicates if the performance would be affected by the TSEP measurement. Another concern of T_j estimation by TSEPs is that most TSEPs are affected by the device degradation. For example, the parasitic inductance and gate capacitance vary with the fatigue of the package and gate oxide, which could lead to significant errors of the gate- or auxiliary-terminal-based methods. In this sense, $V_{ce,Ilow}$ method has advantages because the sensing current is such low that the voltage deviation caused by the package degradation is negligible.

3) MONITORING THE JUNCTION-TO-CASE THERMAL RESISTANCE R_{thjc}

The junction-to-case thermal resistance R_{thjc} can be calculated as

$$R_{thjc} = \frac{T_j - T_c}{P_{loss}} \tag{27}$$

where T_j is the junction temperature that can be estimated by TSEPs, T_c is the case temperature that can be measured directly, and P_{loss} denotes the power loss, including the switching loss and conduction loss. The power loss P_{loss} can be obtained online with a predefined lookup table [45], [57] or curve-fitted model from datasheet [95], [96]. Then, the variation of the calculated R_{thjc} can be monitored.

Furthermore, ΔR_{thjc} indicates the degradation of the IGBT to a certain extent. Hence, *Dawei et al.* use ΔR_{th} to monitor the solder fatigue with a case-above-ambient temperature [45]. By calibrating P_{tot} with different working points for the healthy IGBT, the power loss response-surface is obtained. In addition, a Cauer thermal network of the heatsink

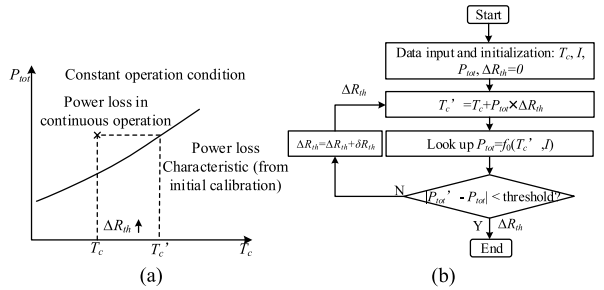

FIGURE 23. Using power losses to monitor the thermal resistance: (a) power losses vs. the case temperature and (b) flowchart to calculate the thermal resistance change ΔR_{th} [42].

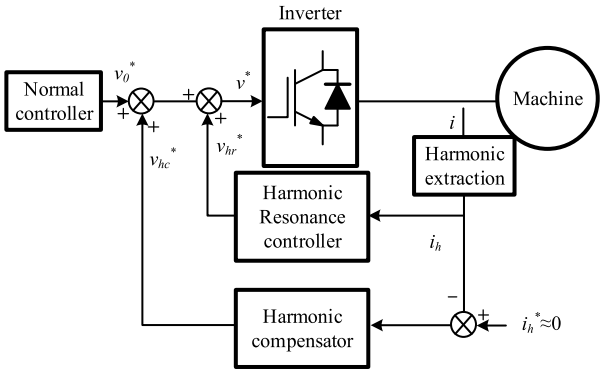

FIGURE 24. Control structure for the harmonic resonance and suppression to monitor device degradation [48].

is developed to calculate the real-time power loss with the case-to-ambient temperature. Besides, the solder fatigue will result in the resistance change ΔR_{th} between chip and substrate or between substrate and baseplate, depending on the solder layer type. Then, $V_{ce,on}$ rises with the subsequently increased T_j, which makes a higher power loss P_{tot}, as illustrated in Fig. 23(a). Finally, ΔR_{th} can be obtained through the flowchart shown in Fig. 23(b). However, it should be careful if the ambient temperature is measured accurately when other heat sources are presented in the application scenery.

Notably, the thermal resistance change ΔR_{th} is induced by the reduced thermal dissipation path. Consider the fact that the crack propagates from the edge to the center, the temperature of the case bottom surface declines while the temperature in the center of the case bottom surface increases [97]. This characteristic can be represented by the ratio of the junction-to-case-center thermal resistance to the junction-to-case-edge thermal resistance. Compared to R_{thjc} method, it is not cost-effective, while it eliminates the influence of the different operation points without all calibrations and is free of ambient temperature.

4) MONITORING THE 5th HARMONIC

The 5th-order harmonic voltage can be extracted by the converter controller without additional hardware, as shown in Fig. 24 and discussed in [48]. The inner-loop harmonic resonance controller amplifies the small error before and after IGBT ageing to enhance the measurement accuracy. In Fig. 24, v_{hc}^* is forced by the outer loop to follow the harmonics produced by the inverter, and then the harmonic voltage can be measured. This method is cost-effective, as it requires no additional hardware. However, the system should operate at the setpoint, which makes it difficult to measure the harmonic online. Additionally, the degraded IGBT cannot be identified as the degradation is detected at the system level, i.e., the confidential level of the identified degradation is low.

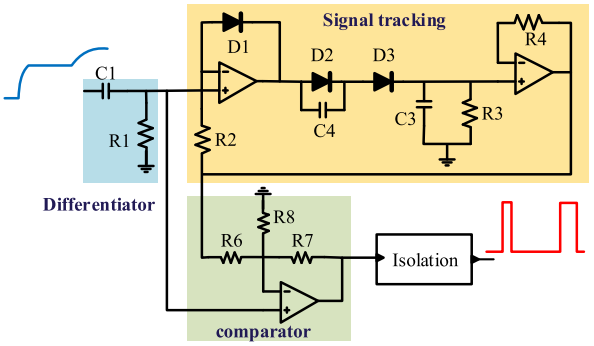

FIGURE 25. t_{gp} measurement circuitry [39].

5) MONITORING THE MILLER-PLATEAU DURATION T_{GP}

The circuitry that measures t_{gp} is shown in Fig. 25 [39]. The RC network receives the gate signal and outputs the differential results to provide the time instant before and after the Miller-plateau. Then, the signal tracking circuit and voltage divider R6, R7, R8 give the adaptive voltage reference for the comparator, so that the circuitry can work under different working points. Next, the output of the differentiator is compared to the adaptive voltage reference to generate the double-pulse signal which implies the information of t_{gp}. Finally, an isolator is used to separate the analogue circuit and digital circuit. There are some details should be noted in the measuring circuitry. First of all, C1 should be small enough so that the gate transients will not be influenced. Besides, R1 should be small enough to ensure high bandwidth and large enough to provide a detectable signal. Meanwhile, the time constant of the RC network should be smaller than 1/10 of t_{gp}. In fact, the measured time interval is not exactly the same with t_{gp}, while it is precise enough to monitor the state of the IGBT.

III. TOLERANCE OF THE CATASTROPHIC FAILURES

The catastrophic failure is caused by overstresses or wear-out, which makes the IGBT uncontrollable. It can be classified into open-circuit failure and short-circuit failure. Disconnections between the chip and terminal or the driver and the terminal may induce open-circuit failures. The former disconnection results from the bond-wire lift-off or bond-wire rupture under high short-circuit currents. In contrast, the latter is mainly caused by vibration, corrosion, and driver failures. The short-circuit failures may be the consequences

of high gate voltages, external failures, latch-up and rapid increases of intrinsic temperatures due to the second breakdown or energy shock, high voltage breakdown or thermal runaway [13]. Short-circuit failures can occur during turn-on transients or on-state operation, which is related to the above mechanisms.

As the focus of this paper is to provide the reliability improvement methods for two-level IGBT-based converters, only this kind of converters are considered below.

A. OPEN-CIRCUIT FAULT DIAGNOSIS METHODS

The diagnosis is to create an indicator or a group of indicators with different combinations under various conditions (healthy and different kinds of open-circuit faults). By identifying the relationship between the indicators and the faults, fault detection and isolation can be achieved. This can be a model-based approach, a signal-based approach or a data-driven approach.

1) MODEL-BASED APPROACH

The model-based approach mainly utilizes the difference between the analytical model and the real system after faults, which follows:

a) Establishing the mathematical model of the converter by means of Switching state function model (SSFM), state-space model (SSM), mixed logical dynamic model (MLDM), model reference adaptive system (MRAS), and so on.
b) Monitoring the current or voltage by a closed-loop or open-loop observer, and comparing the monitored values with the measurements to generate residuals or to directly observe residuals.
c) Performing the diagnosis by mapping the residuals to the fault indicators.

a: SWITCHING STATE FUNCTION MODEL [98]–[100]

Denoting S_k $(k = a, b, c)$ as the switching state function. $S_k =$ 1means the upper IGBT turns on while the lower one turns off and the opposite for $S_k = 0$. Then, the phase voltage can be expressed in (28). Under normal condition, the estimated phase voltage is close to the measured phase voltage and the voltage error $e_{kn} = 0$. Taking the measurement error, discretizing error, and non-ideal switching characteristics like switching delay and dead time into consideration, e_{kn} is not strictly equal to 0. Thus, the voltage threshold h and time threshold T are adopted to avoid the false alarms, which are given as $h = 10$V and $T = 50T_s$. Where T_s is the switching period [98], [99].

$$V_{kn,est} = S_k \cdot V_{dc} \tag{28}$$

For a rectifier, however, the phase-to-phase voltage can be expressed in (29).

$$u_{xy,est} = e_{xy} - i_{xy}R_s - L_s\frac{di_{xy}}{dt} \quad x, y \in (a, b, c),\ x \neq y \tag{29}$$

TABLE 4. Fault diagnostic information.

State	Switching state errors	Faulty switch	Faulty phase
Normal	ε_{ab}=ε_{bc}=ε_{ca}	None	
Faulty	$\varepsilon_{ab} > T_{th}$, $\varepsilon_{bc} = 0$, $\varepsilon_{ca} < -T_{th}$	T_1	a
	$\varepsilon_{ab} < -T_{th}$, $\varepsilon_{bc} = 0$, $\varepsilon_{ca} > T_{th}$	T_4	
	$\varepsilon_{ab} < -T_{th}$, $\varepsilon_{bc} > T_{th}$, $\varepsilon_{ca} = 0$	T_2	b
	$\varepsilon_{ab} > T_{th}$, $\varepsilon_{bc} < -T_{th}$, $\varepsilon_{ca} = 0$	T_5	
	$\varepsilon_{ab} = 0$, $\varepsilon_{bc} < -T_{th}$, $\varepsilon_{ca} > T_{th}$	T_3	c
	$\varepsilon_{ab} = 0$, $\varepsilon_{bc} > T_{th}$, $\varepsilon_{ca} < -T_{th}$	T_6	

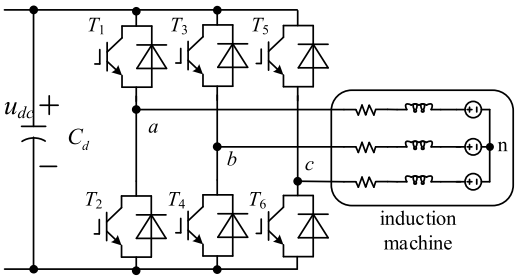

FIGURE 26. Simplified model of two-level VSI fed induction machine drive system.

where $u_{xy,est}$ is the estimated phase-to-phase rectifier voltage and e_{xy} represents the phase-to-phase grid voltage. Then, the switching state and the corresponding error can be estimated by (30).

$$\begin{cases} S_{xy,est} = \dfrac{u_{xy,est}}{V_{dc}} \\ \varepsilon_{xy} = S_{xy} - S_{xy,est} \end{cases} \tag{30}$$

Thus, if T_1 fault happens, switch state error for phase A will be 1 while the errors for the rest two phases are 0. This leads to ε_{ab} greater than the threshold T_{th}, ε_{ca} smaller than $-T_{th}$ and $\varepsilon_{bc} = 0$. Accordingly, all the single switch fault can be diagnosed through TABLE 4 [100].

b: STATE-SPACE MODEL [101]–[106]

As the state model is application-dependent, the two-level voltage source inverter fed induction machine drive system (see Fig. 26) is taken as an example for illustration purpose. It can be described by

$$\begin{cases} \dot{x} = Ax + g(x) + Bu + DT_L \\ y = Cx \end{cases} \tag{31}$$

with

$$A = \begin{bmatrix} -c & 0 & ab & 0 & 0 \\ 0 & -c & 0 & ab & 0 \\ aL_m & 0 & -a & 0 & 0 \\ 0 & aL_m & 0 & -a & 0 \\ 0 & 0 & 0 & 0 & -kf \end{bmatrix},$$

TABLE 5. Relationship between the faulty switch and residual direction.

Faulty switch	T_1	T_2	T_3	T_4	T_5	T_6
Dedicated residual	r_{a-}	r_{a+}	r_{b-}	r_{b+}	r_{c-}	r_{c+}

$$g(x) = \begin{bmatrix} n_p b \lambda_{qr} \omega_m \\ -n_p b \lambda_{dr} \omega_m \\ -n_p b \lambda_{qr} \omega_m \\ -n_p b \lambda_{dr} \omega_m \\ m\left(i_{qs}\lambda_{dr} - i_{ds}\lambda_{qr}\right) \end{bmatrix}$$

$$B = \begin{bmatrix} d & 0 & 0 & 0 & 0 \\ 0 & d & 0 & 0 & 0 \end{bmatrix}^{\mathrm{T}},$$

$$D = \begin{bmatrix} 0 & 0 & 0 & 0 & k \end{bmatrix}^{\mathrm{T}},$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

where L_s and L_r are the stator and rotor self-inductance, L_m denotes the mutual inductance, R_s and R_r indicate the stator and rotor resistance, J is the inertia, f represents the mechanical fiction, i_{ds} and i_{qs} are the stator current in the d- and q-axis, λ_{dr} and λ_{qr} are the rotor flux in the d- and q-axis, ω_m is the motor speed, T_L is the load torque, $a = R_r/L_r$, $b = L_m/\sigma L_s L_r$, $c = L_m^2 R_r/\sigma L_s L_r^2 + R_s/\sigma L_s$, $m = 3n_p L_m/2JL_r$, $d = 1/\sigma L_s$, $k = 1/J$, $\sigma = 1 - L_m^2/L_s L_r$, state vector $x = [i_{ds}, i_{qs}, \lambda_{dr}, \lambda_{qr}, w_m]^{\mathrm{T}}$, input $u = [u_d, u_q]^{\mathrm{T}}$, output $y = [i_{ds}, i_{qs}, w_m]^{\mathrm{T}}$.

Taking the Luenberger observer [88] as an example (other observers, e.g., PI observer, can also be adopted), the stator current in the dq-frame can be observed by

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + g\left(\hat{x}\right) + Bu + DT_L + K_o\left(y - \hat{y}\right) \\ \hat{y} = C\hat{x} \end{cases} \tag{32}$$

Then, the residuals can be obtained as

$$\begin{bmatrix} r_d \\ r_q \end{bmatrix} = \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} - \begin{bmatrix} \hat{i}_{ds} \\ \hat{i}_{qs} \end{bmatrix} \tag{33}$$

If the residual exceeds the threshold, a fault can be detected. For the fault isolation, i.e., to identify the faulty switch, the direction of the threshold is utilized. With three unitary actuator directions in the abc-frame $e_a = [1, 0, 0]$, $e_b = [0, 1, 0]$, $e_c = [0, 0, 1]$, six fault directions can be established as $v_{a+} = ([\mathbf{T}_{abc}]e_a/[\mathbf{T}_{abc}]e_a)$, $v_{a-} = -([\mathbf{T}_{abc}]e_a/[\mathbf{T}_{abc}]e_a)$, $v_{b+} = ([\mathbf{T}_{abc}]e_b/[\mathbf{T}_{abc}]e_b)$, $v_{b-} = -([\mathbf{T}_{abc}]e_b/[\mathbf{T}_{abc}]e_b)$, $v_{c+} = ([\mathbf{T}_{abc}]e_c/[\mathbf{T}_{abc}]e_c)$, $v_{c-} = -([\mathbf{T}_{abc}]e_c/[\mathbf{T}_{abc}]e_c)$. Here, $[\mathbf{T}_{abc}]$ represents the abc-dq transformation. TABLE 5 shows the relationship between the faulty switch and residual direction. It should be noted that false fault recognitions might be avoided, as the direction of each fault indicator is 60-degree apart from others.

Similar to the Luenberger observer, the first-order sliding mode observer can also be utilized with the form of (34) [106].

$$\dot{\hat{x}} = A\hat{x} + Bu + \Lambda I_s \tag{34}$$

where Λ represents the observer gain and I_s is the switching vector.

The ratio r_n of the mean absolute value of measured current and observed current can be calculated in (35). For the normal condition, the ratio is close to 1 because the two currents are almost identical to each other. For one-switch fault condition, however, the ratio is calculated in (36), indicating r_n is smaller than 0.318. As for the open-phase condition, the measured current approaches to 0 and r_n is about equal to 0. Hence, the fault can be detected when r_n is smaller than a threshold K_d.

$$r_n = \frac{\int |i_n| dt}{\int \left|\hat{i}_n\right| dt} \tag{35}$$

$$r_n = \frac{I_m/\pi}{|e_n|} \approx \frac{1}{\pi} = 0.318 \tag{36}$$

where e_n is the faulty component in the observed current which is close to the measured current maximum amplitude I_m.

The fault identification indicator s_n is defined in (37). When it is normal, the mean value of the observed current is close to 0, and thus, s_n is equal to 0. When an open-switch fault occurs, the observed fault component provides a DC bias which makes the observed current totally positive or negative. Hence, s_n equals to 1 for upper switch fault and -1 for lower switch fault.

$$s_n = \frac{\int \hat{i}_n dt}{\int \left|\hat{i}_n\right| dt} \tag{37}$$

c: MIXED LOGICAL DYNAMIC MODEL [16], [107], [108]

For a three-phase two-level converter, it can also be described by

$$v_{ag} = V_{dc}\delta_1, \quad \delta_1 = \bar{s}_2\left(s_1 + \bar{\delta}_a\right) \tag{38}$$

$$v_{bg} = V_{dc}\delta_2, \quad \delta_2 = \bar{s}_4\left(s_3 + \bar{\delta}_b\right) \tag{39}$$

$$v_{cg} = V_{dc}\delta_3, \quad \delta_3 = \bar{s}_6\left(s_5 + \bar{\delta}_c\right) \tag{40}$$

where v_{kg} is the voltage between the phase k ($k = a, b, c$) and the negative pole of the DC-link, $s_1 \sim s_6$ represent the control signal of the corresponding IGBT, V_{dc} denotes the DC-link voltage, and δ_k represents the current direction of each phase (positive if flowing into the load).

Then, the converter can be represented by the mixed logical dynamic model following

$$u_{kn} = Ri_k + L\frac{di_k}{dt} + e_k \quad (k = a, b, c) \tag{41}$$

$$\begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix} = \frac{1}{3}\boldsymbol{K}\begin{bmatrix} u_{ag} \\ u_{bg} \\ u_{cg} \end{bmatrix}, \quad \boldsymbol{K} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \tag{42}$$

$$\dot{\boldsymbol{i}} = \boldsymbol{A}\boldsymbol{i} + \boldsymbol{B}_1\boldsymbol{e} + \boldsymbol{B}_2\boldsymbol{\delta} \tag{43}$$

TABLE 6. Relationship between faulty switches and residual vector phase.

Faulty switches	γ	Faulty switches	γ
Normal	-	T_4	$2\pi/3$
T_1	π	T_3 and T_4	$2\pi/3$, $5\pi/3$
T_2	0	T_5	$\pi/3$
T_1 and T_2	0, π	T_6	$4\pi/3$
T_3	$5\pi/3$	T_5 and T_6	$\pi/3$,

where u_{kn} is the voltage between the phase k and the neutral point of the load, R and L are the load resistance and inductance for each phase, e_k denotes the back electromotive force (EMF) for each phase, $\boldsymbol{i} = [i_a, i_b, i_c]^{\mathrm{T}}$, $\boldsymbol{A}$ = -$\boldsymbol{RI}$/L with $\boldsymbol{I}$ being an identity matrix, $\boldsymbol{B}_1$ = -$\boldsymbol{I}$/L, $\boldsymbol{e} = [e_a, e_b, e_c]^{\mathrm{T}}$, $\boldsymbol{B}_2 = V_{dc}\boldsymbol{K}/3L$, and $\delta = [\delta_1, \delta_2, \delta_3]^{\mathrm{T}}$ is the discrete input as shown in (38) $\sim$ (40).

Accordingly, the open-loop observer based on the mixed logical dynamic model can be described as

$$\dot{\hat{\boldsymbol{i}}} = \boldsymbol{A}\hat{\boldsymbol{i}} + \boldsymbol{B}_1\boldsymbol{e} + \boldsymbol{B}_2\boldsymbol{\delta} \tag{44}$$

Subsequently, the residual is generated as

$$\boldsymbol{i} - \hat{\boldsymbol{i}} = \dot{\tilde{\boldsymbol{i}}} = \boldsymbol{A}\tilde{\boldsymbol{i}} + \boldsymbol{B}_2\,(\boldsymbol{\delta}' - \boldsymbol{\delta}) \tag{45}$$

where $\boldsymbol{\delta}'$ denotes the discrete input of the real plant (considering the control signal of the open-circuit IGBT as 0), and $\boldsymbol{\delta}$ is the discrete input for the observer (generated by the controller). Finally, the fault can be detected if the residual exceeds the threshold and the fault type can be recognized according to the residual vector phase as shown in (46) and TABLE 6.

$$\tilde{i}_\alpha = \tilde{i}_a, \quad \tilde{i}_\beta = \tilde{i}_a + 2\tilde{i}_b/\sqrt{3}, \quad \tilde{\boldsymbol{I}} = \tilde{i}_\alpha + j\,\tilde{i}_\beta = \tilde{I}e^{j\gamma} \tag{46}$$

$$\begin{cases} T_1\ fault:\ C_1 = \bar{\delta}s_1\bar{s}_4C \\ T_2\ fault:\ C_1 = \bar{\delta}s_2\bar{s}_3C \\ T_3\ fault:\ C_1 = \bar{\delta}s_3\bar{s}_2C \\ T_4\ fault:\ C_1 = \bar{\delta}s_4\bar{s}_1C. \end{cases}, \quad C = \frac{d\tilde{i}_N}{dt}\cdot\frac{L_N}{U_d} \tag{47}$$

Nevertheless, when applying this method to a single-phase converter, the diagonal IGBTs cannot be separated unless extra operations are performed to the converter [107]. In order to settle this problem, the changing rate of the residual is adopted to identify the faults, as shown in (47). By adding the switch information to the fault indicators, all the fault types can be identified without extra operations.

d: MODEL REFERENCE ADAPTIVE SYSTEM [109]

For a permanent magnet synchronous motor drive system with a 2-level converter, as shown in Fig. 23, current dynamics in the dq-frame including the open-circuit-induced voltage distortions can be represented by

$$\begin{bmatrix} \dot{i}_q \\ \dot{i}_d \end{bmatrix} = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega_m \\ \omega_m & -\dfrac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} v_q + \Delta v_{q_dist} \\ v_d + \Delta v_{d_dist} \end{bmatrix} + \begin{bmatrix} -\dfrac{\lambda_m\omega_m}{L_s} \\ 0 \end{bmatrix} \tag{48}$$

where λ_m is the flux linkage established by the permanent magnet.

For this reference model, it assumed that the voltage distortions are zero in a healthy model. Thus, it can be described as

$$\begin{bmatrix} \dot{i}_{qm} \\ \dot{i}_{dm} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_s}{L_s} & -\omega_m \\ \omega_m & -\dfrac{R_s}{L_s} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} v_q^* \\ v_d^* \end{bmatrix} + \begin{bmatrix} -\dfrac{\lambda_m\omega_m}{L_s} \\ 0 \end{bmatrix}. \tag{49}$$

Combining (48) and (49), the voltage distortions caused by the open-circuit fault can be obtained as

$$\begin{cases} \Delta v_{q_dist} = L_s\left(\dot{i}_q - \dot{i}_{qm}\right) \\ \Delta v_{d_dist} = L_s\left(\dot{i}_d - \dot{i}_{dm}\right) \end{cases} \tag{50}$$

Considering the dead-time effect, the threshold voltage is selected as $V_{threshold} = m \times V_{dead}$ with m being a positive constant that can minimise the noise/dead-time effect induced false error detection and V_{dead} being voltage distortion caused by the dead-time effect. By transforming Δv_{q_dist} and Δv_{d_dist} to the variables in the abc-frame, the Boolean errors can be obtained as

$$\varepsilon_k = \begin{cases} 1, & \Delta v_{k_dist} > V_{threshold}:\ error \\ 0, & \left|\Delta v_{k_dist}\right| < V_{threshold}:\ normal \\ -1 & \Delta v_{k_dist} < -V_{threshold}:\ error. \end{cases} \tag{51}$$

Based on (51), the faulty switch can be recognized though TABLE 7.

TABLE 7. Relationship between faulty switches and boolean errors.

Faulty switch	ε_a	ε_b	ε_c
T_1	-1	1	1
T_2	1	-1	1
T_3	1	1	-1
T_4	1	-1	-1
T_5	-1	1	-1
T_6	-1	-1	1

Overall, the model-based methods can detect and identify single-switch open fault and phase open fault effectively. Yet its ability to diagnose the double-switch fault has not been reported, which requires further investigations.

2) SIGNAL-BASED APPROACH

Normally, the signal-based approach utilizes the intrinsic characteristic of the faulty converter, which means that the current or voltage behaves differently under healthy and faulty conditions, including the current trajectory pattern,

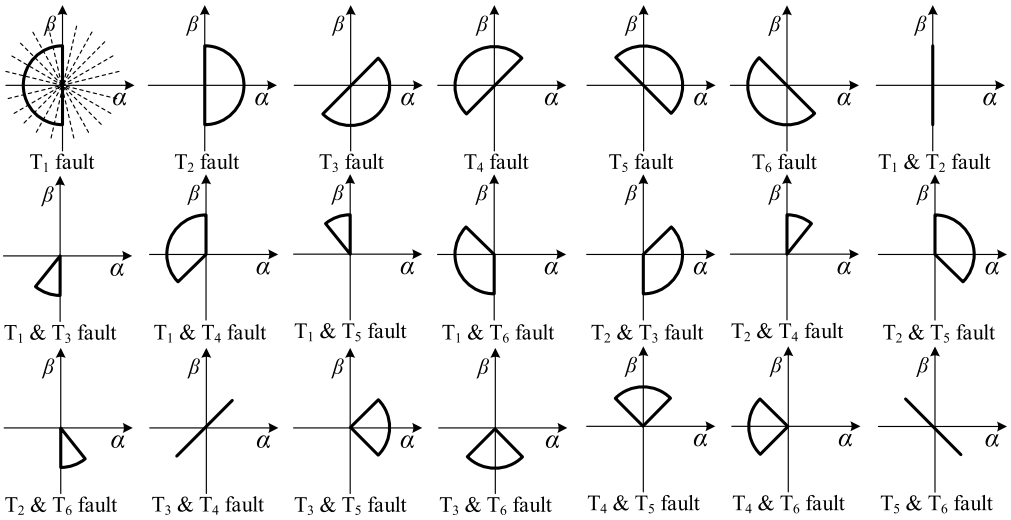

FIGURE 27. Current trajectories in the α β-plane under different open-circuit faults [111].

the mean current (DC current), the reference value and the current distortion. Thus, those signals are employed to identify the faults.

a: CURRENT PATTERN [110]–[112]

The $\alpha\beta$ components of AC currents can be obtained through the Clarke transformation as

$$\begin{cases} i_\alpha = \dfrac{1}{3}\left(2i_a - i_b - i_c\right) \\ i_\beta = \dfrac{1}{\sqrt{3}}\left(i_b - i_c\right). \end{cases} \tag{52}$$

In a healthy condition, the current trajectory in the $\alpha\beta$-plane is a circle. When one or two IGBTs are in the open-circuit fault mode, the trajectory deviates from the circle to become a sector. Depending on the fault type, the sector has different sizes and angles, as demonstrated in Fig. 27. Therefore, the current trajectory pattern recognition can be one way to detect and identify the fault type.

The easiest way to recognize the fault pattern is to calculate the slope of the $\alpha\beta$-current as

$$\psi = \frac{i_{\alpha k} - i_{\alpha k-1}}{i_{\beta k}} - i_{\beta_{k-1}} \tag{53}$$

where i_{jk} and i_{jk-1} represent the sampling at k and $k-1$ instant ($j = \alpha, \beta$). However, it is only effective for the one-switch fault case. Also, it is not able to distinguish the two faulty switches in the same leg. An extra measure that is used to detect the missing half of the phase current is needed to identify the faulty switch, as shown in Fig. 27.

Alternatively, the entire circle can be divided into 24 sections. Define a 24-dimensional vector whose value is given as follows. If the fault pattern vector is in one section, the corresponding element in the vector is denoted as 1. Otherwise, it is -1. Because the fault patterns are different, each fault has a unique identification vector, based on which the faulty switch can be recognized.

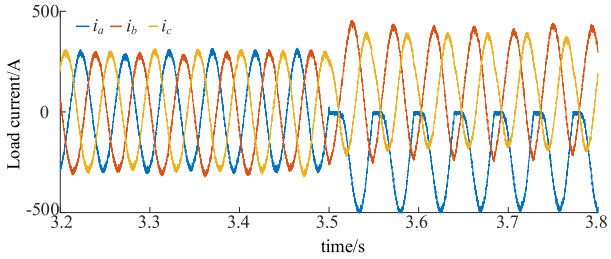

FIGURE 28. Three-phase current under T1 fault.

Additionally, the sector size, the mass center angle, and the difference between the maximum angle and the minimum angle of the sector can also be utilized to identify the faulty switch. In this case, the normalized current is recommended to eliminate the load effects on the sector size, which is given as

$$i_{\alpha_nrm} = \frac{i_\alpha}{\sqrt{i_\alpha^2 + i_\beta^2}}, \quad i_{\beta_nrm} = \frac{i_\beta}{\sqrt{i_\alpha^2 + i_\beta^2}} \tag{54}$$

b: MEAN CURRENT [113]–[121]

If one IGBT is in the open-circuit fault, the three-phase current of the vector-controlled drive system is shown in Fig. 28. The positive half-cycle disappears when the upper IGBT of the corresponding phase is faulty; the lower IGBT fault leads to the disappearance of the negative half-cycle. As a result, the other two phase currents are offset with a DC component because of the regulation of the controller. Consequently, the faulty IGBT can be identified by the polarity of the three-phase current, as summarized in TABLE 8. Nevertheless, this method is not effective under multiple-fault conditions.

The normalized mean current and an auxiliary variable are introduced in [114], which eliminate the load effects and

TABLE 8. Relationship between the three-phase current polarity and the corresponding faulty IGBT.

Phase A	Phase B	Phase C	Faulty IGBT
−	+	+	T_1
+	−	−	T_2
+	−	+	T_3
−	+	−	T_4
+	+	−	T_5
−	−	+	T_6

enable the multi-fault diagnosis.

$$\begin{cases} R_n(k) = \underbrace{\dfrac{\langle i_n(k)\rangle}{\langle |i_n(k)|\rangle}}_{D_n(k)} \cdot \underbrace{\langle w_n(k)\rangle}_{W_n(k)} \\ w_n(k) = \begin{cases} 1, & if \ \ |i_n(k)| \le K_0 \\ 0, & otherwise \end{cases} \end{cases} \tag{55}$$

$$S_n(k) = \frac{2 \cdot \langle |i_n(k)|\rangle}{\langle |i_l(k)|\rangle + \langle |i_m(k)|\rangle} \tag{56}$$

where $\langle\cdot\rangle$ means the average value, K_0 denotes the threshold voltage that is set as 5% of the rated current, $l, m, n \in$ (a, b, c) with $l \neq m \neq n$, and S_n is the auxiliary variable defined as two times the ratio between the mean absolute value of the target phase, and that of the sum of the rest two phases.

Besides, $D_n(k)$ is defined as the normalized mean current and $W_n(k)$ is the long interval of near-zero currents, and then, $S_n(k)$ is utilized to overcome the ill-condition of $R_n(k)$ when two faults are in the same leg. Combining $R_n(k)$ and $S_n(k)$, in total, 27 kinds of faults can be diagnosed. Consider that the current frequency in the drive system is varying according to the motor speed, the variable parameter moving average method is adopted to calculate the mean value adaptively [121].

Alternatively, the normalized current can be given as

$$i_{nN} = \frac{i_n}{\sqrt{i_\alpha^2 + i_\beta^2}}. \tag{57}$$

Under normal conditions, the mean value of the average normalized current can be calculated as

$$\langle |i_{nN}| \rangle = \frac{\omega_s}{2\pi} \int_0^{\frac{2\pi}{\omega_s}} |i_{nN}|\, dt = \frac{1}{\pi}\sqrt{\frac{8}{3}} \approx 0.5198 \tag{58}$$

where ω_s is the current frequency. When an open-circuit fault occurs in the system, one of $\langle |i_{nN}| \rangle$ will be larger than 0.5198, and thus, the fault can be detected. However, $\langle |i_{nN}| \rangle$ carries only the phase information, and that is, the faulty IGBT cannot be identified. Therefore, the mean value of the normalized current should be considered. By classifying $\langle |i_{nN}| \rangle$ into 4 stages and $\langle i_{nN} \rangle$ into positive and negative states, all single- and double-switch fault conditions can be properly detected and identified [115]. Consider that the diagnostic algorithm may not be reliable when the current approach to zero, $\langle i_{nN} \rangle$ is calculated only when the current is larger than 2% of the rated current in [118]. Nevertheless, the fault under low current may be missed. It is recommended in [120] that the inverse absolute phase current can be used to avoid this problem, as shown in (59). Notably, the absolute mean value of the angle of deviation of the Clarke trajectory $\langle |\phi| \rangle$ can be added into the diagnostic system to prevent it from false alarms and to enhance its robustness [117].

$$\left\langle \frac{1}{|i_N|} \right\rangle, \ \begin{cases} i_N = i_N, & |i_N| \ge \xi \\ i_N = \xi, & |i_N| < \xi \end{cases} \tag{59}$$

Apart from the open-switch fault, the intermittent faults which caused by electromagnetic interference or components ageing also exist in industrial applications. In this case, fuzzy logic can be used to identify the faults effectively [119].

However, it must be pointed out that double-switch faults, involving two upper (or two lower) transistor failure, and triple faults, involving also the lower (upper) transistor in the remaining leg, are indistinguishable. For example, the double fault of T_1 and T_3 is indistinguishable from the triple fault of T_1, T_3, and T_6. Besides, the triple-switch fault with two switches in the same leg and the quadruple-switch fault with two healthy switches on the opposite sides of different legs are indistinguishable. For example, the triple-switch fault of T_1, T_2 and T_3 cannot be distinguished from the triple-switch fault of T_1, T_2 and T_6, nor can it be distinguished from the quadruple-switch fault of T_1, T_2, T_3 and T_6.

c: REFERENCE VALUE [122], [123]

If an open-circuit fault in a three-phase two-level converter occurs, some switch combinations of the converter cannot be reached. As a result, errors are produced, since the reference value cannot be tracked perfectly. Further, the controller will try to overcome this by adjusting the reference. With those considerations, the current and voltage reference values can be utilized to diagnose the faults. For instance, if T_1 is faulty (open-circuit fault), the positive half-cycle is zero. Then, the phase-A mean reference current error normalized by the mean absolute value of the current (d_a) can be calculated as

$$\begin{aligned} d_a &= \frac{\langle i_a^* - i_a \rangle}{\langle |i_a| \rangle} \\ &= \frac{\frac{\omega_s}{2\pi}\int_0^{\frac{2\pi}{\omega_s}} I_m \sin(\omega_s t)dt - \frac{\omega_s}{2\pi}\int_{\frac{\pi}{\omega_s}}^{\frac{2\pi}{\omega_s}} I_m \sin(\omega_s t)dt}{\frac{\omega_s}{2\pi}\int_{\frac{\pi}{\omega_s}}^{\frac{2\pi}{\omega_s}} -I_m \sin(\omega_s t)dt} = 1 \end{aligned} \tag{60}$$

where I_m is the current amplitude.

It is also true for other IGBT faulty conditions. However, it cannot identify the phase open condition, and again, (56) is adopted to solve this issue.

d: CURRENT DISTORTION [124]

As mentioned earlier that the IGBT open switch fault will lead to the disappearance of the positive or negative half cycle

of the phase current. On this basis, fault detection can be realised by a zero-crossing detector. Then, by identifying the increasing or decreasing trends of all the phases, the single switch fault can be recognized [124].

It can be found that the signal-based methods are rather simple that only requires a few mathematical operations. This makes it easy to integrate them into the control unit as only a little calculation resource needed. It also worth to point out that both single and double switch faults can be diagnosed by this approach.

3) DATA-DRIVEN APPROACH

The data-driven methods do not require the precise model of the target system. It fulfils the fault detection and localization by means of machine learning. The first step of these methods is to extract the fault features which include the wavelet coefficients, wavelet energy, raw currents, etc. Then, they will be fed to the artificial neural network, which could be the conventional BP neural network or emerging deep network, for training. At last, the well-trained network will be used to finish the open-switch fault diagnosis. It should be pointed out this approach requires the huge scale of data.

a: FEATURE EXTRACTION

The most basic fault feature is the phase current itself with a certain length. In [125], 150 sampling points are acquired with the sampling frequency of 900 Hz to train the network. The length of the current for the diagnostic accuracy for a random vector functional network (RVFL) has been discussed in [126], which shows high accuracy can be achieved if the current length exceeds 60 ms. Besides, the double chain quantum genetic algorithm can be utilized to optimise the current length and the denoising sparse autoencoder can extract the fault feature automatically [127], [128]. In [129], each phase current is shifted by 120 degrees and 240 degrees and performed the Clark transformation to generate the direct currents in d-q axis. Wavelet decomposition is another widely adopted method to extract the fault feature in both time- and frequency-domain. The coefficients of each detail part are used in [130] and the number of decomposition level is determined by the sampling frequency and signal frequency. On the other hand, the energy of each detail part is calculated after the decomposition, after which the principal component analysis is used to reduce the feature dimension. Thus, the training efficiency can be improved [131].

b: NETWORKS

The BP neural network is the most common one in the literature which consists of one hidden layer [129], [130]. Nevertheless, the performance of the BP neural network is not so satisfying. For example, further steps have to be performed on the outputs of the BP neural network to confirm the fault diagnosis results in some cases [129]. Ensemble learning is an optional solution to improve the performance of neural networks. A classifier that consists of 200 single trained RVFL is constructed to diagnose the IGBT open-switch fault in a converter in [126]. Combining with the decision-making process, e.g., the voting process, the faulty IGBT can be detected and identified. Alternatively, the performance can also be improved through the deep network. The 7-hidden-layer sparse autoencoder based deep neural network and 128-hidden-layer long short-term memory network have been proved to be able to provide accurate diagnostic results [125], [128].

The comparison of the above methods is given in TABLE 9 in terms of the diagnostic time, load independency, and complexity. Note that the diagnostic time of the data-driven methods are not given because they are not performed in the control unit like other methods do, i.e., the data are transmitted to the host PC to finish the diagnosis. Meanwhile, it implies that the data-driven approach is more complex than the other two approaches. The huge scale data requirement is another bottleneck for some applications. Its advantage lies in that so long as the different condition data are fed to train the network, it can provide reliable diagnostic results. The diagnostic time of both model-based and signal-based methods are comparable and both of them are simple enough to be integrated into the control unit. However, the signal-based methods are less dependent on the load variation because the normalization will be performed before the diagnostic process. So far, it seems that more papers are focused on signal-based methods and deep learning methods in recent years. The reason could be the simplicity and the effectiveness of the former one and the potential for big data application for the later one.

B. SHORT-CIRCUIT FAULT DETECTION METHODS

The short-circuit fault can be categorised into the hard switch fault (HSF) and the fault-under-load (FUL) [132]. The HSF is referred to as the case when the IGBT is turned-on under short-circuit conditions, while the FUL occurs when the IGBT is on under normal conditions. For the normal conditions, V_{ce} is still high, I_c is zero and V_{ge} starts to increase. At this point, I_g mainly charges C_{ge}, as C_{gc} is much smaller than C_{ge} because of the small C_{dep}. When V_{ge} reaches V_{th}, I_g begins to increase until it rises to the load current and V_{ce} keeps dropping toward the saturation voltage. Then, C_{gc} becomes large, and charged by I_g, which causes the so-called Miller plateau. After that, V_{ge} goes up to the gate input voltage V_D and V_{ce} reaches $V_{ce,on}$. Under the HSF condition, however, V_{ce} cannot be changed, which keeps C_{gc} small. Consequently, the Miller plateau of V_{ge} disappears. Meanwhile, I_c rises fast to the short-circuit current. When the FUL occurs under an on-state IGBT, I_c increases sharply, which causes the IGBT to quite the saturation region and V_{ce} rises quickly from $V_{ce,on}$ to V_{dc}. Therefore, C_{gc} goes back to a small value and the displacement current from C_{gc} to the gate circuit is produced, which increases V_{ge}. The characteristics of the normal, HSF, and FUL conditions are described in Fig. 29, based on which the short-circuit can be detected.

TABLE 9. Comparison of open-circuit fault diagnosis methods.

Approach	Methods	Time	Load independency	Complexity
Model-based approach	SSFM [98-100]	<1~8 ms	low	low
	SSM [101-106]	19 ms	high	low
	MLDM [16,107,108]	8 ms	high	low
	MRAS [109]	0.91 ms	medium	medium
Signal-based approach	Current pattern [110-112]	20 ms	low	low
	Mean current [113-121]	1.3 ms	low	low
	Reference value [122, 123]	10 ms	low	low
	Current distortion [124]	——	medium	medium
Data-driven approach	BP network [129, 130]	——	Low	high
	Ensemble learning [126]	——	Low	high
	Deep learning [125, 128]	——	Low	high

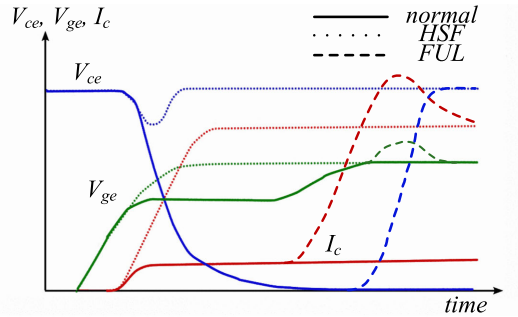

FIGURE 29. Characteristics of the IGBT short-circuit [135].

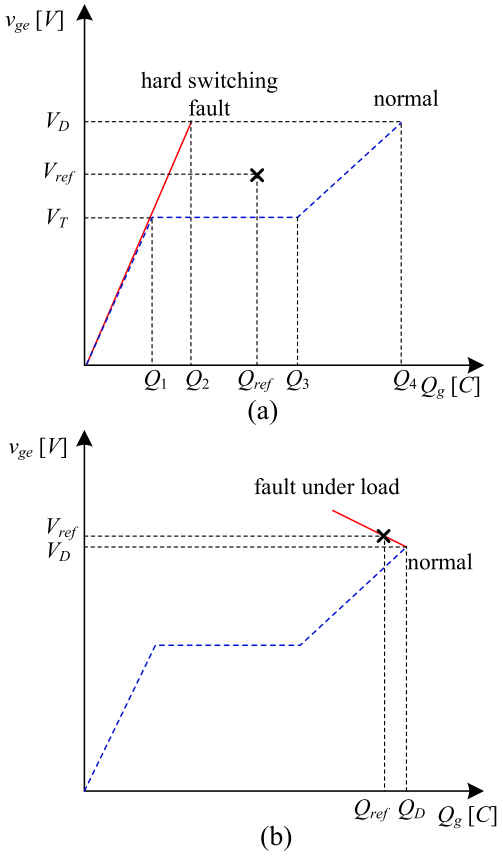

FIGURE 30. Short-circuit detection circuit based on the Miller plateau [138].

1) GATE-BASED APPROACH

a: GATE CHARGE METHOD [133]– [136]

According to the above analysis, the gate charge characteristics under normal conditions and short-circuit fault conditions can be obtained as Fig. 30. Under the normal condition, the amount of gate charge is larger than that under the HSF condition, when V_{ge} is higher than the Miller plateau voltage V_{gp}, and that under the FUL condition when V_{ge} is higher than V_D. Therefore, the threshold voltage and charge can be set, as shown in Fig. 30. In this case, if both above V_{ref} and under Q_{ref} are met, the short-circuit fault can be confirmed. Fig. 31 shows the circuit of the above method. The voltage across the gate resistor is sampled by a differential amplifier and is integrated to obtain the gate charge. Then, it is fed to a comparator to check if it exceeds Q_{ref} or not. The gate-emitter voltage V_{ge} is compared with V_{ref} at Comparator1. Following, an AND gate is utilized to combine the two results to achieve the detection.

b: MILLER PLATEAU TIME METHOD [137], [138]

For the HSF, the Miller plateau disappears as shown in Fig. 29. Hence, the time difference between V_T and V_T+ 5V changes under the normal condition and short-circuit condition. The measurement circuit is shown in Fig. 32. Three amplifiers are adopted to obtain the gate-emitter voltage, which can eliminate the interference caused by the emitter inductance. Then, a hysteresis comparator circuit is utilized to generate the detection pulse. This pulse enables the capacitor to be charged when it is active. With different Miller plateau time, the capacitor has a differently charged voltage, which can represent the time difference. By comparing the capacitor voltage with the threshold, the HSF can be detected. Note that the FUL cannot be detected with this method.

c: GATE VOLTAGE METHOD WITH mILLER PLATEAU [139], [140]

It has been demonstrated earlier that the gate voltage will rise when the FUL happens. Thus, it could be a good indicator to

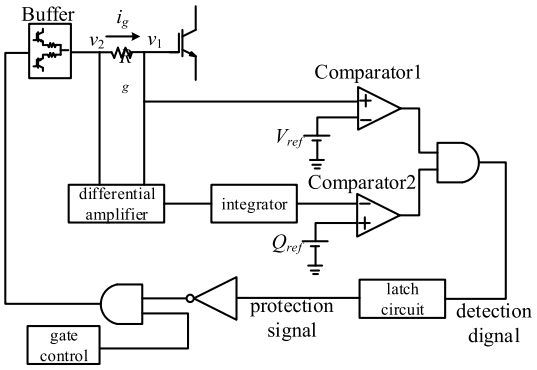

FIGURE 31. Short-circuit detection circuit by the gate voltage method with Miller plateau [140].

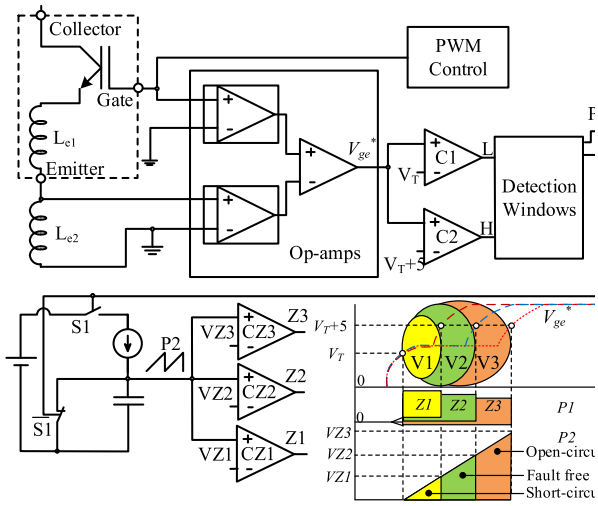

FIGURE 32. Gate charge characteristics under (a) HSF and (b) FUL [136].

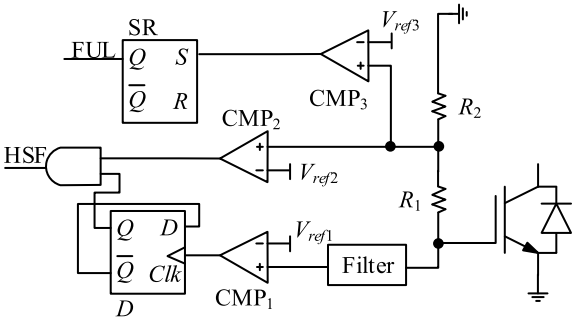

FIGURE 33. Short-circuit detection circuit based on the gate charge characteristic [136].

detect the FUL [141]. It is also true for the high short-circuit inductance case for the HSF because V_{ce} reduces significantly which cause the dV_{gc}/d_t, and thus, the current produced by the voltage variation increases the gate voltage. However, it will be not reliable for the low inductive HSF as V_{ce} reduces slightly [139]. Consequently, the gate voltage and the Miller plateau are combined to detect the short-circuit [139], [140]. The detecting circuit is given in Fig. 33. The gate voltage is

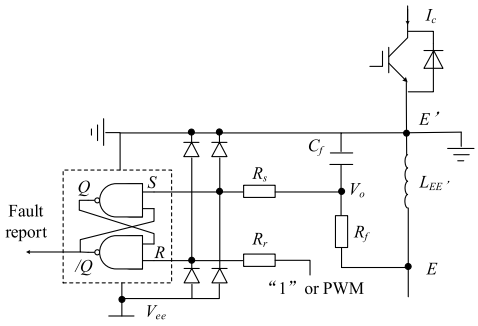

FIGURE 34. Detection circuit of the di/dt. [145].

fed to a filter which converts the two rising edges before and after the Miller plateau into two pulses. Then, the pulses drive the T flip-flop to generate a pulse under the normal operation, which will be latched high when HSF occurs. V_{ref2} is set as (61).

$$V_{ref2} = \frac{R_2}{R_1 + R_2} V_{gp,HSF} \tag{61}$$

where $V_{gp,HSF}$ is the Miller plateau voltage threshold under HSF condition.

Thus, both the outputs of CMP2 and T flip-flop are high when the HSF happens. Accordingly, the AND gate output a signal of HSF. V_{ref3} is set such that it exceeds the gate voltage supply V_D while smaller than the gate voltage under FUL $V_{ge,FUL}$. A possible value is given in (62). Hence, when the voltage drop across R_2 is higher than V_{ref3}, the FUL can be detected.

$$\frac{R_2}{R_1+R_2} V_D < V_{ref3} < \frac{R_2}{R_1+R_2} \times \left(V_D + R_G C_{gc} \frac{dV_{cg}}{dt} \right) \tag{62}$$

2) COLLECTOR-CURRENT-BASED APPROACH

It can be seen from Fig. 29 that the collector current I_c rises sharply to a high level under both the HSF and the FUL. Consequently, the current slop can be utilized to detect the short-circuit fault.

a: DIRECT METHOD [142]–[144]

In this method, the collect current I_c is measured directly by a direct current1-current transformer (DCCT). To achieve reliable detection results, three sample-and-hold (H/S) circuits that can generate two current slopes are adopted with two phase-shifted clocks 1 and 2 (clock 2 lags clock 1 by a half period). This configuration can sample two consecutive slops with the help of two different calculators. Then, comparing both the slopes with the threshold. If the slope exceeds the threshold continuously for two samples, the short-circuit of the IGBT can be determined. Alternatively, the current can also be measured by a shunt resistor [144]. By comparing the sensed voltage with a predefined threshold, the short circuit can be recognized. Another idea is to separate a small part from the main IGBT to form a so-called sense emitter, by which the user can measure the current easily [143].

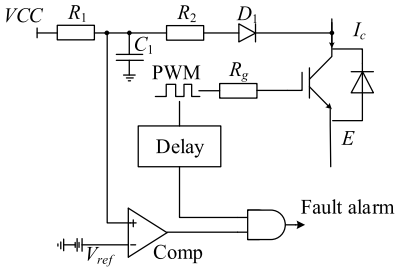

FIGURE 35. Short-circuit detection circuit by the de-saturation approach [150].

b: di/dt METHOD [145]–[148]

The costs of the direct methods are relatively high either for the user or the manufacturer. To reduce the cost, the *di/dt* methods, which get free from the high voltage, are introduced. It is well known that the current variation generates the magnetic flux intensity variation, and thus, the electromotive force will be produced in a coil nearby. A coil near the busbar and a printed circuit board Rogowski coil have been applied in [147], [148]. Also, the electromotive force can be integrated to obtain the current. Therefore, both the current change rate and the current amplitude can be utilized to detect the short-circuit fault. It should be careful with the common-mode voltage when measuring the electromotive force and the DC offset during integrating. The cost can be reduced further by making use of the auxiliary emitter according to [145]. The detection circuit is shown in Fig. 34. When the short-circuit occurs, the rapidly increased current leads to a voltage $V_{EE'}$ on the stray inductor between the power emitter E and Kelvin emitter E'. If an RC filter is applied in parallel with the stray inductance $L_{EE'}$, the transient steep short current can be described as

$$I_c(s) = V_o(s) \cdot \frac{R_f C_f + 1/s}{L_{EE'}} \approx V_o(s) \cdot \frac{R_f C_f}{L_{EE'}} \qquad (63)$$

where C_f, R_f and V_o are the filter capacitance, filter resistance, and output voltage of the filter, respectively. It can be found from (63) that I_c is proportional to V_o with constant C_f, R_f and $L_{EE'}$. Under the normal condition, the S-terminal of the R-S latch is in a high state. After the short-circuit, the S-terminal can reach the maximum allowable low-level input voltage of the latch circuit. Setting the R-terminal to "1" for a single mode and "PWM" for multiple modes, the fault can be detected.

3) DE-SATURATE-APPROACH [132], [149]–[152]

According to Fig. 29, the gate voltage is consistent with the collector-emitter voltage under the normal condition. When the short-circuit fault occurs, however, they are on different trends. With this concept, the fault detection circuit can be designed as Fig. 35.

The comparator is locked by an AND logic operator during the switch-off period. When the IGBT is turned-on, V_{ce} measured by the diode D1 is compared with the threshold voltage V_{ref}. Under the normal condition, the saturation voltage V_{ce} is quite low and V_{ref} is set higher than that. Thus, the AND gate outputs a "0" signal. If the short-circuit fault occurs at this time, IGBT will be out of the saturated region. Because the short current and V_{ce} will rise and rapidly exceed V_{ref}. Then, the fault is detected, and further protection measures will be implemented. However, it should be noted that the voltage V_{ce} will be higher than V_{ref} for a while during the turn-on transient when the AND gate is activated. To avoid false alarms, a delay is introduced, in such a way that the comparator remains locked before the voltage V_{ce} reaches $V_{ce,on}$.

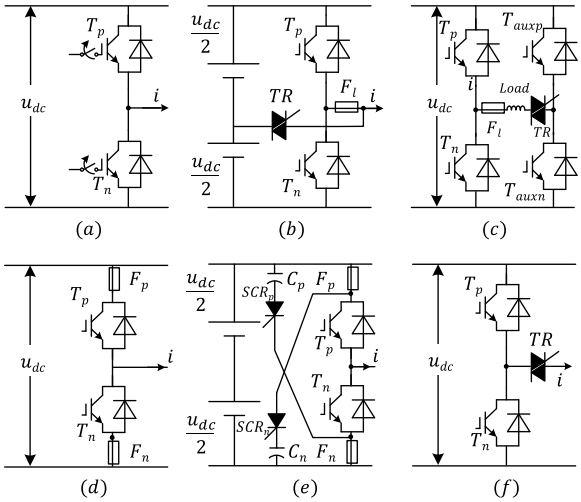

FIGURE 36. Fault isolation circuits: (a) removing gate signal method, (b) fuse-on-load method A, (c) fuse-on-load method B, (d) fuse-on-leg-method A, (d) fuse-on-leg method B and (f) no-fuse method.

The detection time, costs and detection performance of the above short-circuit detection methods are compared in TABLE 10. The gate-based and de-saturation methods are faster than the direct current method because they can finish the detection during the transient processes. In terms of the cost, it is obvious that the direct current method and the de-saturate method are more expensive due to the demand of the high current or voltage components. The gate-based approach and the auxiliary-emitter-based approach are preferred to detect the short circuit because of the fast diagnostic speed and low costs. However, the parasitic parameters variation caused by the degradation should be taken into consideration when setting the thresholds, by which false alarms can be avoided.

C. FAULT ISOLATION CIRCUIT

After a fault is detected, it should be isolated from the main circuit by the fault isolation circuit as soon as possible. Thus, the fault effect propagation can be limited. It is easy to isolate the open-circuit faults by blocking the corresponding gate signals of the faulty IGBTs, as shown in Fig. 36(a). For the short-circuit fault, however, fuses and potential additional components are required.

TABLE 10. Comparison of the short-circuit fault detection methods.

Utilised characteristic	Methods	Time	Cost	FUL detection	HSF detection
Gate transients	Gate charge method	2.8 us	Low	✓	✓
	Miller plateau time method	6 us	Low	✓	×
	Gate voltage method with Miller plateau	About 0.5 us	Low	✓	✓
Collector current	Direct method	9 us	High	✓	✓
	di/dt method	3 us	Low	✓	✓
De-saturate voltage	De-saturate method	2 us	Medium	✓	✓

1) FUSE-ON-LOAD METHOD [153]–[155]

The method isolates the faulty devices by blowing out the fuse. Fig. 36(b) shows a circuit that can deal with the single switch short-circuit fault. When assuming that T_p is shorted and has been detected by the short-circuit detection methods, the TRIAC TR will be triggered. As a result, the fuse F_l will be burned by the shoot-through current, and the faulty leg is isolated. The half DC-link voltage can be obtained through a split capacitor or auxiliary IGBT, depending on the fault-tolerant topology. However, because the fuse is on the load side, the one phase short fault cannot be cleared by this circuit. Fig. 36(c) presents a similar solution. By contrast, this circuit is dedicated to the neutral leg fault-tolerant topology. The load impedance should be low. Thus, the shoot-through current can be large enough to blow the fuse. It should also be pointed out that the current rating of the TRIAC should be high enough to survive under the shoot-through current.

2) FUSE-ON-LEG METHOD [156]–[158]

Fig. 36(d) and Fig. 36(e) show the isolation circuit with fuses on the converter leg. The circuit of Fig. 36(d) stops the PWM and triggers both switches on the faulty leg to blow out the fuses; while, the one of Fig. 36(e) triggers SCR_p and SCR_n on the faulty leg at the same time after the detection. Then, the capacitor charging current will blow the fuses to isolate the fault. In this sense, the value of the capacitance, the current rating of the thyristor and fuse should be selected carefully to ensure reliable isolation.

3) NO FUSE METHOD [159]

A fuse-free solution for isolation is given as Fig. 36(f). When a single switch short-circuit happens (say T_p is faulty), the complementary switch and the TRIAC will be turned-off after the detection. It has been discussed in [159] that the current in the faulty phase will reach zero crossing under this condition. Nevertheless, this circuit cannot handle the phase short-circuit fault.

TABLE 11 compares the complexity and isolation ability of the circuits shown in Fig. 36. Regarding the additional expenses, the cost of a standard two-level three-phase converter is taken as the base as 1-p.u., IGBT and TRIAC as 0.17-p.u., turns ratio adjusted IGBT as 0.10-p.u., capacitor as 0.42-p.u., thyristor as 0.09-p.u. and fuse as 0.09-p.u., and then the cost of all the isolation circuits can be calculated [160]. Considering the capability of isolating all kinds of faults, fuse-on-leg circuits are preferred. However, if the cost is taken into consideration, the circuit in Fig. 36 (d) is promising.

D. FAULT-TOLERANT TOPOLOGY

After the fault has been detected and isolated, the converter should be reconfigured to keep operating, which requires the fault-tolerant topology. Normally, this kind of topology is realised by redundancy for two-level three-phase converters.

1) CONVERTER-REDUNDANT TOPOLOGY [160]–[166]

In this topology, two converters are utilized to drive the motor, which are connected to the dual stator windings or cascaded to the stator winding (see Fig. 37 (a) and Fig. 37 (d)). If a fault occurs, the converter with a faulty switch will be blocked by the isolation circuit, and the healthy converter supplies power to the load. In this case, the trade-off between output power and system cost should be considered. It is assumed that the output voltage and current of the standard converter are 1-p.u.. For the dual stator windings load, the maximum voltage vector and current of the fault-tolerant topology are the same as those in the standard converter, if the turns ratio adjustment is not considered. Otherwise, the current will be reduced to 0.5-p.u., and the cost will decrease at the same time. The cascaded topology works as a two-phase full-bridge converter after faults, which can provide 1-p.u. voltage and 0.58 p.u. current without the turns ratio adjustment, and 0.5-p.u. voltage and 0.58-p.u. current with the turns ratio adjustment. Both of the two topologies require modifying the control.

2) LEG-REDUNDANT TOPOLOGY [153], [155]–[158], [167]–[171]

A fourth leg is adopted as a redundant phase in this topology, which is connected to the three legs through TRIACs, as shown in Fig. 37 (b). Under the normal condition, TRIACs are blocked and the additional leg is inactive. In the case of faulty conditions, the faulty leg will be disconnected by the fault isolation circuit, and the fourth leg will replace it by triggering the corresponding TRIAC. Thus, the system can still work as a three-phase two-level converter. At the same time, the gate signals of the faulty leg are moved to the fourth leg, and minor control modification is required. In this condition, the output current rating and voltage rating are the same as those in the standard converter.

TABLE 11. Comparison of different isolation circuits.

Circuit	Hardware for each leg				Cost	Isolation of			
	Fuse	Thyristor	Triac	Capacitor	(p.u.)	Switch open	Switch short	Phase open	Phase short
Gate signal off	0	0	0	0	0	✓	×	✓	×
No fuse	0	0	1	0	0.50	✓	✓	✓	×
Fuse-on-leg (Fig. 36 (d))	2	0	0	0	0.50	✓	✓	✓	✓
Fuse-on-leg (Fig. 36 (e))	2	2	0	2	2.33	✓	✓	✓	✓
Fuse-on-load	1	0	1	0	0.75	✓	✓	✓	×

N-No; L-Low; M-Medium; H-High; Cost of a standard converter = 1-p.u.

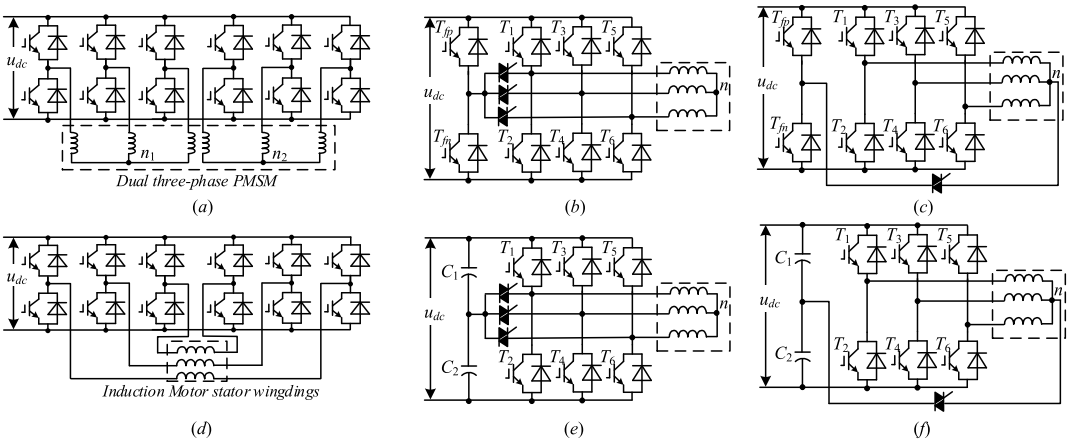

FIGURE 37. Fault-tolerant topologies: (a) converter-redundant topology A, (b) leg-redundant A, (c) leg-redundant B, (d) converter-redundant topology B, (e) split capacitor topology A, and (f) split capacitor topology B.

Another kind of leg-redundant topology connects the fourth leg to the neutral point of the load, which is shown in Fig. 37 (c). The TRIAC is activated after the fault is detected and isolated, by which the system operates as a two-phase full-bridge converter. In this case, the post-configuration with two-phase control can only provide 1-p.u. voltage and 0.58-p.u. current. It should be pointed out that the TRIAC will suffer 1.73 p.u. current because of the zero-sequence current.

3) SPLIT CAPACITOR TOPOLOGY [154], [159], [167], [169], [171]–[179]

The split capacitor topology is similar to the leg-redundant one (see Fig. 37 (e) and Fig. 37 (f)). There are also two connections available. The first one is to replace the faulty leg, working as a four-switch three-phase converter (see Fig. 37 (e)). The other one is connected to the neutral point of the load, working as a four-switch three-phase converter (see Fig. 37 (f)). The reconfiguration method is to trigger the TRIAC, which is identical to the leg-redundant topology. The benefit of this kind of topology is that the cost can be reduced. Nevertheless, the output is reduced. Additionally, the capacitor voltage unbalance should be considered in the control design phase and operation.

TABLE 12 compares the aforementioned fault-tolerant topologies. It should be noted that the isolation circuits are not considered in this comparison. Instead, the cost, output power, efficiency, reliability, and extra requirements of different topologies are focused on. The cost and output capacity are evaluated in p.u. values, with which the efficiency can be calculated by (64). The cost for the 1-p.u. system is the same as that in TABLE 11, and the output power for 1-p.u. is equal to that of the standard converter.

$$\eta = \frac{Output\ power}{Cost} \tag{64}$$

In terms of reliability, the percentage of mean time to failure (MTTF) is used, which is defined as the MTTF increase in the fault-tolerant topology over that of the standard converter. The operation condition is assumed to be identical to [153]. Therefore, the constant failure rates of IGBT and TRIAC are 7.236 and 0.8735 failures per 10^6 hours, respectively. Additionally, the current level factor of the TRIAC is considered, which yields 1.0881 failures per 10^6 hours for the neutral leg and four-switch two-phase topologies, and 0.7025 failures per 10^6 hours for the four-switch three-phase topology. Note that the current and voltage level factors are not considered in the failure rate of the IGBT. The reason is that it is a combination of MOSFET and BJT from the handbook [180]. The MTTF can be calculated by the Markov reliability model and the percentage of the extended MTTF (MTTF%) can be obtained with (65). The extra requirements in TABLE 12 include load type, neutral point accessibility of the load and control modification.

$$MTTF\% = \frac{MTTF_{tolerant} - MTTF_{standard}}{MTTF_{standard}} \tag{65}$$

TABLE 12. Comparison of fault-tolerant circuits.

redundancy	Topology	Cost (pu)	Output power (pu)	η	MTTF%	Special load	Load neutral access	Control modification
Converter redundancy	Dual wingding	2 (1.15*)	1 (0.5*)	0.50 (0.43*)	50%	Yes	No	No
	Cascaded converter	2 (1.15*)	0.58 (0.29*)	0.29 (0.25*)	50%	Yes	No	Yes
Leg redundancy	Fourth leg	1.83	1	0.55	98%	No	No	No
	Neutral leg	1.5	0.58	0.39	96%	No	Yes	yes
Split capacitor	Four-witch three-phase	1.5	0.58	0.39	147%	No	No	yes
	Four-witch two-phase	1.16	0.29	0.25	145%	No	Yes	yes

*- with turns ratio adjustment

Overall, Fig. 38 concludes the reviewed possible online methods that can ensure the reliability of the two-level power converters.

IV. COMPARISON BETWEEN CONDITION MONITORING AND FAULT TOLERANCE

The condition monitoring and the failure tolerance have been review above, both of which can ensure the reliable operation of power converters. However, the effectivenesses of the two approaches may differ according to different target applications. In this section, possible strategies for condition monitoring and failure tolerance will be given first. Then, they will be compared in different aspects, including maintenance availability, converter stress level, costs, mission importance, etc.

A. POSSIBLE STRATEGY FOR MONITORING AND TOLERANCE

It has been discussed in Section II and Section III that there are many ways to realize the condition monitoring and fault tolerance. Therefore, it is necessary to select a possible strategy for each of the solution to be compared.

1) MONITORING STRATEGY

A good monitoring strategy should be able to handle all the common degradations, which have been discussed in Section II. Considering that each degradation mechanism has more than one indicators, and each indicator has several extraction methods, the most cost-effective strategy should be investigated for condition monitoring. For the bond wire fatigue and metallization reconstruction, it can be found from TABLE 1 that $V_{ce,on}$ can be used for monitoring the two degradations. Hence, it is an efficient indicator. If the online performance is considered, it can be extracted either by the diode-based method or by the MOSFET-based method, depending on the applied voltage level and switching frequency. As for the gate oxide degradation, the Miller-plateau duration t_{gp} is preferred because it can monitor the bond wire and the gate oxide simultaneously. At the same time, the cost is low as it can be integrated into the gate driver. When it comes to solder fatigue, it can be monitored by R_{thjc}. The case temperature could be measured by a thermocouple while the junction temperature could be estimated by the V_{ceILow} which is immune to the packaging degradation. Thus, numerous benefits can be expected. Firstly, R_{thjc} is calculated without the effects of packaging degradation and solder fatigue can be monitored more effectively. Then, the temperature-dependent components of $V_{ce,on}$ can be compensated, which implies the states of the bond wire and the metallization can be evaluated accurately. Finally, consider the opposite effects of t_{gp} caused by bond wire fatigue and gate oxide degradation, simultaneous degradation of these two may lead to the unchanged t_{gp}. In this case, V_{ceILow} is only affected by gate oxide degradation, and the health state of the gate can be known. Accordingly, the bond wire state can be inferred easily.

2) TOLERANCE STRATEGY

For the fault-tolerant strategy, the open-circuit fault diagnosis, short-circuit detection and isolation, and fault-tolerant topology are required. According to TABLE 9, the mean current method is the most suitable one for open-circuit diagnosis, as it has a fast response, high load immunity and low complexity. Observations from TABLE 10 indicate that the gate charge method, gate voltage method with Miller plateau and *di/dt* method are the competitive short-circuit detection methods in terms of detection time, cost, and detection performance. The fuse-on-leg (Fig. 36(d)) method is selected to isolate the faults due to its low cost and good isolation ability, which can be seen in TABLE 11. As for the fault-tolerant topology, the best option depends on the specific application. For example, the fourth leg topology is the best solution for the power-critical application, as it has the highest post-fault output power. Similarly, the four-switch three-phase topology is suitable for reliability-critical applications, as it has the highest MTTF%.

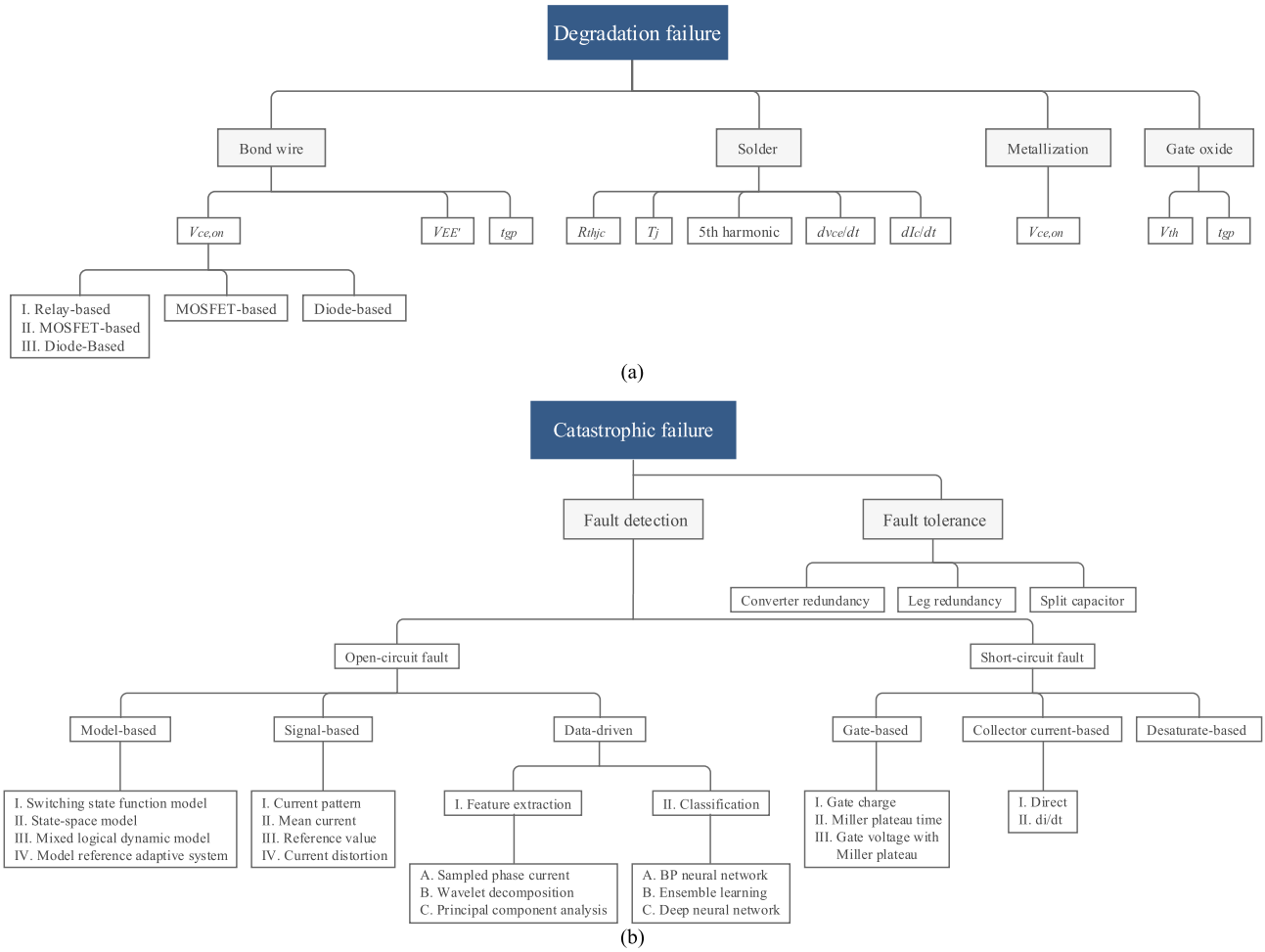

FIGURE 38. Possible online methods that can ensure the reliability of the two-level power converters.

B. SOLUTION COMPARISON FOR DIFFERENT APPLICATIONS

The performance of both condition monitoring and fault tolerance vary with different application domains as they are related to the maintenance availability, the stress level of the converter, cost consideration, mission requirement, etc.

1) MAINTENANCE AVAILABILITY

The maintenance availability is of paramount importance to condition monitoring. Because the converter needs to be maintained as soon as possible after the degradation has been detected, as the degradation will accelerate the wear-out process. If it takes too long to achieve the maintenance, the converter may fail first, making it unreliable. In extreme circumstances, taking the spacecraft as an example, it is almost impossible to be repaired even though the degradation is detected. Thus, the more difficult the available maintenance is, the worse the monitoring performance is. On the contrary, the tolerance strategy is immune to maintenance availability. Because it improves reliability by means of redundancy, which is irrelevant to the maintenance.

2) STRESS LEVEL

The stress level that the converter suffers is another factor that may have impacts on the performance of reliability solutions. Most catastrophic failures are caused by overstresses rather than wear-out, which implies that the monitoring strategy may not be able to ensure the reliability of the converter in this case. The reason lies in that it could not predict this kind of failure and no maintenance can be implemented in time. On the other hand, fault tolerance can detect catastrophic failure and reconfigure the converter timely. Thus, the fault can be mitigated and the converter can be brought back to normal operation. Therefore, the harsher working environment leads to poorer monitoring performance and the tolerance strategy outperforms the monitoring strategy in this case.

3) COST

In industrial applications, the cost is also a key factor in addition to the performance. For the monitoring strategy, the circuit cost mainly comes from the block devices for Vdc, namely, the diodes and/or the MOSFETs. The expense of the measurement of V_{ge} is relatively low, considering that

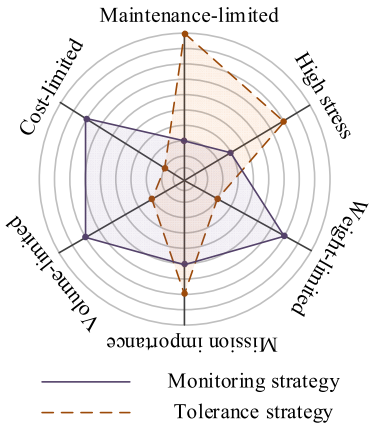

FIGURE 39. Performance comparison between monitoring strategy and tolerance strategy.

it could be integrated into the gate driver. On the contrary, the circuit cost of the failure tolerance strategy is rather high. Although the cost of fault detection circuit/algorithms is low, both of the fault isolation circuit and tolerant circuit require the same level cost as the converter as shown in Table 11 and Table 12. Thus, the monitoring solution is much better than the tolerance when the power rate of the converter is high. Yet this advantage decreases with the decline of the power rate. Meanwhile, it is also true for the volume and weight, because the cost of silicon devices is proportional to the volume and weight. In this sense, the monitoring strategy is better for those applications that are cost-limited, volume-limited and weight-limited, e.g., electric vehicles.

4) MISSION IMPORTANCE

The performance of the two solutions is also affected by the output requirement of the mission. If the output is not constrained to a certain level, i.e., the output could be flexible, the condition monitoring could extend the operational lifetime of the converter employing smart derating even the maintenance is not available. More concretely, when the degradation of the component is detected by the condition monitoring system, the output of the converter will be reduced. As a result, the stress of the component can be diminished and the converter can work for a longer time than expected. Under this condition, the fault tolerance can have similar performance with limited increased cost by utilising the split capacitor topologies given in Fig. 37. Nevertheless, if the output requirement is critical, i.e., no derating or interruption is allowed, fault tolerance has its advantage in this case. Because it requires no maintenance and can deal with high stress.

Overall, the comparison of the aforementioned two strategies for reliable converter operation in different applications is given in Fig. 39. For the condition monitoring, it takes the advantage in the cost, weight and volume-limited applications where the maintenance can be accessed easily. On the other hand, the fault tolerance solution outperforms the condition monitoring when the maintenance is unlikely available and the converter works under high stress for the mission-critical applications.

V. CONCLUSION AND PROSPECTS

In this paper, the monitoring strategies and tolerance strategies that can improve the reliability of the power converters have been reviewed. In terms of monitoring, why IGBT devices degrade, what indicators can be used to monitor the degradation, and how to extract these indicators were discussed and compared in detail. As for the fault tolerance, the fault detection algorithms and circuits, fault isolation circuits and fault-tolerant topologies were further reviewed and compared in this paper, too. Although the monitoring can improve the reliability of power converters, the performance is limited as it is a cheap and affordable method. On the other hand, the fault-tolerant strategies provide a better performance, but the associated cost is also higher.

Besides the advances in reliability enhancement strategies, which have been presented in this paper, we have identified four main challenges to cope with in the coming future:

1) Understanding the multiple-parameter shift caused by wear. All the modern condition monitoring techniques are based on calibration or re-calibration methods during operation over long-term time scales. In the case of multi-dimensional degradation, though, calibration strategies are not effective. This is an intrinsically big challenge in terms of knowledge;

2) Similarly to 1), it is highly demanded to find a way to reliably decouple the temperature-sensitive electrical parameters and damage-sensitive electrical parameters (DSEPs). To achieve this, a deeper physics insight, especially on the damage mechanism side, urges to be gained;

3) Regarding fault-tolerant strategies, reliable detection methods of open-switch fault under near-zero current conditions and multiple faults (i.e. more than three IGBTs failing at the same time) are demanded. Emerging technologies, such as artificial intelligence and deep learning should be explored in the near future;

4) Fault-tolerant topologies are way not as efficient and cheap as expected (see Table 12). New concepts to enhance the overall efficiency of fault-tolerant topologies are highly demanded.

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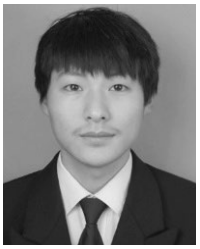

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