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Niazi, Kamran Ali Khan; Yang, Yongheng; Séra, Dezso

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Review of Mismatch Mitigation Techniques for Photovoltaic Modules

Kamran Ali Khan Niazi, Yongheng Yang*, and Dezso Sera

Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark
*yoy@et.aau.dk

Abstract: The installation of Photovoltaic (PV) systems is continuously increasing in both standalone and grid-connected applications. The energy conversion from solar PV modules is not very efficient, but it is clean and green, which makes it valuable. The energy output from the PV modules is highly affected by the operating conditions. Varying operating conditions may lead to faults in PV modules, e.g., the mismatch faults, which may occur due to shadows over the modules. Consequently, the entire PV system performance in terms of energy production and lifetime is degraded. To address this issue, mismatch mitigation techniques have been developed in the literature. In this context, this paper provides a review of the state-of-the-art mismatch mitigation techniques, and operational principles of both passive and active techniques are briefed for better understanding. A comparison is presented among all the techniques in terms of component count, complexity, efficiency, cost, control, functional reliability, and appearance of local maximums. Selected techniques are also benchmarked through simulations. This review serves as a guide to select suitable techniques according to the corresponding requirements and applications. More importantly, it is expected to spark new ideas to develop advanced mismatch mitigation techniques.

1. Introduction

A significant part of the energy is extracted from the coal, which is actually very limited throughout the world. Therefore, it is necessary to replace the coal with other energy sources to address the issues. In recent years, solar and wind energy has gained much popularity [1]. Compared to other renewable energy resources, the solar PV technology has been in continuous growth for many years and is considered one of the main sources of the clean and green energy [2, 3]. PV energy has already become a competitive candidate in the energy sector [4, 5]. The growth rate of PV installation is consistently high and still increases. Globally, the growth rates have reached 6.3% and 1.7% of installed capacity and electricity generation, respectively [6-9].

A complete grid-connected PV system is exemplified in Fig. 1, which consists of a solar PV array, PV converters, a battery, a PV inverter and a filter (LCL) to remove the harmonics after conversion from the DC-AC inverter [10, 11]. The power from the PV array can be processed by the power electronic converters [12-14] (see Fig. 1) and the maximum power is extracted by means of the maximum power point tracking (MPPT) control [15-19]. The MPPT controls the PV systems to operate at the maximum power point (MPP) and then the system delivers the maximum power to the load (and also the grid) under given solar irradiance and temperature conditions [20-26].

As shown in Fig. 1, the energy source of a PV system is its PV panels (i.e., the PV array), which can be configured through several PV modules. In this way, the PV modules connected in series and/or parallel can reach the required voltage and current [27, 28]. However, the performance of series- and parallel-connected PV modules is sensitive to faults that may occur in practice [29-31]. Among various faults, mismatch faults are the most commonly observed ones in PV systems [32-34], which typically occur due to shading on PV modules [35-37]. The shading may be a result of object blocking, bird drops, wildlife or passing clouds, which in turn affects the series-connected PV modules, contributing to a reduction in the current [38-40]. The reduced current due to mismatching causes power losses, which are dissipated in solar PV cells within the shaded module(s)/cell(s). The power

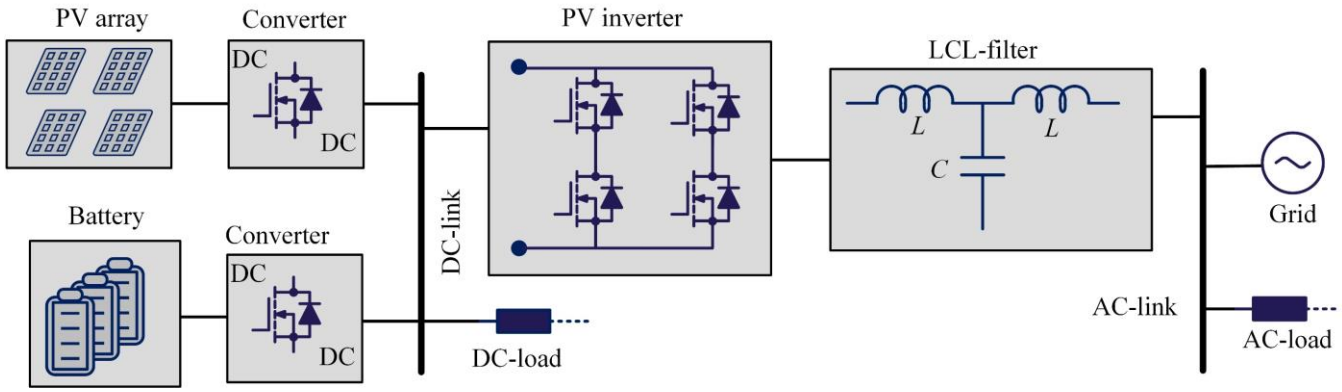


Fig. 1. *Grid-connected PV system with battery storage and DC-load*

dissipation in the shaded cell(s) increases the cell temperature and eventually, may create hotspots [41]. In this case, the shaded cell(s) is reverse-biased as a load instead of a generator [42-44], and hence, it further accelerates the wear-out or aging of the solar PV cells. In all, the overall power generated by the PV array may be significantly reduced [45, 46] in the case of mismatch faults. That is, mismatch faults not only affect the output power but also affect the PV module lifetime [47, 48] and its reliability [49]. As a result, the cost of PV energy may be affected eventually.

To improve the lifetime of the PV modules (and thus, the entire PV systems) and also to maximize the energy harvesting from the solar PV modules, mismatch mitigation techniques have been developed over the years and reported intensively in the literature [50-59]. This is also enabled by the advancement of power electronics, which are becoming more and more integrated into PV modules to mitigate potential mismatch incidents. For instance, in [50], a traditional bypassing diode was presented, which bypasses the PV modules while being shaded. Differential power processing (DPP) architectures are another type of power converters [53-57], being increasingly used in PV systems to lower the mismatch effect. DPP converters only process the mismatch power among the PV modules, and thus power losses in the DPP architectures are low, compared to all other available architectures. As an alternative, in [51], [52], and [58], smart bypass diodes, bipolar junction transistors (BJT), and MOSFETs can be adopted to achieve bypassing in the case of mismatch events. Generally, all these techniques bypass the PV modules like the technique presented in [50], but with reduced power losses during bypassing (i.e., improved efficiency). In all, the appearance of multiple local peaks (local maxima's) due to mismatching among the series-connected PV modules may be avoided, when the power electronics-based techniques/ topologies are adopted. In this way, the output power as well as the lifetime of PV modules can be enhanced, which in turn contributes to the improved performance of the entire PV systems. However, there are only the corresponding implementation methods, efficiency, advantages, and disadvantages without going into the details of the operating principle of these mitigation techniques that have discussed in [60] and [61]. There are no clear rules on how to select the mismatch mitigation technique according to specific applications. It thus calls for a thorough review of the topologies to cater for more high-performance PV systems with power electronics.

Considering the above, a detailed analysis of the prior-art solutions to the mismatch fault is presented in this paper from the topological perspective. The working principle of each mitigation technique has also been briefly discussed for better understanding. In addition, selected techniques are compared to further demonstrate the discussions in terms of output power. The review aims to bring forth current advances in shading mitigation techniques for the maximum energy yield from solar PV systems. The rest of the paper is organized as follows. Section 2 presents the types and causes of mismatch faults in PV modules, while in Section 3, an review of the state-of-the-art mismatch mitigation techniques is discussed. Section 4 presents a benchmarking of selected techniques, including the traditional bypass diode, series MOSFETs with traditional bypass diodes, PV-PV buck-boost, switched-capacitor, and the buck-boost and switched-capacitor (BBSC) converter techniques through simulations. A detailed comparison of all the techniques is presented as well in Section 4 to guide the selection of proper methods. Finally, Section 5 gives the concluding remarks.

2. TYPES AND CAUSES OF MISMATCH FAULTS

Mismatch faults can be classified into temporary and permanent types [62], as shown in Fig. 2. Soldering, impurities in the material, PV manufacturing variations and degradation of PV modules due to aging are certain reasons for the internal mismatching. It may lead to approx. 10% reduction of the output power [62] and is classified as permanent faults in PV modules. While the power losses due to bypassing diodes, power electronic converters and shading are considered as external reasons for mismatching in PV modules [63, 64]. In practice, shading (shadows) occurs more frequently [65]. It should be pointed out that dust accumulation on the PV module glass degrades the glass transmittance, thus decreasing the PV module power output [66]. The average degradation due to dust is accordingly around 6.2%, 11.8%, and 18.7% for the exposure periods of one day, one week and one month [67]. Moreover, the shading effect on an individual cell is also affected by the cell

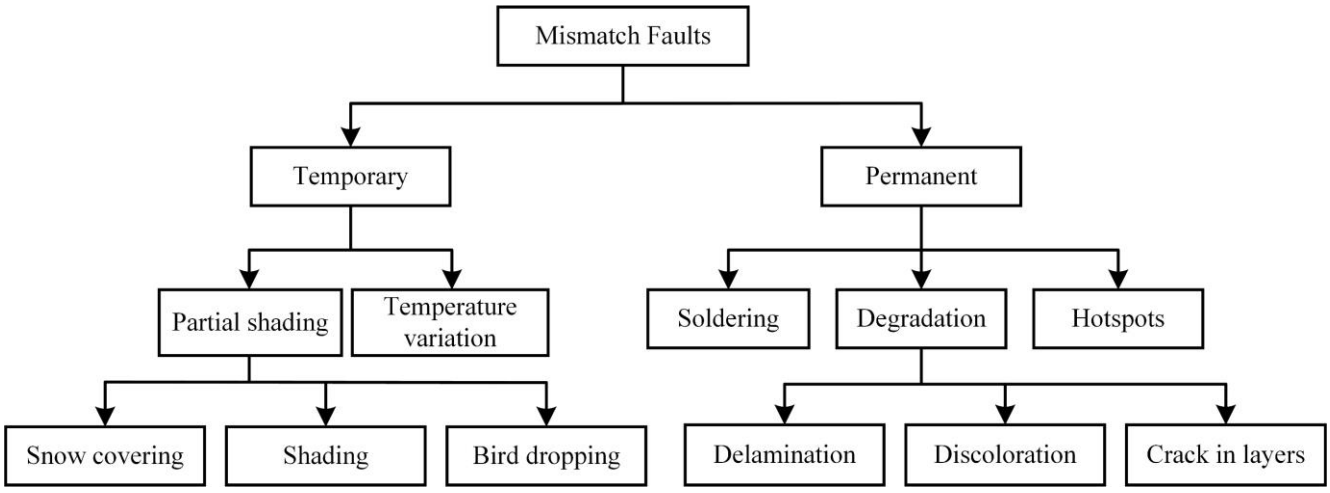


Fig. 2. *Classification and possible causes of mismatch faults in solar PV modules (notably, temporary mismatch faults can also become permanent if remain for long time, e.g., hotspots)*

parameters, e.g., the shunt and series resistance that is related to the change in the reverse current [68, 69]. Nevertheless, the mismatch fault induces heating, due to which the PV cell(s) or module(s) can reach to a high temperature that can further result in permanent damage to the module [70-72]. The above temporary mismatch faults cause around 5-10 % energy losses in Germany and Japan, while 3-6 % in Spain [73]. Clearly, all these faults have an impact on the efficiency (energy yield) of the entire system as well as the lifetime of an individual PV module [74]. In the following, the fault generation mechanisms are illustrated.

2.1. Temperature variation

The temperature variation has a significant and direct effect on the current-voltage (I-V) curves of PV modules [75, 76]. It has a non-linear effect on the output power. The change in temperature causes a variation in the open circuit voltage of PV modules. Temperature increases correspond to lower open circuit voltages, which in turn affects the MPP point. The variation in the MPP point causes mismatching between PV modules [77]. In industry, the temperature at the standard test condition (STC) for PV modules is 25 °C. However, practical PV modules are operated at lower or higher outdoor temperatures [78, 79]. After long-term operation, PV modules with the same specifications may have different MPP points due to temperature variations.

2.2. Shading

According to the *photovoltaic* effect, the output performance of PV systems varies with the intensity of the solar irradiance that strikes the modules, typically referred to as an irradiance profile. It is possible that PV modules in a system may have non-uniform irradiance profiles due to shading, which affects their output power [59, 80]. The shading may be homogenous or non-homogenous. If the distribution of the shadow is the same all over the modules, it is called homogenous, while the unbalanced distribution is known as non-homogenous. The non-homogenous shading may be a consequence of passing clouds, birds drop, object blocking, and shading from poles or trees, as shown in Fig. 3(a) and (b). All these shading types introduce mismatch to PV modules. Additionally, shading may also produce hotspots, which can be visible through thermal images.

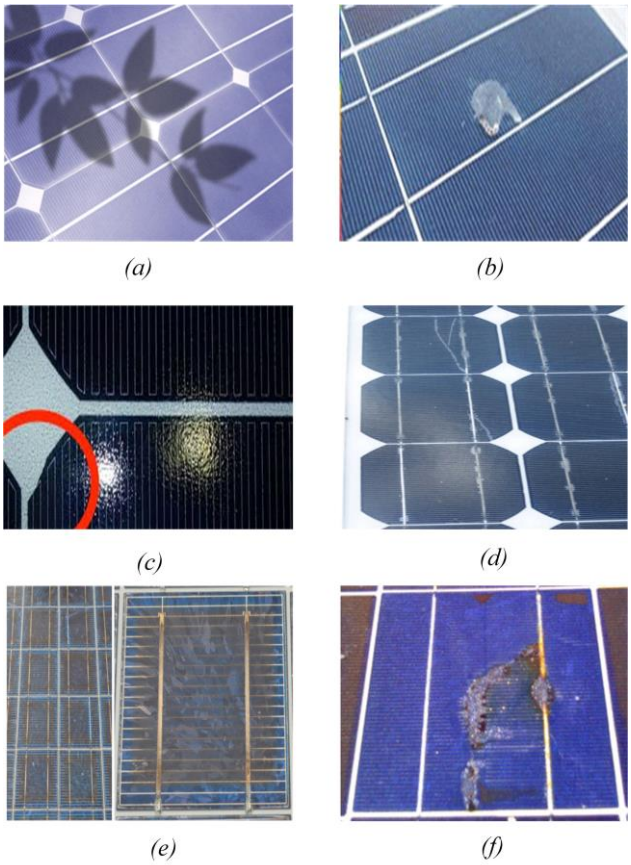


Fig. 3. *Mismatch fault causes:* ***(a)*** *shading,* ***(b)*** *bird drop,* ***(c)*** *soldering,* ***(d)*** *cracks,* ***(e)*** *discoloration, and* ***(f)*** *delamination*

2.3. Soldering

PV modules are manufactured with various materials, which can be soldered together, as shown in Fig. 3(c). Due to the degradation of the solder joints, failures may occur in the entire PV module [72, 81, 82]. The degraded joints are normally operated at a high temperature, which can weaken the connection between materials and cause deformation in the PV modules. The deformation will result in mismatching in the system and increase the series resistance. The increased resistance further consumes power, leading to hotspots and possibly arcing at the joints, and consequently, it can affect the overall PV performance.

2.4. Degradation

The performance of a PV module is also affected by the degradation [83-85]. The degradation may be a result of many consequences, e.g., degradation of power devices, loss of adhesion, packaging material fatigue, and moisture. The degradation of PV modules is also related to the operating condition [86]. In certain cases, the detection of degradation with a human eye is impossible. For instance, as shown in Fig. 3(d), micro-cracks are difficult to identify manually, which however affect the performance of the PV module. Then, electroluminescence (EL) cameras [87] are specially used to detect micro-cracks in PV modules [88].

Additionally, the discoloration is the most commonly occurred degradation, as exemplified in Fig. 3(e). It is related to a change of colour of the PV cell material with time. In the case of discoloration, the colour of certain PV cells becomes yellow and sometimes even brown. The performance of the modules with discoloration is then degraded, because the sun light cannot properly reach the solar PV cells due to the presence of the additional layer (i.e., the discoloured area).

Delamination is also a type of degradation [89-91], which can be detected from the detachment of the PV layers, as shown in Fig. 3(f). It is a major degradation issue, which commonly occurs in hot and humid climates [92]. The delamination degradation can lead to serious effects. For instance, it may cause light decoupling, where reflection increases, and water penetration inside the modules. The water penetration appears as a bubble, which in turn becomes a cause of heat dissipation. The delamination effect is much severer, when it occurs in the borders of the modules. In this case, apart from the power losses, electrical risks to the modules may arise [93].

2.5. Hotspots (temporary and permanent)

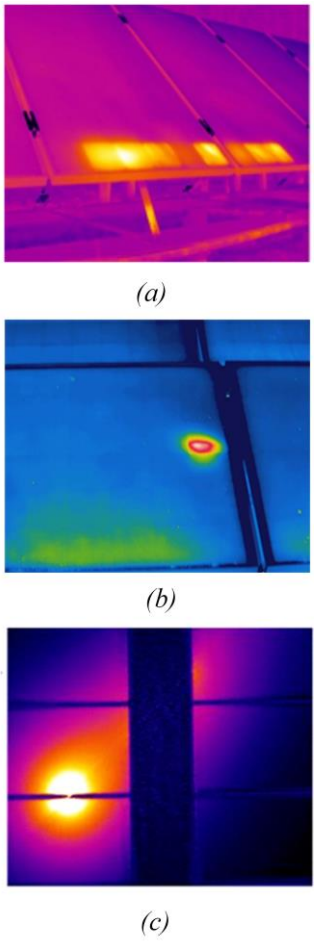
The high-temperature part of the PV module appears as a hotspot, as demonstrated in Fig. 4 [94-96]. This can

happen temporarily or permanently. For instance, due to bird dropping, the shaded cells may be heated up temporarily, and go back to normal conditions when the bird is removed. However, if the incident lasts for a long period, the hotspot may become permanent. Fig. 4(a) shows hotspots on PV modules due to shadows. As mentioned above, if these hotspots stay longer, the PV cell or even the entire PV module may be damaged permanently [97, 98]. Hotspots can also be generated, e.g., in the case of PV cell failures (Fig. 4(b)) or damaged gridlines (Fig. 4(c)). In certain cases, the defects due to manufacturing may lead to permanent hotspots in PV modules, which may be avoided by ensuring the quality monitoring. In the case of hotspots, PV cells are producing less power, compared to other series-connected PV cells, and thus it may operate in the reverse mode. As a consequence, the hotspot cells consume power instead of producing, then leading to temperature increases and can cause up to 6% power reduction [99].

3. MISMATCH MITIGATION TECHNIQUES

To reduce the effect of mismatching, bypass diodes are commonly used in practice, as shown in Fig. 5. Bypass diodes are connected in parallel with the PV sub-modules to provide a path to the current generated by the non-shaded cells. Each of these sub-modules normally consists of 20-24 series-connected PV cells, and the corresponding parallel bypass diodes are denoted by D_1, D_2, and D_3, as shown in Fig. 5 [100, 101]. However, these bypass diodes produce extra peaks in the overall output power, where there is partial shading or uneven solar irradiance variations [102-104]. The multiple peaks of power-voltage (P-V) curve may disturb the MPPT method. Therefore, each MPPT method should optimize the power output by searching for the global peak [105], known as the global MPPT. Nevertheless, there are several mismatch fault mitigation techniques reported in the literature [106-110], as categorized in Fig. 6, where it can be observed that many efforts have been made to the power electronics-based methods. These techniques have variations in the circuit configuration to maximize the PV output by minimizing the mismatch effects. Various mismatch mitigation techniques are discussed in this section, including:

- Bypass diodes techniques
- Bipolar junction transistor (BJT) bypass technique
- Series MOSFET bypass technique
- Active sensing-based technique using MOSFETs
- Distributed power electronics-based techniques



(a)

(b)

(c)

Fig. 4. *Hotspots in solar PV modules due to mismatching:* ***(a)*** *hotspots due to shadow,* ***(b)*** *hotspot due to damage cells, and* ***(c)*** *hotspot due to damaged gridline*

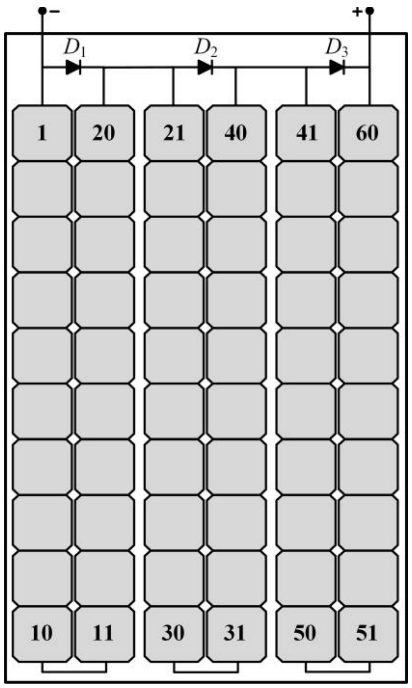


Fig. 5. *Internal structure of a PV module (60 cells in series) with parallel-connected bypass diodes (D_1, D_2, and D_3)*

3.1. Bypass diodes techniques

In a PV module, across each sub-module, a bypass diode is connected in parallel to reduce the effect of mismatching by limiting the reverse voltage [111-113], as aforementioned. These diodes protect the shaded cell(s) from heating up. The equivalent sub-module (SM1 and SM2) circuit with bypass diodes D_1 and D_2 is shown in Fig. 7. The bypass diode D_1 helps to reduce the chance of damage to the sub-modules during shading, as shown in Fig. 7(b), where I_b is the current from diode D_1. The power-voltage (P-V) curve of the module is shown in Fig. 7(c). In Fig. 7(c), it is shown that there is more than one maximum during shading, which challenges the maximum power tracking. The diode D_1 limits the high reverse voltage across the shaded cell(s) of SM1 from the series-connected un-bypassed PV sub-module SM2. However, it should be noted that hotspots may still appear, even when the bypass diodes are adopted [50]. Nevertheless,

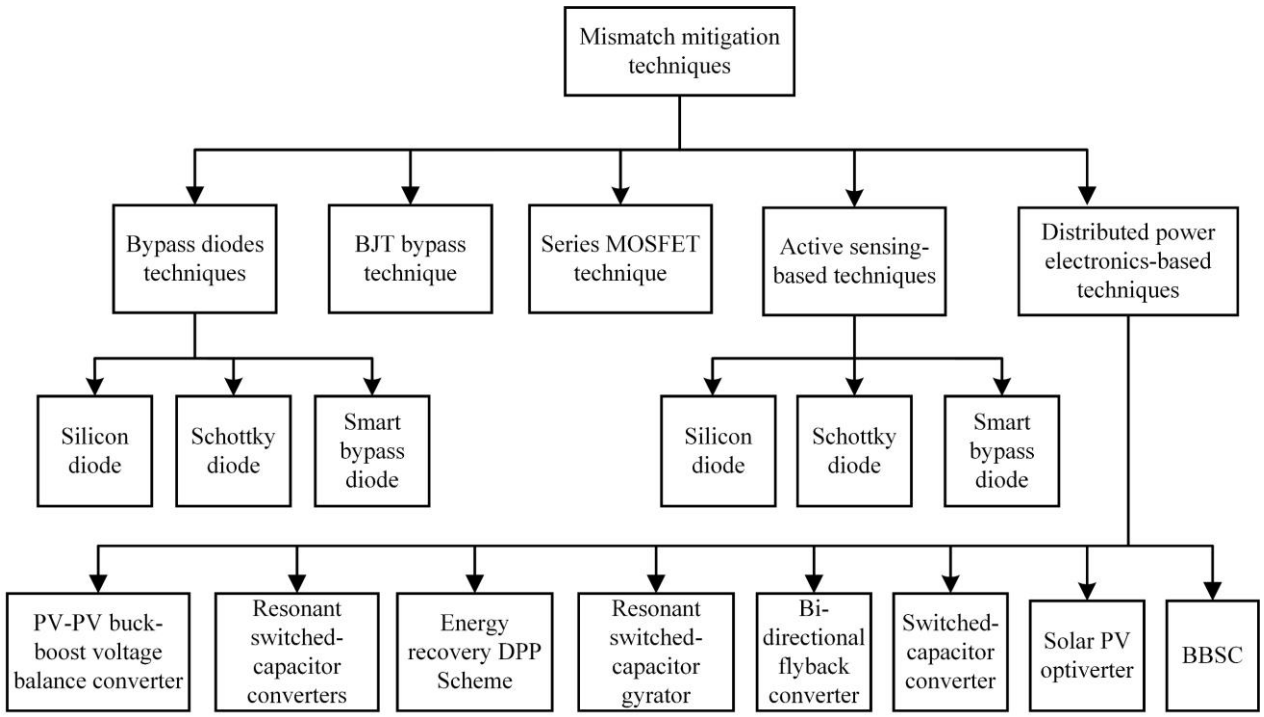


Fig. 6. *Classification of mismatch mitigation techniques (BJT – bipolar junction transistor; PV – photovoltaic; DPP – differential power processing; BBSC – buck-boost and switched-capacitor converters)*

adding bypass diodes is the simplest and easiest way to reduce mismatch effects.

Furthermore, the type of diodes will affect the performance of this technique. In this paper, three kinds of bypass diodes are reviewed, i.e., the silicon diode, the Schottky diode (traditional diode) and the smart bypass diode [114, 115]. These bypass diodes have the same function. However, the operating principle of the smart bypass diode is different. The forward or ON-state voltage (V_F) is also different among these diodes. Silicon bypass diodes have the highest forward voltage, i.e., V_F = 0.7 V [116]. The forward voltage of Schottky diodes is between 0.4-0.5 V, while the forward voltage of smart bypass diodes is very low, which is approximately 25 mV. Therefore, power losses in smart bypass diodes are very low. Considering the ON-state voltage, the power losses in Schottky diodes are less than silicon diodes, when they are adopted in PV modules for bypassing.

Silicon and Schottky bypass diodes have a simple PN junction, which require breaking down the junction potential during shading, but smart bypass diodes have a different internal structure. As shown in Fig. 8, a smart bypass diode uses a transistor (Q_1) to mimic the diode behaviour [58, 115]. The use of the transistor as a bypass element results in a lower forward voltage (about 25 mV), compared with a Schottky diode. In addition to the transistor Q_1, a controller with a field-effect transistor (FET) driver, a charge pump and a capacitor C_1 are included, as shown in Fig. 8. Once a sub-module is shaded, the current will flow through the body diode of Q_1, which creates a potential difference across the anode and the cathode. The potential charges the capacitor C_1 with the help of a charge pump in every cycle. Afterward, the capacitor C_1 turns the transistor Q_1 ON to provide a path to the bypass current. The sub-module is eventually bypassed and protected like the traditional bypass diode.

It should be pointed out that, in all bypass diode techniques, bypass diodes only limit the negative voltage across the shaded cell(s) to some extent. Multiple local peaks will appear under partial shading. Therefore, finding the global peak becomes difficult for the MPPT algorithms when partial shading occurs. That is, a sophisticated global MPPT algorithm is required. Nevertheless, there are still stresses within the sub-modules, which may degrade the shaded cell(s). Overall, the efficiency of the bypass diode techniques is low, but it is the most economical way to the mismatching. The power losses during bypassing can be expressed as

$$P_L = V_D I_b \tag{1}$$

where I_b is the current passing through the bypass diode, V_D is the forward voltage drop of the diode, and P_L is the power losses of the bypass diode.

3.2. Bipolar Junction Transistor (BJT)-based bypass technique

The bipolar transistor can also be used to bypass the shaded PV sub-module. A BJT transistor replaces the conventional bypass diode, as shown in Fig. 9. The BJT switching is controlled by MOSFET transistors Q_1 and Q_2 without any control circuitry [51, 52], as shown in Fig. 9. The gate (G_1) to source (S_1) voltage of the transistor Q_1 is equal to the SM1 voltage. Hence, Q_1 remains ON all the time even in the normal operation. Similarly, the gate (G_2) to source (S_2) voltage of the transistor Q_2 is equal to the drain (D_1) to source (S_1) voltage of the transistor Q_1. When there is no shading, the series current passes through the transistor Q_1, which is connected in series with the sub-module (SM1), as shown in Fig. 9(a). In the case of shading, the BJT turns ON to provide a path to the bypass current (I_b), as shown in Fig. 9(b). In the traditional diode bypass technique, e.g., using a Schottky bypass diode, the voltage of the sub-module is negative, but in the BJT-based technique, the voltage of the sub-module

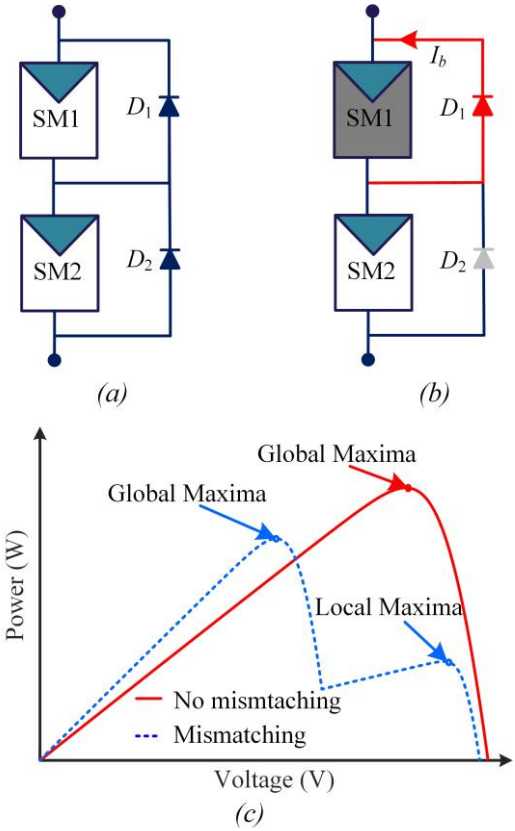


Fig. 7. *PV sub-modules (SM1 and SM2) with a parallel-connected bypass diodes D_1 and D_2: **(a)** schematic diagram, **(b)** schematic showing the current flow direction while shaded and bypassed [50], **(c)** P-V characteristic of series-connected two PV sub-modules while one is shaded (mismatching occurs). Here, I_b is the bypass current through the bypassing diode D_1*

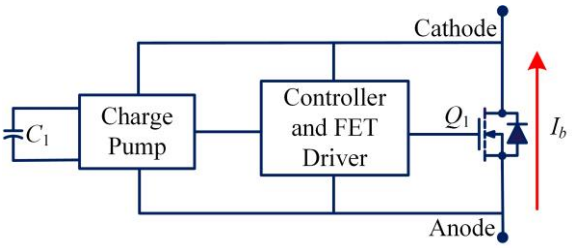


Fig. 8. *Internal structure of a smart bypass diode (SM74611) [115]. Here, I_b is the bypass current through Q_1*

remains positive. That is, it shares the negative voltage of the shaded cell(s) with the internal resistance (R_{on}) of the series connected transistor Q_1. Notably, the transistor Q_1 remains in the ON-state under shading and normal conditions. The BJT is operating in the deep saturation region. Therefore, the forward voltage drop of the BJT is very low [117, 118], which enhances the overall output power by reducing the bypass power losses that can be given as

$$P_L = V_{CE} I_b \tag{2}$$

where I_b is the current passing through the *BJT*, V_{CE} is the voltage between the collector and the emitter of the *BJT*. In all, this topology alleviates the hotspot(s) and increases the sub-module life (thus, the entire module) by reducing the revere voltage across the shaded PV cell(s). Although there is

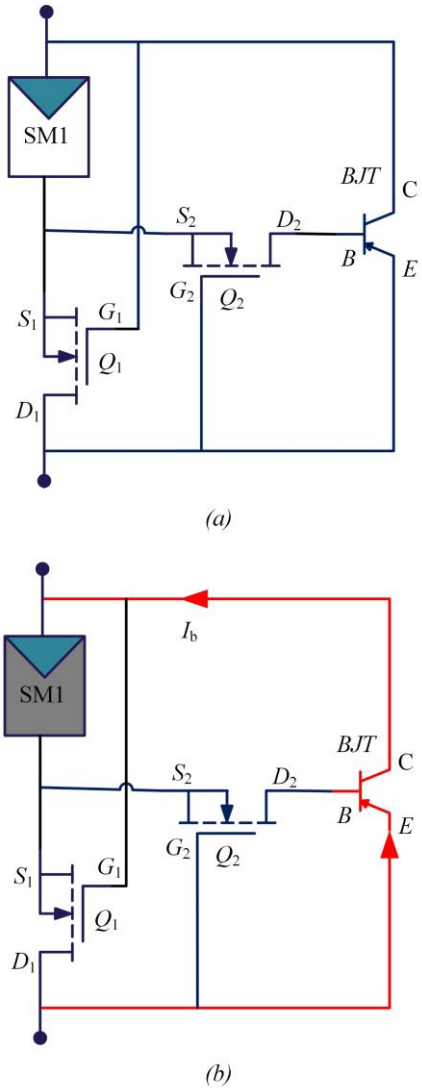


***Fig. 9.** Bipolar junction transistor-based bypass technique: **(a)** schematic diagram and **(b)** schematic showing the current flow direction while shaded and bypassed [118]. Here, I_b is the bypass current through the BJT*

no need for any control circuitry for this topology, but the choice of Q_1 and Q_2 adds more complexity and cost.

3.3. Series MOSFET bypass technique

This technique consists of a power MOSFET Q_1, which is connected in series with SM1, as shown in Fig. 10. The topology also includes a parallel-connected bypass diode D (carries the current I_b), e.g., a silicon bypass diode. Figs. 10(b) and (c) show the current directions during the non-shading and shading operation, respectively. The MOSFET Q_1 keeps ON all the time and carries a current I_p. Therefore, there are unnecessary power losses on the internal resistance (R_{on}) of the MOSFET Q_1 under uniform solar irradiance, but the transistor Q_1 can share the reverse voltage drop when shaded [119-121], as illustrated in Fig. 10(c). During the bypass condition, the current I_p flows through R_{on} and SM1 is still producing power, whose dissipation is shared by R_{on}. This is like the case in Fig. 9. Hence, with this technique, the temperature of the shaded PV cell(s) decreases [41], possibly leading to increased sub-module reliability (consequently, the entire PV module). The bypassing diode operates the same as the methods in Section 3.1.

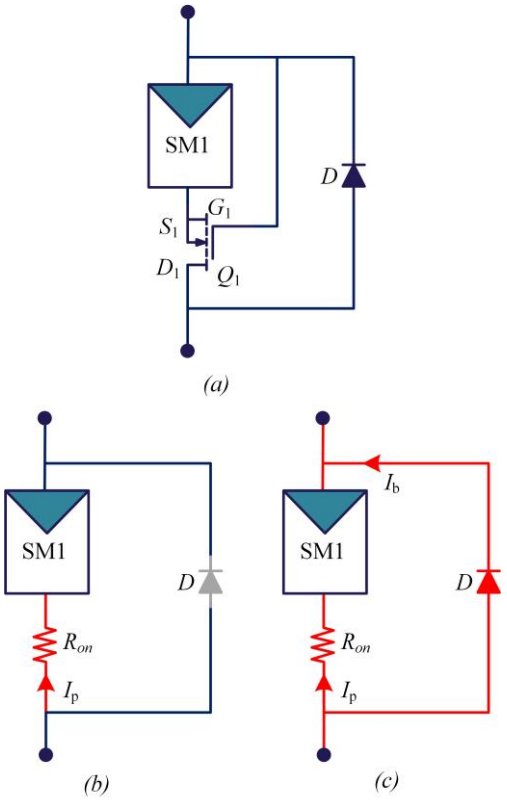


Fig. 10. *Series-MOSFET-based bypass technique [115]:* ***(a)*** *schematic diagram,* ***(b)*** *current flow direction under normal conditions and the bypass diode is in OFF-state, and* ***(c)*** *current direction when the sub-module is shaded, and the bypass diode is in ON-state. Here, I_b is the bypass current through the diode D and I_p is the sub-module (SM1) current passing through SM1, respectively*

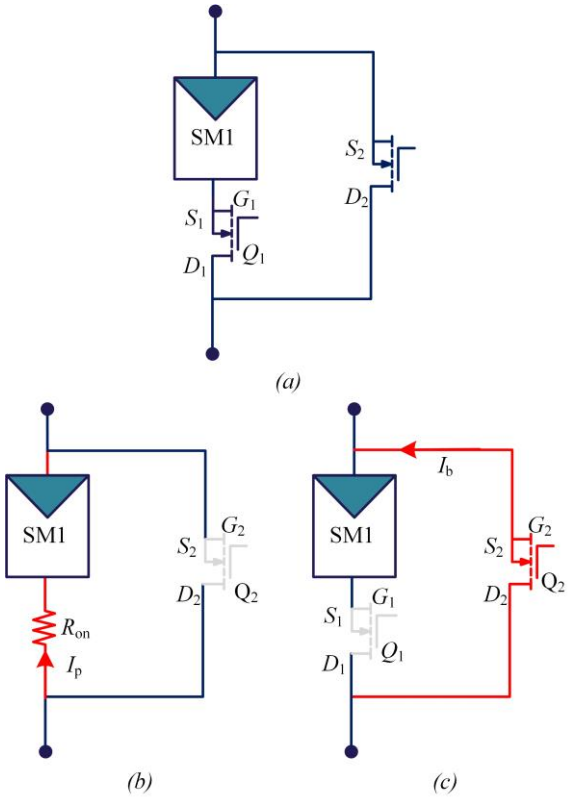


Fig. 11. *Active sensing-based bypassing using MOSFETs [122]:* ***(a)*** *schematic diagram,* ***(b)*** *current flow direction when there is no shading and the bypass transistor is in OFF-state, and* ***(c)*** *current flow direction when there is shading, and the bypass transistor is in ON state. Here, I_b is the bypass current through the MOSFET S_2 and I_p is the sub-module (SM1) current passing through SM1, respectively*

It is worth mentioning that the power losses are more in the normal operation, when silicon and Schottky diodes are adopted. Nevertheless, this technique decreases the hotspot temperature and reduces power losses during shading. Moreover, it does not require any separate active sensing circuitry or any additional supply to keep the MOSFET Q_1 ON, being simple and easy to implement.

3.4. Active sensing-based technique using MOSFETs

Power losses on bypass diodes are significant due to the large forward voltage drop. Therefore, an effective solution is needed to replace the conventional bypass diodes. To reduce the power losses during bypassing, an active topology [122] can be adopted, as shown in Fig. 11, which requires the impedance of the string to detect hotspots. Compared to the previous techniques, this topology uses another MOSFET Q_2 as the bypassing element to mitigate potential hotspots and reduce bypassing power losses. Similarly, the MOSFET Q_1 is connected in series with SM1, but it can eliminate the mismatch effects and hotspots by disconnecting SM1 when the shading occurs. The active switch Q_2 is used to reduce the losses in the case of shading.

According to Fig. 11, the power switch Q_1 is in ON-state when there is no shading and the current I_p passes through it. Therefore, there will be continuous power losses on Q_1 in the normal operation, as shown in Fig. 11(b). When the sensor detects the hotspot, Q_1 is turned OFF and Q_2 is turned ON, as demonstrated in Fig. 11(c). Then, the SM1 is isolated and protected. The current I_b passes through Q_2 without affecting other sub-modules or generating hotspots. In general, this topology provides a permanent solution to avoid hotspots in PV modules, as the shaded PV sub-modules are completely disconnected. However, active sensing and continuous monitoring inevitably increase the overall system complexity and cost. The continuous power dissipation on the transistor Q_1 in the normal operation mode is another drawback. The power losses during bypassing are given as

$$P_L = V_{DS} I_b \tag{3}$$

where I_b is the current passing through the MOSFET Q_2, V_{DS} is the voltage between the drain and the emitter of the MOSFET Q_2, and P_L is the power loss of the MOSFET Q_2.

3.5. Distributed power electronics-based techniques

With the advancement of the power semiconductor technology, distributed power electronics [123-127] can be integrated or embedded at the module level to mitigate mismatching effects. DPP converters [53, 56], PV balancers [128], PV equalizers [129, 130] are typical representatives. Among those, the DPP technique has attracted much attention in recent years, as demonstrated in Fig. 12(a). There are also various DPP converter topologies reported in the literature. In general, in DPP converters, PV sub-modules [131] operate at the MPP (no local maxima's). When potential shading occurs

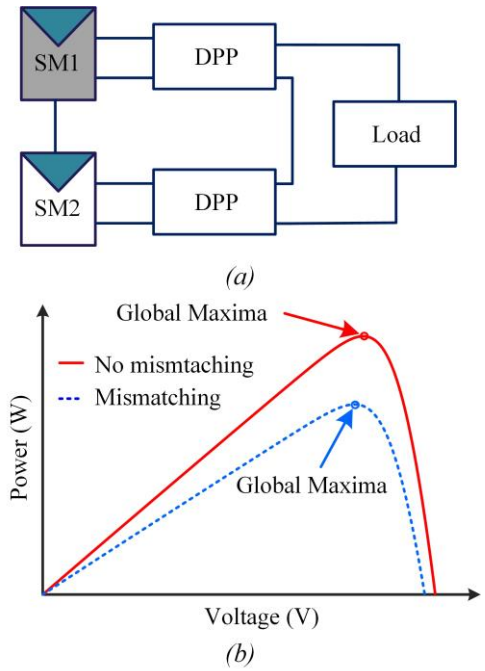


Fig. 12. *PV sub-modules (SM1 and SM2) with parallel-connected DPP topologies:* ***(a)*** *schematic diagram when SM1 is shaded and* ***(b)*** *the P-V characteristic of series-connected two PV sub-modules during mismatching and no mismatching before reaching the current limit of DPP converter*

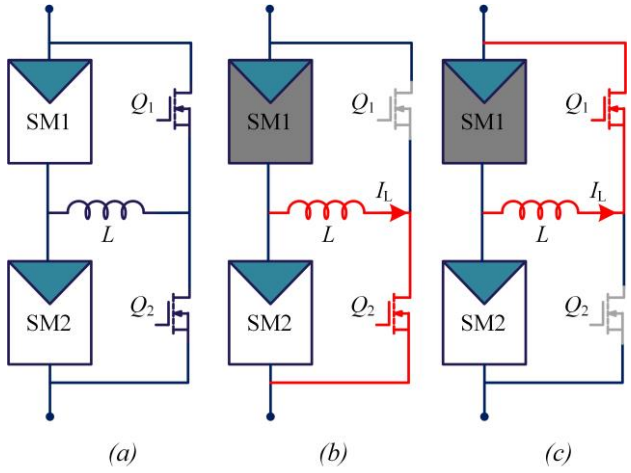


Fig. 13. *Switched-inductor PV-PV voltage balance converter [124]:* ***(a)*** *schematic diagram containing two series-connected PV modules SM1 and SM2 without shading,* ***(b)*** *SM1 is shaded and Q_1 is OFF and Q_2 is ON, and* ***(c)*** *SM1 is shaded and Q_1 is ON and Q_2 is OFF. Here, I_L is the mismatch current passing through the inductor L*

(SM1 is shaded in Fig. 12(a)), only the mismatch power will be processed by the DPP system [55]. In this case, as compared in Fig. 12(b), the DPP operation presents only one global peak under mismatching and normal conditions. This simplifies the MPPT, while ensuring more power harvesting.

Notably, under normal conditions, the DPP converters and other power electronic-based techniques should not process any power beyond the mismatch power to maintain the system efficiency. In fact, these power converters operate like controllable current sources to "buffer" the differential power (then, alleviate the mismatch). It is possible to use distributed power converters at any level—module-by-module, module-to-bus, string-by-string, or even sub-module-by-sub-module. Several prior-art power electronic-based mismatch mitigation topologies are briefly discussed in the following.

3.5.1. PV-PV buck-boost voltage balance converter

A PV-PV buck-boost converter was introduced in [124, 132]. It is used to balance the voltages between series-connected sub-modules during mismatching. As it is shown in Fig. 13, the converter uses a voltage equalization topology to reduce the mismatch effect by complementarily switching the transistors Q_1 and Q_2 [55]. In addition, an inductor L is connected between the two PV sub-modules (SM1 and SM2). The operation principle of this converter can be explained as follows. When there is shading, the currents generated by the two sub-modules will not be identical. For example, as shown in Fig. 13(b), the larger current through SM2 will charge the inductor L, when Q_2 is ON (Q_1 is OFF). When Q_2 is OFF (Q_1 is ON), the stored energy in L will then be released to the load, as shown in Fig. 13(c). Thus, the load will see only one maximum. Nevertheless, the switching will induce power losses that can be found as [132]

$$P_{SWLOSS} = 2k_0\left[V_G\sqrt{\frac{V_G}{2V_B}} + 4V_D I_L\sqrt{\frac{V_D}{V_B}}\right]f_{SW} \qquad (4)$$

in which k_0 is a device constant that depends on material parameters and the available die area, V_B is the breakdown voltage of the device, V_D is the voltage at the device terminal, V_G is the voltage at the gate terminal, I_L is the current passing through the inductor, and f_{sw} is the switching frequency of the power device.

Notably, this balance converter shown in Fig. 13 can also be extended to many PV modules. It is worth mentioning that the converter can also be implemented using switched-capacitor topologies [133] or buck-boost (switched-inductor) converters [134, 135]. In addition, as the converter system only processes the mismatch power between the sub-modules [136-138], it is termed as a DPP converter. This converter maintains low power losses but has a low performance under severe mismatch.

3.5.2. Switched-impedance-based topologies

The resonant switched-capacitor converter [133], resonant switched-capacitor gyrator converter [139-141], and switched-capacitor converter [142] are other types of DPP converters that utilize the parallel ladder architecture to alleviate the effect of mismatching. Fig. 14 exemplifies a switched-impedance ladder-based topology with resonant impedance (Z). It should be noted that the impedance can be of various possible combinations of resistors, which can be equal to the series resistance of capacitors and inductors along with the series resistance of PV modules, inductors, and capacitators [133]. This topology can be utilized at the module level or the sub-module level (SM1 and SM2).

When there is no mismatching, the power switches are in OFF-state, as shown in Fig. 14(a). Otherwise, during shading, as shown in Figs. 14(b) and (c) (SM1 is shaded), the power switches start to operate complimentarily. When they are switched to terminal 1, the impedance is energized, as shown in Fig. 14(b); to terminal 2, the energy is released to the load, as shown in Fig. 14(c). Clearly, in this case, only the mismatch current I_d is passing through the switches. Notably, the sub-module(s) should have the same number of series PV

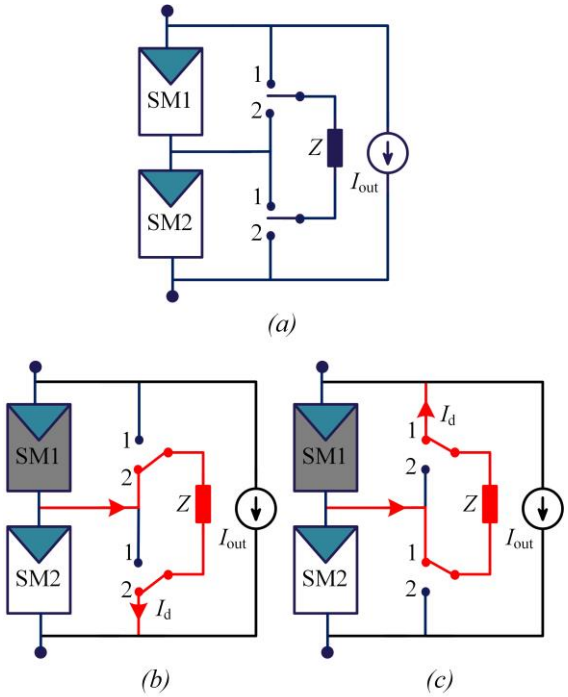


Fig. 14. *Switched-impedance-based topologies:* ***(a)*** *schematic diagram containing two series-connected PV modules SM1 and SM2 without shading,* ***(b)*** *operation when SM1 is shaded and switches are connected to terminal 2, and* ***(c)*** *operation when SM1 is shaded and switches are connected to terminal 1*

cells with the same technology (to avoid inherent voltage mismatch) [57, 143]. With this technique, each sub-module operates close to the MPP.

To further illustrate this technique, Fig. 15 shows two switched-impedance-based topologies. More specifically, a resonant switched-capacitor gyrator converter is shown in Fig. 15(a), which consists of a resonant tank [129], [130]. This switched-capacitor gyrator can equalize the voltage of the series-connected PV sub-modules, i.e., SM1 and SM2, in the case of partial shading. It only processes the mismatch power between the PV sub-modules, as mentioned previously. The operation principle is further illustrated as follows. Referring to Fig. 14 (assuming that SM1 is shaded), firstly, the resonant tank is charged by switching Q_2 and Q_4 ON (i.e., connected to terminal 2 in Fig. 14). Afterwards, Q_2, Q_4 are OFF and Q_1, Q_3 ON (i.e., connected to terminal 1 in Fig. 14), leading to the energy release from the resonant tank. Finally, Q_2 and Q_3 are turned ON, and then the resonant tank will be short-circuited. The short-circuit creates the required charge-balance and reverses the voltage polarity of the flying capacitor C (discharges the residual voltage across the capacitor), and thus the voltage at the end of the switching period for Q_3 equals to the voltage at the beginning of Q_1. During the stage, the resonant circuit behaves like a voltage-dependent current source. Notably, the operating sequences of the switches are important to obtain the desired output. The switching power losses can be obtained as [132]

$$P_{SWLOSS} = 4k_0 V_G \sqrt{\frac{V_G}{V_B}} f_{SW} \tag{5}$$

In addition to the gyrator converter, which operates at resonating frequency, the switched-capacitor (SC) converter [57] can also be adopted. As shown in Fig. 15(b), the resultant

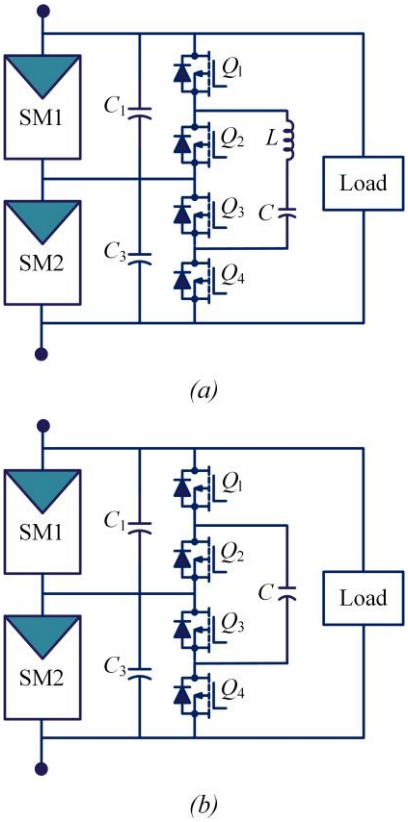


Fig. 15. *Schematics of switched-impedance-based topologies:* ***(a)*** *resonant switched-capacitor gyrator converter [139] and* ***(b)*** *switched-capacitor (SC) converters [133]. Here, C is the capacitor for charge distribution, and L is the inductor to form the resonant tank*

DPP converter only processes a fraction of the power, i.e., the mismatch power. In the SC converter, the ladder structure is adopted to balance the power between the shaded and non-shaded PV sub-modules [144]. The operation principle is the same as the one discussed above. In all, there are power losses in the topologies due to the use of many power switches (see Fig. 15), which can be expressed as [132]

$$P_{SWLOSS} = 4k_0 \left[V_G \sqrt{\frac{V_G}{V_B}} + V_D I_L \frac{R_{EFF}}{R_{ESR}} \sqrt{\frac{V_D}{V_B}} \right] f_{SW} \tag{6}$$

with

$$R_{EFF} = \frac{1}{f_{SW} C}$$

where R_{EFF} is the effective resistance, C is the capacitor for charge distribution, and R_{ESR} is the effective series resistance of the passive components in the topology. SC converter can recover a large amount of power, which is normally lost during the bypassing operation of PV modules. Overall, the switched-impedance-based topologies achieve high efficiency through harvesting the mismatch power. The topology cost is still high due to the presence of more power switches along with the relatively complicated design, e.g., digital signal processors (DSP), gate drivers, and sensors.

3.5.3. *Energy recovery DPP scheme*

The energy recovery DPP topology was proposed in [145], which is shown in Fig. 16. The scheme is based on the voltage equalization concept [106], which was originally adopted for batteries. In PV module applications, a constant voltage among the series-connected PV sub-modules can be

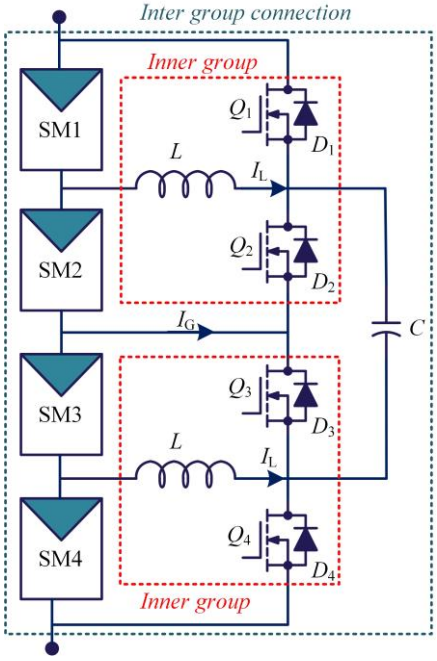


Fig. 16. *Schematic of the energy recovery DPP scheme for four series-connected PV sub-modules [145], where a capacitor C is for the inter group operation (charge distribution between two groups), and L is for the inner group charge distribution. Here, I_L is the mismatch current within a group, which is passing through the inductor L and I_G is the mismatch current between the series-connected groups*

maintained. As shown in Fig. 16, the transistors Q_1, Q_2, Q_3, and Q_4 are connected in parallel to the sub-modules. An inductor (L) is connected between SM1 and SM2 or SM3 and SM4, forming an inner group. Here, Q_1 and Q_2 or Q_3 and Q_4 operate complimentarily. A capacitor (C) is used to extend the structure by creating a link between series-connected converters. Like the previous topologies, the power switches and the passive components are utilized to recover the energy losses during mismatching.

Taking the inner group in Fig. 16 as an example, the operation principle is explained. When there is shading, the mismatch current I_L will be diverted to the inductor L within the group by switching the transistors Q_1 and Q_2. The inductor L stores the extra energy in one cycle and releases it through the freewheeling or body diodes. As a result, the mismatch effect is alleviated. This topology shows a noticeable improvement in the output power when there is severe shading. The improved output power may compensate for the power losses on the additional components in this topology, which requires a detailed cost-benefit analysis.

3.5.4. Bi-directional flyback converter (BFC)

A bi-directional flyback converter (BFC) was proposed in [131] to achieve the balancing under partial shading for PV modules. It can overcome the mismatch issues to a large extent. The schematic diagram of the converter is shown in Fig. 17, consisting of four switches Q_{1pri}, Q_{1sec}, Q_{2pri}, and Q_{2sec}, where I_{1pri} and I_{2pri} are the currents flowing from the primary side, while I_{1sec} and I_{2sec} from the secondary side of the transformers. In addition, I_{string} denotes the total output current from the series-connected sub-modules (i.e., SM1 and SM2). Furthermore, as observed in Fig. 17, each sub-module

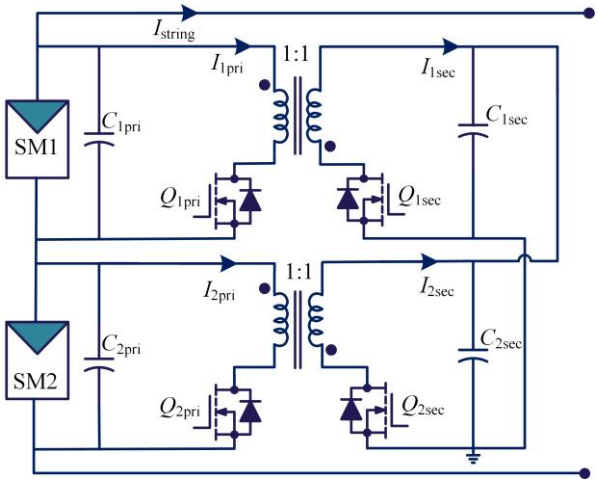


Fig. 17. *Isolated-port DPP architecture with bi-directional flyback converters (BFC) [131]*

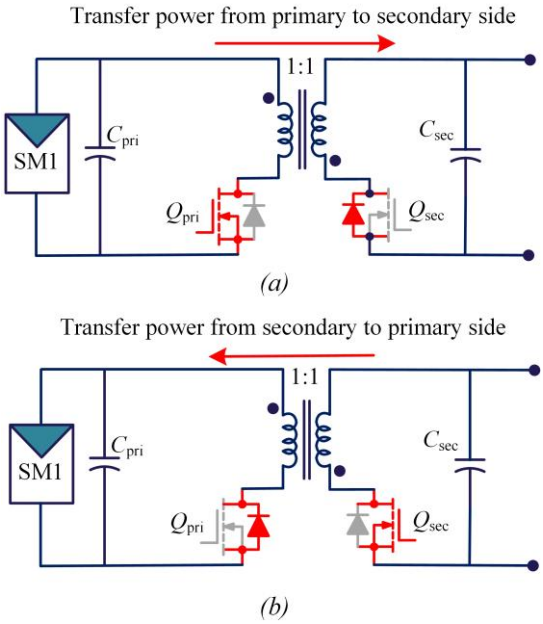


Fig. 18. *Operation principle of isolated-port DPP architecture with bi-directional flyback converters (BFC) [131]: **(a)** transferring power from primary to secondary side and **(b)** transferring power from secondary to primary side*

has a parallel flyback converter, and the two share the common isolated-port to realize the mismatch balancing. In addition, the BFC has voltage isolation and a higher efficiency compared to the PV-PV and PV-bus DPP architectures discussed in the above.

The BFC has a conversion ratio close to the unity. Therefore, the voltage at the primary side is equal to the secondary side. Moreover, it is operated in the discontinuous conduction mode (DCM) under slight mismatch conditions, while in the continuous conduction mode (CCM) under severe mismatch conditions to reduce the power losses. The BFC is operated with a duty cycle of 50% and a high frequency. The operating principle of the BFC is shown in Fig. 18. As observed in Fig. 18, the energy transfer should be bidirectional in a way to process the differential power between submodules. The details of the operation can be found in [131]. In all, the overall output power of PV modules during partial shading can be improved by this converter.

However, more switches increase the overall complexity of the system like the other DPP converters, which should be justified further.

3.5.5. Buck-Boost Switched-Capacitor Converter

In fact, the DPP scheme based on the PV-PV buck-boost voltage balance converter (Fig. 13) and the switched-capacitor converter (Fig. 15(b)) [146] can be combined as a buck-boost switched-capacitor converter. The entire topology is shown in Fig. 19, where the buck-boost converter is highlighted in cyan and the switched-capacitor converter in orange. As observed in Fig. 19, the converter has six active power devices, six diodes, four inductors, and two capacitors (the capacitors in parallel with the submodules are not shown for simplicity).

In the buck-boost operating mode, Q_1, Q_3, D_2, D_4, L_1, L_2, L_3, and L_4 are involved, while Q_2, Q_4, C_{13}, C_{35}, D_3, and D_6 are in the buck-boost and the switched-capacitor schemes. All the switches are controlled at a duty cycle of 50% and the BBSC only operates under partial shading conditions. In addition, this topology achieves fast voltage equalization among the PV sub-modules. However, this topology uses much more switches compared to the single buck-boost and switched-capacitor topologies along with an additional partial shading detection circuit (highlighted in orange). Thus, the hybrid BBSC increases the complexity and the cost.

3.5.6. More Electronics PV Modules

Recently, an optiverter was proposed in [147] for solar PV modules, as shown in Fig. 20. The optiverter is one of the examples demonstrating how power electronics are being used in PV modules to harvest maximum power under partial shading. The optiverter can extract noticeable power from the PV modules (M_1) even at a very low available voltage level, where the mismatch effect is not eliminated. The optiverter is a technology that bridges the PV power optimizers and PV micro-inverters (PVMIC). It is an expensive topology due to the presence of many passive and active switches. However, with the advancement of power electronics technology, it may initiate the development of novel power converters that can address the mismatch issues but also achieve high voltage boosting for PV modules.

4. BENCHMARKING OF SELECTED MISMATCH MITIGATION TECHNIQUES

In order to compare the performance of the above-discussed topologies, simulations are performed with various

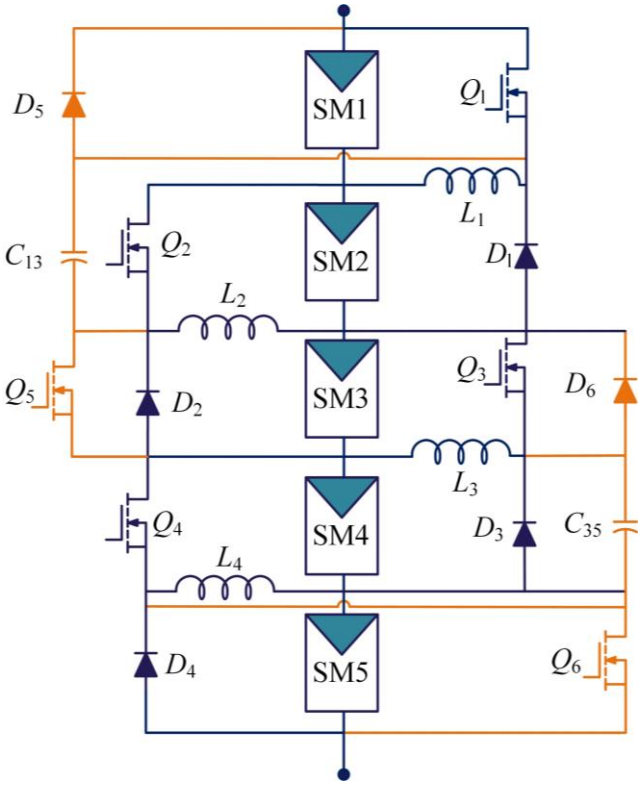


Fig. 19. *Generalized power circuit diagram of the buck-boost converter and the switched-capacitor converter (BBSC) [146]*

partial shading conditions. Three PV sub-modules (SM1, SM2, and SM3) are used and connected in series to evaluate the performance of selected bypass topologies, as shown in Fig. 21. The benchmarked topologies include traditional bypass diode (Fig. 7), series MOSFET with traditional bypass diode (Fig. 10), PV-PV buck-boost (Fig. 13), switched-capacitor (Fig. 15(b)), and the BBSC (Fig. 19). The parameters of the PV sub-modules are shown in Table 1. In the simulations, the irradiance level (S) on the first sub-module, i.e., SM1, is varied from 0 W/m^2 to 1000 W/m^2, as shown in Fig. 22, while the irradiance level on the other two sub-modules (i.e., SM2 and SM3) are kept constant (1000 W/m^2). The values for the inductor and capacitor are set as 50 μH and 100 μF, respectively, and the switching frequency is 100 kHz for all the topologies. Simulation results are shown in Fig. 23.

It can be observed from Fig. 23 that in general, the performance of the selected DPPs is better than the passive

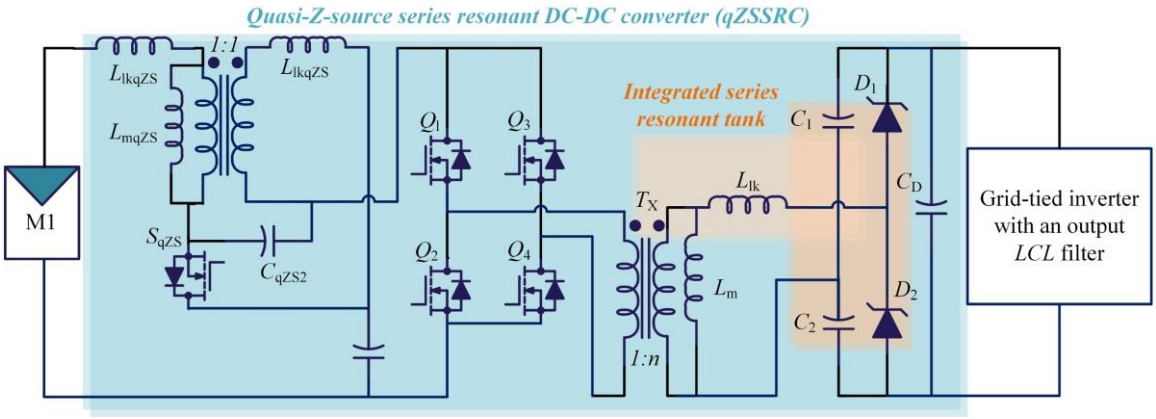


Fig. 20. *Generalized power circuit diagram of the solar PV optiverter (PVOPT) with more integrated power electronics [147]*

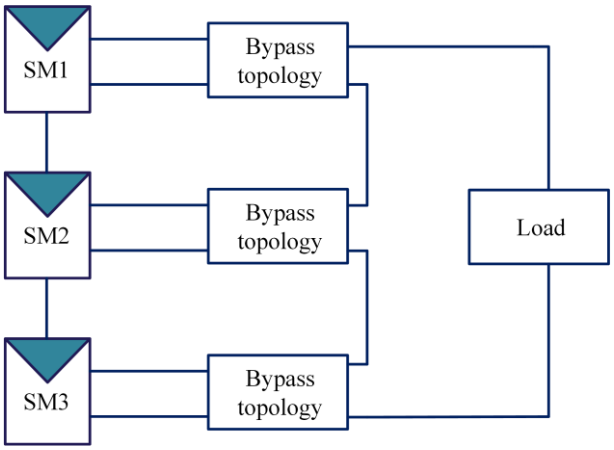


Fig. 21. *Schematic diagram of series-connected PV sub-modules. Various cases are evaluated through simulations by varying the irradiance (W/m^2) on sub-module1 (SM1)*

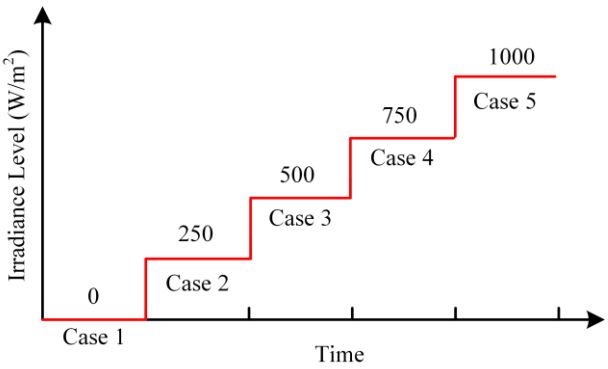


Fig. 22. *Solar irradiance profile for the first sub-module (SM1) in Fig. 21, while the solar irradiance level for the other two sub-modules is 1000 W/m^2 for all cases*

Table 1 Ratings of PV sub-modules under test

Related Maximum Power (P_{max})	60 W
Voltage at P_{max} (V_{mp})	17.10 V
Current at P_{max} (I_{mp})	3.50 A
Open-Circuit Voltage (V_{oc})	21.10 V
Short-Circuit Current (I_{sc})	3.80 A

bypass techniques, i.e., the traditional Schottky bypass diode technique. The PV-PV buck-boost topology (Fig. 13), the switched-capacitor converter (Fig. 15(b)), and the BBSC topology (Fig. 19) have the maximum output power for all the cases. More specifically, with a decrease in irradiance from 1000 W/m^2 to 500 W/m^2 on SM1, the output power is decreased gradually when the traditional Schottky bypass method and series MOSFET-based topology are adopted. In this case, the sub-module (SM1) is not bypassed. When the solar irradiance level is further reduced from 500 W/m^2 to 0 W/m^2, bypassing diodes are switched ON, which makes the output power clamped to a constant (around 120 W) for the traditional topology and the series MOSFET-based topology, as observed in Fig. 23. In contrast, other topologies will not "short-circuit" the sub-module, but divert the mismatch current to the DPP converters to continuously supply the load. Thus, a higher output power is achieved, as shown in Fig. 23. In all, the simulations have verified that the DPP converters

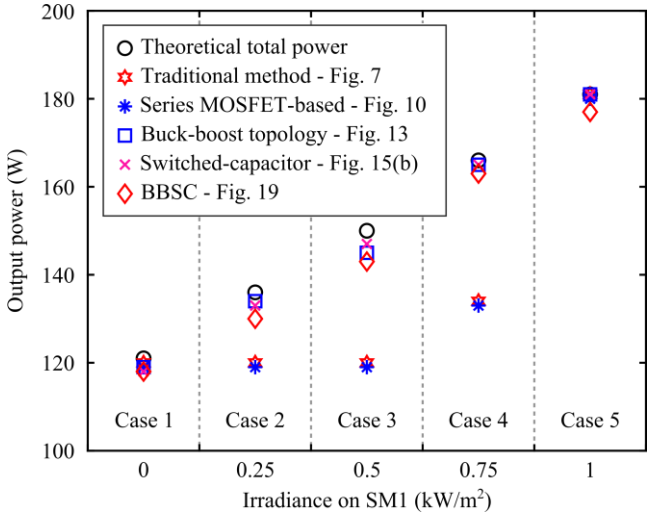


Fig. 23. *Output power of the PV module consisting of three sub-modules under partial shading with selected bypassing techniques. The solar irradiance on the other two sub-modules is 1000 W/m^2 in the simulations*

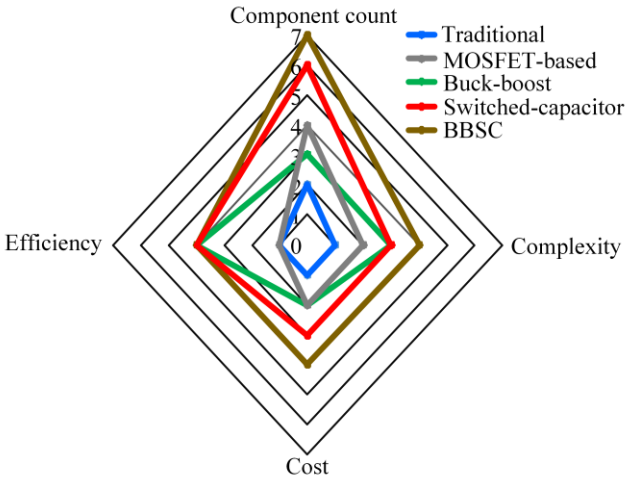


Fig. 24. *Comparison of the selected techniques in Fig. 23 in terms of component count, complexity, cost, and efficiency*

can improve the energy harvesting of PV modules in the case of partial shading.

Additionally, in Fig. 24, a comparison of these techniques is further performed in terms of component count, complexity, cost, and efficiency. Notably, the efficiency of the techniques is calculated by simply considering the overall power received at the output and the input power. Each axis in the spider chart represents a performance parameter that is qualitatively assessed in a range from low to high starting from the centre point except for the efficiency parameter (should be high in numbers). As it is observed in Fig. 24, the DPP conveters can improve the performance, but increased complexity and cost are also associated.

Furthermore, Table 2 provides another benchmarking of all the discussed topologies in terms of circuit complexity, losses/overall efficiency, cost, control complexity, functional reliability, and MPPT control (global or local maximums). Here, the functional reliability (performance and robustness) refers to the required operation of the topology for which they are particularly designed, i.e., mismatch mitigation without failures. These parameters depend upon the number of active

Table 2 Comparison of different mismatch mitigation techniques

Ref.	Techniques	Component count	Complexity	Efficiency	Cost	Control Strategy	Functional Reliability	Local Maxima's
[50]	Traditional bypass diode	*p*	Low	Low	Low	None	Limited	Yes
[65]	Silicon bypass diode	*p*	Low	Low	Low	None	Limited	Yes
[114]	Smart bypass diode	*p*	Low	Medium	Low	None	Limited	Yes
[114]	Series MOSFET with Si diode techniques	2*p*	Medium	Low	Medium	None	Medium	Yes
[115]	Series MOSFET with Smart bypass diode techniques	2*p*	Medium	Medium	Medium	None	Medium	Yes
[117]	Series MOSFET with traditional bypass diode techniques	2*p*	Medium	Low	Medium	None	Medium	Yes
[118]	Bi-polar junction transistor (BJT)	3*p*	High	Low	High	None	Limited	Yes
[122]	MOSFET bypass technique	2*p*	Medium	Medium	Medium	Medium	High	Yes
[124]	PV-PV buck boost voltage balance converter	3(*p*-1) (*p*= 2, 3, …)	High	High	Medium	Complex	High	No
[131]	Bi-directional flyback converter	5*p*	High	High	High	Complex	High	No
[133], [139]	Switched-impedance-based converters	3*p*-1 (*p*= 2, 3, …)	High	High	High	Complex	High	No
[145]	Energy recovery DPP scheme	-	High	High	High	Complex	High	No
[146]	BBSC	-	Very High	High	Very High	Complex	High	No

**p* is the number of PV modules

and passive circuit elements in each topology, which in turn increases the complexity in their control strategy. The component number includes both active and passive circuit elements of the topologies, which are based on the implementation for only two series-connected PV sub-modules. As observed in Table 2, the complexity of each topology increases with their control strategies, while the efficiency, cost and the losses in these topologies are more dependent on the number of active and passive components.

In general, the active bypassing techniques with DPP converters achieve higher energy yield from the PV modules, but also, they are complicated, as mentioned previously. Among all the discussed mitigation techniques, the DPP techniques perform better than the traditional bypass diode and other mitigation techniques, especially in efficiency, as compared in Table 2. Moreover, the active bypassing techniques also enable a simple MPPT control, as there is only one maximum. In all, the benchmarking provides guiding information when selecting the techniques according to applications.

It should be pointed out that the DPP architectures are relatively new and not matured enough, and thus they are not fully commercialized by the PV converter manufacturers. The main reason hindering the commercialization lies in the still relatively high cost of the DPP converters, which usually consist of many components (passive and active power devices) as summarized in Table 2. Nevertheless, with the development of power electronics, the DPP techniques or

other power electronic-based mismatch techniques will emerge. In that case, more module-level power converters will improve the energy harvesting from solar PV modules, and also bring higher reliability to the entire PV systems, potentially leading to reduced cost of PV energy.

5. Conclusions

In this paper, mismatch mitigation techniques for PV modules were discussed. Various types of mismatch effects were presented, which may occur in practice. Many passive and active techniques were overviewed in this paper. Their operational principles were elaborated briefly. Simulations were provided for selected techniques. The benchmarking results confirm that:

1) Passive techniques are simple in operation with low cost but not efficient in comparison to the active techniques, mostly based on power electronics.
2) Power electronic-based active techniques are used to maximize the output power and alleviate the mismatch effect. The active techniques are relatively complicated in operation with high cost but more effective, as most of them only process the differential or mismatch power between PV sub-modules.

Although several techniques were compared in terms of cost, efficiency, complexity, control strategy, etc, in this paper, it is not easy to select a specific mismatch mitigation technique. However, the benchmarking provided in this paper may initiate the development of new mismatch mitigation techniques for PV modules. Notably, with more advances in power electronics and lower cost in data storage, the next-generation PV modules will be highly power electronic-integrated, and they will become smart PV modules. In that regard, more module-integrated topologies/converters should be developed, which may be inspired from this review.

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