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Abstract: Among all converters, one of the most prominent technologies employed in multi-infeed ac/dc (MIACDC) smart grids is the modular multilevel converters (MMCs). The core part of the MIACDC grids is their dc-voltage power port. All MMC's components in a dc-voltage power port – which are capable of significantly impacting on the dynamics – are mathematically modelled in the space-phasor representation using the rotating *dq*-frame. Afterwards, the effects of each submodule capacitors and arm inductors on the dc-voltage power port's dynamics are investigated and analysed, separately. This paper mathematically shows that the former is affecting the low-frequency range of the bandwidth, and the latter is impacting on the high-frequency one. Moreover, this paper demonstrates that a robust, optimal controller synthesized by the μ-analysis is a good candidate to induce both robust stability and performance in an MMC-based dc-voltage power port. In order to illustrate the contributions of this article, detailed mathematical analyses; comparative results simulated by the switching model of MMC; and experimental results produced by a test rig, which is able to examine the transient performance of an MMC-based dc-voltage power port, are provided. For comparison, the results of the PI-Lead controller and those of another controller optimally synthesized have been provided.

1 Introduction

Under the paradigm of smart grids, the power systems have significantly been moved toward integrating more renewables in dc shape, battery energy-storage systems etc. and forming fully integrated power and energy system (FIPESs). In FIPESs, dc power networks are merged into ac grids, entitled multi-infeed ac/dc (MIACDC) power grids – e.g. multi-terminal dc (MTDC) grids, super grids, meshed high-voltage direct current (HVDC) grids, and hybrid ac/dc modernised microgrids [1–9]. Different technologies are being employed in MIACDC grids, among which the modular multilevel converter (MMC) is one of the emerging and pioneering technologies in the power electronics industry nowadays. In fact, among all converters' topologies, two-level and neutral-point-clamped (NPC) ones are giving ground to the MMC technology for various technical reasons as MMC has significantly been developed in the power industry [9–28].

In all technologies, the ac-side and dc-side dynamics are highly coupled. Indeed, the stability and transient performance of the dc side and those of the ac side are highly interconnected. Also, the employed control strategies can vary from communication-based controllers to master-based regulators with no need for communication infrastructures as well as autonomous control methods. The dc-voltage power port is the vital section of MIACDC grids, which enables us to regulate the dc voltage using the aforementioned control strategies (or other ones) in MIACDCs [29, 30].

According to the space-phasor representation and control theory of voltage-sourced converters (VSCs), the instantaneous power of all different energy-storing components plays a key role in the whole dc-voltage dynamics – as per VSCs' control techniques (see [30–33] and references therein). Although both recent and early research works on grid-tied MMCs and their topologies/controls have conducted comprehensive studies associated with the operation and controls of these converters [10–28], none of them have proposed any control design strategy for the MMC-based dc-voltage power ports considering their robust operating. There is a need to synthesise a controller – which is able to optimally and robustly control the dc voltage by these highly emerging converters and assure both robust stability and performance.

In this paper, it will be demonstrated that based on practical values of different energy-storing elements in an MMC, the amount of the energy stored in all submodule capacitors can easily be reached to that of the dc-link capacitor of the MMC, and also, the amount of the energy stored in the arm inductors can reach half of the energy stored in the ac-side filter. Moreover, a compressive dynamic model which is taking into account the instantaneous power of every capacitive in addition to inductive elements inside of the MMC-based dc-voltage power port is investigated and extracted in this paper. It has been shown that inductive elements, i.e. arm inductors, influence the dc-voltage dynamics in the high-frequency range of the bandwidth. However, capacitive elements, i.e. submodule's capacitors, affect the dynamics in the low-frequency range of the bandwidth. When compared to the two-level VSC with the same capacity, the converter-side voltage, dc-link capacitor, and ac-side filter, the arm inductors are forcing the minimum/non-minimum phase zero, for inversion/rectification mode, to move closer to the imaginary axis (i.e. the jω-axis), and submodule capacitors are pushing the dominant pole closer to the jω-axis for both inversion and rectification modes according to the provided mathematical analysis. In other words, for the non-minimum phase zero, the zero is getting stronger, so the phase reduction increases, and for the close-to-jω-axis pole, the pole is getting closer to the unstable region. Consequently, both aforementioned phenomena endanger the stability of the closed-loop system and make the controller synthesis more critical [30].

Moreover, there are variations in the MMC operating points (including operating modes), which result in the creation of and changes in the non-minimum phase dynamics of the MMC. Especially, when there are steep changes in an operating point, the dynamics of the non-minimum phase zero – which is produced by the energy stored in both the ac-side and arm filters – dominates the dc-side's dynamics. Also, the number of capacitors connecting to the dc link is changing after generating each switching signal; it also leads to a variation of the equivalent capacitor, which affects

both stability and transient performance of the dc-voltage dynamics. It is noteworthy that the equivalent capacitor will be affected and altered not only by the number of submodule capacitors connected to the dc link during each switching signal but also by the connection/disconnection of different devices to/from the dc network owing to their front-end capacitors employed as the dc filter. Finally, the disturbance signals influencing the dc-voltage dynamics are external injected/absorbed power (or equivalently current) into/from the dc network, along with the three-phase summation of the square of circulating currents and its derivatives. As a result, if the methodology suppressing the circulating current fails to act and/or fails to perform well, the dc-voltage performance is getting poor [9, 15, 24].

The contributions of this paper are as follows. (i) This paper proposes a thorough dynamic model of the MMC-based dc-voltage ports (using the space-phasor representation in the *dq* frame) – showing various detailed dynamics, their impacts, and effective disturbances signals in the dynamics described in the *dq* frame. (ii) On the basis of the captured model, this paper employs an optimal controller proposed for having robust performance criteria using classical robust control theories, because of the existing changes in the non-minimum phase zeros as well as pole locations which are significant. (iii) Furthermore, this research guarantees the robust performance and stability of the dc-voltage dynamics with respect to the changes in the MMC operating point, equivalent dc-link capacitance, and the energy stored in the arm inductors in order to achieve the robustness and stability in the MIACDC power systems. (iv) Last but not least, this paper also minimises the H_∞ norm of the closed-loop transfer function using the proposed dc-voltage controller to attenuate the effect of all impactful disturbance signals captured here – e.g. external currents, the square of the circulating currents, their derivatives etc. – as much as possible. This is another key contribution of this paper to MMC-based dc-voltage power ports by which we can tackle and address the stated problems associated with them.

The remainder of this paper has been structured as follows. The dc-voltage power port built by the MMC technology is mathematically modelled in Section 2. In Section 3, the small-signal linearised model of the MMC utilised in the dc-voltage power port structure is physically analysed, eigenvalue studies and frequency response are provided, and the small-signal linearised model is compared with that of a typical two-level VSC. In Section 4, the process of controller design using the space-phasor representation in the *dq* frame is provided; the proposed controller using DK-iteration method to optimally design a μ-synthesis robust controller is also studied. Section 5 provides relevant case studies required and conducts simulations studies. To test the functionality of the proposed controller, comparative simulation results are produced in order to assess the transient performance of the proposed robust controller. Finally, for further evaluation of the proposed controller, Section 5 provides experiments conducted by a laboratory-scale setup – which is able to examine the dynamics under test.

2 Mathematical model of the MMC-based dc-voltage power port

A typical representative MMC-based dc-voltage power port employed in MIACDC grids is shown in Fig. 1. The system parameters are given in the Appendix, and for simplicity and pure focus on the dc-voltage power port dynamics – considering the instantaneous power of ac-side filters, it is supposed that the dc-side filter is a single capacitor [30]. Consequently, C_{eq} is the equivalent capacitor reflected into the dc side as a representative capacitance of all other devices and components forming the MIACDC or MTDC grids. As in previous cases [29, 30, 34, 35], grid-connected VSC working as the dc-voltage power port should be applied to control the dc-link voltage to prevent conflict between controllers employed in MIACDC grids.

To extract the whole dynamics of the MMC-based dc-voltage power port, all components taking part in exchanging the energy between the dc side and the ac grid have to be taken into account. To this end, the first section shows the non-linear mathematical model of MMC-based dc-voltage power port considering the instantaneous power of all energy-storing elements in the configuration as shown in Fig. 1. Afterwards, the second section has been allocated to find and formulate the linearised small-signal model of the total dynamic system around a general operating point based on the approach provided and presented in [30].

2.1 Dynamic model of MMC-based dc-voltage power port

Considering Fig. 1, (1) describes the energy balance across the reflected equivalent capacitor of dc grid in the grid-connected VSC in MMC-based dc-voltage power port [30]. All 'P's in (1) are representing the instantaneous power of different parts, configuring the MMC-based dc-voltage power port

$$\begin{cases} P_{\text{ext}} - P_{\text{R}_{\text{loss}}} - P_{\text{C}_{\text{eq}}} = P_{\text{DC}} \\ P_{\text{DC}} = P_{\text{energy-storing-components-in-MMC}} + P_{\text{t}}, \\ P_{\text{t}} = P_{\text{AC-side-filter}} + P_{\text{grid}} \end{cases} \tag{1}$$

where P_{ext} is the instantaneous power being injected into the dc energy pool by other components and devices connected to the dc grid (which is negative when it is absorbed from the dc energy pool); P_{Rloss} is the MMC power losses modelled via an R_{loss} (which models the MMC power loss); P_{Ceq} is the instantaneous power of the equivalent capacitor lumped in the dc grid; P_{DC} is the instantaneous power converted to the ac shape by MMC; $P_{\text{energy-storing-components-in-MMC}}$ is the instantaneous power stored in all submodule capacitors commanded to be turned on/off by the switching signals, in addition to the instantaneous power stored in the arm inductor; P_{t} is the instantaneous power of the power converted to the ac shape; $P_{\text{AC–side–filter}}$ is the instantaneous power of ac-side filter; and P_{grid} is the instantaneous power injected into the grid – where it can be negative when it is absorbed from the grid.

Having deeply looked at (1), from a classical control perspective, it is obvious that P_{ext} is an external disturbance, which should be rejected by the controller of the dc-voltage power port considering its dynamics. Equation (1) can be summarised in (2) accordingly

$$\begin{aligned} P_{\text{ext}} - P_{\text{R}_{\text{loss}}} - P_{\text{C}_{\text{eq}}} = P_{\text{energy-storing-components-in-MMC}} \\ + P_{\text{AC-slide-filter}} + P_{\text{grid}}, \end{aligned} \tag{2}$$

where P_{Rloss}, P_{Ceq}, $P_{\text{AC–side–filter}}$, and P_{grid} are calculated using (3) as provided in [31, 35]

$$\begin{cases} P_{\text{R}_{\text{loss}}} = \dfrac{V_{\text{DC}}^2}{R_{\text{loss}}} \\ P_{\text{C}_{\text{eq}}} = 0.5C_{\text{eq}}\dfrac{\text{d}V_{\text{DC}}^2}{\text{d}t} \\ P_{\text{AC-side-filter}} = 0.75L\dfrac{\text{d}((I_d)^2 + (I_q)^2)}{\text{d}t}, \\ \qquad +1.5(R + r_{\text{on}})((I_d)^2 + (I_q)^2) \\ P_{\text{grid}} = 1.5I_d v_{sd} \end{cases} \tag{3}$$

where (see (4)) . C_{eq} is the equivalent capacitor seen from the dc network (which is affected and made by connection/disconnection of different devices to/from the dc link); $S_{\text{upper–SM \#}i}$ and $S_{\text{lower–SM \#}i}$ are the switching signal commands to the ith submodule in the upper and lower sections, respectively; they are '1' when $S_{1\text{–SM \#}i}$ is '1' (and $S_{2\text{–SM \#}i}$ is thus '0') and they are '0' when $S_{1\text{–SM \#}i}$ is '0' (and $S_{2\text{–SM \#}i}$ is thus '1') in the upper and lower sections, respectively; L_{arm} is the inductance of the arm inductor; and R_{arm} is its resistance. To find the V_{DC}'s dynamics, the calculation of $P_{\text{energy–storing–components–in–MMC}}$ is the key to model and analyse this paper. $P_{\text{energy–storing–components–in–MMC}}$ is calculated according

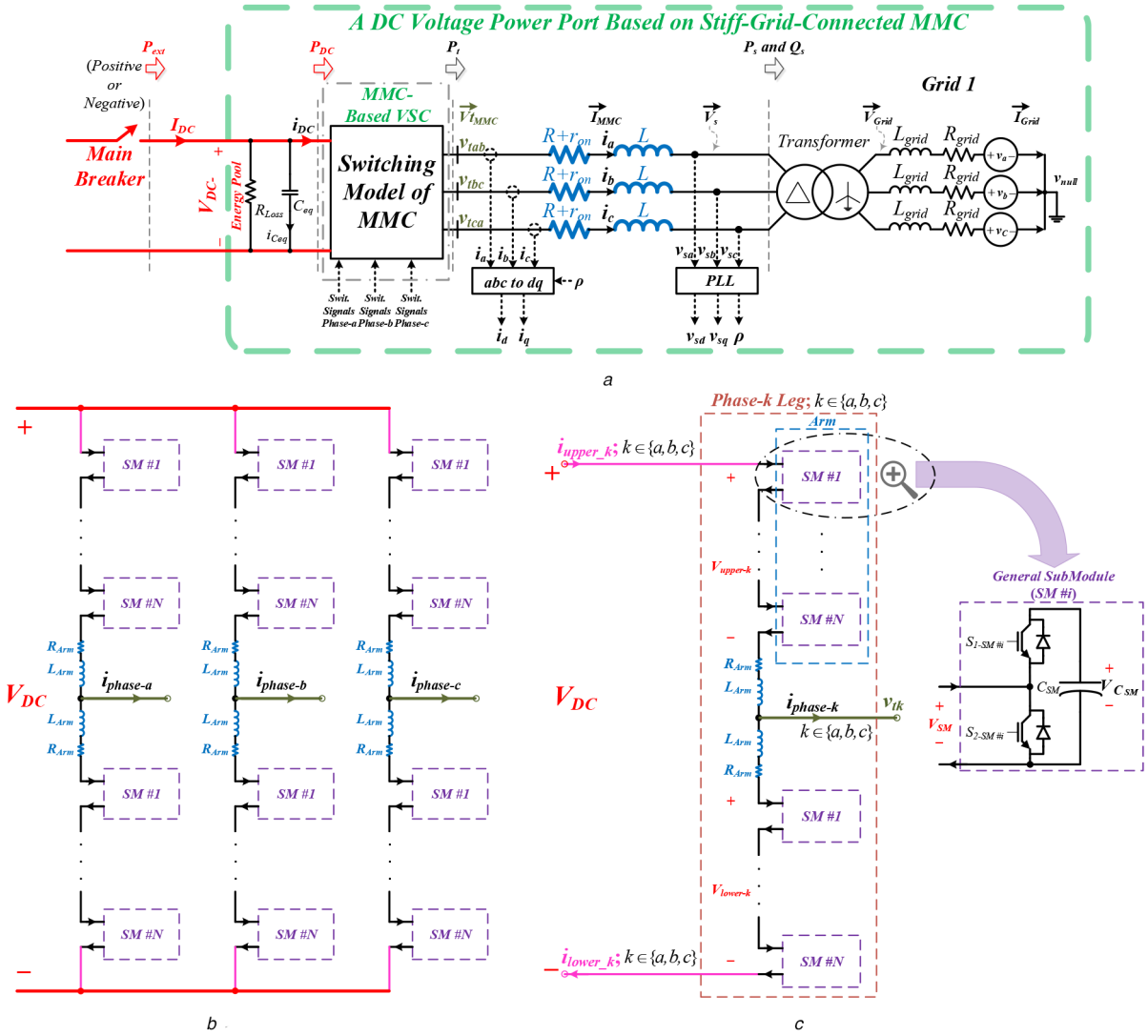

Fig. 1 *Grid-connected MMC*

(a) dc-Voltage power port made by the MMC technology including some of the important space-phasor variables, ***(b)*** **F**ull configuration of an MMC, ***(c)*** Detailed MMC's leg k (which is associated with either phase-a, -b, or -c) in the dc-voltage power port

$$
\begin{aligned}
V_{\mathrm{DC}} &= \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{upper-SM\#}i}V_{C_{\mathrm{upper}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{a}} + R_{\mathrm{arm}}i_{\mathrm{upper-phase-a}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{upper-phase-a}}}{\mathrm{d}t} \\
&\quad + \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{lower-SM\#}i}V_{C_{\mathrm{lower}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{a}} + R_{\mathrm{arm}}i_{\mathrm{lower-phase-a}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{lower-phase-a}}}{\mathrm{d}t} \\
&= \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{upper-SM\#}i}V_{C_{\mathrm{upper}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{b}} + R_{\mathrm{arm}}i_{\mathrm{upper-phase-b}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{upper-phase-b}}}{\mathrm{d}t} \\
&\quad + \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{lower-SM\#}i}V_{C_{\mathrm{lower}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{b}} + R_{\mathrm{arm}}i_{\mathrm{lower-phase-b}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{lower-phase-b}}}{\mathrm{d}t} \\
&= \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{upper-SM\#}i}V_{C_{\mathrm{upper}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{c}} + R_{\mathrm{arm}}i_{\mathrm{upper-phase-c}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{upper-phase-c}}}{\mathrm{d}t} \\
&\quad + \underbrace{\sum_{i=1}^{N}\left(S_{\mathrm{lower-SM\#}i}V_{C_{\mathrm{lower}-k-\mathrm{SM\#}i}}\right)}_{\text{for phase}-\text{c}} + R_{\mathrm{arm}}i_{\mathrm{lower-phase-c}} + L_{\mathrm{arm}}\frac{\mathrm{d}i_{\mathrm{lower-phase-c}}}{\mathrm{d}t},
\end{aligned}
\tag{4}
$$

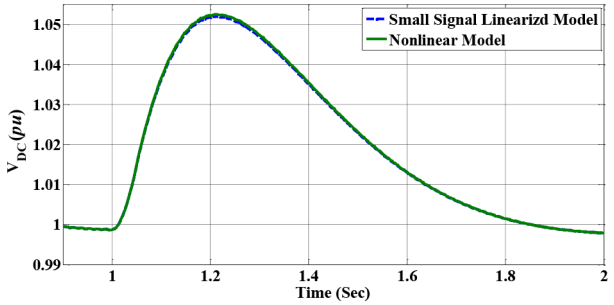

Fig. 2 *Model validation of (6) for 5% change in the operating point of MMC working in the inversion mode at nominal power – with the parameters specified in Table 1*

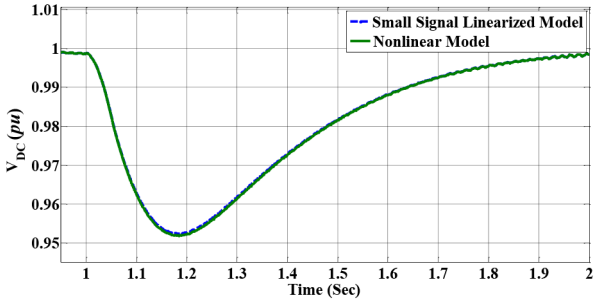

Fig. 3 *Model validation of (6) for 5% change in the operating point of MMC working in the rectification mode at nominal power – with the parameters specified in Table 1*

to the instantaneous power of both arm inductors, and all capacitors switched in the upper part of the leg in addition to the lower one. As a result, (5) is able to formulate $P_{\text{energy–storing–components–in–MMC}}$

$$
\begin{aligned}
&P_{\text{energy-storing-components-in-MMC}} \\
&= 0.5\sum_{k=a}^{c}\sum_{i=1}^{N} S_{\text{upper-SM\#}i} C_{\text{upper-}k\text{-SM\#}i} \frac{\mathrm{d}V^2_{C_{\text{upper-}k\text{-SM\#}i}}}{\mathrm{d}t} \\
&\quad +0.5\sum_{k=a}^{c}\sum_{i=1}^{N} S_{\text{lower-SM\#}i} C_{\text{lower-}k\text{-SM\#}i} \frac{\mathrm{d}V^2_{C_{\text{lower-}k\text{-SM\#}i}}}{\mathrm{d}t} \\
&\quad +0.5\frac{\mathrm{d}\left\{\sum_{k=a}^{c}(L_{\text{Arm}} i^2_{\text{upper-}k}) + \sum_{k=a}^{c}(L_{\text{arm}} i^2_{\text{lower-}k})\right\}}{\mathrm{d}t} \\
&\Rightarrow P_{\text{energy-storing-components-in-MMC}} \\
&= 0.5\sum_{k=a}^{c}\sum_{i=1}^{N} S_{\text{upper-SM\#}i} C_{\text{upper-}k\text{-SM\#}i} \frac{\mathrm{d}V^2_{C_{\text{upper-}k\text{-SM\#}i}}}{\mathrm{d}t} \\
&\quad +0.5\sum_{k=a}^{c}\sum_{i=1}^{N} S_{\text{lower-SM\#}i} C_{\text{lower-}k\text{-SM\#}i} \frac{\mathrm{d}V^2_{C_{\text{lower-}k\text{-SM\#}i}}}{\mathrm{d}t} \\
&\quad +0.5\frac{\mathrm{d}(0.75 L_{\text{arm}} I^2)}{\mathrm{d}t} + 0.5\frac{\mathrm{d}\left\{\sum_{k=a}^{c}[L_{\text{arm}} 0.5 i^2_{\text{circulating-phase-}k}]\right\}}{\mathrm{d}t},
\end{aligned}
\tag{5}
$$

where $C_{\text{upper–}k\text{–SM }\#i}$ and $C_{\text{lower–}k\text{–SM }\#i}$ are the capacitors connected to the ith submodule in the upper and lower legs, respectively, and $i_{\text{circulating–phase–}k}$ are the circulating current associated with *phase-k*, whose k can be either a, b, or c.

After mathematical manipulations, the small-signal linearised dynamics of MMC-based dc-voltage power port is obtained by (6) – see (6), where '~' indicates the perturbed signal around the *equilibrium point* of each variable; $k_{\text{upper–}m}$ and $k_{\text{lower–}m}$ are integer numbers in the set of {1, 2, 3, …, N} based on the MMC's modulation indexes – it is noteworthy that $k_{\text{upper–}m}$ and $k_{\text{lower–}m}$, according to the operation principle of MMCs, are not equal [36] – I and V are the general values associated with the amplitude of the space vectors of the ac current injected into the grid and MMC's ac-side terminal voltage, i.e. $\boldsymbol{I}_{\text{Grid}}$ and $\boldsymbol{V}_{\text{t–MMC}}$, respectively; I_{d0} and I_{q0} are the *equilibrium points* of the d and q components of $\boldsymbol{I}_{\text{MMC}}$; V_{sd0} and I_{q0} are the *equilibrium points* of the d and q components of $\boldsymbol{V}_{\text{s}}$, i.e. low-side transformer's voltage at the point of common coupling (PCC); and $\mathscr{L}$ is the Laplace transform operator.

Table 1 Parameters of the MMC in Fig. 1 and Zone I in Fig. 9

rated power	100 MVA
grid 1 voltage	138 kV at 60 Hz
short-circuit ratio at the PCC	5.00
converter-side ac voltage	25.00 kV
transformer voltage rating	138/25 kV
transformer power rating	100 MVA
transformer leakage inductance	0.05 pu
transformer loss	0.01 pu
capacitance per cell ($C_{\text{SM \#}i}$)	2000 μF
number of cells (N)	20
carrier frequency (f_{s})	800 Hz
$C_{\text{DC–link}}$	150 μF
P_{loss} and corresponding R_{loss}	0.95 MW/1769.5 Ω
switch resistance	1.0 mΩ
diode resistance	1.0 mΩ
$r_{\text{on}} + R$ and L	30 mΩ and 6.69 mH
R_{arm} and L_{arm}	20 mΩ and 4.00 mH
parameters of current PI controller	$K_{\text{p}} = 6.69$ Ω and $K_{\text{i}} = 30$ Ω/s
parameters of PLL PID controller	$K_{\text{p}} = 180$; $K_{\text{i}} = 3200$; and $K_d = 1$
parameters required to find the nominal transfer function $G(s)$ in (7)	$I_{d0} = -1.633$ kA and $C_{\text{eq0}} = 3.8$ mF

The first term of (6) is the linear time-invariant (LTI) transfer function of the non-linear plant, which should be controlled around general operating points, as described in (8). The second, the third, the fourth, the fifth, the sixth, and the seventh terms of (6) are acting as disturbance signals for controlling the small-signal linearised transfer function according to the classical control theory. Among them, the second, the fourth, and the fifth terms are significantly affecting the output according to the typical physical and practical parameters of MMC-based dc-voltage power port discussed in the Appendix.

2.2 Validation of the small-signal linearised dynamic model

For model validation purposes, the small-signal model is validated and compared with the non-linear model for two different transfer functions, which are generated by (6) around two values of the power associated with both nominal inversion and rectification modes of operation – with the parameters specified in Table 1 in the Appendix. Two cases have been considered; first, the corresponding transfer functions have been extracted from (6) considering the nominal I_{d0} in inversion mode. Then, a 5% change in the operating point is applied in order to increase the power, and the dynamic response of the dc voltage is captured. Second, the same procedure is applied and repeated for the rectification mode. Figs. 2 and 3 are demonstrating the model validation of (6).

Figs. 2 and 3 reveal that acceptable compatibility between the non-linear dynamic model and the small-signal linearised model extracted from the non-linear plant working at the nominal operating point, as expressed in (6), for both inversion and rectification mode, respectively. Indeed, both curves are very well-matched for both responses of the non-linear and linearised dynamic model. Thus, the results show the validity of the linearised model for which the LTI robust controller will be synthesised because of the perfect match observed between the response of the small-signal linearised model extracted and the physical plant dynamics.

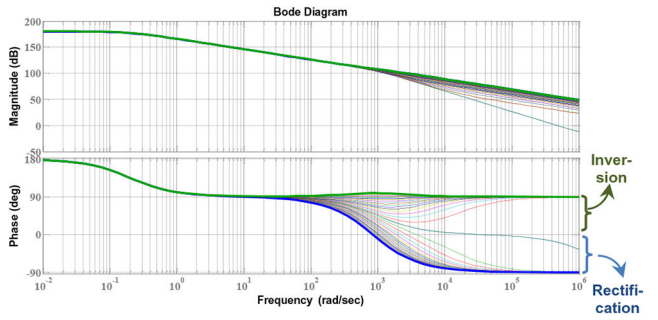

Fig. 4 *Bode diagram of (6) for the operating point variation from inversion to rectification mode – with the parameters specified in Table 1 in the Appendix*

3 Dominant dynamics of the MMC-based dc-voltage power ports

3.1 Physical analysis of (6)

With respect to (6), it reveals that the instantaneous power stored in arm inductors interacts with dc-voltage dynamics in the same way as the ac filter inductor. Indeed, since the value of arm inductors is comparable with that of the ac-side filter, as reported in the Appendix, its stored energy should be considered from the physics perspective, as also shown in (6), when it is interacting with dc-side power and its dynamics.

3.2 Eigenvalues and frequency response analysis

The frequency response of (6) is shown in Fig. 4 to illustrate the effect of different values of I_{d0} on the small-signal dynamics while other parameters are kept fixed to their nominal values stated in the Appendix. Also, the value of $2\big((3/8k_{\text{upper}-m})+(3/8k_{\text{lower}-m})\big)C_{\text{SM}}-$ defined and named as $C_{\text{SM},\,k_{\text{upper/lower}-m}}-$ is easily able to reach and be comparable with that of the capacitor connected to the dc side of a typical (see (6)) dc-voltage power port made by MMC-based converter technology (according to the value of different parameters specified in the Appendix). As a result, C_{eq} is dramatically altered not only by connecting/disconnecting new devices to/from the dc energy pool but also by changing the value of $C_{\text{SM},\,k_{\text{upper/lower}-m}}$. It should be pointed out that the value of $C_{\text{SM},\,k_{\text{upper/lower}-m}}$, which is affected by operating point variations, is reflected by the value of k_m; the effect of the value of $C_{\text{SM},\,k_{\text{upper/lower}-m}}$ on the small-signal linearised model has been demonstrated in Fig. 5. Indeed, the value of $C_{\text{SM},\,k_{\text{upper/lower}-m}}$ is altered from zero to the nominal value, and subsequently, its effect on (6) is investigated in order to reveal the impact of the capacitive energy-storing components on the dynamics of the MMC-based dc-voltage power port when compared with the usual two-level-VSC-based technology.

Also, $C_{\text{SM},\,k_{\text{upper/lower}-m}}$, L_{arm} is another energy-storing component, which is inductive and similarly has an influence on the dc-voltage power based on MMC technology as (6) shows. The bode diagram, as well as the zero map of (6), has been illustrated in Fig. 6 to take into account the L_{arm}'s impact on the dynamics of the MMC-based dc-voltage power port when compared with the usual two-level-VSC-based technology.

4 Proposed controller for the vector control of the MMC-based dc-voltage power port

It is noteworthy that this paper takes advantage of vector control of the MMC-based dc-voltage powers – which requires some practical considerations. First, to make the active and reactive power controls decoupled, the *dq* frame has been used. The use of the *dq* frame requires phase-locked loop (PLL), whose performance/stability is impacted by the grid weakness and distortions. In this paper, we have benefited from all solutions to the aforementioned practical considerations. This work does not contribute to those issues and gets benefit from currently available

$$
\begin{aligned}
&\tilde{V}_{\text{DC-S}}(s)\\
&=\underbrace{\frac{-\left[0.75L_{\text{arm}}+2L_{\text{arm}}^2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}+1.5L\right]I_{d0}R_{\text{loss}}s-(1.5R_{\text{arm}}+3(R+r_{\text{on}}))I_{d0}R_{\text{loss}}-1.5V_{sd0}R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\tilde{I}_d(s)}_{\text{the first term}}\\
&+\frac{R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\tilde{P}_{\text{ext}}(s)\\
&-\frac{\left[0.75L_{\text{arm}}+2L_{\text{arm}}^2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)+1.5L\right]I_{q0}R_{\text{loss}}s-(1.5R_{\text{arm}}+3(R+r_{\text{on}}))I_{q0}R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\tilde{I}_q(s)\\
&-\frac{0.25L_{\text{arm}}R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\mathscr{L}\left(\sum_{k=a}^{c}\frac{\mathrm{d}\tilde{i}^2_{\text{circulating}-\text{phase}-k}}{\mathrm{d}t}\right)\\
&-\frac{0.5R_{\text{arm}}R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\mathscr{L}\left(\sum_{k=a}^{c}\tilde{i}^2_{\text{circulating}-\text{phase}-k}\right)\\
&-\frac{0.5L_{\text{arm}}^2R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}\right)C_{\text{SM}}\right]R_{\text{loss}}s+1}\mathscr{L}\left(\sum_{k=a}^{c}\frac{\mathrm{d}\left(\frac{\mathrm{d}\tilde{i}_{\text{circulating}-\text{phase}-k}}{\mathrm{d}t}\right)^2}{\mathrm{d}t}\right)\\
&\underbrace{+\frac{R_{\text{loss}}}{0.5\left[C_{\text{eq}}+2\left(\frac{3}{8k_{\text{upper}-m}}+\frac{3}{8k_{\text{lower}-m}}C\right)_{\text{SM}}\right]R_{\text{loss}}s+1}\mathscr{L}\left(f\left(\frac{\mathrm{d}\tilde{V}^2}{\mathrm{d}t},\,\tilde{i}_{\text{circulating}-\text{phase}-k}\right)\right)}_{\text{all disturbance signals}}.
\end{aligned}
\tag{6}
$$

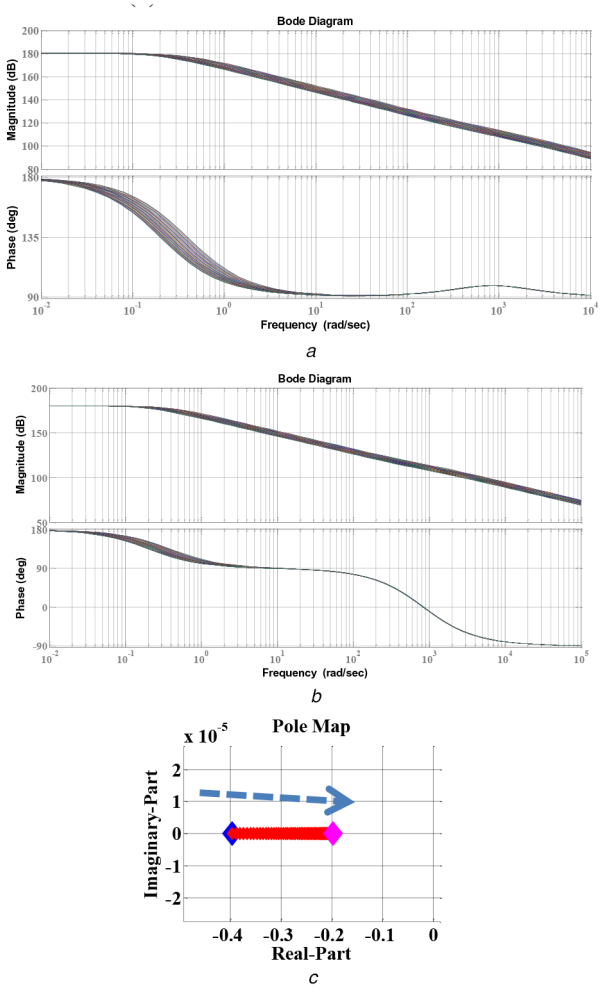

Fig. 5 *Effect of the value of $C_{SM,k_{upper/lower-m}}$ on (6)*

(a) Bode diagram for the nominal power in inversion mode, ***(b)*** Bode diagram for the nominal power in rectification mode, ***(c)*** Pole map in both inversion and rectification modes; the arrow shows the effect of the $C_{SM,\,k_{upper/lower-m}}$ increase – with the parameters specified in Table 1 in the Appendix

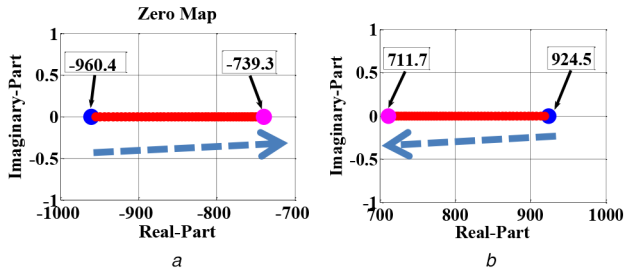

Fig. 6 *Effect of the value of L_{arm} on (6)*

(a) Zero map in inversion mode, ***(b)*** Zero map in rectification mode – with the parameters specified in Table 1 in the Appendix (the arrow shows the effect of the L_{arm} increase)

solutions proposed by the industry and academia [30, 31]. For example, this paper considered that the grid connected to the MMC is strong, and if not, the PLL structure and control gains have been adjusted accordingly [37–40]. Also, the PLL control is able to effectively reject the distortions of grid voltage to feed the *dq*-frame structure [30, 37–40]. Finally, not least, there are effective feedforward signals embedded in the *dq*-frame control architecture, which are improving the control performance [30, 41]. All of these assure that the control response is not affected by other possible factors, so this paper contributes to the MMC-based dc-voltage power port's performance improved by the use of a novel control algorithm.

The proposed structure is a controller with one degree of freedom; hence, both reference tracking and disturbance rejection capabilities have to be simultaneously guaranteed. As a result, the controller is synthesised and designed according to the internal model principle in order to guarantee both reference tracking and disturbance rejection of step signals both at the input and at the output [42]. The proposed control structure based on μ-analysis algorithm is demonstrated in Fig. 7. Fig. 7*a* shows the proposed control structure and Fig. 7*b* reveals the procedure of synthesising μ-analysis robust optimal controller.

The μ-synthesis controller using the DK-iteration method is employed to optimally synthesise the controller. The reason behind the fact is that one of the most common ways to optimally reject the disturbance signal affecting the output is to minimise the H_∞ norm from the filtered disturbance signals to the filtered output in the presence of weighted uncertainty using the structured singular values μ-synthesis. Therefore, the μ-synthesis approach is to apply the DK-iteration method [43, 44].

It is noteworthy that though the polynomial method and adaptive control suggested and proposed in [45–47] can be a candidate and be used for designing the robust dc-link voltage control [35], it is not applicable to the problem addressed in this paper. The reason why that approach is not suitable is that the whole problem can be solved using optimal DK-iteration method directly. This is true because the range of I_{d0} variation is not very wide, and therefore, the changes in C_{eq} can be covered and considered along with I_{d0} variations. The following will discuss the procedure of building Fig. 7*b*.

All possible transfer functions have randomly been generated by MATLAB to have one structure that models all changeable variables, as discussed in Section 3. The uncertain small-signal linearised system expressed by (6) includes three uncertain elements, which are all coefficients of the numerator in addition to the first derivative coefficient of the denominator. All stated coefficients are affected by I_{d-0}, $C_{SM,\,k_{upper/lower-m}}$, and C_{eq}. To find the optimal solution for the given robust controller synthesis, it is often appropriate to simplify the uncertainty model while approximately retaining its overall variability for the purpose of optimal feedback synthesis, 60 random samples of all possible transfer functions changing within uncertain coefficients have been generated, and then, nominal transfer function and its related unmodelled dynamics have been extracted using the MATLAB Robust Control Toolbox [43, 44]; they are referred to as $G(s)$ and $W(s)$ in Fig. 7*b*, respectively, and according to the parameters reflected in the Appendix, $G(s)$ and $W(s)$ are found as (7) and (8); the used parameters with which transfer function $G(s)$ has been extracted are given in the Appendix

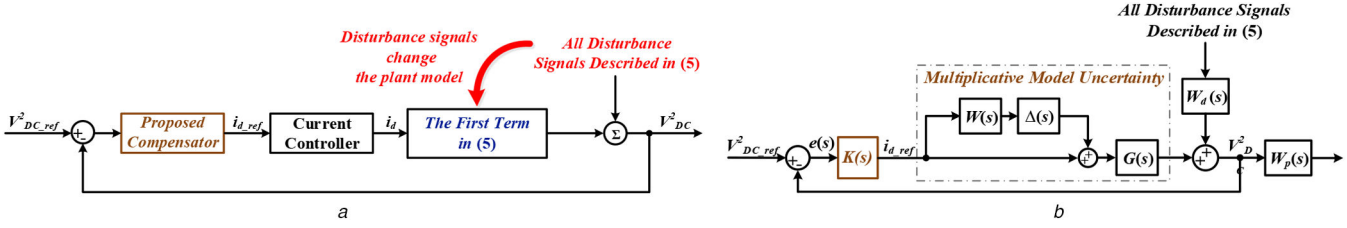

Fig. 7 *Proposed dc controller*

(a) Employed plant model for the controller design of MMC-based dc-voltage power port, ***(b)*** Procedure of modelling the discussed plant uncertainties for synthesising the robust, optimal controller based on μ-analysis

$$G(s) = \frac{1.258 \times 10^{+8} s - 1.366 \times 10^{+11}}{s^2 + 1003s + 2643} \tag{7}$$

$$W(s) = \frac{3.304s^2 + 6.322s + 2.912}{s^2 + 5.668s + 2.68} \tag{8}$$

In addition, the employed transfer functions $W_d(s)$ and $W_p(s)$ in the process of robust optimal controller synthesis are given by the equations below:

$$W_d(s) = \frac{10^3}{s + 10^{-3}} \tag{9}$$

$$W_p(s) = \frac{10^3}{s + 10^{-3}} \tag{10}$$

According to the proof provided in [43, 44], the synthesised controller based on the DK-iteration method guarantees both robust performance and stability with varying coefficients affected by alteration of I_{d-0}, $C_{\text{SM, }k_{\text{upper/lower}-m}}$, and C_{eq} provided that $G(s)$ is chosen as (7) and $W(s)$ is selected as (8). In addition, $W_d(s)$ is selected using (9) to reject P_{ext} at low frequencies as much as possible by minimising the H_∞ norm from disturbance to the output. Besides, in order to induce internal model dynamics and, thus, facilitate a simple control design with appropriate transient performance, $W_p(s)$ is selected to be (10).

Robust controller synthesis toolbox has been subsequently employed to search and extract the optimal controller $K(s)$ using the DK-iteration method. The controller $K(s)$ provided in (11) has been designated using the robust controller design approach via the DK-iteration method and model order reduction algorithms [43] (see (11)) . The synthesised controller using (11) is a single transfer function applied in the one-degree-of-freedom structure, as depicted in Fig. 7*a*, which simplifies and facilitates the utilisation on practical controller processors. Also, from the perspective of implementation, it is relatively easy to employ commercial-grade signal processors for programming the fourth-order transfer function as it is the case in (11) [35].

Fig. 8 reveals that the overall closed-loop system including MMC with the proposed control algorithm is robustly stable considering the effect of the system parameters mismatch. It also demonstrates that it is not only robust stable but also robust performance since the bode plot – as well as pole–zero map – of the closed-loop system stays in an almost fixed region. Moreover, the counterpart of Fig. 8 (which compares the closed-loop system when including regular proportional–integral (PI)-lead controller instead of the proposed one) has been provided in Section 5.2 – where this paper compares the PI-lead controller response with that of the proposed controller.

5 Simulation results

5.1 Performance of the proposed controller

The complete system simulated consists of an MIACDC (or equivalently a multi-infeed HVDC) system built by the MMC-based technology, a wind energy generation system, and a battery energy-storage system (BESS) as it has been depicted in Fig. 9 – which is able to excite a wide range of all dynamics under test in an MIACDC architecture [31, 35]. Indeed, the MMC-based converter is functioning as the dc-voltage power port (denoted as Zone I) in order to test the functionality of the proposed controller. The other converter, denoted as Zone II, is working in the usual PQ-controlled mode in order to absorb/inject power from/into the dc energy pool. The third converter, denoted as Zone III, is able to mimic the lumped model of a group of renewable energy source,

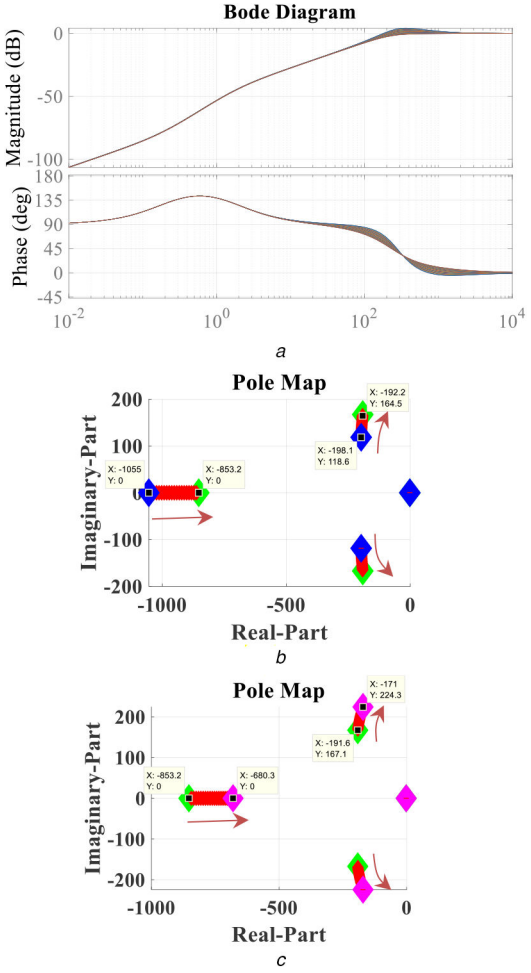

Fig. 8 *Stability study of the whole closed-loop system with the proposed controller*

(a) Disturbance rejection performance considering operating points in Fig. 4 and all parameter changes in Figs. 5 and 6, ***(b)*** Pole–zero map of the closed-loop system for part (a) when the operating mode changes from the nominal inversion (blue) to no power, also known as static compensator (STATCOM) mode (green), ***(c)*** Pole–zero map of the closed-loop system for part (a) when the operating mode changes from the STATCOM mode (green) to the nominal rectification (magenta)

which can produce dc power (e.g. the full-scale wind turbine system in this case) in order to build a super grid. Finally, the BESS has been employed in Zone IV in order to build up a thorough MIACDC system with complete devices, which are capable of exchanging energy. Comprehensive data and information including capacities, ac/dc-voltage levels, and parameters – which, for example, consist of the PI controller's gains – have been tabulated in the Appendix. The switching model of MMC-based VSC has been implemented in the MATLAB-Simulink environment in order to simulate more realistic events. The robust controller synthesised in (11) is implemented in order to assess its time response.

The following test scenarios have been simulated to validate the functionality of the proposed controller; it is noteworthy that in the following simulation results, the base power and the base dc voltage of the entire MIACDC power system are 100 MVA and 41.0 kV, respectively, for power system per unit (pu) calculation purposes:

Test cases I – In these test cases, Zone I first energises the whole MIACDC grid, then Zone III is generating 0.33 pu active power into the dc grid at $t = 2.0$ s. Then, Zone IV begins to discharge 0.33

$$K(s) = \frac{-24.6764 \times 10^{-10} s^4 - 0.0039 \times 10^{-5} s^3 - 0.0095 \times 10^{-5} s^2 - 0.0032 \times 10^{-5} s - 47.3541 \times 10^{-12}}{s^4 + 0.4122s^3 + 0.001103s^2 + 8.183 \times 10^{-7} s + 1.265 \times 10^{-10}} \tag{11}$$

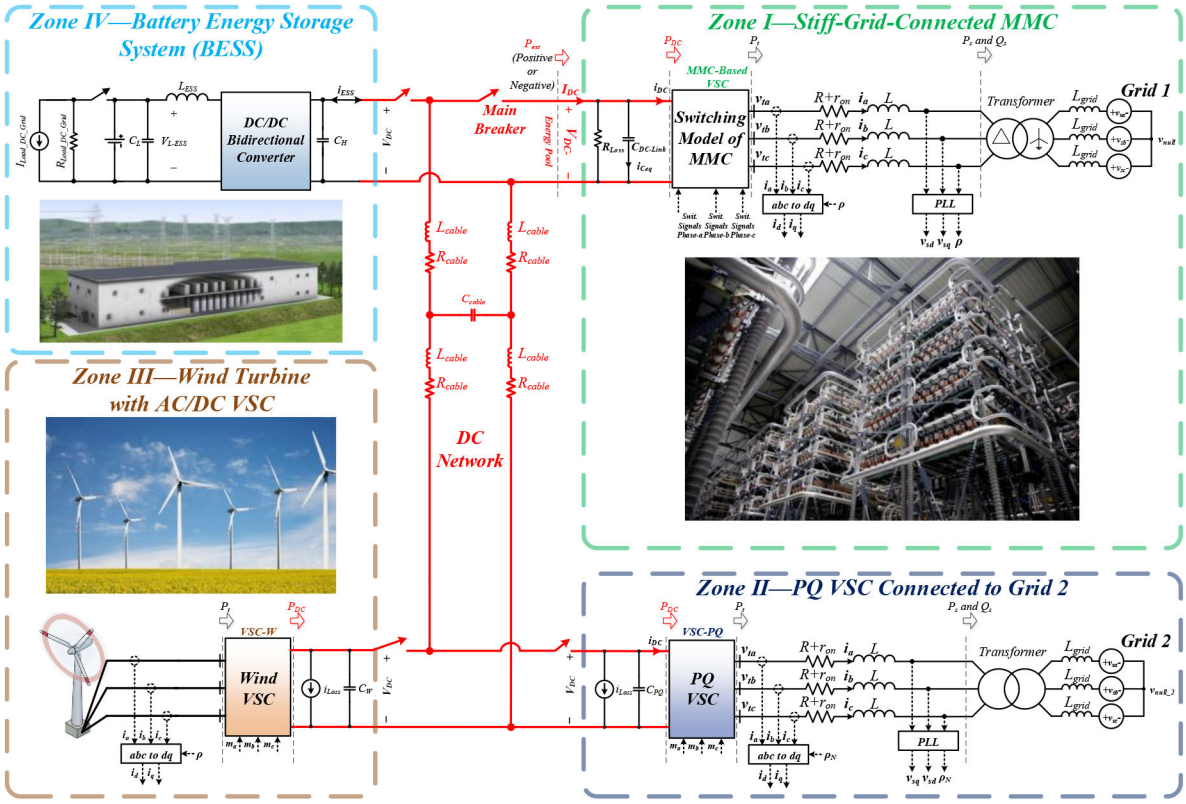

Fig. 9 *Comprehensive overview of the simulated power system for exciting a wide range of all dynamics [31, 35]*

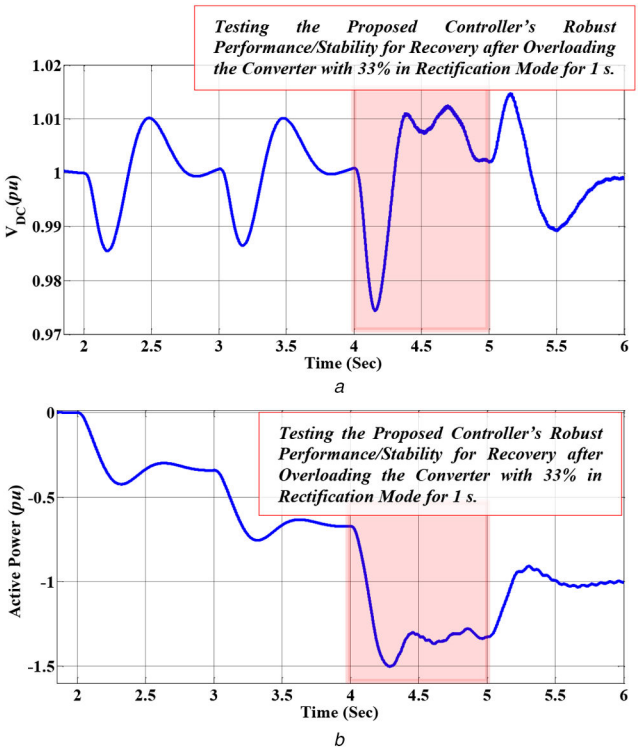

Fig. 10 *Simulation results of Fig. 9 with the proposed controller expressed by (11) for Test Cases I*
(a) dc Voltage, ***(b)*** Active power of MMC

pu active power from its stored energy into the dc network at $t = 3.0$ s. Afterwards, Zone II is injecting 0.67 pu power into its ac grid at $t = 4.0$ s in order to overload Zone I with 33.33% active power in rectification mode and test the functionality of the proposed controller to assess its transient performance in keeping the stability of dc-voltage dynamics. It is supposed that the protection system is not working, and the mentioned test is conducted in order to evaluate the controller response in case of sudden changes and variations in the active power (and hence the operating point). Finally, the set point of Zone II is altered to 0.34 pu at $t = 5.0$ s in order to inject 0.34 pu power into its ac grid and return to Zone I. This action will result in having the nominal active power in the rectification mode. It should be pointed out that in Test Cases I in order to better gauge the effectiveness of the proposed controller performance of optimally rejecting the disturbances signals associated with circulating currents – as per (6) – this paper deliberately does not take any action to control circulating current using additional controls. Fig. 10 depicts the time response of both dc-voltage dynamics and the active power of the MMC, i.e. Zone I, in pu in order to analyse the transient performance of the suggested controller. Accordingly, Figs. 11 and 12 demonstrate additional related simulation results related to Fig. 10 – which are line-to-line voltages, line currents, and upper/lower voltages.

Test Cases II – Here, Zone I first energises the whole MIACDC grid, then Zone II is absorbing 0.33 pu active power from the dc grid at $t = 2.0$ s. Then, Zone IV starts charging 0.33 pu from the dc network to charge its battery at $t = 3.0$ s. Afterwards, Zone II is absorbing 0.67 pu power from dc power system at $t = 4.0$ s in order to overload Zone I with 33.33% active power in the inversion mode and test the functionality of the proposed controller to appraise its transient performance in order to keep the stability of the dc-voltage dynamics. It is again supposed that the protection system is not working, and the mentioned test is conducted to examine the controller response in case of sudden changes and variations in the active power, and hence the operating point. Finally, the set point of Zone II is altered to 0.34 pu at $t = 5.0$ s in order to absorb 0.34 pu power from dc network and return to Zone I (and hence the nominal active power of Zone I in the inversion mode). Fig. 13 demonstrates the time response of both dc-voltage dynamics and the active power of the MMC, i.e. Zone I, in pu in order to judge the transient performance of the suggested regulator. It is noteworthy that also in Test Cases II in order to better gauge the effectiveness of the proposed controller performance of optimally rejecting the disturbances signals associated with circulating currents – as per (6) – this paper intentionally does not take any action to control circulating current using additional controls (similarly in Test Cases I). Accordingly, Figs. 14 and 15 demonstrate additional related simulation results related to Fig. 13

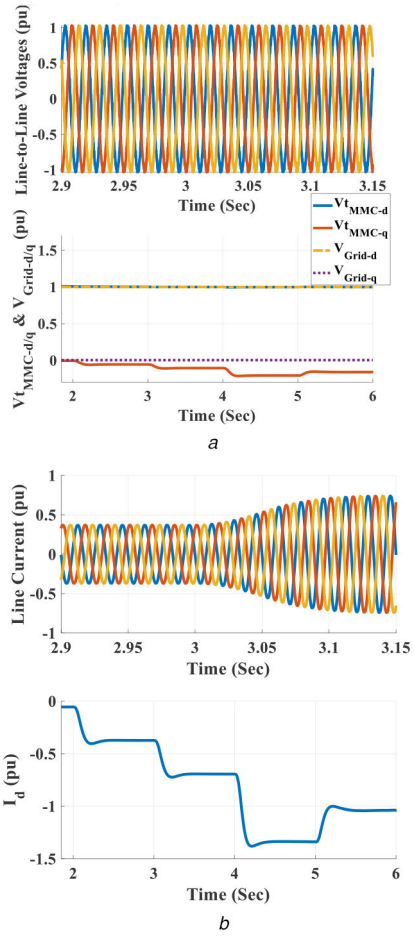

Fig. 11 *Voltage/current signals associated with Fig. 10*
(a) Sample of the line-to-line voltages (including its repetition in the *dq* frame and that of line-to-line grid voltages), ***(b)*** Sample of the line currents of MMC

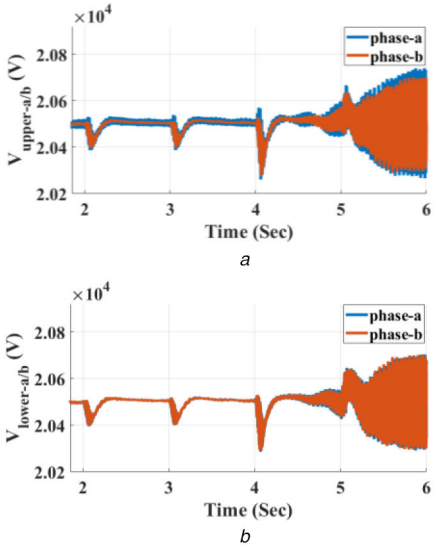

Fig. 12 *Arm voltages associated with Fig. 10;*
(a) MMC's upper arm of V_{upper}, ***(b)*** MMC's lower arm of V_{lower}

– which are line-to-line voltages, line currents, and upper/lower voltages.

Concerning robust controller design, the proposed synthesised controller has been designed based on an uncertain value for parameter C_{eq}, so the value of the capacitor of the other devices is considered in order to have the total value of C_{eq} within the presupposed uncertain range as discussed in the Appendix. As depicted in Figs. 10 and 13, the proposed controller is able to

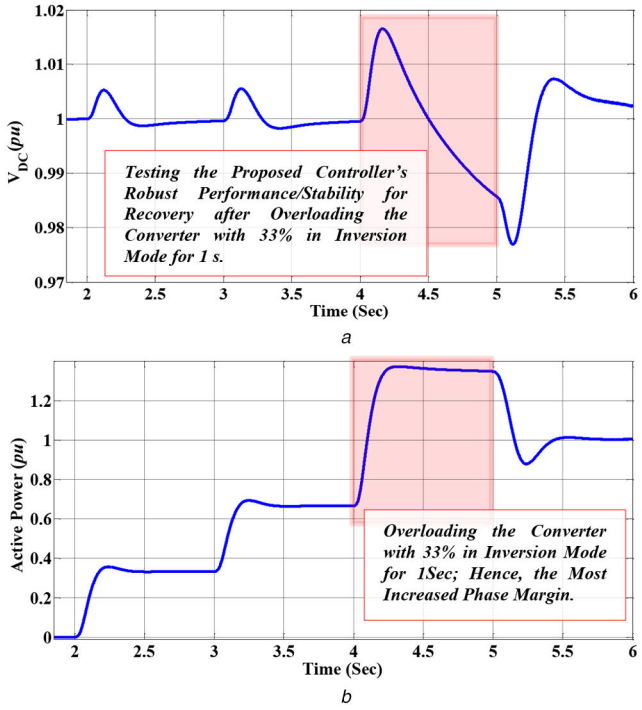

Fig. 13 *Simulation results of Fig. 9 with the proposed controller expressed by (11) for Test Cases II*
(a) dc Voltage, ***(b)*** Active power of MMC

robustly stabilise the dc voltage of the whole MIACDC grid. Besides, the proposed controller shows the robust performance in regulating dc voltage with respect to changes in the operating point, as well as the equivalent dc-link capacitor, i.e. C_{eq}. As demonstrated in Figs. 10 and 13, the overshoots and the undershoots of the response are almost the same, which are 1.5 and 2.5%, respectively, for different operating points and changes in the value of C_{eq}; the settling time of the response is almost the same, which is around 1 s, for different operating points as well as changes in the value of C_{eq}.

5.2 Comparison of the performance of the proposed controller with that of the PI controller

To do a comparison, this section will compare the performance of the proposed controller with that of the PI controller. The PI controller has been designed for the worst-case scenario, i.e. maximum rectification mode by considering L_{arm} dynamics on the dc-voltage dynamics. Besides, the PI controller has been augmented with a lead compensator to improve the stability and phase margin induced by a non-minimum phase zero [31, 39, 42] – as seen from and appeared in the zero of (6). The synthesised PI controller enhanced with lead compensator, i.e. $K_{\text{PI-lead}}(s)$, has been expressed in the equation below:

$$K_{\text{PI-lead}}(s) = \frac{-0.0055903848 \times 10^{-6} s - 1.996566 \times 10^{-6}}{s} \times \frac{0.57s + 1}{0.0042s + 1} \quad (12)$$

For different operating points, the phase margins induced by the above-mentioned designed regulator $K_{\text{PI–Lead}}(s)$ have been reported via curves shown in Fig. 16. As illustrated in Fig. 16, the synthesised PI-lead controller is able to stabilise the closed-loop system with an acceptable phase margin, which is about 51° for the nominal rectification mode and 82° for the nominal inversion mode. For other operating points, more details can be seen in Fig. 16.

Figs. 17 and 18 reveal the simulation results of the system response under the cases performed for the proposed controller, i.e. Case I and Case II as elaborated in Section 5.1. As shown, the PI-

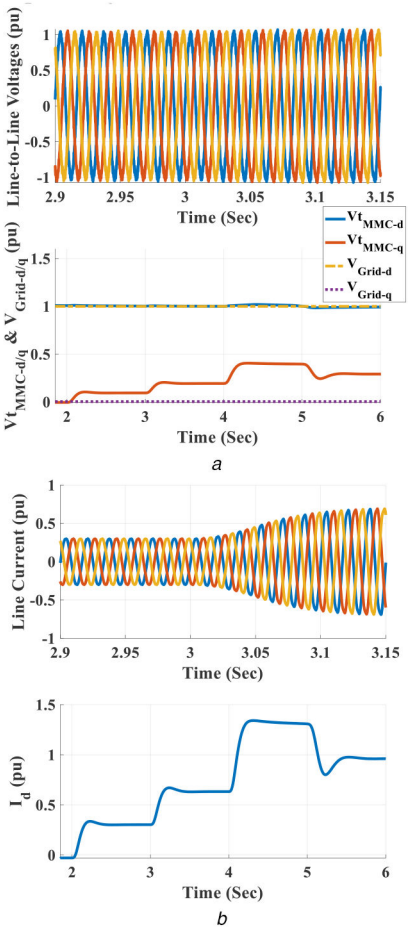

Fig. 14 *Voltage/current signals associated with Fig. 13*
(a) Sample of the line-to-line voltages (including its repetition in the *dq* frame and that of line-to-line grid voltages), ***(b)*** Sample of the line currents of MMC

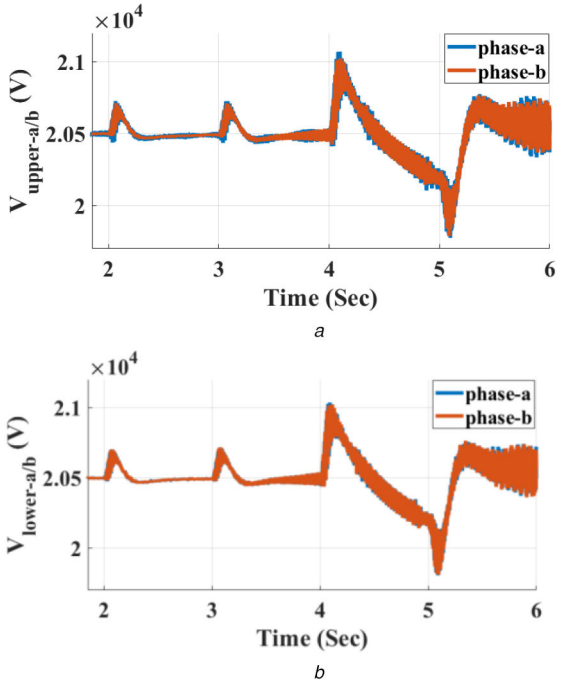

Fig. 15 *Arm voltages associated with Fig. 13*
(a) MMC's upper arm of V_{upper}, ***(b)*** MMC's lower arm of V_{lower}

lead controller is not able to show the robust performance in regulating dc voltage with respect to variations in the operating point, as well as the equivalent dc-link capacitor, i.e. C_{eq}. In other words, as demonstrated in Figs. 17 and 18, the overshoots and

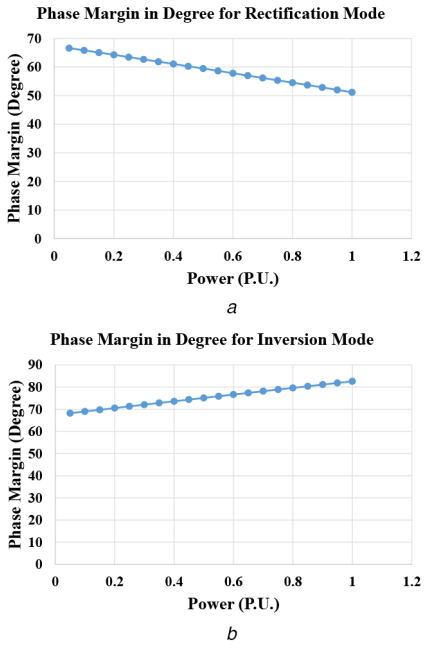

Fig. 16 *Phase margin induced by the PI-lead controller described by (12) for*
(a) Rectification mode, ***(b)*** Inversion mode

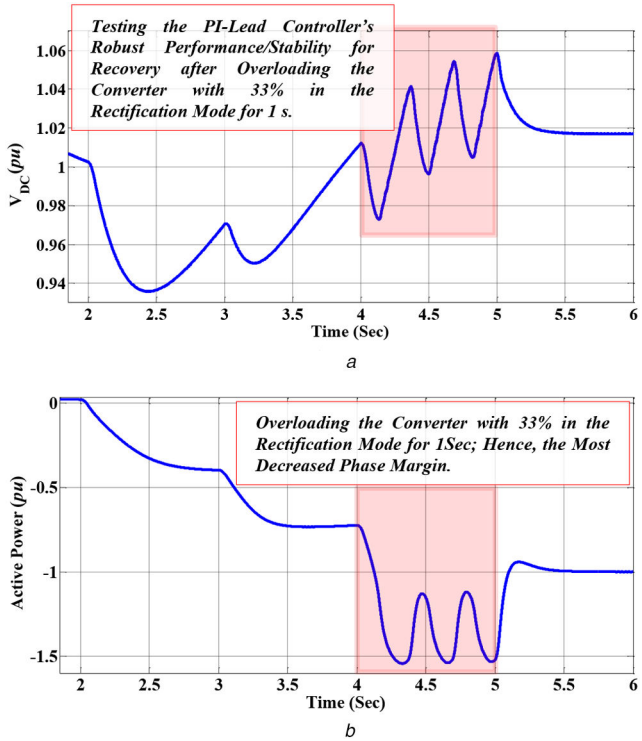

Fig. 17 *Simulation results of Fig. 9 with the PI-lead controller expressed by (12) for Test Cases I*
(a) dc Voltage, ***(b)***MMC active power

undershoots of the response are 'not' the same for different operating points and changes in the value of C_{eq} – contrary to the outcomes that the proposed controller has resulted in as detailed in Section 5.1. Additionally, the settling time of the response has not been remarkably consistent for different operating points, as well as changes in C_{eq} value – again contrary to the outcomes that the suggested controller has resulted in. This can simply be verified and justified by finding the overall closed-loop system including MMC with the PI-lead controller (12). As regards this, Fig. 19 shows the counterpart of the same analysis performed for the proposed controller, which is shown in Fig. 8. As Fig. 19 proves, the $K_{\text{PI–lead}}(s)$ is not able to induce robust performance since the

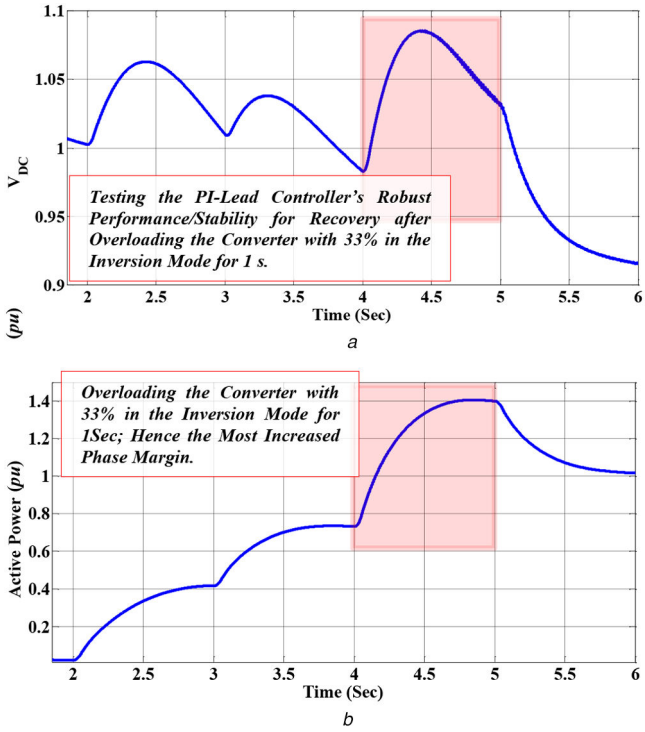

Fig. 18 *Simulation results of Fig. 9 with the PI-lead controller expressed by (12) for Test Cases II*
(a) dc Voltage, ***(b)*** MMC active power

poles/zeros vary in a much larger region compared with that of Fig. 8.

5.3 Proposed controller's performance compared with the response of another robust controller

In this section, the controller proposed in [35] is redesigned and resynthesised for the case of MMC-based dc-voltage power port in order to check the L_{arm}'s effect on the output. Indeed, this case is equivalent to considering a two-level-VSC-based dc-voltage power port with the same parameters as stated in the Appendix with only one change, which is considering that the L_{arm} value is equal to 'zero.' After repeating the procedure suggested in Section 4.2 for this case, the synthesised controller is reached as expressed in the equation below: (see (13)) . Equation (13) is employed in the MATLAB Simulink to simulate Case I as explained in Section 5.1. Its associated results are shown in Fig. 20, where it can be seen that the robust controller designed without considering L_{arm} dynamics in (6) is *not* able to show the robust stability in regulating dc voltage with respect to variations in both the operating point and the equivalent dc-link capacitor, i.e. C_{eq}. Indeed, owing to the fact that the L_{arm} dynamics was ignored for synthesising the aforementioned robust controller, the dc-voltage response shows an unacceptable transient performance – which demands to consider L_{arm} dynamics when designing robust controllers in order to have acceptable transient performance. Fig. 20 also motivates the fact that the mentioned dynamics are able to deteriorate the dc-voltage performance when the MMC's operating point changes as it dramatically impacts the dc-voltage response. Consequently, robust performance is not seen though the controller has been synthesised in order to have robust performance because to the fact that one of impactful dynamics – i.e. those of induced by L_{arm} – is ignored in the small-signal linearised model of the total dynamics.

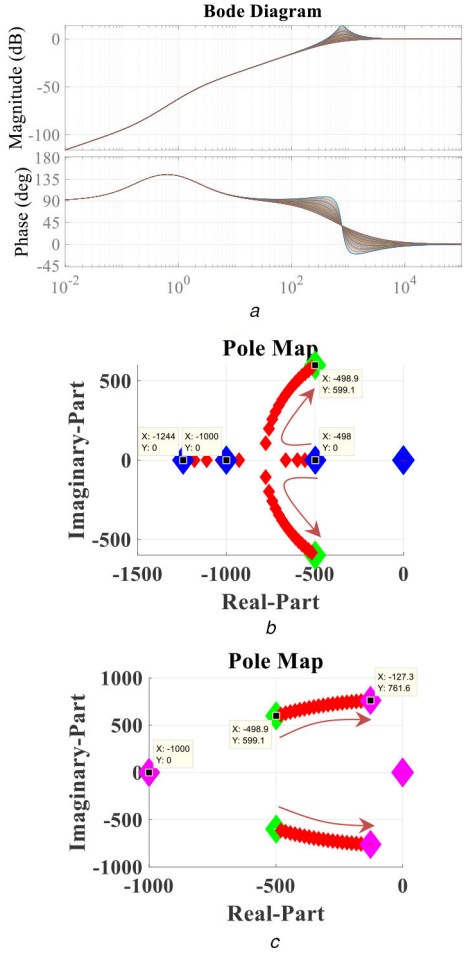

Fig. 19 *Stability study of the whole closed-loop system with the PI-lead controller*
(a)–(c) Counterparts of Figs. 8*a–c*, respectively, for the closed-loop system with the PI-lead controller (12)

6 Experimental results

For further evaluation of the proposed controller, a laboratory-scale experimental test rig is employed. The system is composed of a grid-connected VSC, which is able to test the transient performance of an MMC-based dc-voltage power port in an MIACDC architecture.

The test rig includes insulated gate bipolar transistors built by 'SKM 50 GB 123 D' modules, 'SKHI 21A (R)' gate drives, and protection circuits-all from SEMIKRON Company. The ac-side filter inductance and resistance are 2.4 mH and 0.06 Ω, respectively. The dc-link capacitance and inductance are 2.04 mF and 1.50 mH, respectively. The three-phase converter is nominally rated at 35 A and 208 V. However, it has been 'de-rated' in order to be able to have sufficiently strong non-minimum dynamics caused by the stated operating point for controller's performance validation purposes and create the same dynamics of interest (see experimental section of [31, 35]).

The converter's inductor currents and the voltages are measured by 'IsoBlock I-ST-1c' current sensors and 'IsoBlock V-1c' voltage sensors from Verivolt, respectively. The converter is interfaced with a 'MicroLabBox (MLBX)' from dSPACE. The proposed control algorithm is executed and run by a dual-core 2 GHz 'NXP (Freescale) QorlQ P5020' real-time processor. The pulse-width modulation signals are generated by 'Xilinx Kintex-7 XC7K325T' field-programmable gate arrays connected to digital inputs/outputs. The MLBX interface board is equipped with eight 14 bit, 10 Msps,

$$K(s) = \frac{-5.2019\times10^{-10}s^4 - 0.0040\times10^{-5}s^3 - 0.0112\times10^{-5}s^2 - 0.0045\times10^{-5}s - 39.3190\times10^{-12}}{s^4 + 0.4712s^3 + 0.0009696s^2 + 5.778\times10^{-7}s + 7.847\times10^{-11}} \quad (13)$$

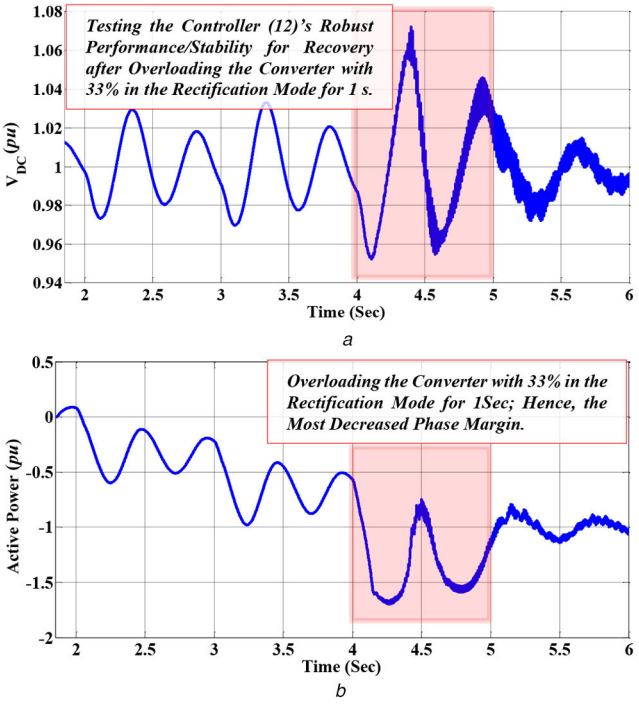

Fig. 20 *Simulation results of Fig. 9 with the controller expressed by (13) for Test Cases I*
(a) dc Voltage ***(b)*** MMC active power

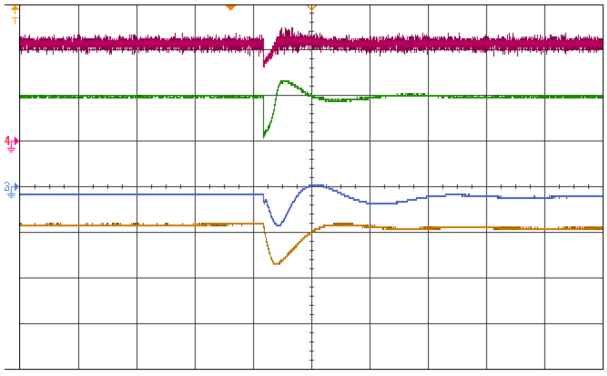

Fig. 21 *Experimental results of the proposed controller response to a harsh change in the dynamic, active load*

differential analogue-to-digital channels to interface the measured signals to the control system (with the functionality of free-running mode). The software code is generated by the Real-Time-WorkShop in the Simulink environment. The proposed controller has been examined under harsh operating point variations and 0.5 pu load change using an active load.

For the first case, after energising dc-voltage power port, in order to effectively test the control functionality and transient response to a sudden, harsh change in dynamic, active load is applied – i.e. an intentionally created, long-lasting, harsh dc motor current (for testing the controls during operating point variations). This has been achieved by connecting a dc motor (from Lab-Volt®) without any start-up consideration associated with powering up a dc motor. In this way, a large variation in the *d*-component of current (within an acceptable range) is applied, so the controller performance is experimentally – and also as accurately as possible – tested for sudden changes in the disturbance signals. Figs. 21 and 22 demonstrate the aforementioned experimental results associated with the proposed controller and another robust controller as detailed in Section 5.

As predicted, Fig. 21 shows an acceptable control response related to robustly rejecting the disturbances caused by large, sudden operating point variations – which is testing the transient performance for extremely harsh changes. Fig. 22 demonstrates that the other type of robust controller is not able to induce robust

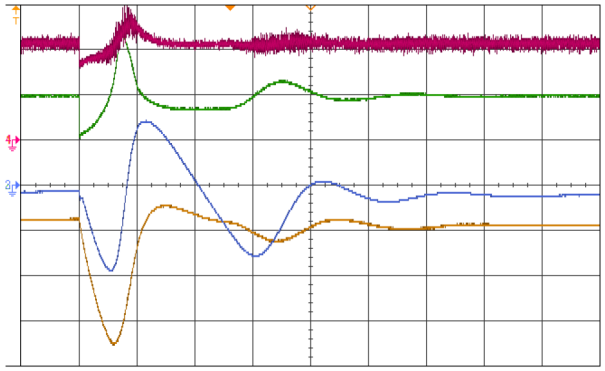

Fig. 22 *Experimental results of the other robust controller response to a harsh change in the dynamic, active*

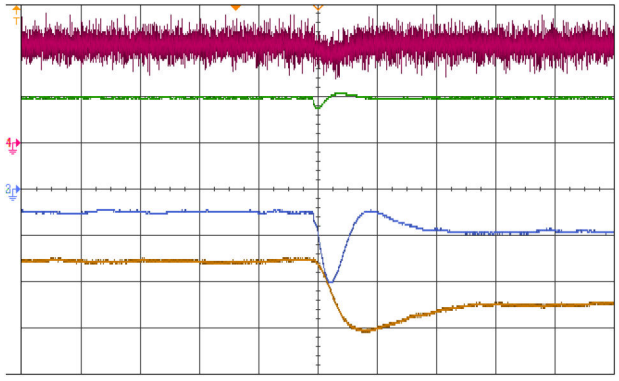

Fig. 23 *Experimental results of the PI controller response to a 0.5 pu active load*

performance – because of not including complete dynamics of an MMC-based dc-voltage power port as detailed in Section 5.3.

For the second case, after loading an energised dc-voltage power port with 0.5 pu active load, a new 0.5 pu active load will be connected. As anticipated, Fig. 23 shows a satisfactory control response related to optimally rejecting the active load disturbances.

In both of the above-mentioned cases, in order to only see the dc-voltage controller response, all considerations associated with the dc-voltage power ports have been taken into account – including reactive support for the grid weakness, appropriate gains for PLL, and other points mentioned at the beginning of Section 4. Fig. 23 shows the above-mentioned experimental results associated with the proposed controller. In Figs. 21–23, the dark magenta trace is the *d*-component of the ac voltage of the PCC in pu (500 mV/div); the green trace is the V_{dc} of the dc-voltage power port in pu (500 mV/div); the blue trace is the I_d of the dc-voltage power port in pu (500 mV/div); the brown trace is the I_q of the dc-voltage power port in pu (50 mV/div); and the horizontal axis is (500 ms/div).

7 Conclusion

The dc-voltage power port based on MMC technology, which is one of the most important parts of the MIACDC grids, is nowadays gaining more attention to be applied in the power industry – compared with the dc-voltage power port based on the two-level and NPC VSC technologies. In this paper, the dynamics of the MMC-based dc-voltage power port have been comprehensively analysed considering all of the energy-storing components. It was shown that those impact on different frequency ranges of the whole dynamics and create effective disturbances, e.g. the square of the circulating currents and its derivatives, and more. Consequently, the controller should be able to optimally reject the disturbances' influence on the output stability and transient performance and consider the parameter variations owing to the connection/disconnection of different devices to/from the dc grid. Therefore, this paper proposed a robust controller, which is based on the μ-

analysis and synthesised it in order to optimally minimise H_∞ and reject the most important disturbances – when the MMC's operating points/condition change in the MIACDC grid. For comparison purposes, the commonly designed PI-lead controller was examined under the same test cases, for which the proposed robust control was tested and simulated. Furthermore, the response of the proposed robust controller was compared with the response of another robust controller, which can be designed for a typical two-level-VSC-based dc-voltage power port. Mathematical analyses, comparative simulations, and experiments reveal the effectiveness of the proposed controller when compared with the typical PI-lead controller, as well as the robust regulators previously suggested for two-level-VSC technologies.

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10 Appendix

The parameters of Fig. 1 and Zone I in Fig. 9 are given below (see Table 1).

The parameters of the simulated system in Fig. 9 are given below (see Tables 2–5).

Table 2 Parameters of Zone II: VSC-PQ

rated power	67.0 MVA
grid 2 voltage	138.00 kV at 60 Hz
P_{loss}	0.64 MW
R	0.06 mΩ
L	300 μH
switch resistance	1.0 mΩ
diode resistance	1.0 mΩ
parameters of current PI controller	$K_p = 0.3$ Ω and $K_i = 3.5$ Ω/s
parameters of PLL PID controller	$K_p = 180$; $K_i = 3200$; and $K_d = 1$
C_{PQ}	3000 μF

Table 3 Parameters of Zone III: VSC-W

rated power	33.0 MVA
P_{loss}	0.31 MW
R	0.06 mΩ
L	300 μH
switch resistance	1.0 mΩ
diode resistance	1.0 mΩ
parameters of current PI controller	$K_p = 0.3$ Ω and $K_i = 3.5$ Ω/s
C_{eq}	3000 μF

Table 4 Parameters of Zone IV: BESS bidirectional conv

power rating	33.0 MW
R	0.06 mΩ
L	300 μH
switch resistance	1.0 mΩ
diode resistance	1.0 mΩ
parameters of current PI controller	$K_p = 0.3$ Ω and $K_i = 3.5$ Ω/s
R	0.06 mΩ
L	300 μH
C_H	1000 μF
L_{BESS}	100 mH
C_L	6000 μF

Table 5 Parameters of the dc grid

rated voltage	41.0 kV
dc-cable length	300 km
R_{cable}	0.82 mΩ/km
C_{cable}	0.014 mF/km
L_{cable}	0.98 μH/km