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Lee, Sze Sing; Yang, Y.; Siwakoti, Yam Prasad

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A Novel Single-Stage Five-Level Common-Ground-Boost-Type Active Neutral-Point-Clamped (5L-CGBT-ANPC) Inverter

Sze Sing Lee, *Senior Member, IEEE*, Yongheng Yang, *Senior Member, IEEE*, Yam Siwakoti, *Senior Member, IEEE*

***Abstract*- The conventional active neutral-point-clamped (ANPC) inverter inherits excellent high frequency common mode voltage (CMV) mitigation ability but with a restricted voltage gain. This letter proposes a novel 5-level ANPC inverter that is able to accomplish voltage-boosting feature within a single-stage dc-ac power conversion. A common ground in the proposed topology not only mitigates the high frequency CMV, but also enhances the dc-link voltage utilization. The proposed topology exhibits less voltage stress and higher compactness when compared with a conventional two-stage 5-level ANPC inverter. It saves three power switches and one capacitor, while enhancing the overall efficiency. Simulations and experimental tests have validated the overall operation, efficacy, and practicality of the proposed ANPC inverter.**

I. INTRODUCTION

The evolution of power electronics technology has accelerated the penetration of various renewable energy resources into power grid [1]. In this context, there is a growing tendency in the development of different kinds of power converters which are well-suited to a variety of applications. Transformerless inverters which eschew the use of bulky transformers, for instance, are one of the popular types of converters that are recently gaining increasing attention in photovoltaic (PV) applications. However, the lack of galvanic isolation between the dc source and ac output inevitably leads to a high common mode voltage (CMV), which in turn, results in the risk of high leakage current emission [2].

The high frequency CMV issue is an important ongoing research topic in any transformerless topologies. It has been addressed mostly by adopting certain dedicated modulation techniques and inverter topologies with additional clamping circuits. However, it is interesting to note that the established ANPC inverter which has currently been commercialized [3], [4], is able to mitigate the CMV inherently merely with its structure. With the neutral of its ac output being connected to the midpoint of the dc-link, the stray capacitor of the PV cells are clamped across the dc-link capacitors and thus preventing the leakage current [5]. One limitation of the ANPC inverters is their restricted voltage gain since it can only generate a maximum ac voltage level that is only half of the dc-link voltage. Thus, a two-stage structure, which encompassed a front-end boost converter as illustrated in Fig. 1, is usually required to meet the dc-link voltage requirement of at least being double of the ac peak voltage.

Recently, tremendous attempts have been made by incorporating switched-capacitors (SCs) into an ANPC inverter structure to increase the voltage gain [6]–[10]. The SCs are discharged in series with the dc-link capacitors to generate a boosted voltage level, rendering an enhanced voltage gain. However, it should be noted that it is mandatory for the SCs to be charged in parallel with the dc-link capacitors prior to supplying the load. This subsequently results in current spikes. Besides, their discontinuous dc source current strictly hinders their applications for PV systems. Both the identified limitations in these SC-based topologies made them less attractive as compared to the two-stage ANPC inverter in Fig. 1.

With the above, this letter contributes to a novel single-stage 5-level ANPC inverter with voltage-boosting capability, as depicted in Fig. 2. It is an alternative to the conventional two-stage 5-level ANPC inverter in Fig. 1, with added merits such as:

(1) Reduced switch count from 10 to 7.
(2) Reduced capacitor count from 3 to 2.
(3) Enhanced dc-link voltage utilization.
(4) Reduced inverter voltage stresses, thus low cost and high efficiency.
(5) Provision of a common ground, mitigating leakage currents.
(6) Single-stage dc-ac conversion with voltage-boosting.

The remainder of this letter is organized as follows. In Section II, the steady-state analysis of the proposed ANPC topology is presented. Simulation and experimental results are discussed in Section III. Finally, concluding remarks are provided in Section IV.

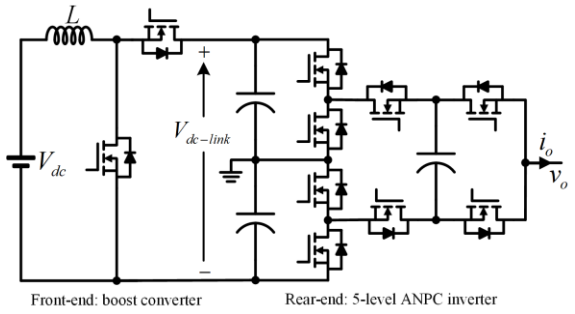


Fig. 1. Conventional two-stage 5-level ANPC inverter.

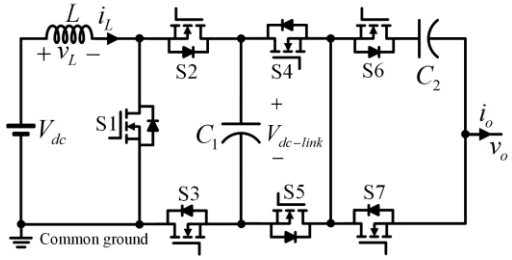


Fig. 2. Proposed single-stage 5-level common-ground-boost-type active neutral-point-clamped (5L-CGBT-ANPC) inverter.

II. Proposed 5L-CGBT-ANPC Inverter

A. Steady-State Analysis

Fig. 2 shows the proposed 5L-CGBT-ANPC topology which realizes voltage-boosting and 5-level ac voltage generation within a single-stage operation. When comparing with the conventional two-stage 5-level ANPC inverter in Fig. 1, the proposed topology requires fewer components (three fewer switches and one fewer capacitor). A common ground is provided for the dc source and ac output that not only ensures high frequency CMV mitigation, but also enhances the dc-link voltage utilization. It is worth emphasizing that the maximum attainable ac voltage level is equal to the dc-link voltage, which is doubled in contrast to the conventional ANPC inverter.

The switching states and their corresponding circuit diagrams are illustrated in Fig. 3. The proposed topology is controlled with level-shifted pulse-width modulation (PWM), where the PWM modulator consists of a switching state generator and a switching signal generator as depicted in Fig. 4.

The boost inductor L is charged with a constant duty-cycle D that boosts the dc-link voltage across C_1 to

$$V_{dc-link} = V_{\max} = V_{C_1} = \frac{V_{dc}}{1-D}. \quad (1)$$

The capacitor C_2 voltage is naturally balanced at half of the dc-link voltage. Therefore, five voltage levels are generated between $+V_{dc-link}$ and $-V_{dc-link}$ with the peak of the fundamental ac voltage being written as

$$\hat{V}_{o,1} = \frac{MV_{dc}}{1-D} \quad (2)$$

where M is the modulation index and $D \geq 2M-1$. Considering the minimum D, the voltage gain can be given as

$$G = \frac{\hat{V}_{o,1}}{V_{dc}} = \frac{M}{2(1-M)}. \quad (3)$$

Fig. 5 further illustrates the operation of the proposed inverter controlled by a level-shifted pulse-width modulation (PWM) scheme. Based on the current waveform, t_1 and t_{avg} can be respectively written as

$$t_1 = \frac{T_o}{2\pi}\sin^{-1}\frac{1}{2M} \quad (4)$$

$$t_{avg} = \frac{1}{2\pi f_o}\sin^{-1}\frac{I'_{C_1}}{\hat{I}_{o,1}}. \quad (5)$$

Considering the electric charge for half fundamental cycle by calculating the area under the current waveform from 0 to $T_o/2$, the voltage ripple of C_2 can be written as

$$\Delta V_{C_2} = \frac{\hat{I}_{o,1}}{\pi f_o C_2}\left[1+\frac{\pi}{2M}-2\cos\left(\sin^{-1}\frac{1}{2M}\right)-\frac{1}{M}\sin^{-1}\frac{1}{2M}\right] \quad (6)$$

where $\hat{I}_{o,1}$ is the peak of the fundamental load current and f_o is the output frequency.

The voltage ripple of the capacitor C_1 consists of high-frequency f_s (triangular carrier frequency) and low-frequency f_o components. The high-frequency ripple can be derived following the same analysis for the boost converter that gives

$$\Delta V_{C_1,f_s} = \frac{DI'_{C_1}}{f_s C_1} \quad (7)$$

where $I'_{C_1} = \frac{\hat{I}_{o,1}}{M\pi^2}\left[\pi(3M-1)+2(1-2M)\sin^{-1}\left(\frac{1}{2M}\right)\right]$ (8)

is the average value of i'_{C_1} depicted in Fig. 5. Considering charge balance, the low-frequency voltage ripple of C_1 can be computed by calculating the electric charge supplied by the capacitor from t_{avg} to $T_o/2 - t_{avg}$,

$$\Delta V_{C_1,f_o} = \frac{1}{2\pi f_o C_1}\left[2\hat{I}_{o,1}\cos\left(\sin^{-1}\frac{I'_{C_1}}{\hat{I}_{o,1}}\right)-\pi I'_{C_1}+2I'_{C_1}\sin^{-1}\frac{I'_{C_1}}{\hat{I}_{o,1}}\right]. \quad (9)$$

The boost inductor current ripple at f_s induced by PWM is similar to that of the conventional dc-dc boost converter such that

$$\Delta I_{L,f_s} = \frac{DV_{dc}}{f_s L}. \quad (10)$$

Considering ideal dc source that is free from low-frequency ripple, the relationship between the low-frequency voltage ripple across L and C_1 is

$$\Delta V_{C_1,f_o} = \frac{\Delta V_{L_1,f_o}}{1-D} \quad (11)$$

where $\Delta V_{L_1,f_o}$ is the low-frequency voltage ripple across L. The low-frequency inductor current ripple can be determined by considering (11) and its impedance at fundamental frequency

$$\Delta I_{L,f_o} = \frac{(1-D)\Delta V_{C_1,f_o}}{2\pi f_o L}. \quad (12)$$

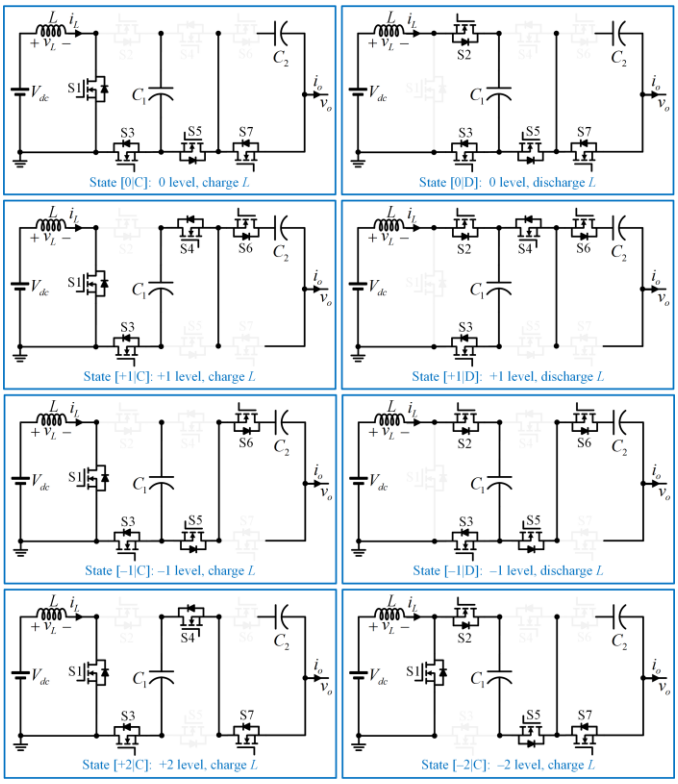


Fig. 3. Switching states of the proposed 5L-CGBT-ANPC inverter.

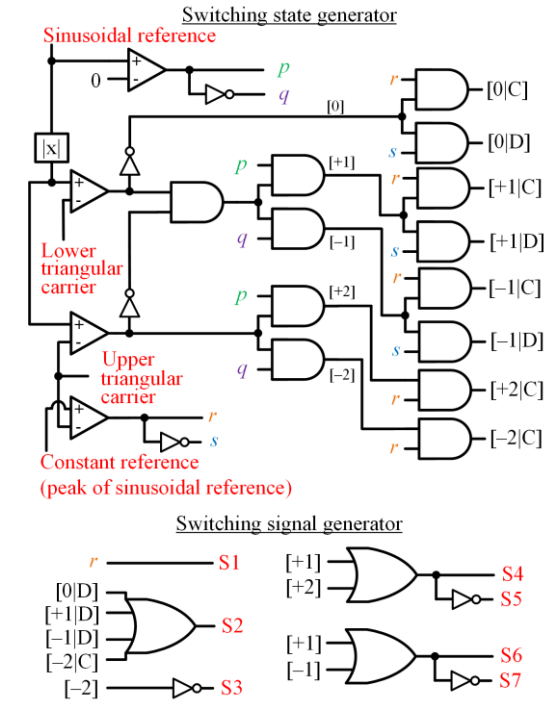


Fig. 4. PWM modulator of the proposed 5L-CGBT-ANPC inverter.

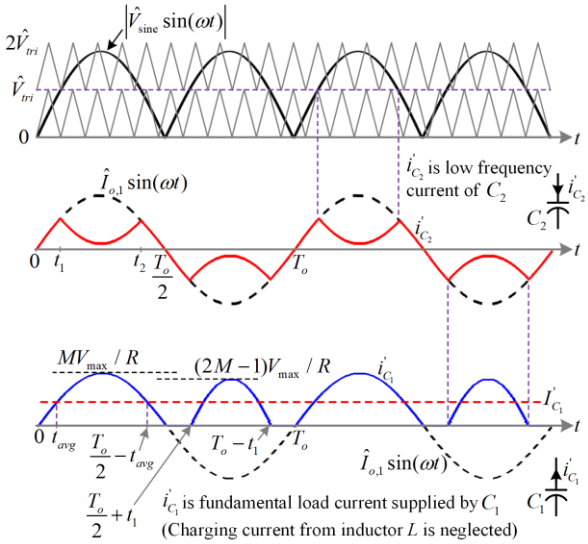
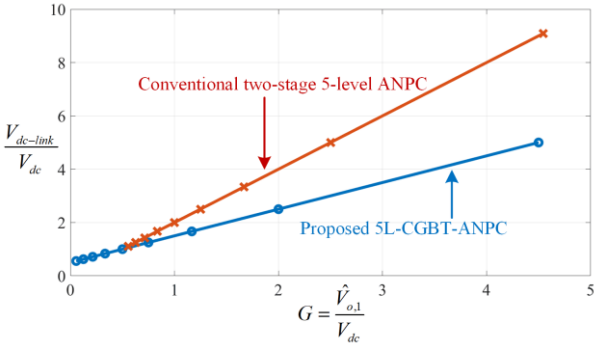
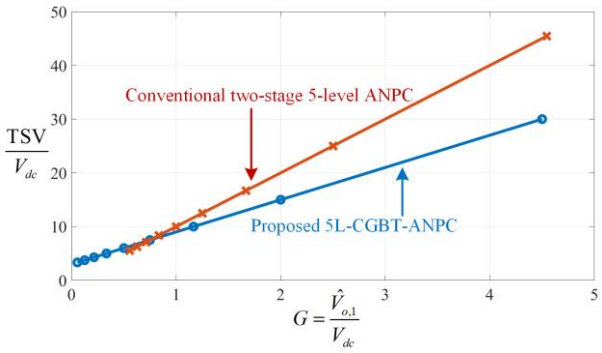


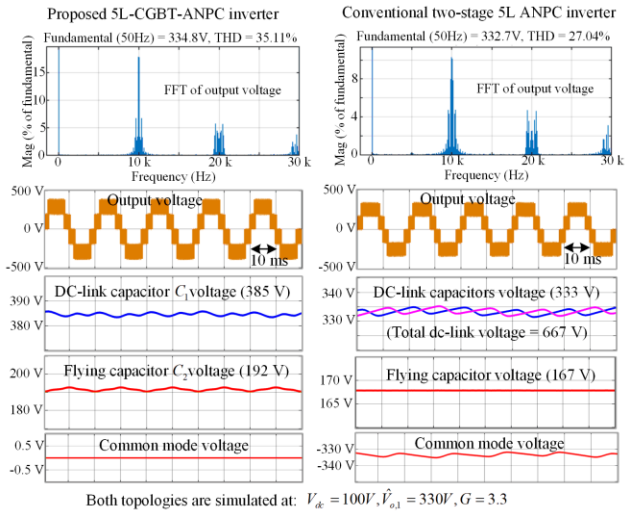
Fig. 5. Level-shifted PWM for the proposed inverter and analysis of the capacitor voltage ripples at a low-frequency.



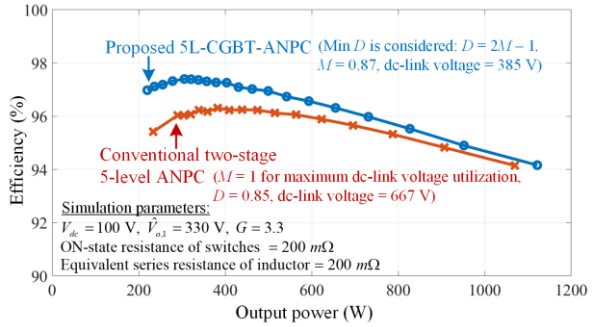
(a)



(b)



(c)



(d)

Fig. 6. Comparison between the proposed 5L-CGBT-ANPC inverter and the conventional two-stage 5-level ANPC inverter: (a) normalized dc-link voltage, (b) normalized total standing voltage (TSV), (c) simulation waveforms, and (d) efficiency.

B. Comparison with Two-Stage 5L-ANPC Inverter

In this section, a comparative study is conducted to evaluate the merits of the proposed 5L-CGBT-ANPC inverter by benchmarking it with the two-stage 5-level ANPC topology shown in Fig. 1. The dc-link voltage and voltage gain are normalized as shown in Fig. 6(a). Both topologies provide the equivalent voltage gain when the same dc source and ac output voltages are considered. Note that the proposed topology exhibits a lower dc-link voltage. In other words, it possesses higher dc-link voltage utilization. Additionally, this

also indicates that it has lower voltage stresses on its power switching devices, as also proven by its significantly lower total standing voltage (TSV) in Fig. 6(b).

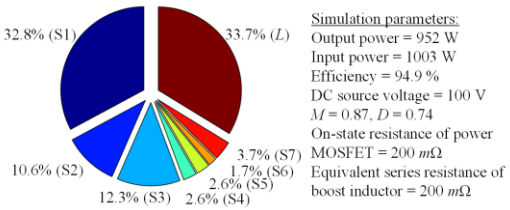


Fig. 7. Simulated power losses distribution.

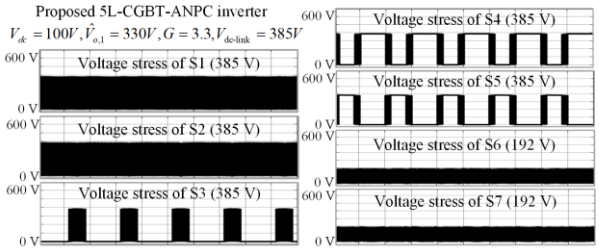


Fig. 8. Simulated voltage stress.

Fig. 6 (c) shows the corresponding simulation waveforms for both the topologies when 230 V rms ac voltage generation from a 100-V dc source is considered. As anticipated, the proposed inverter demonstrates significantly lower dc-link voltage of only 385 V as compared to 667 V in the two-stage ANPC inverter. Note that higher flying capacitor voltage ripple in the proposed topology is due to the charging and discharging of C_2 by the load current at fundamental frequency. Although the self-balancing of C_2 results in slightly higher ac voltage THD, there is marginal impact on the size of output filter components. This is because the dominant harmonics of the proposed topology are concentrating around the triangular carrier frequency, as similar to the case of the conventional ANPC inverter.

Fig. 6(c) shows that both topologies provide excellent high frequency CMV suppression. The CMV in the conventional ANPC inverter is observed to oscillate at fundamental frequency around –333 V while the CMV in the proposed topology is ripple-free at 0 V. This again confirms the effectiveness of the proposed common-ground structure in CMV mitigation.

Further comparison in Fig. 6(d) demonstrates the higher efficiency of the proposed topology which is mostly attributed to its less number of switches as well as its single-stage dc-ac power conversion feature. Its power losses distribution at approximately 1 kW as well as the simulated blocking voltage across each power switch is depicted in Fig. 7 and Fig. 8, respectively. In short, despite the slight expense of higher flying capacitor C_2 voltage ripple, the proposed topology outperforms the conventional two-stage ANPC inverter in terms of switch count, capacitor count, dc-link voltage utilization, voltage stress, and overall efficiency.

III. Simulation and Experimental Results

To validate the operation of the proposed 5L-CGBT-ANPC inverter, an experimental prototype was implemented with the following parameters: V_{dc} = 40 V, C_1 = C_2 = 1000 µF, L = 3 mH, f_s = 10 kHz, load resistance = 100 Ω, load inductance = 0.1 H, M = 0.9, and the minimum D of 0.8 is considered. The experimental setup is depicted in Fig. 9.

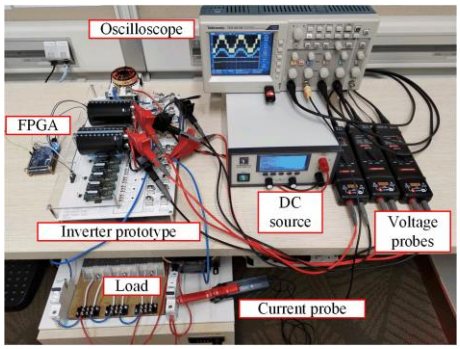


Fig. 9. Experimental setup.

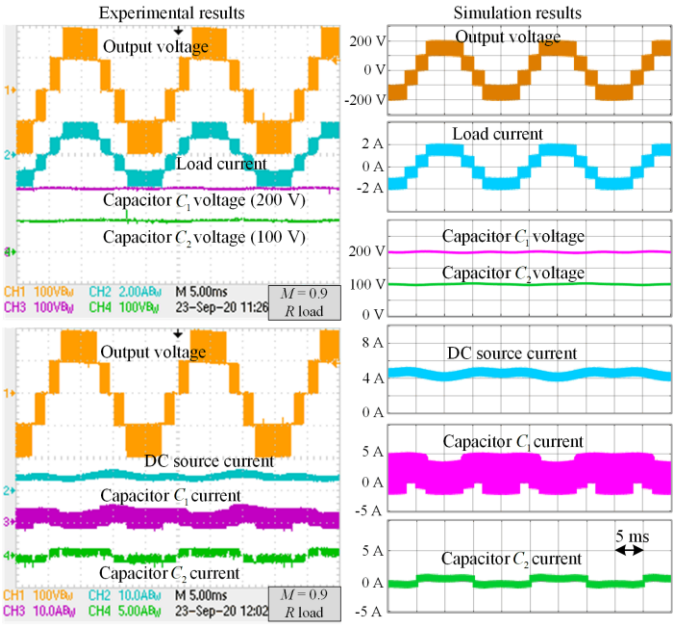


Fig. 10. Experimental results and simulations under a purely resistive R load.

Fig. 10 shows the measured and simulated waveforms when a purely resistive load is considered. Considering the boost inductor L charged by a dc source with a constant duty-cycle D of 0.8, the dc-link voltage is boosted to 200 V, signifying a fivefold voltage-boosting from the dc source to the dc-link. Five symmetrical voltage levels are clearly seen between 200 V and –200 V. It can also be seen that the capacitor C_2 is naturally balanced at 100 V and the dc source current is continuous. Note that neither the dc source current nor the capacitors current are subjected to the current spike issue as in the existing SC-based inverters.

For an RL (resistive-inductive) load depicted in Fig. 11, the load current is sinusoidal with its amplitude being

approximately 1.7 A. Considering the load impedance magnitude of 105 Ω, the calculated peak fundamental ac voltage is 179 V. Therefore, the voltage gain is approximately the same as the theoretical value of 4.5. In addition, a good agreement is observed between the experimental and simulation results in Figs. 10 and 11. Fig. 12 continues to capture the transient behavior of the experimental prototype. When the load is switched from *RL* to *R* load, it is apparent that the load current changes instantaneously without deteriorating the ac output voltage.

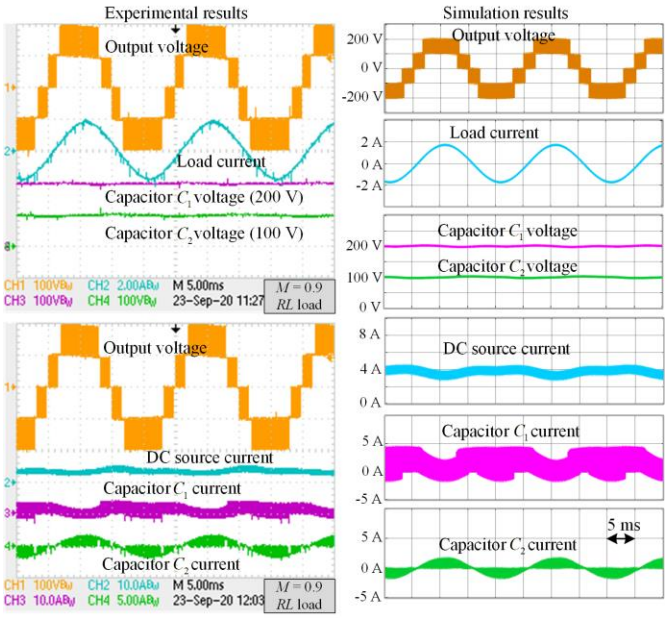


Fig. 11. Experimental results and simulations under a series resistive-inductive *RL* load.

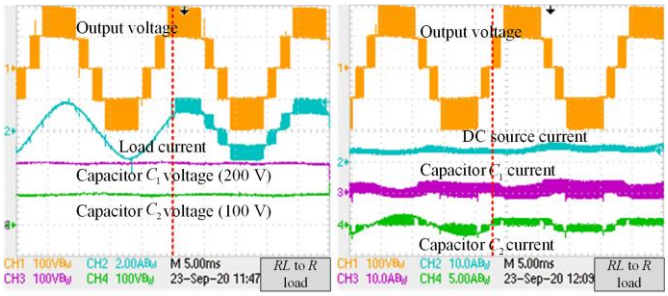


Fig. 12. Experimental transient response of the proposed inverter from *RL* to *R* load.

IV. Conclusion

A novel 5-level ANPC inverter is proposed in this letter. The proposed topology inherits high frequency CMV mitigation ability as in the conventional ANPC inverter, while gaining additional advantages such as voltage-boosting capability, enhanced dc-link voltage utilization, reduced voltage stress, and higher compactness. Most importantly, all the aforementioned features can be achieved within a single-stage operation with no trade off in efficiency. The operation of the proposed topology has been analyzed and validated through simulations and experimental tests. Good agreement can be found among the theoretical analysis, simulations, and experimental results, proving that the proposed 5-level ANPC inverter could be a viable and promising alternative to the conventional two-stage ANPC topology.

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