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A Currentless Submodule Individual Voltage Balancing Control for Modular Multilevel Converters

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Abstract— The capacitor voltage balancing is one of the most important issues for safe and reliable operation of the MMC. This paper proposes a currentless submodule individual voltage balancing control (SMIVBC) to realize capacitor voltage balancing in the MMC. Through regulating the dc component in each SM capacitor current by modulation index *m*-based SMIVBC or phase angle *θ*-based SMIVBC, each SM capacitor voltage can be individually controlled to follow reference value, which can realize capacitor voltage balancing in the MMC. The proposed SMIVBC not only requires no sorting technique to select the SMs in the MMC avoiding sorting algorithm, but also requires no knowledge of current in the MMC, which reduces the sensors and sampling signals, saves the cost and improves the reliability. Simulation studies with professional tool PSCAD/EMTDC and experiment studies with a down-scale prototype in the laboratory are both conducted and their results confirm the effectiveness of the proposed SMIVBC for the MMC.

***Index Terms*—Capacitor voltage control, currentless, individual control, modular multilevel converters, submodule.**

I. INTRODUCTION

The modular multilevel converter (MMC) was developed in the early 2000s [1]. It consists of a number of cascaded submodules (SMs) to produce multilevel voltage configuration [2-4]. The high number of voltage level enables a significant reduction in the device's average switching frequency without compromising power quality [5]. Due to the features such as modularity and scalability, the MMC is attractive for medium-/high-voltage and high-power application in the industry [6-9].

Capacitor voltage balancing is one of the most important issues for the MMC. To date, a number of voltage balancing control algorithms have been presented for the MMC. Generally, there are mainly two types of methods including sorting-based method and individual control-based method [10].

Several sorting-based methods are presented for voltage balancing control in the MMC. References [10-13] present the voltage balancing control method based on the number of the SMs turned on and the arm current in each control period. In order to reduce switching frequency to reduce the power loss, reference [14] only switches the extra SMs in the next control period for voltage balancing; reference [15] presents the slow-rate and hybrid capacitor voltage-balancing strategy; reference [16] presents a low-switching frequency power module balancing method based on balancing adjusting number; references [17-21] present the voltage-balancing method with the switching frequency at grid frequency; reference [22] presents a low complexity implementation of the voltage balancing algorithm without any conditional execution requirements for reducing the switching frequency; reference [23] presents an adaptive voltage-balancing method with reduced switching frequency to make a trade-off between the switching losses and the balancing effect. Reference [24] presents a capacitor voltage balancing control method based on the high-frequency harmonic current at the carrier frequency in each arm of the MMC. Reference [25] presents a voltage-balancing method for the MMC under the phase-shifted carrier-based PWM scheme, where the pulses are sorted and distributed based on the energy associated with the pulses. Reference [26] presents a hierarchical permutation cyclic coding strategy to evenly distribute the switching gate signals among the SMs of each arm within a permutation time for capacitor voltage balancing in the MMC. Reference [27] presents a model predictive control strategy that takes the advantage of a cost function minimization technique to realize the voltage balancing for the MMC. In above sorting-based control, all the measurement and control are normally centralized in a digital signal processor, which requires that the algorithm executes in each control cycle and increases the computational burden, especially for the MMC with a large number of SMs.

The individual control is another solution to realize capacitor voltage balancing in the MMC, where the capacitor voltage in each SM is individually controlled. The individual control avoids the sorting algorithm in comparison with the sorting-based capacitor voltage control method, especially for the MMC with a large number of SMs, which improves the system modularity [13]. Reference [28] presents several individual control methods for MMC capacitor voltage

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balancing through adding capacitor voltage balancing compensation signal in both upper and lower arms. The capacitor voltage balancing compensation signal can be obtained in three ways including the product of the flow direction signal of corresponding arm current and the error between reference capacitor voltage and measured capacitor voltage, the product of the corresponding arm current and the error between reference capacitor voltage and measured capacitor voltage, the product of the corresponding load current and the error between reference capacitor voltage and measured capacitor voltage. Reference [29] presents an individual control for MMC voltage balancing through adding the capacitor voltage balancing signal, which is derived from the corresponding grid current and the error between reference capacitor voltage and measured capacitor voltage. However, all above methods require the exact knowledge of the arm current or the grid current.

In this paper, a currentless SM individual voltage balancing control (SMIVBC) is proposed to realize capacitor voltage balancing in the MMC. In the SMIVBC, each SM capacitor voltage is individually controlled by the dc component in the corresponding SM capacitor current, while the dc component in the SM capacitor current can be controlled by the modulation index m or the phase angle θ of the reference signal for the corresponding SM. The proposed SMIVBC based on m-SMIVBC and θ-SMIVBC can effectively realize the SM capacitor voltage balancing in the MMC with the advantages as follows. The proposed SMIVBC does not require a sorting technique to select the SMs, which avoids the sorting algorithm for the MMC, especially for the MMC with a large number of SMs. What is more, the proposed SMIVBC can be realized without the knowledge of the current, which reduces sensors, eliminates the adverse effects caused by the sensor noise and improves the reliability.

The paper is organized as follows. In Section II, the basic operation principles of the MMC are presented. Section III analyzes the capacitor voltage regulation relationship. Section IV proposes the SMIVBC. Sections V and VI adopt simulations and experimental tests, respectively, to verify the proposed control. Finally, Section VII presents the conclusion.

II. Operation Principles of MMCs

A three-phase MMC is shown in Fig. 1(a), which consists of six arms. Each arm contains n identical SMs and an arm inductor L_s. Fig. 1(b) shows the i-th SM in the upper arm of phase A, which is a half-bridge structure and made up of the switch/diode T_1/D_1, T_2/D_2 and a dc capacitor C_{sm} [16].

Table I shows two normal states of the i-th SM in the upper arm of phase A, including "ON" state and "OFF" state. When the SM works at "ON" state, the T_1 is switched on and the T_2 is switched off. Here, the charge or discharge of the capacitor C_{sm} relies on the direction of the arm current i_{ua}. If the i_{ua} is positive, the capacitor voltage u_{caui} increases with the charge of capacitor C_{sm}; otherwise, the u_{caui} decreases with the discharge of C_{sm} if the i_{ua} is negative. When the SM works at "OFF" state, the T_1 is switched off and the T_2 is switched on. Here, the C_{sm} is bypassed and the capacitor voltage u_{caui} remains unchanged.

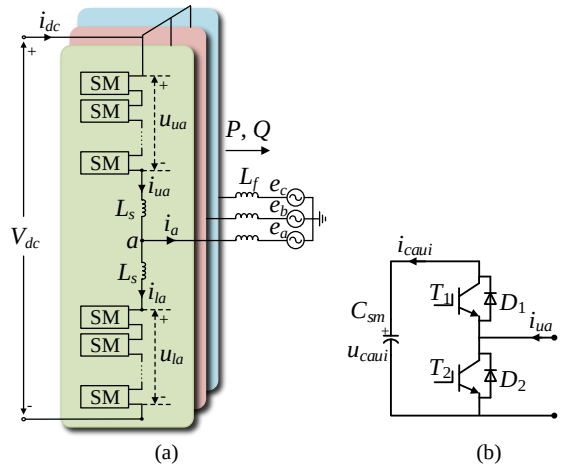

Fig. 1. (a) Three-phase MMC system. (b) SM unit.

TABLE I
SM Operation

state	T_1	T_2	i_{ua}	C_{sm}	u_{caui}
ON	on	off	≥0	Charge	Increased
			<0	Discharge	Decreased
OFF	off	on	≥0 or <0	Bypass	Unchanged

According to [18], the MMC output voltage in phase j (j=a, b, c) is

$$u_j = \frac{u_{lj} - u_{uj}}{2} \tag{1}$$

where u_{uj} and u_{lj} are the total output voltages of the series-connected SMs in the upper and lower arms of phase j, respectively, as shown in Fig. 1(a).

III. Analysis of SM Capacitor Voltage Regulation

A. Analysis of Capacitor Voltage

Suppose that the ac current in phase A is

$$i_a = I_m \cos(\omega t + \theta) \tag{2}$$

and the circulating current in the MMC is suppressed, the upper arm current i_{ua} in phase A can be expressed as

$$i_{ua} = \frac{I_m}{2}\cos(\omega t + \theta) + \frac{i_{dc}}{3} \tag{3}$$

where I_m and θ are peak value and phase angle of the current i_a at the ac side of the MMC, respectively. ω is the fundamental angular frequency. i_{dc} is the dc-link current of the MMC.

According to [30] and [31], the capacitor current i_{caui} in the i-th SM of the upper arm of phase A, can be expressed as

$$i_{caui} = i_{ua} \cdot \frac{1 + y_{au}}{2} \tag{4}$$

with

$$y_{au} = -m \cdot \cos(\omega t) \tag{5}$$

where y_{au} is the reference for the upper arm of phase A. m is modulation index. Substituting (3) and (5) into (4), the capacitor current i_{caui} can be rewritten as

$$i_{caui} = \underbrace{i_{cdc}}_{\textbf{DC Component}} + \underbrace{\left[\frac{I_m}{4}\cos(\omega t + \theta) - \frac{m i_{dc}}{6}\cos(\omega t)\right]}_{\text{Fundamental Component}} - \underbrace{\frac{m I_m}{8}\cos(2\omega t + \theta)}_{\text{Second-order Component}} \tag{6}$$

with

$$i_{cdc} = \frac{i_{dc}}{6} - \frac{mI_m}{8}\cos(\theta) \quad (7)$$

According to (6), the dc component i_{cdc} is zero in the steady-state operation of the MMC. In addition, the SM capacitor voltage can be regulated by the i_{cdc}, as

- capacitor voltage is increased by increase of i_{cdc};
- capacitor voltage is reduced by reduction of i_{cdc}.

According to (7), the i_{cdc} in each SM can be controlled by the corresponding modulation index m or the phase angle θ, which depends on the MMC operation mode. Fig. 2 shows eight MMC operation modes, where $\vec{u}_s$ and $\vec{i}_s$ are the vectors of the MMC voltage u_a, u_b, u_c and current i_a, i_b, i_c, respectively, and $\vec{u}_s$ aligns along with the x-axis. The phase angle between $\vec{u}_s$ and $\vec{i}_s$ is θ.

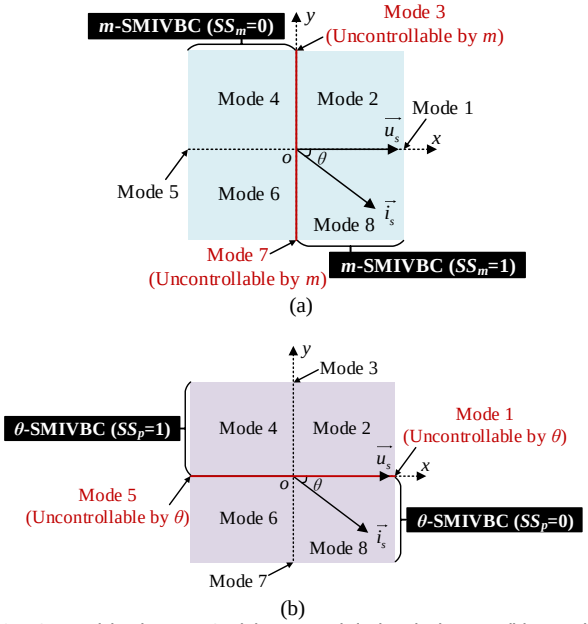

Fig. 2. Control in the MMC. (a) By modulation index m. (b) By phase angle θ.

In mode 1, θ=0, the active power P is positive and the reactive power Q is 0. In mode 2, $0<\theta<\pi/2$ and $P>0$, $Q>0$. In mode 3, $\theta=\pi/2$ and $P=0$, $Q>0$. In mode 4, $\pi/2<\theta<\pi$ and $P<0$, $Q>0$. In mode 5, $\theta=\pi$ and $P<0$, $Q=0$. In mode 6, $\pi<\theta<3\pi/2$ and $P<0$, $Q<0$. In mode 7, $\theta=3\pi/2$ and $P=0$, $Q<0$. In mode 8, $3\pi/2<\theta<2\pi$ and $P>0$, $Q<0$.

B. Control of i_{cdc} by Modulation Index m

The control of i_{cdc} by m for the i-th SM in the MMC under different operation modes are shown in Table II and Fig. 2(a), as follows.

1) Mode 1, 2 and 8: $P>0$. Here, $i_{dc}>0$ and $\cos(\theta)>0$. According to (7), the i_{cdc} can be increased by the reduction of m and reduced by the increase of m.
2) Mode 3 and 7: $P=0$. Here, $i_{dc}=0$ and $\cos(\theta)=0$. According to (7), the i_{cdc} can not be controlled by m.
3) Mode 4, 5 and 6: $P<0$. Here, $i_{dc}<0$ and $\cos(\theta)<0$. According to (7), the i_{cdc} can be increased by the increase of m and reduced by the reduction of m.

TABLE II
CONTROL OF i_{cdc} BY M

Mode	P	i_{dc}	$\cos(\theta)$	m	i_{cdc}
1, 2, 8	>0	>0	>0	Inversely proportional	
3, 7	0	0	0	Uncontrollable	
4, 5, 6	<0	<0	<0	Proportional	

Table II shows that, the i_{cdc} in each SM capacitor current can be controlled by the corresponding modulation index m of the reference signal for each SM when the MMC works in various operation modes except Modes 3 and 7. When the MMC works in the right side of the y-axis, the i_{cdc} is proportional to the m; when the MMC works in the left side of the y-axis, the i_{cdc} is inversely proportional to the m.

C. Control of i_{cdc} by Phase Angle θ

The control of i_{cdc} by θ for the i-th SM in the MMC under different operation modes are shown in Table III and Fig. 2(b), as follows.

1) Mode 1: $P>0$ and $Q=0$. Here, the $\cos(\theta)$ reaches its maximum 1. According to (7), the i_{cdc} can not be regulated by θ.
2) Mode 2: $P>0$ and $Q>0$. Here, $i_{dc}>0$ and $\cos(\theta)>0$. According to (7), the i_{cdc} can be increased by the increase of θ and reduced by the reduction of θ.
3) Mode 3: $P=0$ and $Q>0$. Here, $i_{dc}=0$. According to (7), the i_{cdc} can be increased by the increase of θ and reduced by the reduction of θ.
4) Mode 4: $P<0$ and $Q>0$. Here, $i_{dc}<0$ and $\cos(\theta)<0$. According to (7), the i_{cdc} can be increased by the increase of θ and reduced by the reduction of θ.
5) Mode 5: $P<0$ and $Q=0$. Here, the $\cos(\theta)$ reaches its minimum -1. According to (7), the i_{cdc} can not be regulated by θ.
6) Mode 6: $P<0$ and $Q<0$. Here, $i_{dc}<0$ and $\cos(\theta)<0$. According to (7), the i_{cdc} can be increased by the reduction of θ and reduced by the increase of θ.
7) Mode 7: $P=0$ and $Q<0$. Here, $i_{dc}=0$. According to (7), the i_{cdc} can be increased by the reduction of θ and reduced by the increase of θ.
8) Mode 8: $P>0$ and $Q<0$. Here, $i_{dc}>0$ and $\cos(\theta)>0$. According to (7), the i_{cdc} can be increased by the reduction of θ and reduced by the increase of θ.

TABLE III
CONTROL OF i_{cdc} BY θ

Mode	Q	i_{dc}	$\cos(\theta)$	θ	i_{cdc}
1	0	>0	1	Uncontrollable	
5	0	<0	-1		
2	>0	>0	>0	Proportional	
3		0	0		
4		<0	<0		
6	<0	<0	<0	Inversely proportional	
7		0	0		
8		>0	>0		

Table III shows that, the dc component i_{cdc} in each SM capacitor current can be controlled by the corresponding phase angle θ of the reference signal for each SM when the MMC works in various modes except Modes 1 and 5. When the MMC works above the x-axis, the i_{cdc} is proportional to the θ; when the MMC works below the x-axis, the i_{cdc} is inversely proportional to the θ.

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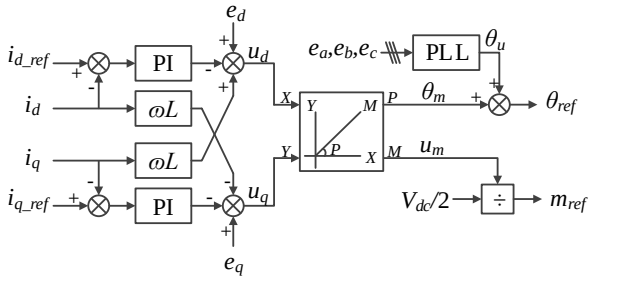
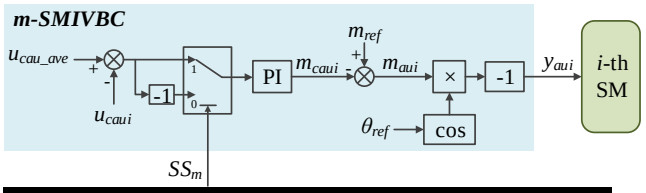
IV. Proposed SM Individual Voltage Balancing Control for MMCs

The central control for the MMC is shown in Fig. 3(a), where the e_a, e_b, e_c are the grid voltages and the i_a, i_b, i_c are the grid currents, as shown in Fig. 1(a). e_d, e_q and i_d, i_q are the dq-axis components of the grid voltage and current, respectively. $L=L_s/2+L_f$. L_f is filter inductance, as shown in Fig. 1(a). Based on the control objective of the three-phase MMC system such as active power control, reactive power control and dc-link voltage control, the current references i_{d_ref} and i_{q_ref} can be obtained [14], [18]. The vector control method is adopted in Fig. 3(a), which regulates the i_d, i_q to follow the current references i_{d_ref} and i_{q_ref}, respectively, and generates the dq-axis voltage references u_d and u_q, respectively. Afterwards, the angle compensation component θ_m and the peak value u_m of the voltage reference can be obtained as

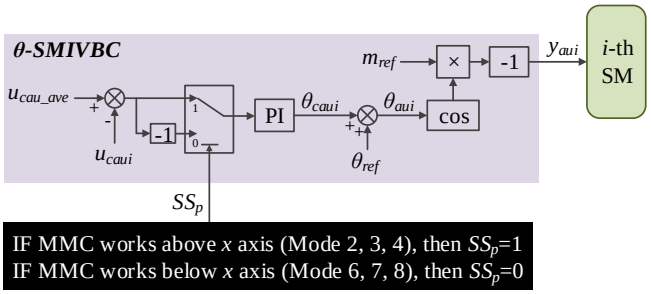
$$\begin{cases} \theta_m = \tan^{-1}(u_q / u_d) \\ u_m = \sqrt{u_d^{\,2} + u_q^{\,2}} \end{cases} \tag{8}$$



(a)



(b)



(c)

Fig. 3. (a) Central control of MMCs. (b) m-SMIVBC for the i-th SM in the upper arm of phase A. (c) θ-SMIVBC for the i-th SM in the upper arm of phase A.

The modulation index m_{ref} of the reference signal is $m_{ref}=2u_m/V_{dc}$. V_{dc} is the dc-link voltage of the MMC. In Fig. 3(a), the phase angle θ_u of the grid voltage can be obtained by the phase locked loop (PLL). The phase angle of the reference signal is $\theta_{ref}=\theta_m+\theta_u$.

For each SM in the MMC, the m-SMIVBC and θ-SMIVBC based on the relationship between i_{cdc} and m, θ in each SM are proposed, as shown in Figs. 3(b) and (c), respectively, to force the capacitor voltages in the arm to follow their average value and keep the capacitor voltage balancing in the MMC, as follows.

A. Proposed m-SMIVBC

Fig. 3(b) shows the proposed m-SMIVBC for the i-th SM in the upper arm of phase A. For each SM, the PI controller is used to regulate its modulation index m to ensure the capacitor voltage balancing. Fig. 3(b) shows the PI controller is used to produce the compensation modulation index m_{caui} for the i-th SM in the upper arm of phase A. The modulation index m_{aui} for the i-th SM in the upper arm of phase A is

$$m_{aui} = m_{ref} - m_{caui} \tag{9}$$

The reference for the i-th SM in the upper arm of phase A is

$$y_{aui} = -m_{aui} \cdot \cos(\theta_{ref}) \tag{10}$$

The implementation of the proposed m-SMIVBC is related to the operation mode of the MMC, where the selection signal SS_m is 1 when the MMC works in Mode 1, 2, 8; the selection signal SS_m is 0 when the MMC works in Mode 4, 5, 6, as shown in Fig. 3(b).

1) SS_m=1: If the capacitor voltage u_{caui} in the i-th SM is less than the average voltage u_{cau_ave} in the upper arm of phase A, the PI controller would increase the m_{caui} and reduce the m_{aui}. As a result, the dc component in the capacitor current would be increased according to Table II to increase u_{caui} to follow u_{cau_ave}. If $u_{caui}>u_{cau\_ave}$, the PI controller would reduce the m_{caui} and increase the m_{aui}. As a result, the dc component in the capacitor current would be reduced according to Table II to reduce u_{caui} to follow u_{cau_ave}.
2) SS_m=0: If $u_{caui}<u_{cau\_ave}$, the PI controller would reduce m_{caui} and increase m_{aui}. As a result, the dc component in the capacitor current would be increased according to Table II to increase u_{caui} to follow u_{cau_ave}. If $u_{caui}>u_{cau\_ave}$, the PI controller would increase m_{caui} and reduce m_{aui}. As a result, the dc component in the capacitor current would be reduced according to Table II to reduce u_{caui} to follow u_{cau_ave}.

Based on above analysis, the proposed m-SMIVBC can be applied to the MMC in some applications. For the MMC works with the power transferring from dc side to ac side such as medium-voltage motor drive [3], [32] and grid integration of photovoltaic system [33], the proposed m-SMIVBC with SS_m=1 can be adopted for the MMC. For the MMC works with the power transferring from ac side to dc side such as the active rectifier of the medium-voltage motor drive [2], [3], the m-SMIVBC with SS_m=0 can be adopted for the MMC.

B. Proposed θ-SMIVBC

Fig. 3(c) shows the proposed θ-SMIVBC for the i-th SM in the upper arm of phase A. For each SM, the PI controller is used to regulate its phase angle θ to ensure the capacitor voltage balancing. Fig. 3(c) shows the PI controller is used to produce the compensation phase angle θ_{caui} for the i-th SM in the upper

arm of phase A. The phase angle θ_{aui} for the i-th SM in the upper arm of phase A is

$$\theta_{aui} = \theta_{ref} + \theta_{caui} \tag{11}$$

The reference for the i-th SM in the upper arm of phase A is

$$y_{aui} = -m_{ref} \cdot \cos(\theta_{aui}) \tag{12}$$

The implementation of the proposed control is related to the operation mode of the MMC, where the selection signal SS_p is 1 when MMC works in Mode 2, 3, 4; the selection signal SS_p is 0 when MMC works in Mode 6, 7, 8, as shown in Fig. 3(c).

1) SS_p=1: If u_{caui}<u_{cau_ave}, the PI controller would increase θ_{caui} and increase θ_{aui}. As a result, the dc component in the capacitor current would be increased according to Table III to increase u_{caui} to follow u_{cau_ave}. If u_{caui}>u_{cau_ave}, the PI controller would reduce θ_{caui} and reduce θ_{aui}. As a result, the dc component in the capacitor current would be reduced according to the Table III to reduce u_{caui} to follow the u_{cau_ave}.
2) SS_p=0: If u_{caui}<u_{cau_ave}, the PI controller would reduce θ_{caui} and reduce θ_{aui}. As a result, the dc component in the capacitor current would be increased according to Table III to increase u_{caui} to follow u_{cau_ave}. If u_{caui}>u_{cau_ave}, the PI controller would increase θ_{caui} and increase θ_{aui}. As a result, the dc component in the capacitor current would be reduced according to the Table III to reduce u_{caui} to follow the u_{cau_ave}.

Based on above analysis, the proposed θ-SMIVBC can be applied to the MMC in some applications such as the MMC based STATCOM for reactive power regulation [3], [34], where the θ-SMIVBC with SS_p=1 is adopted for the MMC if sending reactive power to the ac grid; the θ-SMIVBC with SS_p=0 is adopted for the MMC if absorbing reactive power from the ac grid.

V. Simulation Studies

To verify the proposed SMIVBC for the MMC, an MMC system shown in Fig. 4 is built and simulated with the professional time-domain simulation tool PSCAD/EMTDC. The system parameters are shown in the Table IV. Figs. 5~13 show the performance of the MMC under the proposed SMIVBC, where the base value for the power is 5 MVA, the base value for grid voltage is the peak value of the grid line-to-line voltage. The base value for the current is the peak value of the grid current when active power is 5 MW and reactive power Q is 0. The base value for the capacitor voltage is the rated capacitor voltage.

A. MMC in Operation Mode 1 & m-SMIVBC

Fig. 5 shows the performance of the MMC working in Mode 1. According to Fig. 3, the proposed m-SMIVBC with SS_m=1 is adopted. Fig. 5(a) shows that the grid line-to-line voltage u_{ab} leads grid current i_a 30°. Here, the P is 1 p.u. and the Q is 0. Fig. 5(b) shows the upper and lower arm current i_{ua} and i_{la} in phase A. With the proposed control, the upper and lower arm capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 5(c).

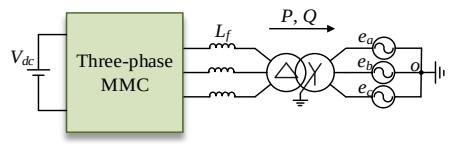


Fig. 4. Block diagram of the simulation system.

TABLE IV
Simulation System Parameters

Parameters	Value
DC-link voltage V_{dc} (kV)	6
RMS value of grid line-to-line voltage (kV)	33
Grid frequency (Hz)	50
Transformer voltage rating	3 kV/33 kV
Number of SMs per arm n	6
Rated capacitor voltage (kV)	1
Nominal SM capacitor C (mF)	15
Inductor L_s (mH)	2
Filter inductor L_f (mH)	0.5
Carrier frequency (kHz)	1

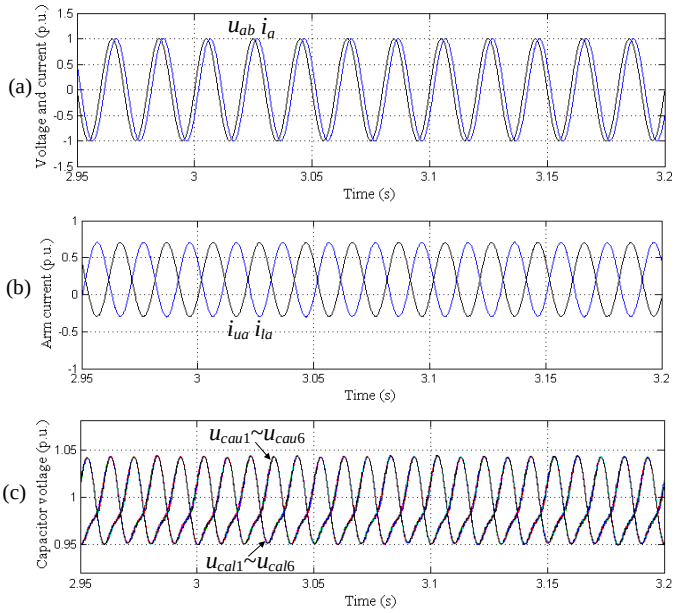


Fig. 5. (a) u_{ab} and i_a. (b) i_{ua} and i_{la}. (c) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

B. MMC from Operation Mode 8 to 2 & m-SMIVBC

Fig. 6 shows the performance of the MMC working from Mode 8 to 2. According to Fig. 3, the proposed m-SMIVBC with SS_m=1 is adopted here. Fig. 6(a) shows that the P is 1 p.u. and the Q is gradually changed from -0.4 p.u. to 0.4 p.u. With the proposed control, the capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 6(b).

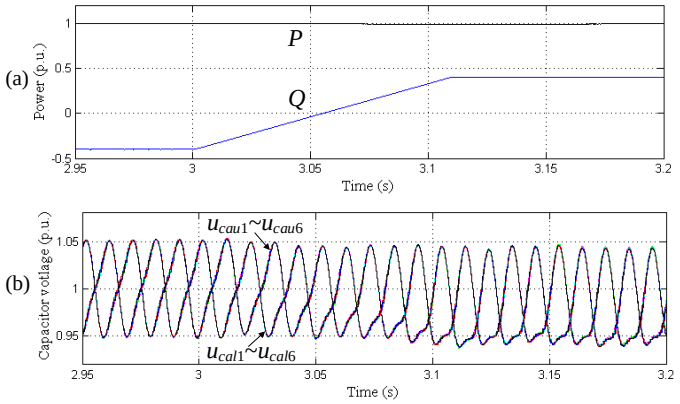


Fig. 6. (a) P and Q. (b) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

C. MMC in Operation Mode 5 & m-SMIVBC

Fig. 7 shows the performance of the MMC in Mode 5, where the proposed *m*-SMIVBC with SS_m=0 is adopted. In this situation, the P is -1 p.u. and Q is 0. Fig. 7(a) shows that the u_{ab} lags i_a 150º. Fig. 7(b) shows the i_{ua} and i_{la} in phase A. With the proposed control, the capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 7(c).

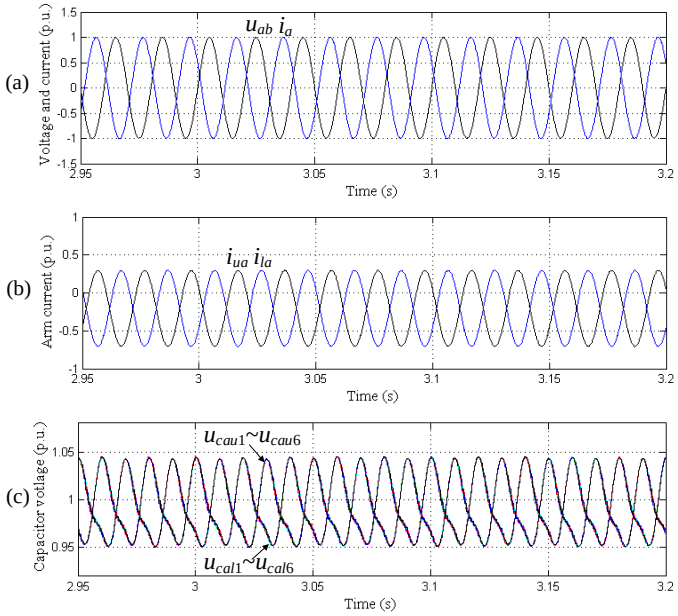


Fig. 7. (a) u_{ab} and i_a. (b) i_{ua} and i_{la}. (c) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

D. MMC from Operation Mode 6 to 4 & m-SMIVBC

Fig. 8 shows the performance of the MMC working from Mode 6 to 4. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=0 is adopted here. Fig. 8(a) shows that the P is 1 p.u. and the Q is gradually changed from -0.4 p.u. to 0.4 p.u. With the proposed control, the capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 8(b).

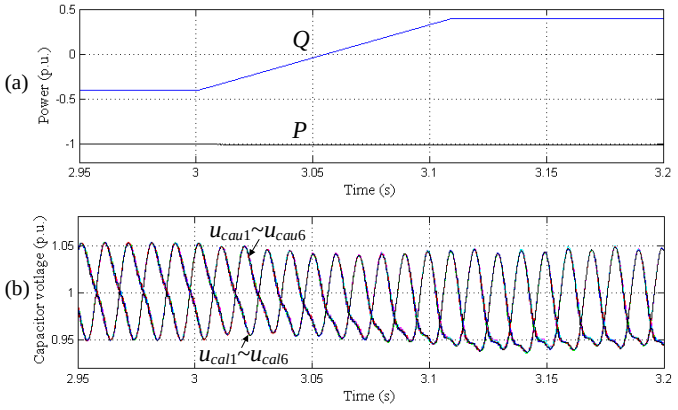


Fig. 8. (a) P and Q. (b) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

E. MMC in Operation Mode 3 & θ-SMIVBC

Fig. 9 shows the performance of the MMC working in Mode 3. According to Fig. 3, the proposed θ-SMIVBC with SS_p=1 is adopted here. Fig. 9(a) shows that u_{ab} leads i_a 120º. In this situation, the P is 0 and Q is 1 p.u. Fig. 9(b) shows the upper and lower arm current i_{ua} and i_{la} in phase A. With the proposed control, the upper arm capacitor voltages u_{cau1}~u_{cau6} and the lower arm capacitor voltages u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 9(c).

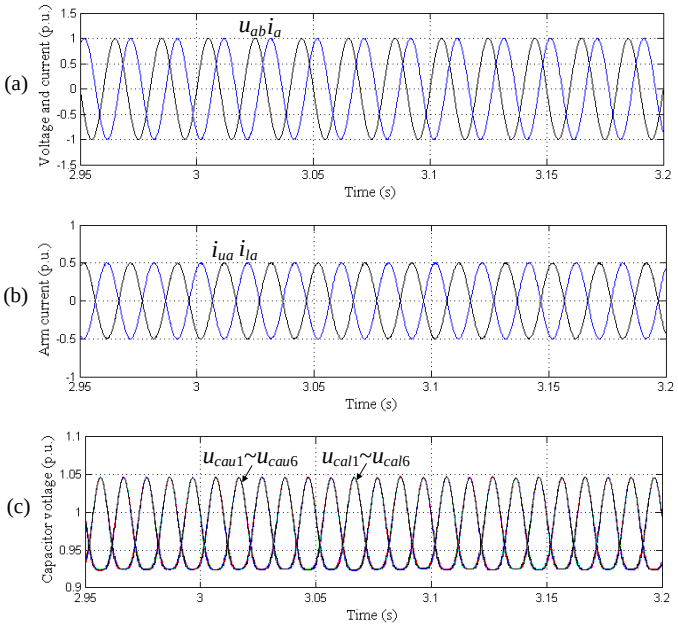


Fig. 9. (a) u_{ab} and i_a. (b) i_{ua} and i_{la}. (c) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

F. MMC from Operation Mode 4 to 2 & θ-SMIVBC

Fig. 10 shows the performance of the MMC working from Mode 4 to 2. According to Fig. 3, the proposed θ-SMIVBC with SS_p=1 is adopted here. Fig. 10(a) shows that the Q is 1 p.u. and the P is gradually changed from -0.4 p.u. to 0.4 p.u. With the proposed control, the u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 10(b).

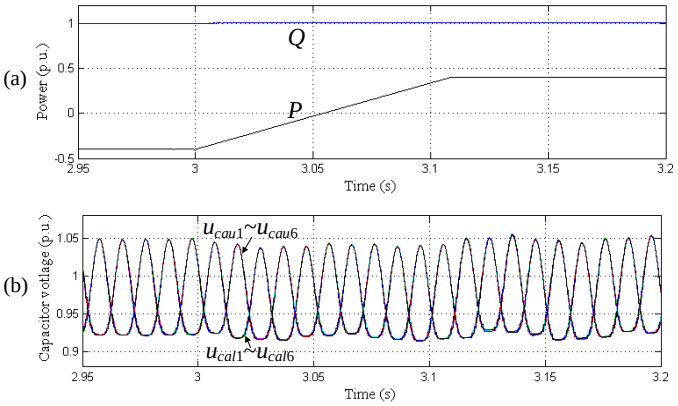


Fig. 10. (a) P and Q. (b) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

G. MMC in Operation Mode 7 & θ-SMIVBC

Fig. 11 shows the performance of the MMC working in Mode 7. According to Fig. 3, the proposed θ-SMIVBC with SS_p=0 is adopted here. Fig. 11(a) shows that u_{ab} lags i_a 60º. In this situation, the P is 0 and Q is -1 p.u. Fig. 11(b) shows the upper and lower arm current i_{ua} and i_{la} in phase A. With the proposed control, the capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 11(c).

H. MMC from Operation Mode 6 to 8 & θ-SMIVBC

Fig. 12 shows the performance of the MMC working from Mode 6 to 8. According to Fig. 3, the proposed θ-SMIVBC with SS_p=0 is adopted here. Fig. 12(a) shows that the Q is -1 p.u. and the P is gradually changed from -0.4 p.u. to 0.4 p.u. With the proposed control, the u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced, as shown in Fig. 12(b).

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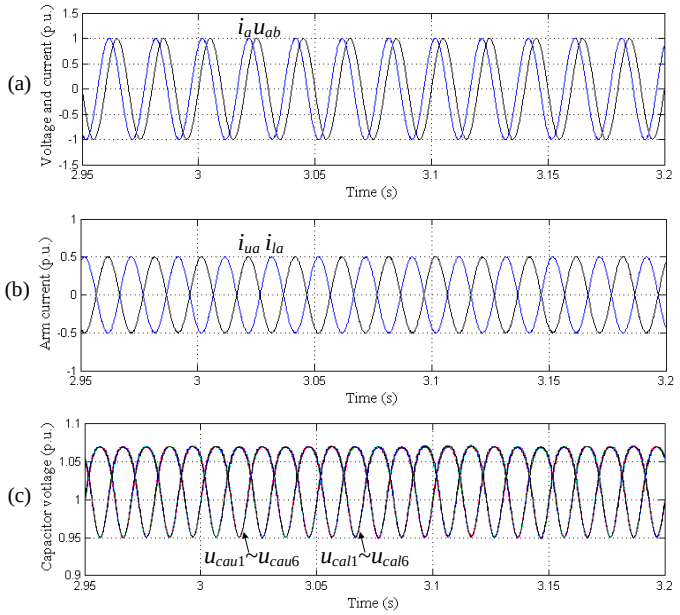


Fig. 11. (a) u_{ab} and i_a. (b) i_{ua} and i_{la}. (c) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

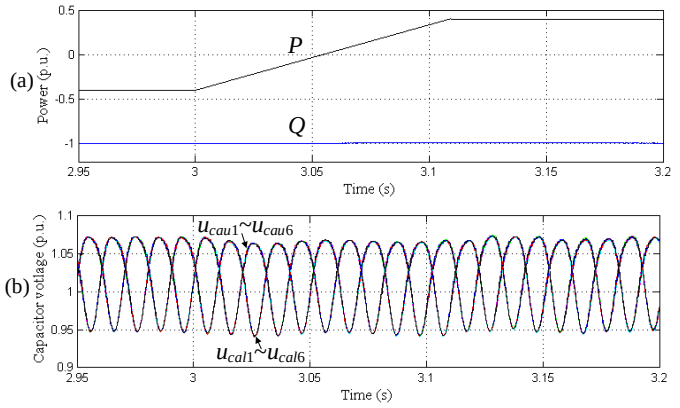


Fig. 12. (a) P and Q. (b) u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6}.

I. MMC under Various Frequencies

Fig. 13 shows the performance of the MMC under various ac-side frequencies. Here, the MMC works in Mode 1 and the proposed *m*-SMIVBC with SS_m=1 is adopted. For Figs. 13(a)~(d), the P is 4 MW, 3 MW, 2 MW and 1 MW, respectively; the ac-side frequency is 40 Hz, 30 Hz, 20 Hz and 10 Hz, respectively. Figs. 13(a)~(d) show that the capacitor voltages u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} are kept balanced by the proposed control under various frequencies.

VI. Experimental Studies

A three-phase MMC prototype, as shown in Fig. 14(a), is built in the laboratory to confirm the proposed SMIVBC. Fig. 14(b) shows the photo of the experimental setup. A dc power supply (LAB/SMS6600) parallel with the load is used to support the dc link. The ac side of the MMC is connected to the grid via an autotransformer *AT* and an isolation transformer *T*. The IXFK48N60P is used as switch/diode. The control algorithm is implemented in the digital signal process (DSP) controller and the pulse signal from the controller is transferred to the driving panel of each SM by the optical fiber. The system parameters are shown in Table V.

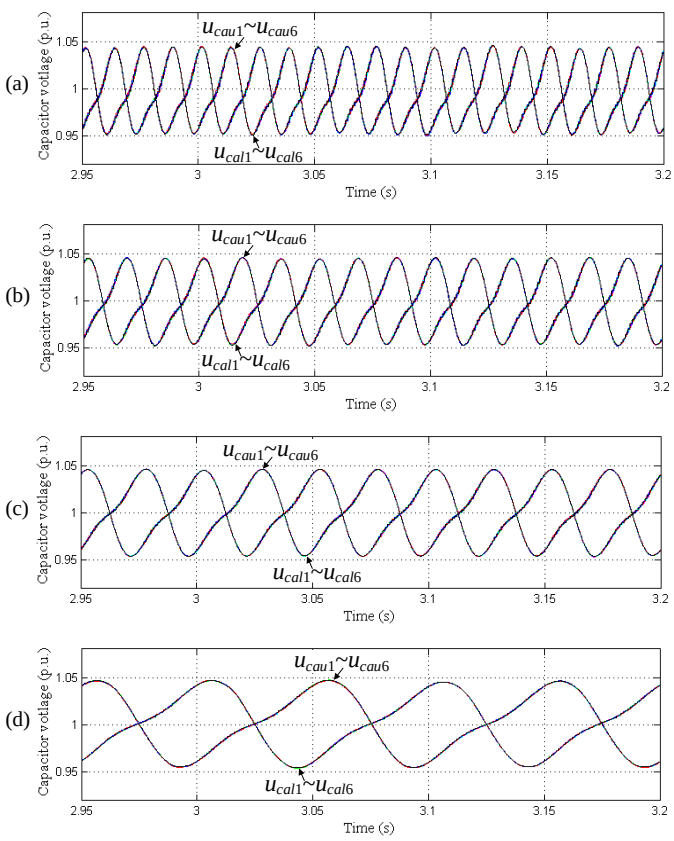
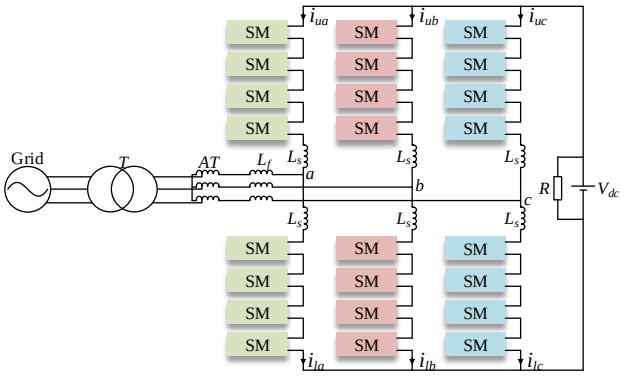
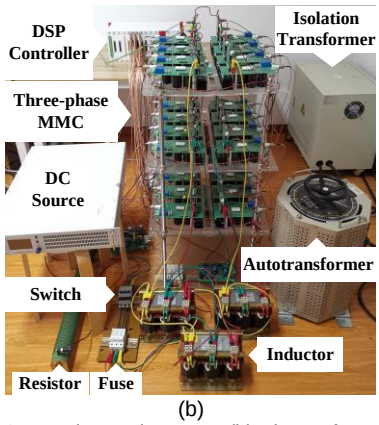


Fig. 13. u_{cau1}~u_{cau6} and u_{cal1}~u_{cal6} under various frequencies. (a) 40 Hz. (b) 30 Hz. (c) 20 Hz. (d) 10 Hz.



(a)



(b)

Fig. 14. (a) MMC experimental system. (b) Photo of experimental setup.

TABLE V
EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
DC-link voltage V_{dc} (V)	200
RMS value of line-to-line voltage at MMC side of *AT*	82
Grid frequency (Hz)	50
Number of SMs per arm n	4
Nominal capacitor C_{sm} (mF)	2.35
Inductor L_s (mH)	3
Filter inductor L_f (mH)	3
Switching frequency (kHz)	1

A. MMC in Mode 1 & m-SMIVBC

Fig. 15 shows the performance in phase A of the MMC, where the MMC works in Mode 1. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=1 is adopted here. In this case, the active power P is step changed from 500 W to 1 kW. Fig. 15 shows the upper arm capacitor voltages u_{cau1}~u_{cau3}, the lower arm capacitor voltages u_{cal1}~u_{cal3}, the upper arm current i_{ua}, the lower arm current i_{la}, the ac current i_a and the line-to-line voltage u_{ab}, where the line-to-line voltage u_{ab} leads the ac current i_a 30º. Along with the increase of the active power, the i_{ua}, i_{la}, i_a, the ripples of the upper arm capacitor voltages u_{cau1}~u_{cau3} and the ripples of the lower arm capacitor voltages u_{cal1}~u_{cal3} are increased. With the proposed control, the upper arm capacitor voltages u_{cau1}~u_{cau3} and the lower arm capacitor voltages u_{cal1}~u_{cal3} are kept balanced.

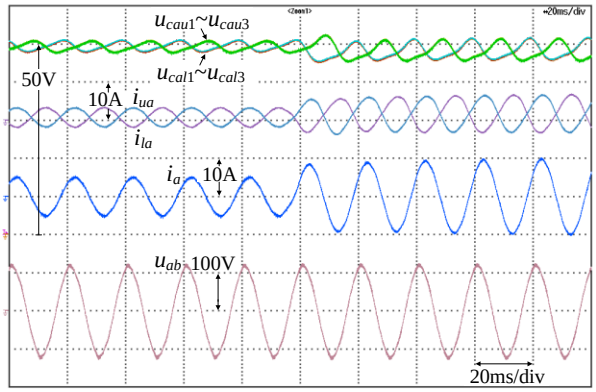


Fig. 15. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

Fig. 16 shows the dynamic performance of the MMC. In stage-I, the capacitor voltages are kept balanced by *m*-SMIVBC. In stage-II, the proposed *m*-SMIVBC is disabled, which leads to divergence of the capacitor voltages. However, after the propose *m*-SMIVBC is enabled again in stage-III, the dc component in the SM capacitor current, whose voltage is less than the reference value, will be controlled to a positive value, which will result in the increase of the SM capacitor voltage; the dc component in the SM capacitor current, whose voltage is more than the reference value, will be controlled to a negative value, which will result in the reduction of the SM capacitor voltage. As a result, the capacitor voltages in the arm recover to balancing again in stage-III.

B. MMC from Mode 2 to 8 & m-SMIVBC

Fig. 17 shows the performance in phase A of the MMC, where the MMC works from Mode 2 to 8. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=1 is adopted here. In this case, the P is 800 W and Q is step changed from 600 Var to -600 Var. Fig. 17 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed *m*-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

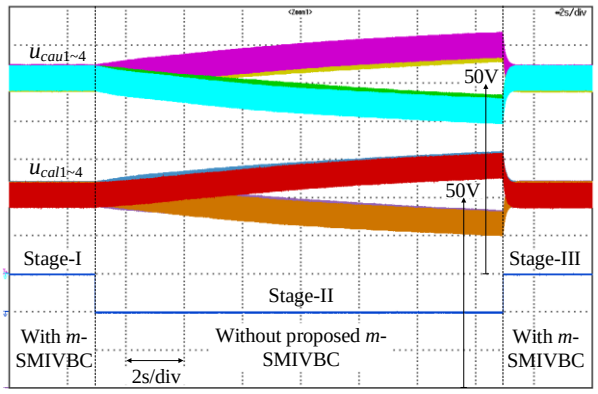


Fig. 16. u_{cau1}~u_{cau4} (10 V/div), u_{cal1}~u_{cal4} (10 V/div).

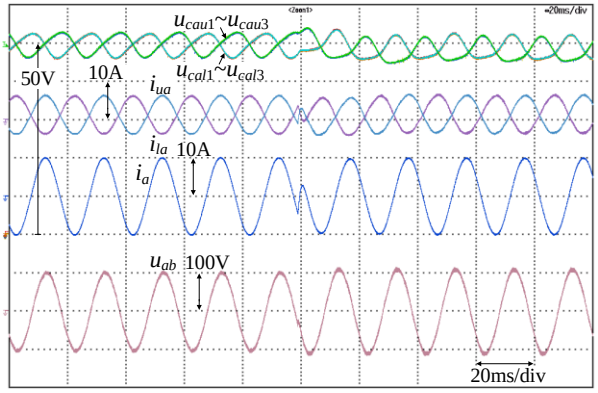


Fig. 17. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

C. MMC in Mode 5 & m-SMIVBC

Fig. 18 shows the performance in phase A of the MMC, where the MMC works in Mode 5. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=0 is adopted here. In this case, the P is step changed from -500 W to -1 kW. Fig. 18 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}, where u_{ab} lags i_a 150º. Along with the reduction of the P, the i_{ua}, i_{la}, i_a, the ripples of u_{cau1}~u_{cau3} and the ripples of u_{cal1}~u_{cal3} are increased. With the proposed *m*-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

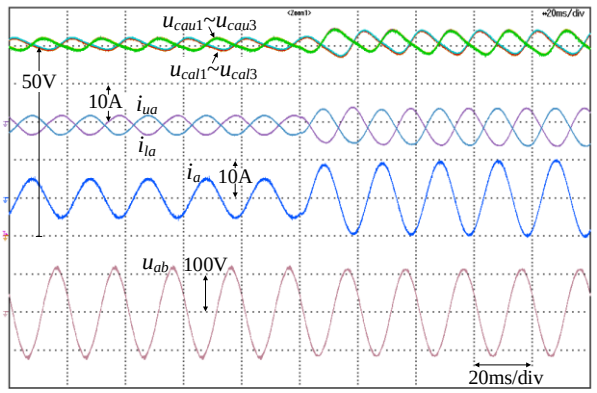


Fig. 18. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

D. MMC from Mode 4 to 6 & m-SMIVBC

Fig. 19 shows the performance in phase A of the MMC, where the MMC works from Mode 4 to 6. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=0 is adopted here. In this case, the *P* is -800 W and *Q* is step changed from 600 Var to -600 Var. Fig. 19 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed *m*-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

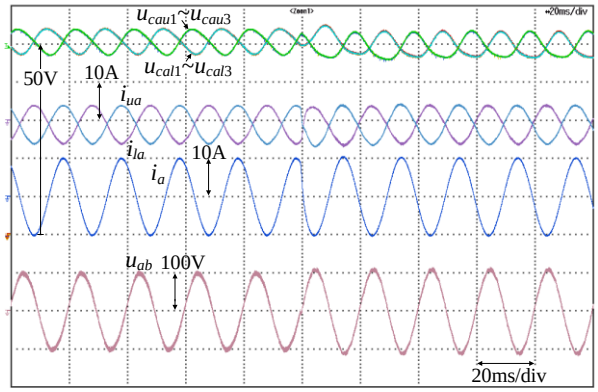


Fig. 19. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

E. MMC in Mode 3 & θ-SMIVBC

Fig. 20 shows the performance in phase A, where the MMC works in Mode 3. According to Fig. 3, the proposed *θ*-SMIVBC with SS_p=1 is adopted here. In this case, the *Q* is step changed from 500 Var to 1 kVar. Fig. 20 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}, where u_{ab} leads i_a 120°. Along with the increase of the *Q*, the i_{ua}, i_{la}, i_a, the ripples of u_{cau1}~u_{cau3} and the ripples of u_{cal1}~u_{cal3} are increased. With the proposed *θ*-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

Fig. 21 shows the dynamic performance of the MMC. In stage-I, the upper and lower arm capacitor voltages in phase A are kept balanced by the proposed *θ*-SMIVBC. In stage-II, the proposed *θ*-SMIVBC is disabled, which leads to divergence of the capacitor voltages. However, after the action of the propose *θ*-SMIVBC in stage-III, the dc component in the SM capacitor current, whose voltage is less than the reference value, will be controlled to a positive value, which will result in the increase of the SM capacitor voltage; the dc component in the SM capacitor current, whose voltage is more than the reference value, will be controlled to a negative value, which will result in the reduction of the SM capacitor voltage. As a result, the capacitor voltages in the arm recover to balancing again in stage-III.

F. MMC from Mode 2 to 4 & θ-SMIVBC

Fig. 22 shows the performance in phase A of the MMC, where the MMC works from Mode 2 to 4. According to Fig. 3, the proposed *θ*-SMIVBC with SS_p=1 is adopted here. In this case, the *Q* is 800 Var and *P* is step changed from 600 W to -600 W. Fig. 22 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed *θ*-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

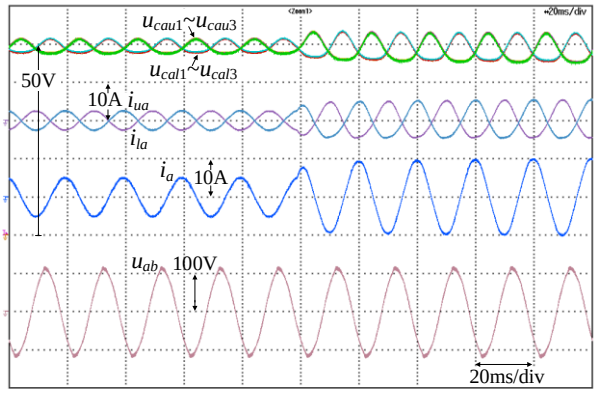


Fig. 20. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

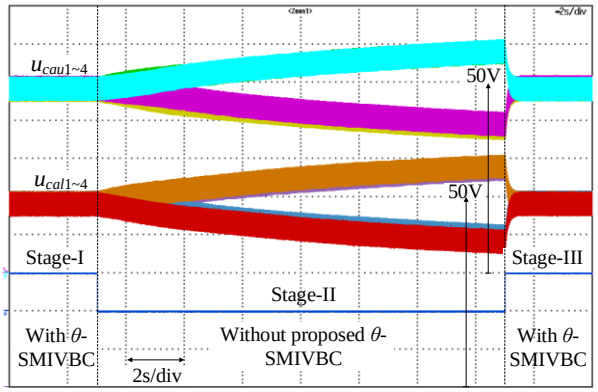


Fig. 21. u_{cau1}~u_{cau4} (10 V/div), u_{cal1}~u_{cal4} (10 V/div).

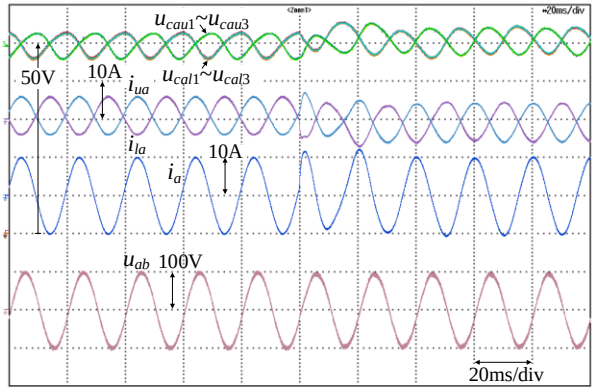


Fig. 22. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

G. MMC in Mode 7 & θ-SMIVBC

Fig. 23 shows the performance of the MMC in phase A, where the MMC works in Mode 7. According to Fig. 3, the proposed *θ*-SMIVBC with SS_p=0 is adopted here. In this case, the *Q* is step changed from -500 Var to -1 kVar. Fig. 23 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}, where u_{ab} lags i_a 60°. Along with the reduction of the *Q*, the i_{ua}, i_{la}, i_a, the ripples of u_{cau1}~u_{cau3} and the ripples of u_{cal1}~u_{cal3} are increased. With the proposed *θ*-SMIVBC, the capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

H. MMC from Mode 8 to 6 & θ-SMIVBC

Fig. 24 shows the performance in phase A of the MMC, where the MMC works from Mode 8 to 6. According to Fig. 3, the proposed *θ*-SMIVBC with SS_p=1 is adopted here. In this case, the *Q* is -800 Var and *P* is step changed from 600 W to

-600 W. Fig. 24 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed θ-SMIVBC, the upper and lower arm capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

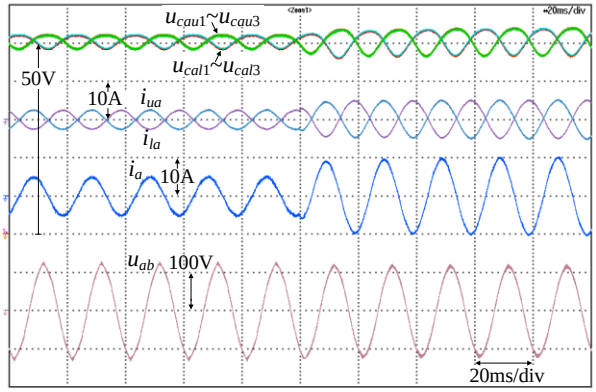


Fig. 23. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

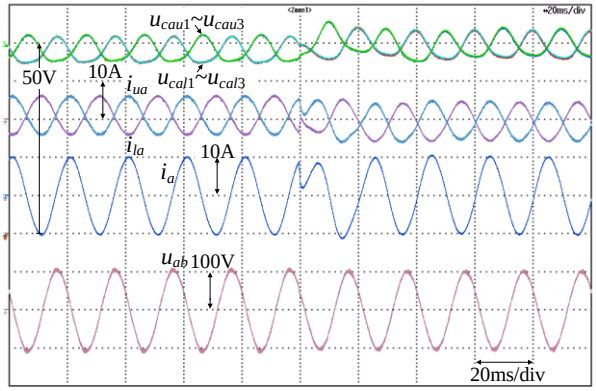


Fig. 24. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (10 A/div), i_{la} (10 A/div), i_a (10 A/div) and u_{ab} (100 V/div).

I. MMC under Low Frequency

Figs. 25 and 26 show the performance in phase A of the MMC, where the dc side of the MMC is connected to the dc power supply and the dc-side voltage is 200 V; the ac side of the MMC is the three-phase series-connected resistor and inductor load. The resistance is 60 Ω and the inductance is 4 mH in the series-connected resistor and inductor load. According to Fig. 3, the proposed *m*-SMIVBC with SS_m=1 is adopted for the capacitor voltage balancing control.

Fig. 25 shows the performance of the MMC when the ac-side voltage frequency is 10 Hz, where the modulation index is step changed from 0.8 to 0.5. Fig. 25 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed control, the upper arm capacitor voltages u_{cau1}~u_{cau3} and the lower arm capacitor voltages u_{cal1}~u_{cal3} are kept balanced.

Fig. 26 shows the performance of the MMC when the ac-side voltage frequency is 5 Hz, where the modulation index is step changed from 0.8 to 0.5. Fig. 26 shows u_{cau1}~u_{cau3}, u_{cal1}~u_{cal3}, i_{ua}, i_{la}, i_a and u_{ab}. With the proposed control, the capacitor voltages u_{cau1}~u_{cau3} and u_{cal1}~u_{cal3} are kept balanced.

VII. CONCLUSION

This paper proposes a currentless SMIVBC for MMCs. The capacitor voltage in each SM can be controlled by the dc component in capacitor current. The dc component in capacitor current can be regulated by the modulation index except that the MMC works with zero active power or regulated by the phase angle except that the MMC works with zero reactive power. With proposed SMIVBC, the capacitor voltage can be kept balanced in the MMC. In addition, the proposed SMIVBC does not require a sorting technique to select the SMs, which avoids the sorting algorithm, especially for the MMC with a large number of SMs. What is more, each SM capacitor voltage can be kept balanced without the knowledge of current, which reduces sensors and sampling signals, saves cost and improves reliability. Simulation with professional tool PSCAD/EMTDC and experiment with a down-scale prototype are both conducted to verify the effectiveness of the proposed SMIVBC.

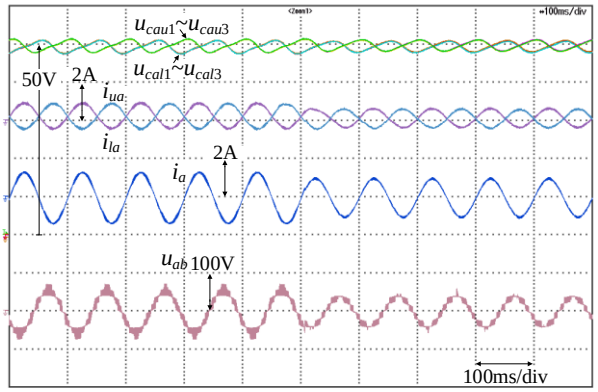


Fig. 25. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (2 A/div), i_{la} (2 A/div), i_a (2 A/div) and u_{ab} (100 V/div).

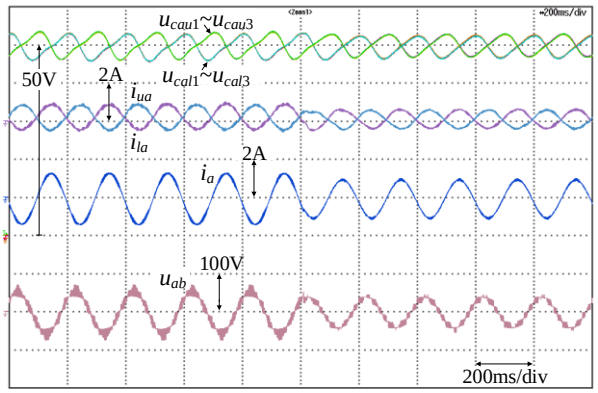


Fig. 26. u_{cau1}~u_{cau3} (10 V/div), u_{cau1}~u_{cau3} (10 V/div), i_{ua} (2 A/div), i_{la} (2 A/div), i_a (2 A/div) and u_{ab} (100 V/div).

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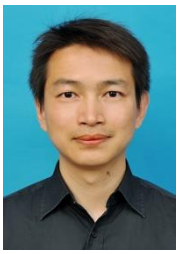

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