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A New Multilevel Inverter Topology With Reduced Power Components for Domestic Solar PV Applications

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ABSTRACT Power electronic converters are used to nullify the input fluctuations from a solar photovoltaic unit because of intermittent solar irradiance and to make the terminal voltage grid compatible with the desired frequency. The conventional two-level converters suffer from low power quality and high voltage stress. In this article, a new multilevel inverter topology called Dual Source Multilevel Inverter (DS-MLI) with fewer power switches is proposed for solar PV power conversion systems. It can operate in symmetric and asymmetric operating modes with no cascading. This reduces the switching components required to produce several levels in the staircase voltage waveform. A closed-loop control algorithm is designed using the state-space averaging technique, and we assess the dynamic behaviour of the system under step change. We carry the simulation out in MATLAB environment. The experimental prototype of DS-MLI rated 1 kW is fabricated using FGA25N120-ANTD IGBTs, and an eco-sense made solar PV emulator is used for analysing the performance of DS-MLI while interfacing with solar PV unit. We compare the suggested scheme with its conventional counterpart in the aspects of components required, cost and efficiency, and the results are presented.

INDEX TERMS DS-MLI, multilevel inverter, solar PV, power conversion, fundamental frequency switching.

I. INTRODUCTION

With technology, the price of the solar PV panels and the associated accessories has reduced drastically over the years [1]. This resulted in tremendous growth in the installed capacity from 50 GWp in 2010 to 633 GWp in 2019 around the world [2]. It is expected to increase at the same pace in the years to come. Because of the intermittency in solar irradiance, the voltage delivered at the terminals of a solar PV unit will be continuously fluctuating, and power electronic converters are used to deliver a regulated terminal voltage under this varying irradiance [3]. The conventional two-level inverters suffer from high switching voltage stress, low power quality and efficiency, as stated in [4], [5]. Also, the two-level inverters need an isolation transformer to prevent the EMI noise caused by common-mode voltage, as explained in [6]. To overcoming these drawbacks, multilevel inverters are being used for grid integration of solar PV units [7]. Among the three classical multilevel inverter topologies, the Cascaded H-Bridge Multilevel Inverters (CHB-MLI) is preferred for solar power conversion because of their modularity and simple control circuitry [8]. For the given 'n' number of sources, the CHB-MLI will synthesize 2n+1 level, i.e., with two DC sources it can synthesize five levels.

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Thus, the CHB-MLI topologies require a higher number of switches for the higher number of levels in the terminal voltage [9]. They focus the recent research on reducing the number of switches in CHB-MLI topology [10]. A Cross Connected Sources based Multilevel Inverter (CCS-MLI) topology, which requires 2n+2 switches for 'n' number of sources, is proposed in [11]. Here, the number of switches in the conduction path is high at a higher number of levels, and its asymmetric operation is yet to be explored. A sub-MLI module with reduced power components is explained in [12] wherein all the switches in the level adder are bidirectional. They discuss an envelope types basic unit which can be cascaded with many such units for the higher number of levels in the terminal voltage in [13]. But the topology requires a minimum of four independent sources. It gives a cascaded asymmetric MLI in [14] which can deliver 49 levels, but the blocking voltage across each switch is fourteen times the primary source which makes the application of this topology to higher voltage levels less likely. In the new asymmetric multilevel inverter topology suggested in [15], 12 switches are required to synthesize 21 levels in the terminal voltage in asymmetric mode. However, in the symmetric mode, it can offer only nine levels with 10 switches; also, it requires multiple independent sources, and for the addition of every source, it will add two more switches in the circuit. A cross-connected multilevel inverter is suggested in [16], but it requires cascading for asymmetric operation. The DS-MLI suggested in this article addresses the above concerns with its ability to operate in symmetric and asymmetric modes without cascading and with fewer components.

To maintain the DC-link voltage and grid current quality while interfacing the solar PV unit to the grid through DS-MLI, a suitable control loop needs to be developed. The dynamic performance of MLI with a control loop has been investigated by different authors. A Lyapunov based fast terminal sliding mode Q-V control for grid coupled hybrid solar PV and wind system is presented in [17], and this nonlinear control algorithm provides faster error tracking capability and robustness, but it lacks anti-inference ability. In [18], a fast and fixed switching frequency finite control set-model predictive control algorithm with delay compensation is used in a two-level voltage source inverter-based distributed generation system, but the multiple switching frequencies result in a sluggish response. A control algorithm for monophase cascaded H-bridge multilevel inverter it suggests based solar energy conversion system in [19], this method provides DC capacitor balancing and high-power quality during partial shading and panel mismatch conditions. A 2-cell Cascaded H-Bridge (CHB) multilevel inverter with unequal DC sources and 9- level operation is explained in [20], [21]. But all the above control techniques have drawbacks, like nonlinear characteristics and complex control. Here, a dual loop control technique with outer voltage control and inner current control to facilitate the interfacing of solar PV unit to the grid through DS-MLI is suggested. Thus, this article contributes to.

i) develop an H-Bridge based DS-MLI topology which requires fewer power switches when compared to the topologies found in recent literature and can achieve symmetric and asymmetric operation without cascading

ii) design a dual loop control scheme which gives better dynamic response under changing irradiance conditions.

We organise the rest of the paper: Section 2 and 3 explain the construction and switching operation of DS-MLI in symmetric and asymmetric mode. In section 4, and 5, the simulation of DS-MLI, and design of control loops are presented, and we analyse the stability of the system. Section 6 and 7 present the experimental results got while operating DS-MLI in isolated and grid-connected modes, and we give the conclusion in section 8.

II. DUAL SOURCE MULTILEVEL INVERTER

The dual-source multilevel inverter comprises only two independent voltage sources, and hence it is named so. The two independent sources V_{S1} and V_{S2} connected in level adder of the inverter circuit such that one source (V_{S1}) in the lower arm and the other in the upper arm (V_{S2}) as shown in the Fig.1. It bases the number of steps in the staircase waveform on the number of capacitors clamped in the lower and upper arm of the level adder. We get the polarity reversal using a polarity changer, which is an H-Bridge unit. When the voltage of both the independent sources is equal, then the inverter is said to be in symmetric mode. The inverter will be in asymmetric mode when the two voltage sources are at different voltages.

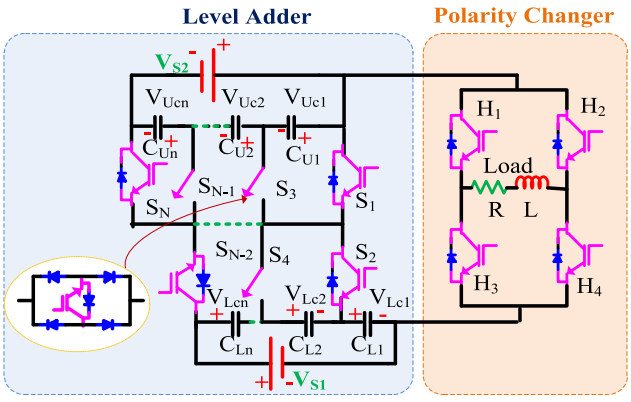

FIGURE 1. Proposed multilevel inverter topology.

The equations to determine the different design parameters for the number of capacitors (Nc) clamped to each arm, during symmetrical and asymmetrical operation of the topology is given in Table 1. From the table, we can find it that if the number of capacitors clamped in each arm is 2, the number of IGBTs required can be calculated as 9 (i.e., (2 x2) +5). Further for asymmetrical operation, if the number of capacitors connected in the lower arm is 2 and the magnitude of V_{s1} is fixed as V_{dc}, then the magnitude of voltage source connected to upper arm V_{s2} will be twice the magnitude of V_{s1}.

TABLE 1. Inverter parameters.

Parameter	Symmetric	Asymmetric
Number of IGBTs (N_{switch})	$2N_c+5$	$2N_c+5$
Number of Levels (N_{Level})	$4N_c+1$	$\{N_c[(N_c\times 2)+2]\}+1$
Voltage Magnitude of Sources	$V_{s2}=V_{s1}$	$V_{s2}=N_cV_{s1}$

III. SWITCHING SEQUENCE FOR SYMMETRIC AND ASYMMETRIC OPERATION

We can get the two independent voltage sources VS1 and VS2 using two solar PV units or capacitors. To understanding the symmetric operation, the voltage delivered by the two sources of DS-MLI is considered as $V_{S1} = V_{S2} = 160V$. For asymmetric mode, it is $V_{S1} = 110V$ and $V_{S2} = 220$ V. With two capacitors connected in each arm, the DS-MLI synthesises a nine-level staircase waveform during symmetric operation and thirteen levels during the asymmetric mode. The switches conducting to synthesise each level in both the modes are shown in Table 2 and Fig.2. In Table 2 'L' shows the level number. From Table 2, we observe it that the step size is 80V in symmetric operation and 55 V in asymmetric operation. For synthesising a voltage wave with 50 Hz, each step lasts for a duration of 1.25 ms in symmetric operation and 0.833 ms during asymmetric operation.

TABLE 2. Switching sequence of DS-MLI during symmetric and asymmetric operation.

Symmetric mode			Asymmetric Mode	
Voltage Produced (V)	Switches Conducting	L	Switches Conducting	Voltage Produced (V)
+ 80	S_1,S_2,H_1,H_4	1	S_1,S_2,H_1,H_4	+55
+ 160	S_2,S_3,H_1,H_4	2	S_1,S_4,H_1,H_4	+110
+240	S_3,S_4,H_1,H_4	3	S_2,S_3,H_1,H_4	+165
+320	S_4,S_5,H_1,H_4	4	S_3,S_4,H_1,H_4	+220
- 80	S_1,S_2,H_2,H_3	5	S_2,S_5,H_1,H_4	+275
- 160	S_2,S_3, H_2,H_3	6	S_4,S_5,H_1,H_4	+ 330
-240	S_3,S_4, H_2,H_3	7	S_1,S_2,H_2,H_3	-55
- 320	S_4,S_5, H_2,H_3	8	S_1,S_4, H_2,H_3	-110
0	H_1,H_2/H_3,H_4	9	S_2,S_3, H_2,H_3	-165
The additional levels synthesised in asymmetric operation		10	S_3,S_4, H_2,H_3	-220
		11	S_2,S_5, H_2,H_3	-275
		12	S_4,S_5, H_2,H_3	-330
		13	H_1,H_2/H_3,H_4	0

From Table 3 and Fig. 2, we observe it that except S_3 all the switches in the level adder undergoes two additional conduction periods in asymmetric mode when compared to the symmetric operation. This additional conduction delivers the additional levels in asymmetric operation.

TABLE 3. Switching instants of individual switches.

Switch	Number of times turned ON in a cycle of 20 ms	
	Symmetric mode	Asymmetric mode
S_1	2	4
S_2	4	6
S_3	4	4
S_4	4	6
S_5	2	4
H-Bridge Switches	1	1

IV. SIMULATION OF DS-MLI

The IGBT switch in MATLAB environment is used to simulate the Dual Source Multilevel Inverter. To achieving symmetric operation, we connect a 160 V DC source in lower and upper arms of DS-MLI. It achieves the asymmetric operation with DC sources rated 110 V and 220V, as stated earlier in section III. The IGBT switches in DS-MLI are controlled by using a fundamental frequency switching scheme called Nearest Level Modulation. In NLM method, the switching pulses for triggering the IGBTs to synthesize a voltage level is got by comparing the reference sine wave with the prior voltage level added to the nearest constant value that may range from 0.1 to 1 as shown in Fig.3a. We have established it in [22]–[24] that an NLM constant value of 0.4 is optimal since the Total Harmonic Distortion and the magnitude of lower order harmonics are less at a value of 0.4 as observed in Fig 3b.

We get the switching angle for each voltage level using (1)

$$\alpha_k = sin^{-1}\left(\frac{A-0.6}{N_{step}}\right) \tag{1}$$

where,

$$A = 1, 2, 3 \ldots \left(\frac{N_{level}-1}{2}\right) \tag{2}$$

$$N_{step} = \left(\frac{N_{level}-1}{2}\right) \tag{3}$$

The Constant 0.6 in equation 1 is got by subtracting the nearest level constant 0.4 from 1. The values of switching angle α_1 to α_4 (for symmetric operation) and α_1 to α_6 (for asymmetric operation) can be got using (1). We can calculate the other angles concerning π using the sine wave symmetry.

$$\text{THD} = \frac{\sqrt{\sum_{i=3,5,7}^{\infty} V_{0i}}}{V_{of}} \tag{4}$$

where,

$$V_{0i} = \frac{2\sqrt{2V}}{\pi}\sqrt{\sum_{i=1,3,\ldots\infty}\sum_{k=1}^{N_{level}}\left(\frac{cos\,(i\alpha_k)}{i}\right)} \tag{5}$$

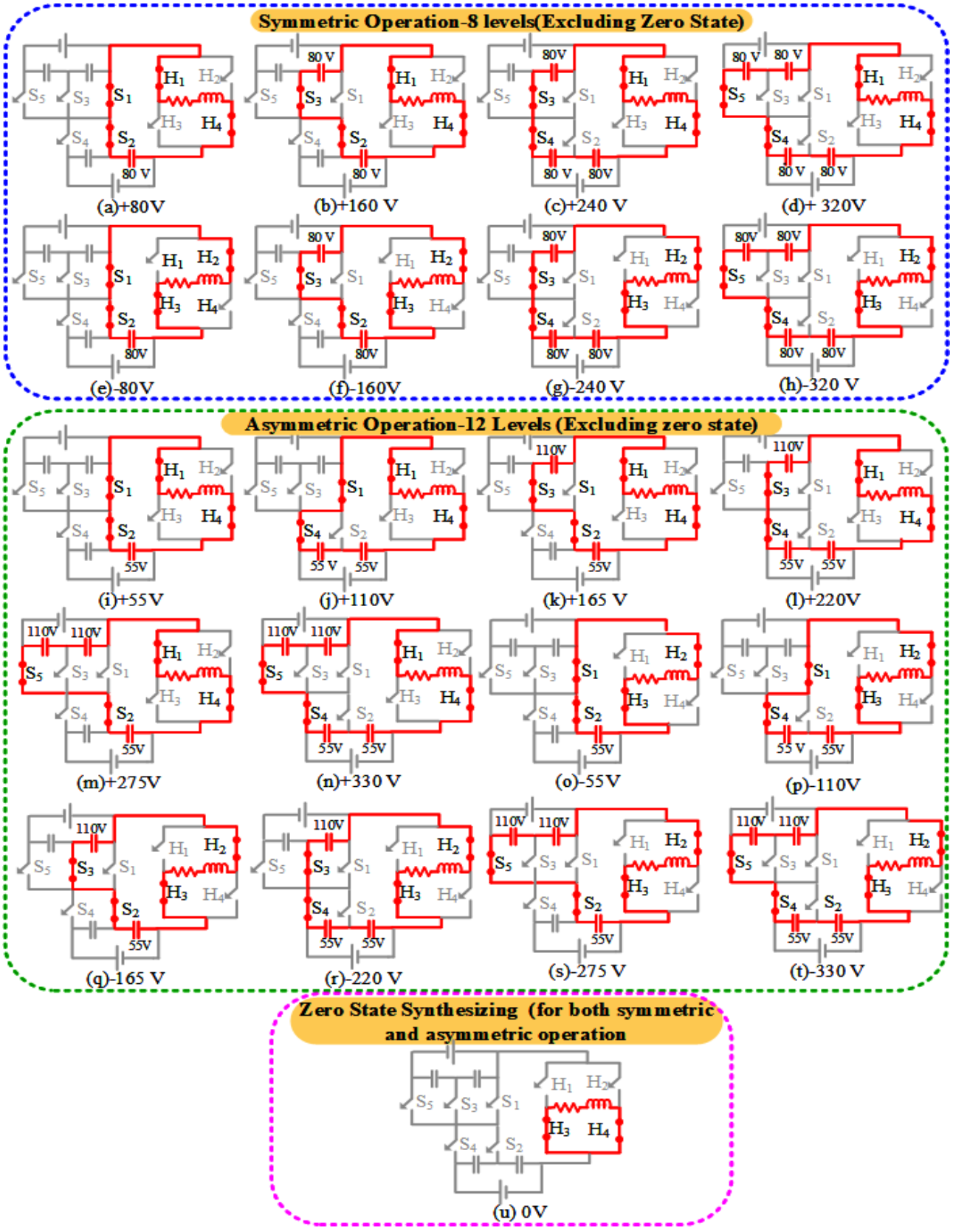

FIGURE 2. Equivalent circuit and conduction path to synthesize different voltage step.

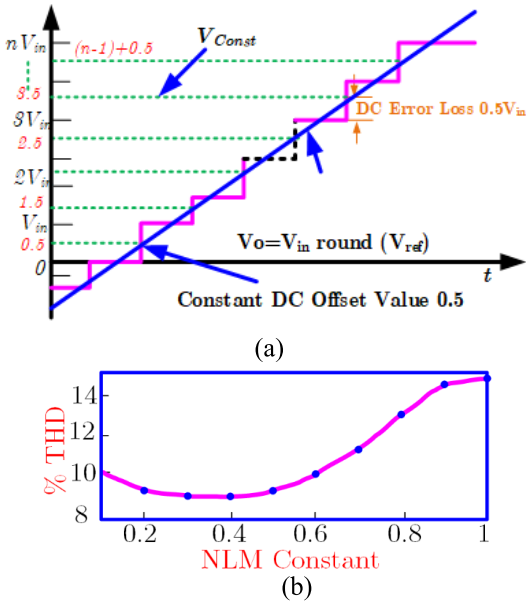

FIGURE 3. (a) NLM method (b) %THD Vs NLM constant.

We calculate the percentage THD of the voltage using (4) with the values V_{oi} and V_{of} which are the RMS value of harmonic and fundamental voltage component in the output voltage as given in [25].

The simulation results got for symmetric operation is shown in the Fig.4. Fig.4a depicts the nine-level terminal voltage with peak value 320 V with $N_{step} = 4$ and step size of 80 V. The load has a resistance of 200 ohms and inductance of 70 mH. Therefore, the peak value of the load current got is 1.6 Ampere as shown in the Fig.4b. We observe the Voltage THD as 9.09% in Fig.4c. The DS-MLI synthesizes 13 levels during asymmetric operation, as shown in the Fig.5a. From (4) and (5) we understand it that the number of levels in the terminal voltage waveform of an inverter is inversely proportional to its percentage THD. Thus, with the higher number of levels in the voltage waveform (330V), the percentage voltage THD of DS-MLI during asymmetric operation is only 6.25% as shown in Fig.5c. Therefore, for a load, the percentage THD is 30% less if the DS-MLI is operated in asymmetric mode.

A. VOLTAGE STRESS

At a maximum modulation index, a two-level inverter (VSI, CSI or ZSI) needs 600V in its DC link to deliver a 230V RMS at its terminals. This maximum voltage will appear in the switches and the load alternatively during inverter switching. Which is termed as dv/dt stress. The parameter dv/dt stress varies with voltage and rate of change of time (switching frequency). Higher the stress, higher will be the heat emitted from the switch, and hence it requires more massive heat sink and load insulation [26], [27]. The case becomes worse if we use a switching scheme with switching frequency between kHz. To minimize the dv/dt stress, either the voltage

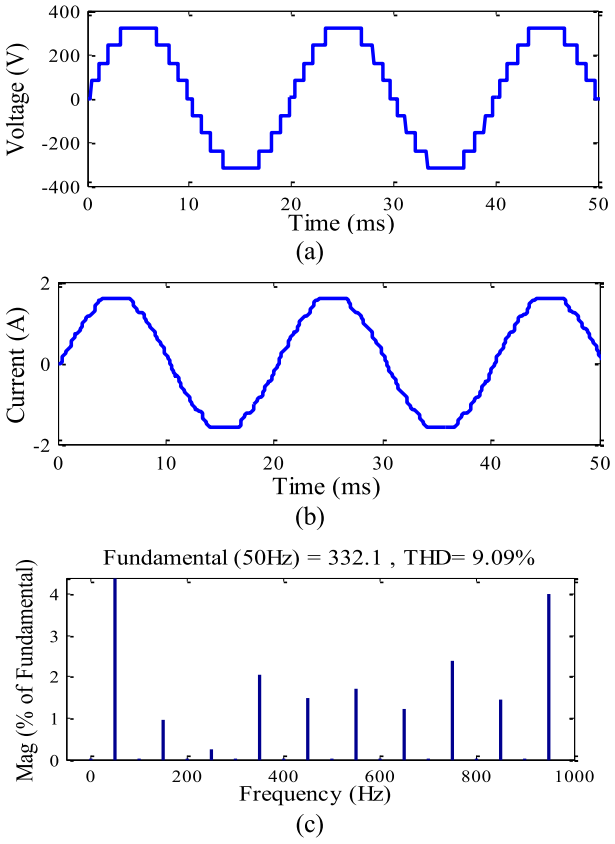

FIGURE 4. Simulation results of DS-MLI during symmetric operation. (a) 9-Level Voltage. (b) Load current. (c) Harmonic Spectrum of voltage THD.

can be reduced or we should increase the time between subsequent switching. In DS-MLI during symmetrical operation, the maximum voltage transition is restricted to 320 V/4, where 4 is the number of steps in a half cycle. In asymmetric operation, it is 55 V with 6 steps for a peak voltage of 330V. The exponential reduction in dv/dt stress with the increase in the number of capacitors during symmetric and asymmetric operation is depicted in Fig.6. From the figure, we infer it that for the same number of capacitors, the switching stress decreases drastically in asymmetric operation.

V. INTERFACING DS-MLI WITH SOLAR PV DESIGN OF VOLTAGE BALANCING CONTROLLER

The single-phase DS-MLI fed PV grid-connected system with LCL filter is shown in Fig.7. The Control loops of DSMLI is designed using a small-signal model; here state-space averaging technique is used to develop the small-signal model. To derive the state-space model of DSMLI, following assumptions are made 1. All the switches are lossless 2. DSMLI is operated in asymmetrical mode 3. Inverter side inductance current I_L, Grid side inductance I_{Lg} and Filter capacitor voltage (V_c) is state variables [28].

The equivalent circuit got after applying the assumptions to Fig.7 is shown in Fig.8, and we use it for deriving the state-space model.

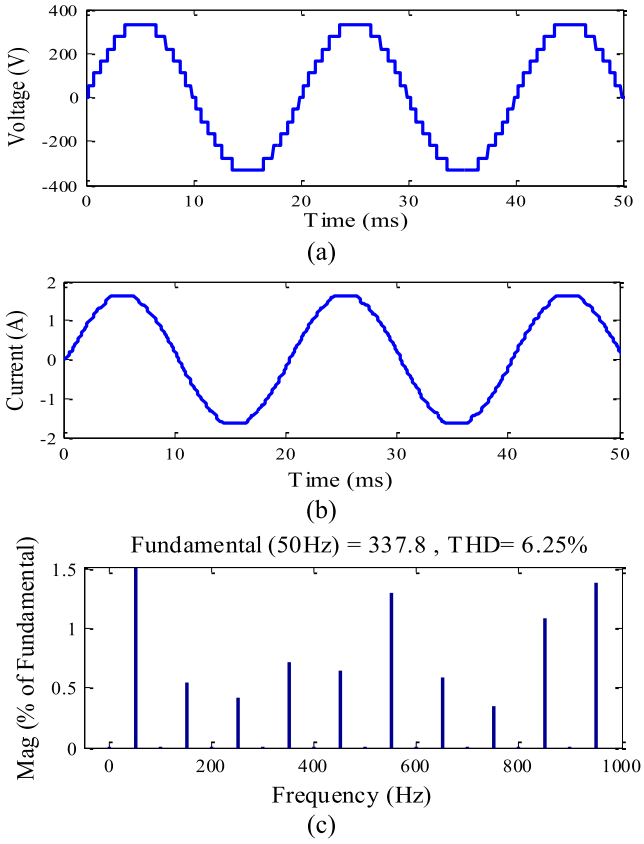

FIGURE 5. Simulation results of DS-MLI during asymmetric operation. (a) 13-Level Voltage. (b) Load current. (c) Harmonic Spectrum of voltage THD.

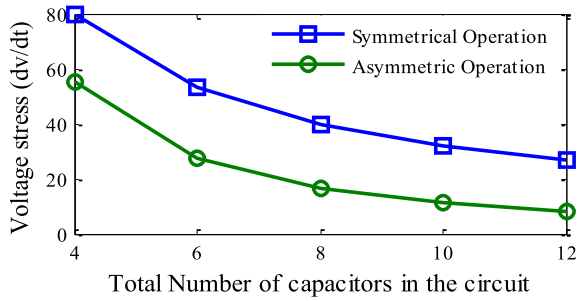

FIGURE 6. Voltage stress got for the number of capacitors.

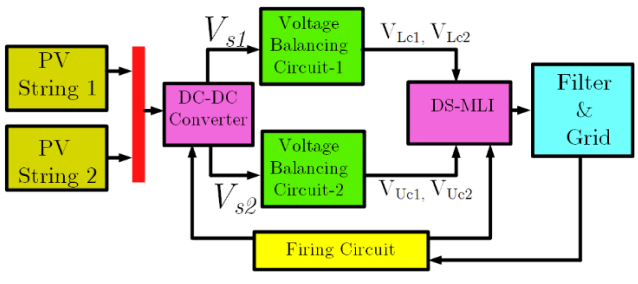

FIGURE 7. Schematic for interfacing solar PV strings to the grid through DS-MLI.

From Fig.8 by applying KVL and KCL, we can get the state-space model equation of the state variable inductor

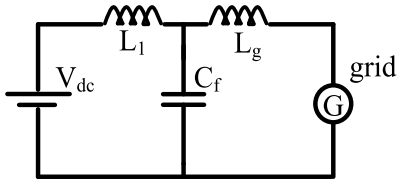

FIGURE 8. Equivalent circuit of the power conversion scheme.

current (I_L), Grid side inductance (I_{Lg}) and filter capacitor voltage (V_c):

$$V_{dc} - V_L - V_C = 0$$

$$L\frac{di_L}{dt} = V_{dc} - V_C = \frac{dI_c}{dt} = \frac{V_{dc}}{L} - \frac{V_c}{L} \tag{6}$$

$$L\frac{di_{Lg}}{dt} = -V_g - V_{Cf} = \frac{dI_{Lg}}{dt} = -\frac{V_g}{L_g} - \frac{V_c}{L_g} \tag{7}$$

$$I_L = I_c + I_{Lg}$$

$$C\frac{dV_c}{dt} = I_L - I_{Lg};\ \frac{dV_c}{dt} = -\frac{I_L}{C} - \frac{IL_g}{C} \tag{8}$$

From (6)- (8), the state-space model of the system is planned:

$$\frac{d}{dt}\begin{bmatrix} I_L \\ I_{Lg} \\ V_C \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_g} \\ \frac{1}{C} & \frac{-1}{C} & 0 \end{bmatrix}\begin{bmatrix} I_L \\ I_{Lg} \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{I_g} \\ P0 \end{bmatrix}\begin{bmatrix} V_{dc} & V_g & 0 \end{bmatrix}$$

By taking the Laplace transforms for the state variables shown in the above equation

$$SI_L(s) = -\frac{V_c(s)}{L} + \frac{V_{dc}(s)}{L} \tag{9}$$

$$I_L(s) = -\frac{V_c(s)}{LS} + \frac{V_{dc}(s)}{LS} \tag{10}$$

$$SI_g(s) = -\frac{V_c(s)}{L_g} + \frac{V_g(s)}{L_g} \tag{11}$$

$$I_g(s) = -\frac{V_c(s)}{SL_g} + \frac{V_g(s)}{SL_g} \tag{12}$$

By simplifying (9) (10), (11) & (12), the output capacitor voltage (Vc) to input DC-link voltage (V_{dc}) transfer function is got as follows

$$\left.\frac{V_c(s)}{V_{dc}(s)}\right|_{V_g(s)=0} = \frac{CL_g}{SC\left[S^2LL_g + 1\right] + 1}$$

Which implies

$$\left.\frac{V_c(s)}{V_{dc}(s)}\right|_{V_g(s)=0} = \frac{CL_g}{S^3CLL_g + SC + 1} \tag{13}$$

On substituting $V_c(s)$ in $I_L(s)$

$$I_L(s) = \frac{I_L(s)}{LCS^2} + \frac{I_g(s)}{LCS^2} + \frac{V_{dc}(s)}{LC}$$

Which implies

$$I_L(s)\left[\frac{LCS^2 - 1}{LCS^2}\right] = \frac{I_g(s)}{LCS^2} + \frac{V_{dc}(s)}{LC} \tag{14}$$

By simplifying (10) to (14), the output current (I_L) to input DC-link voltage (V_{dc}) transfer function is deduced as

$$\left.\frac{I_L(s)}{V_{dc}(s)}\right|_{I_g(s)=0} = \frac{CS}{LCS^2-1} \tag{15}$$

With the DC-link voltage balancing and current control transfer function got from the state-space model, the stability of the system is analysed by using a Bode plot with the parameters specified in Table 4.

TABLE 4. The parameters for the proposed system.

Parameter	Symbol	Value
AC-source voltage (Grid voltage)	Vg	230V, 50 Hz
Inverter filter inductance	L	0.27 mH
Input filter capacitance	C	300 µF
DC link capacitance	C_{Link}	C= 0.042F
DC bus voltage	V_{dc}	660 V
Grid filter inductance	Lg	0.27mH

A. ANALYSIS OF INDUCTANCE AND CAPACITANCE VARIATION AND ITS EFFECTS ON SYSTEM PERFORMANCE

In this section, the impact of inductance and capacitance on the dynamic characteristic of the DS-MLI is analysed. By using the system's transfer function, the practical value of inductor and capacitor is determined through frequency response bode plot analysis to improve the stability of the system.

1) EFFECT OF INDUCTANCE VARIATION

The bode plot of the system's transfer function for the variation of inductance is shown in Fig. 9.

It shows the gain margin and phase margin at different inductance values in Table 5. From Table 5; it is found that for the inductance of 0.3 mH the gain and phase margins are 29.9dB and 13.4° respectively. When the inductance value is increased beyond 1mH, it produces more oscillations, resulting in a lower phase margin, thus inducing harmonics and making the system unstable.

2) EFFECT OF CAPACITANCE VARIATION

The dynamic performance of the system is investigated by varying the capacitance value, and corresponding results are shown in Fig. 10 and Table 6 and is found that 300 microfarad gives 49.2dB gain margin and 75.8° of phase margin respectively and hence the system is stable.

At other capacitance values, the gain margin and phase margin are low, resulting in more ripples and thus pushing the system into an unstable state.

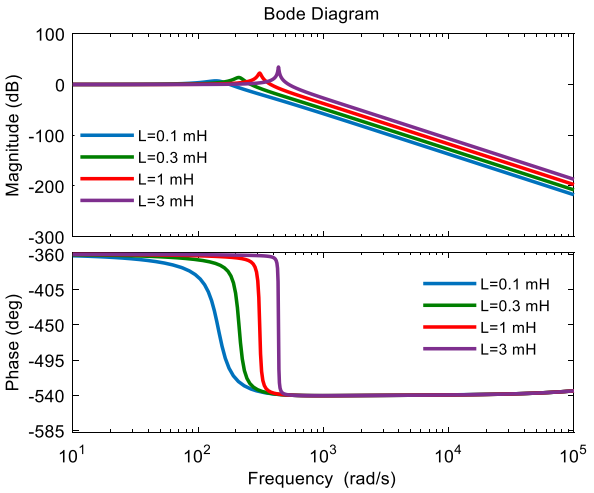

FIGURE 9. Bode plot of inductance variation.

TABLE 5. Effect of inductance variation.

Inductance value (mH)	Gain Margin (dB)	Phase Margin (deg)
0.1	39.6	32.6
0.3	29.9	13.4
1	18.8	4.15
3.33	5.68	0.563

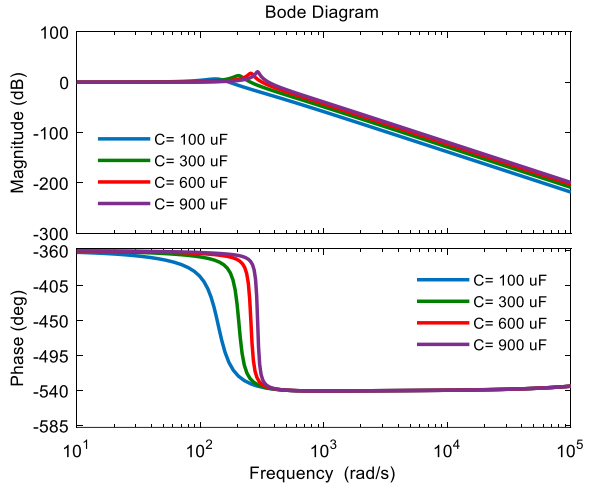

FIGURE 10. Bode plot of Capacitance variation.

TABLE 6. Effect of capacitance variation.

Capacitance value (µF)	Gain Margin (dB)	Phase Margin (deg)
100	54.4	134
300	49.2	75.8
600	24.6	7.87
900	20.8	5.24

From the above analysis, the optimum value of inductance and capacitance are found using the DC-link voltage

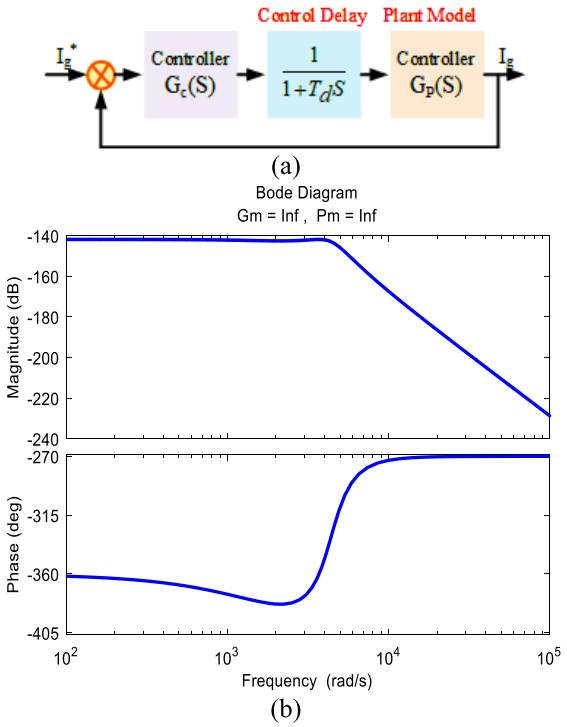

FIGURE 11. (a) Voltage balancing control scheme (b) Open loop voltage control.

balancing and current control transfer function equations as 0.3mH and 300μF, respectively. The stability of the system is analyzed by using frequency response Bode plot with the parameters specified in Table 4.

B. DESIGN OF VOLTAGE BALANCING CONTROLLER (VBC LOOP)

The Fig.11a shows the DC-link voltage balancing control scheme of DS-MLI. The plant transfer function G_p (s) is controller using a PI controller with appropriate K_i and K_p values tuned. The voltage regulation loop includes the average voltage controller (AVC), which regulates the total active power balance between the DSMLI and the grid.

The Fig.11b shows the open-loop bode plot of the AVC with $K_p = 0.6$, $K_i = 2$ wherein the gain margin (GM) and Phase Margin (PM) are infinity and hence the AVC loop is unstable. Fig.12 shows the closed-loop bode plot of the AVC, where the proportional-integral parameters are designed as k_p, $= 1.2$, k_i, $= 0.002$ for which a gain margin (GM) of 49.2 dB and a phase margin (PM) of 75.8° is attained, thus the stability of the VBC loop is improved. The DSMLI draws maximum active power from the DC link source to uphold the DC link voltage at the preferred level. This is achieved by a dual loop control method, which regulates the DC link capacitor voltage, the grid voltage and the inverter current. In the inner current control loop, the grid current's quadrature axis component will zero in the controller to generate maximum active power at unity power factor.

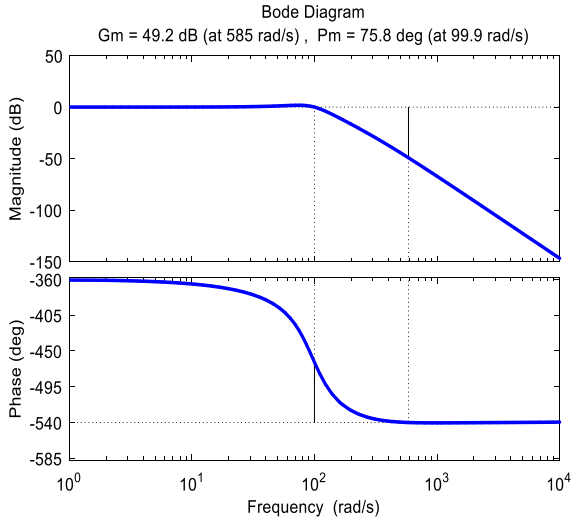

FIGURE 12. Closed-loop voltage control.

C. CURRENT-LOOP CONTROL SCHEME

The current control scheme of DS-MLI is shown in Fig.13. The output current to we represent the input transfer function as a plant, and the Proportional-Integral (PI) controller controls it. Figure. 14 shows the bode diagram of an open-loop current control transfer function. From the figure, we can observe it that the crossover frequency is high, which results in more oscillation making the system unstable. For stabilizing the system, a compensator PI controller with reference tracking is introduced in the closed-loop system. The transfer function Bode plot of the compensated closed-loop system is shown in Fig.15. In Fig.15, we observe it that the

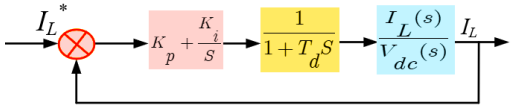

FIGURE 13. The current Control scheme of DS-MLI.

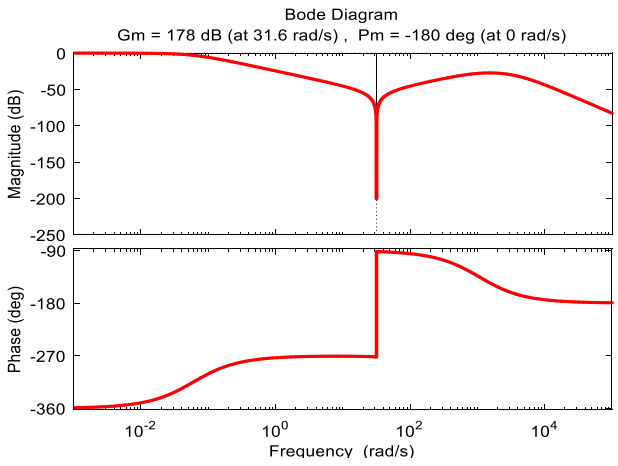

FIGURE 14. Bode plot of open loop current control.

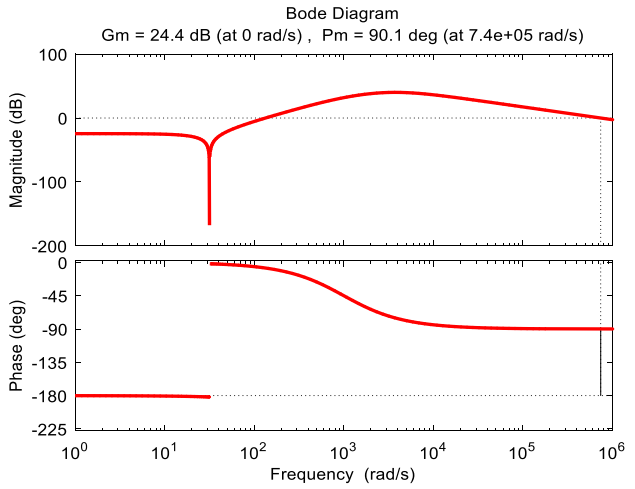

FIGURE 15. Bode plot of closed-loop current control.

gain margin is 24.4 dB and the phase margin is 90° which improves the stability of the system. The open-loop and the closed-loop response of DSMLI are depicted in Fig.16a. We observe it that closed-loop has less steady-state error and peak overshoot when compared to open-loop system. Thus the closed-loop system produces fewer ripples and harmonics. Further, the dynamic response of the closed-loop DSMLI is investigated by applying a step-change in irradiance from 800 W/m^2 to 1000 W/m^2 at 4.5 ms, as shown in Fig.16b. From Fig.16b, we can infer it that the system reaches a steady-state within 2.5 ms after the change in irradiance, and this ensures that the system has a fast dynamic response.

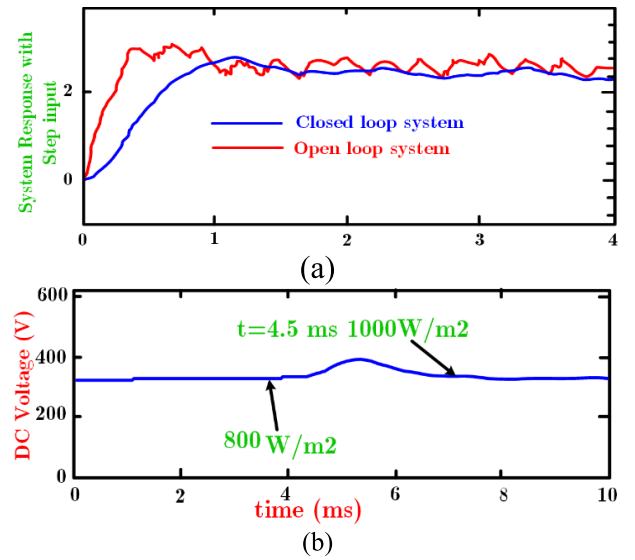

FIGURE 16. (a) System's response for step input (b) Dynamic response of the system with controller.

VI. EXPERIMENTAL RESULTS

To validating the theoretical and simulation results, experiments are carried out with an isolated solar PV unit feeding a load through DS-MLI and with a closed-loop power conversion scheme and the results are presented in the following sections.

A. ISOLATED OPERATION OF DS-MLI

An experimental prototype of DS-MLI rated 1kW is constructed to validate the simulation results. The components used for construction and we give their rating below in Table 7. It makes the experimental setup to feed a load with 200Ω resistance and 70mH inductance. The load voltage, load current and THD got in symmetric operation are shown in Fig 17a, 17c and 17e, respectively. From these figures, we can observe it that under the constant input voltage from the solar PV emulator, the DSMLI delivers a 9-level output voltage waveform with a THD of 9.7%. The experimental THD is slightly higher than the simulated values as the FGA25N120-ANTD switches have a finite turn ON and Turn off time unlike its simulated counterpart wherein the switches turn ON and OFF instantaneously. The Fig. 17b, 17d and 17f portrays the experimental voltage, current, and THD of asymmetric operation, respectively. Here, with an increase in steps, the THD has come down to 7.1%. We can also observe it that during the asymmetric operation, the current waveform is smoother because of the above reason. The blocking voltage across the H-Bridge switch H_1 is measured during symmetric and operations and presented in Fig.17. g and 17.h, from which it can be observed that the dv/dt stress is comprehensively low when compared to 230 V in the two-level inverter.

TABLE 7. Components used in the isolated operation set up.

S.No	Component	Rating	Quantity
1	Capacitor	80V,1000μF	6
2	Capacitor	200V,470 μF	2
3	Inductor	70mH	1
4	IGBT	FGA25N120-ANTD	9
5	Ecosense made solar PV emulator	1 kW	1
6	Load resistance	200Ω	1
7	FPGA Spartan 6 processor	-	1

B. COMPARISON OF DS-MLI WITH OTHER TOPOLOGIES

The components required for obtaining nine levels in the output voltage for different multilevel inverter topologies presented in the literature are compared with the DS-MLI, and we present the results in Table 8.

From Table 8, we can observe it that the number of components required for DS-MLI is relatively less when compared to the other topologies. The higher number of capacitors used in the topology facilitates its asymmetrical operation without cascading. Also, it provides a tactical advantage in single point voltage regulation during grid interfacing.

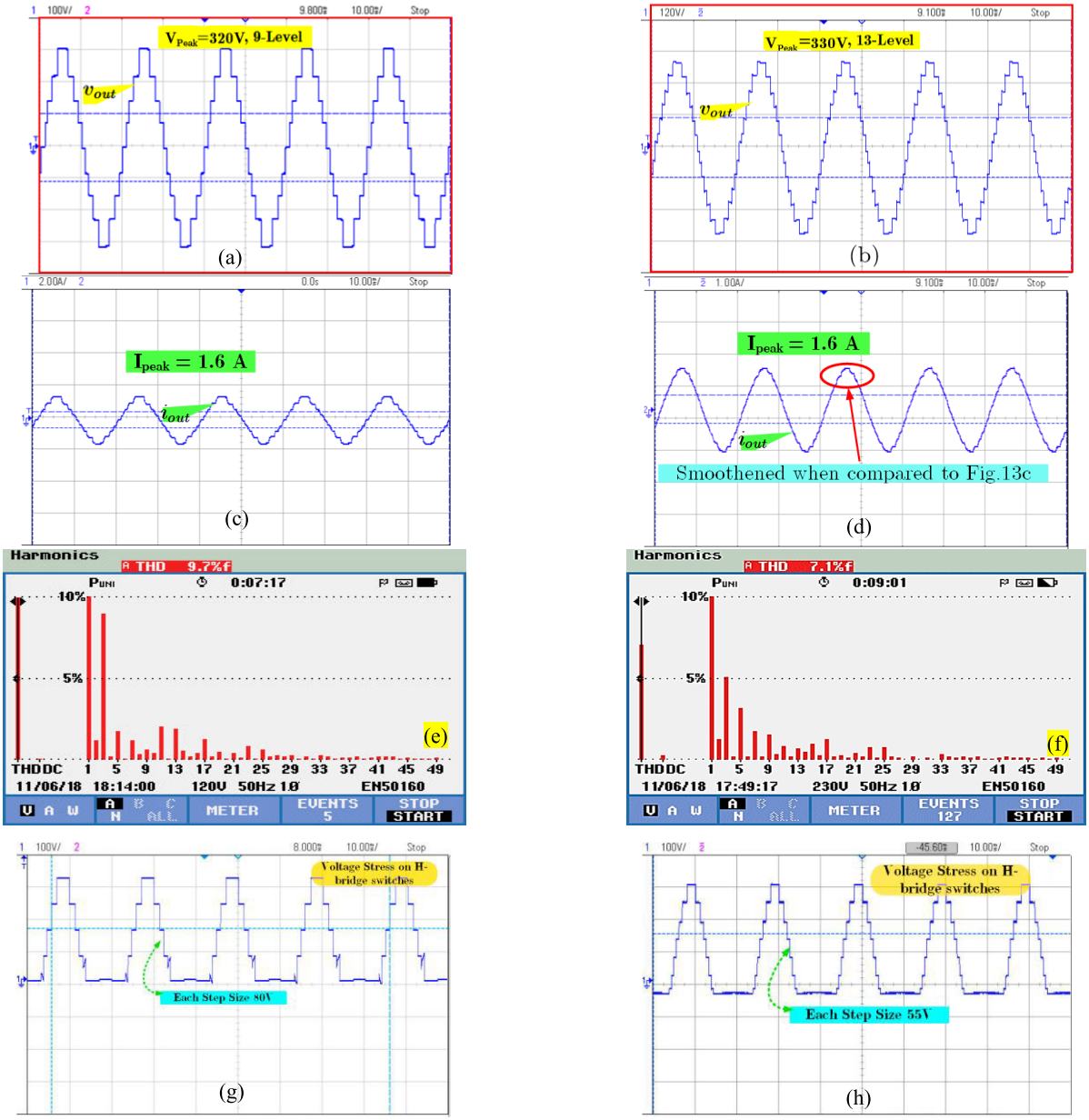

FIGURE 17. Experimental results (a) (c), (e) 9-level voltage, current, THD got during symmetric operation, (b), (d), (f) 13-level voltage, current, THD got during asymmetric operation, (g) Voltage stress across H_1 during symmetric operation, (h) Voltage stress across H_1 during asymmetric operation.

TABLE 8. Comparison of components required.

Number of Components	[12]	[29]	[14]	[15]	CHB	DSMLI
IGBTs	10	10	12	10	36	9
Drivers	8	10	12	10	36	9
Sources	4	4	4	4	4	2
Capacitors	-	-	-	-	-	4

C. EFFICIENCY COMPUTATION

An inverter will experience losses because of the turn-on and turn off time of the switches and internal switch resistance called switching and conduction losses, respectively. By using the linearized switching approximation characteristics [7], the switching and conduction losses can be calculated as follows.

1) SWITCHING LOSS

The switching loss is the sum of power lost during turn-on and turn-off period of the switches. For a practical switch, we can estimate the power lost while we turn it ON as given in (16)

$$P_{sw-n} = \frac{1}{6}\left(f_s \times V_{swb} \times I_{swc} \times t_{on}\right) \tag{16}$$

Similarly, the power loss while the switch is turning off can be determined using (17)

$$P_{sw-f} = \frac{1}{6} f_s V_{swb} I_{swc} t_{off} \tag{17}$$

The total loss per switching state will be the sum of (16) and (17). Here f_s is the switching frequency of the switch, V_{swb} is the blocking voltage across the switch, I_{swc} is the conduction current through the switch, t_{on} and t_{off} are the time required for the switch to turn ON and turn off, respectively.

2) CONDUCTION LOSS

The conduction loss is the power dissipated in a switch when it is in ON-state, and it can be computed by using (18)

$$P_{conduction} = \frac{V_{swc} I_{swc}}{t_{total}} (t_{total} - t_{off} - t_{on}) \tag{18}$$

The total loss per switch (P_{LS}) per switching state is the sum of equations (16) to (18). So, the total power loss across the inverter is

$$P_{Loss} = \sum_{s=1}^{9} P_{LS} \tag{19}$$

The efficiency of the inverter can be determined using the equation (20)

$$\eta = \frac{P_{load}}{P_{in} + P_{loss}} \tag{20}$$

In switch S_1, for a load of 0.26 kW (rms), the blocking voltage is 160 V (peak) in a symmetric mode, and the conduction current is 1.2A. From the datasheet of FGA25N120-ANTD, the turn on and turn-off times are taken as 10 nanoseconds and 190 nanoseconds, respectively. The switching loss per switching instant is 0.00576W. The switch conducts during two switching states and thus has four switching instants and the switching loss incurred in switch S_1 is 0.02304W. Similarly, the conduction loss at switch S_1 is 0.50415W. The total switching loss is the continuous sum of switching loss across all the switches, and it is 0.12 W; similarly, the total conduction loss is 7.04 W. Therefore, the total loss is 7.2 W, and the efficiency estimated using (20) is nearly 97%. Similarly, the efficiency at loads 0.5kW, 0.75 kW and 1 kW are computed for DS-MLI and portrayed in Fig.18. From the Fig.18, we can find it that the efficiency of DS-MLI is higher than the CHB-MLI topology.

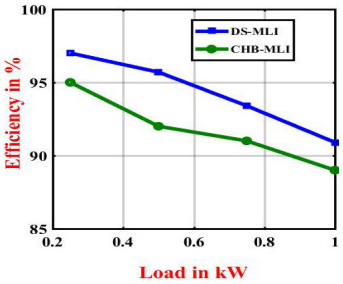

FIGURE 18. Efficiency curve.

D. ISOLATED OPERATION UNDER DISTURBANCE

The eco sense made solar PV emulator has four output channels. It connects the solar PV emulator to DS-MLI such that the outputs from two of the four channels are considered as V_{s1} and V_{s2} delivering equal voltages. Both the channels are clamped to two capacitors and used for the upper and lower arm of the DS-MLI. We subject the input irradiance of the channel connected to the upper arm of the DSMLI to a step-change in irradiance, and it shows the observation in the Fig.19.

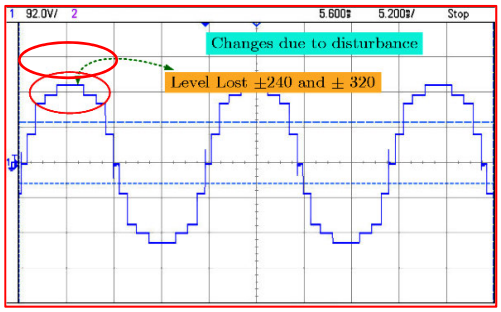

FIGURE 19. Symmetrical operation of DS-MLI when V_{s1} is subjected to a disturbance.

Similarly, when the step-change in irradiance applies to one of the two channels during asymmetric operations, the number of levels lost is higher when compared to symmetric operation as shown in the Fig.20.

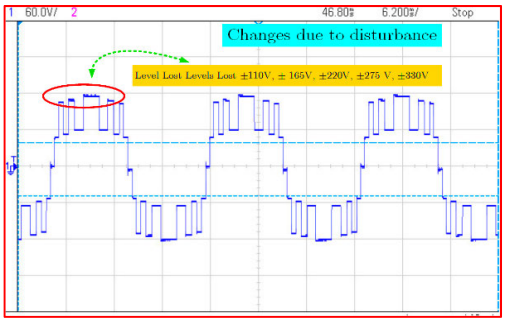

FIGURE 20. Asymmetrical operation of DS-MLI when V_{s1} is subjected to a disturbance.

To maintain the DC-link voltage and grid current quality while interfacing the solar PV unit to the grid through DS-MLI, a modified single DC bus bar collector scheme is suggested and we present the experimental results in the following section.

VII. INTERFACING OF SOLAR PV UNIT TO GRID THROUGH DS-MLI

A single DC bus bar collector-based control scheme is proposed in [30]. In this scheme, it connects the multiple solar PV strings to a common DC bus bar, with a DC-DC converter

TABLE 9. Comparison of components required for closed-loop system.

S.No	Components required	Specification	Unit Cost in USD	Control Scheme proposed in [30]				Dual Source Multilevel Inverter			
				For 9-levels	Cost in USD	For 13 levels	Cost in USD	Symmetric Mode	Cost in USD	Asymmetric Mode	Cost in USD
1	Capacitor	450 V,1500 µF	41.51					1	41.51	1	41.51
2	Capacitor	300 V, 1500 µF	24.13							1	24.13
3	Capacitor	200 V, 470 µF	1.6					2	48.44	3	72.66
4	Capacitor	80 V, 1000 µF	1.82					4	46.24	2	23.12
5	Capacitor	44 V, 1500 µF	3.05	4	12.2	6	18.3				
6	Inductor	700 µH	1.96	4	7.84	6	11.76	1	1.96	1	1.96
7	Inductor	1.6 mH	1.56					1	1.56	1	1.56
8	Inductor	1.2 mH	1.02					1	1.02	1	1.02
9	Diode	1N3208	3.63	4	14.5	6	21.78	9	32.67	9	32.67
10	MOSFET	IRL530PBF	0.62	4	2.48	6	3.72	1	0.62	1	0.62
11	MOSFET	IRF1644GPBF	2.48					2	4.96	2	4.96
12	IGBT	FGA5N120-AD	1	12	12	24	24	9	9	9	9
13	Flyback Transformer	-	15	4	60	6	90				
14	Efficiency at 1 kW	-	-	89%				91%			
15	Approximated total Cost in USD	-	-	109.04		169.56		103.78		-	125.87

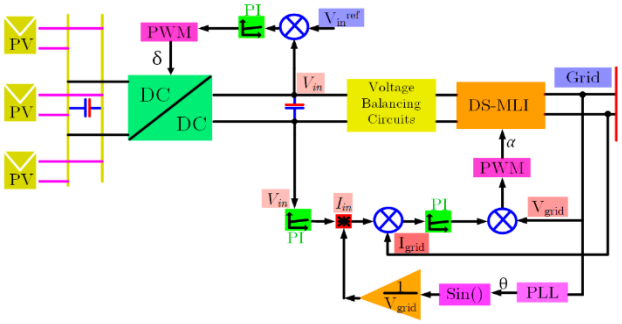

FIGURE 21. Modified Single DC-Bus bar collector scheme.

connected to each string. It connects this DC bus bar to the grid through a grid-tied conventional Cascaded H-Bridge Multilevel Inverter. The DC links tapped from the common DC bus bar through a fly-back converter acts as the independent source for each H-Bridge unit. Even though the energy yield and operation range are higher in the said scheme, the efficiency is less because of multiple conversion stages involved.

A modified single DC bus bar-based control scheme with DS-MLI is used in this article, as shown in the Fig.21. In the suggested scheme, the converters connected to each string are eliminated, and the multiple fly-back converters are replaced with a single buck-boost converter and a voltage balancing circuit. Therefore, the efficiency of the system will be higher for the reduction in the number of components. Since the voltage level involved in domestic applications is between 230 V. The voltage stress across the converter is bearable.

A 1kW solar PV unit is realized with an eco-sense made solar PV emulator and connected to the grid using the proposed scheme. The voltage, real power, reactive power, current and power factor observed in the grid-tied DS-MLI is shown in Fig. 22a and Fig.22b. For an RMS voltage of 230 V, the solar PV unit delivers a current of 4.3 amperes. The LC filter used in the grid side aided in eliminating the lower order harmonics and thus reducing the voltage THD to 2.6% as shown in Fig.22c. We observe the current THD as 2.9%, as shown in Fig.22d. The minimum lower order harmonic content observed in Figure 22c originates from the ripples from the DC link, which is less influential in the circuit performance. The modified single DC bus bar collector scheme with DS-MLI is compared with the single DC bus bar collector scheme with CHB-MLI in the aspects of the number of components required. We present cost and efficiency and the observations in Table 9. From Table 9, we can find it that the proposed conversion scheme requires less number of components. In particular, the multiple fly-back transformers used in the conventional conversion scheme are eliminated, which brought down the cost of the proposed conversion scheme to 125 USD, which is 30% less when compared to to conventional counterpart. The cost of the components of the proposed topology differs from the cost of the components used in [30]. Because of the specification, the components used in the two topologies differs from each other. The usage of fly-back transformers in [30] increases its cost drastically, as observed in Table 9.

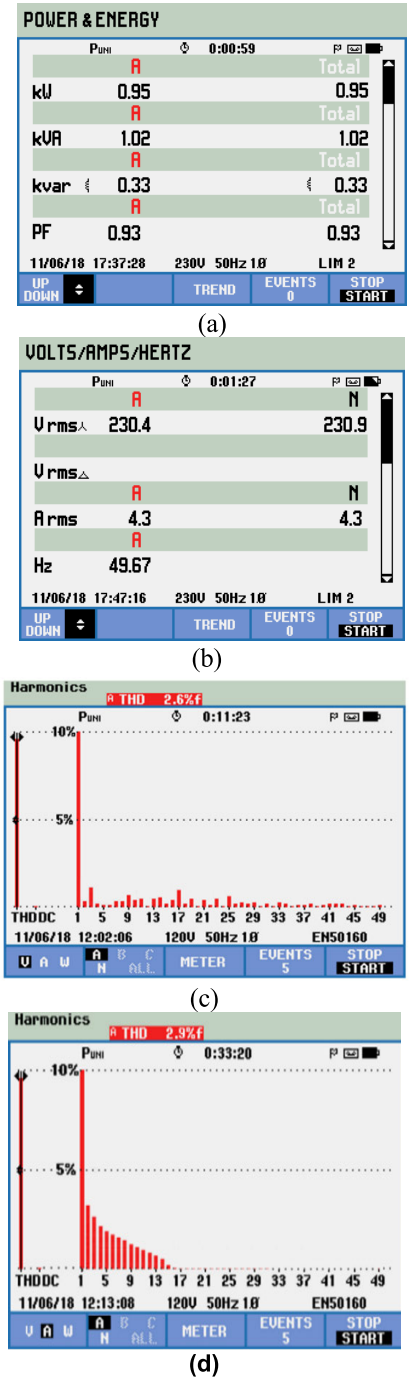

FIGURE 22. (a) Voltage and Current, (b) Power and Power factor, (c) Voltage THD (d) Current THD.

VIII. CONCLUSION

A multilevel inverter topology called Dual-source multilevel inverter is suggested for domestic rooftop solar PV units. The inverter topology can synthesize nine-levels and thirteen levels using nine switches during symmetric and asymmetric operation, respectively. Further, a modified single DC bus bar-based control scheme with reduced power components is suggested to interface solar PV unit to grid through DS-MLI. The transfer function of the control scheme is derived, and its stability is assessed and proved satisfactory. The efficiency of the DSMLI based grid-connected solar PV is 92% at 1kW, which is 3% high when compared to the scheme found in recent literature. Further, the lesser number of components utilised in the scheme will bring down the cost to $125, which is considerably lower than the $170 incurred in the existing system.

NOMENCLATURE

C_f	-	Filter capacitance
DS-MLI	-	Dual Source Multilevel Inverter
F_s	-	Switching frequency
$G_c(s)$	-	Controller transfer function
$G_p(s)$	-	Plant transfer function
I_l	-	Current through inverter side inductance
I_{Lg}	-	Current through grid side inductance
I_{swc}	-	Current through the switch
I_{swc}	-	Conduction current through the switch
K_i	-	Integral gain
K_p	-	Proportional gain
Nc	-	Number of capacitors clamped in lower/upper arm of DS-MLI
N_{Level}	-	Number of levels
N_{step}	-	Number of steps in the positive/Negative half cycle of the terminal voltage
N_{switch}	-	Number of switches
$P_{conduction}$	-	Conduction loss
PLL	-	Phase-Locked Loop
P_{loss}	-	The power loss of the inverter
P_{LS}	-	Power lost in each switch
P_{sw-f}	-	Power lost during turn off
P_{sw-n}	-	Power lost during turn on
PV	-	Photovoltaic
PWM	-	Pulse Width Modulation
THD	-	Total Harmonic Distortion
t_{off}	-	The time required for the IGBT to turn off
t_{on}	-	The time required for the IGBT to turn ON
V_{0f}	-	The magnitude of the fundamental voltage component
V_c	-	Filter capacitor voltage
V_{dc}	-	The voltage at the input dc-link
V_L	-	The voltage across the inductor
V_{oi}	-	The magnitude of harmonic voltage components
V_{s1}	-	The magnitude of voltage delivered by the DC voltage source connected in the lower arm
V_{s2}	-	The magnitude of voltage delivered by the DC voltage source connected to the upper arm
V_{swb}	-	Blocking voltage across the switch
V_{swc}	-	The voltage drop across the switch during conduction
α_k	-	Switching angle

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