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Analysis and Investigation of Hybrid DC–DC Non-Isolated and Non-Inverting Nx Interleaved Multilevel Boost Converter (Nx-IMBC) for High Voltage Step-Up Applications: Hardware Implementation

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ABSTRACT In significant cases, the generated voltage needs to be step-up with high conversion ratio by using the DC-DC converter as per the requirement of the load. The drawbacks of traditional boost converter are it required high rating semiconductor devices and have high input current ripple, low efficiency, and reverse recovery voltage of the diodes. Recently, the family of Multilevel Boost Converter suggested and suitable configuration to overcome the above drawbacks. In this article, hybrid DC-DC non-isolated and non-inverting Nx Interleaved Multilevel Boost Converter (Nx-IMBC) is analyzed in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) with boundary condition and investigated in detail. The Nx-IMBC circuit combined the features of traditional Interleaved Boost Converter (IBC) and Nx Multilevel Boost Converter (Nx-MBC). The modes of operation, design of Nx-IMBC and the effect of the internal resistance of components are presented. The comparison study with various recent DC-DC converters is presented. The experimental and simulation results are presented with or without perturbation in input voltage, output power and output reference voltage which validates the design, feasibility, and working of the converter.

INDEX TERMS DC-DC, high step-up, hybrid converter, interleaved, low voltage stress, low current ripples, multilevel, non-isolated, non-inverting, voltage multiplier.

I. INTRODUCTION

When the current world energy scenario is analyzed, all the nations of the world is riveted towards ingestion of exhaustible sources to beget the energy and to feed the energy requisites. The idea of energy generation is entirely unaffordable, which would eventually create paucity of fossil fuels soon. As a result, the entire focus has increasingly shifted towards inexhaustible energy sources [1]–[5]. There are so many ways to generate power using these sources like solar, wind, fuel-cell, tidal etc. Among these sources, solar energy is one of the conventional renewable sources due to abundance,

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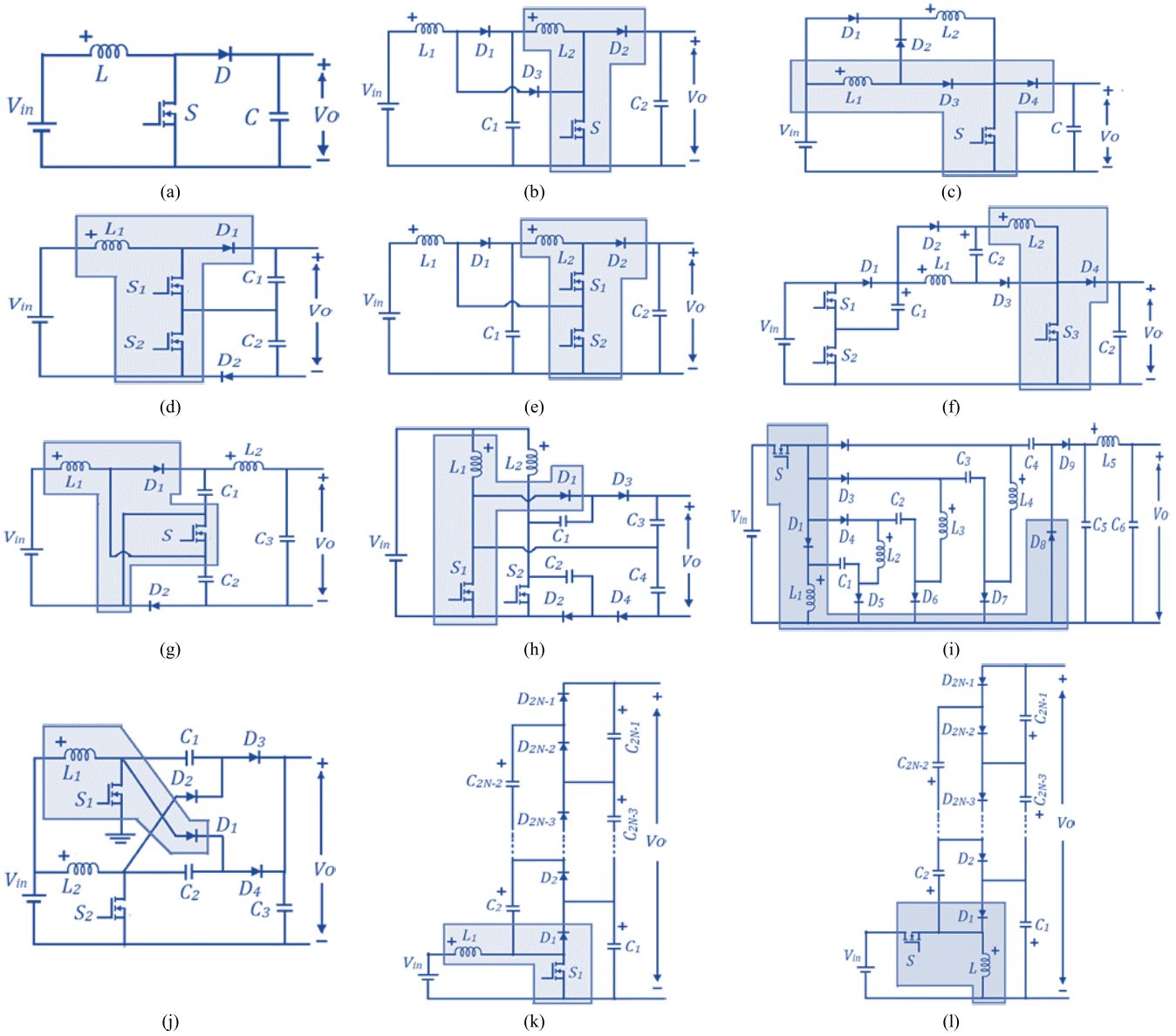

FIGURE 1. Power circuit of recently addressed converter (a) Conventional Boost Converter, (b) Single switch Quadratic Boost Converter (QBC), (c) Switched Inductor (SI) Boost Converter, (d) Conventional Three-Level Boost Converter, (e) Quadratic Three-Level Boost Converter, (f) Converters using bootstrap capacitors and boost inductors, (g) Switched-Capacitor Based Boost Converter, (h) Two-phase quadrupled interleaved boost converter, (i) Extra high voltage (HV) dc-dc converter, (j) High-voltage gain two-phase interleaved boost converter using one VMC, (k) Nx Multilevel Boost Converter (MBC), (l) inverting Multilevel Buck-Boost Converter (MBBC). Note: Shaded area denotes the structure of the Boost converter.

eco-friendly, free of cost and continuously developing with the advancement in photovoltaic cells which is leading to the high efficiency of the solar system. Photovoltaic technology is tenaciously growing with betterment in photovoltaic cells which ultimately leads to the priceless powered nation and the world too [6]. More and more renewable energy sources such as solar arrays, wind turbines, and fuel cell stacks are widely employed for front-end DC/DC applications [7], [8]. These inexhaustible energy sources need a DC-DC converter with a high conversion ratio to augment the voltage magnitude to feed the power grid or power DC-AC converter (Inverter) [9], [10]. The solar arrays give out low output voltage which certainly cannot suffice the voltage requisite. Therefore, the low voltage fed to boost converter to inflate the voltage level to suffice the application requirements [11]–[13]. A traditional Boost converter (Fig. 1(a)) is not preferred practically to fulfil the high voltage demand due to its design constraints, low efficiency and diode reverse recovery problem etc. [14], [15].

For attain a high voltage conversion ratio, many DC-DC converters with the different boosting technique are reviewed in [16]. Isolated topologies introduce transformer, results in bulky and costly circuitry [17], [18]. Unfortunately, a significant voltage spike across the switch observed due to leakage

TABLE 1. Conversion ratio Of recent DC-DC converter.

Converter Topology	Voltage Conversion Ratio, D= Duty Cycle
Traditional DC-DC Boost Converter	1/(1-D)
Switched Inductor (SI) DC-DC Boost Converter	(1+D)/(1-D)
Single switch DC-DC Quadratic Boost Converter (QBC)	$1/(1-D)^2$
Traditional Three-Level DC-DC Boost Converter	2/(1-D)
Quadratic Three-Level DC-DC Boost Converter	$1/(1-D)^2$
Converter using bootstrap capacitors and boost Inductors	3+D/1-D
Switched Capacitor Based DC-DC Boost Converter	(1+D)/(1-D)
2-phase quadrupled Interleaved Boost Converter (IBC)	4/(1 − D)
High-voltage gain 2-phase Interleaved Boost Converter (IBC) using one VMC (Voltage Multiplier Cell)	(VMC + 1)/(1 − D)
Extra-High Voltage (HV) DC-DC Converter	4/(1-D)
Nx Multilevel Boost Converter (Nx MBC)	N/(1-D)
N-level Multilevel Buck Boost Converter (MBBC)	-(D+(N-1)/(1-D))

inductance of the transformer. Thus, energy regeneration and clamping techniques are employed to recycle the energy and to limit the voltage stress [19], [20]. However, these techniques make the circuit complex and increase the cost of the converter. Coupled Inductor employed in the converter, e.g., coupled inductor-based boost converter [21], three winding coupled inductor [22], [23] to attain high voltage conversion ratio. However, additional input filter and active clamped techniques are required to minimize the input current ripple when turns ratio increased to meet desired voltage level, and complex structure is the main drawbacks of these converters [24], [25]. Interleaved converters based on coupled inductor are proposed to attain higher voltage conversion ratio with minimum input current ripple and higher efficiency [26], [27]. Nevertheless, complicated design, control, winding arrangement, and high frequency coupled inductor are the main challenges for these converters.

Numerous non-isolated converters are proposed to achieve high voltage conversion ratio without using a transformer and coupled inductor [28], [29]. Several existing DC-DC converter topologies are analyzed, and the power circuits of DC-DC converter topologies are depicted in Fig. 1 and their voltage conversion ratio is given in the Table-1. Cascaded Boost Converter (CBC) and Quadratic Boost Converter (QBC) are employed in [29], [30], whereas the method of cascading the necessary converters causes very high voltage stresses across the switches. Moreover, the efficiency is likely to get lessened with rising stages because of the several synchronous control switches and semiconductor device losses. In QBC (Fig. 1(b)), when the control switch turned OFF, the voltage across control switch is equal to the output voltage. Thus, high voltage rating control switch is required to design QBC, which increases the cost and decreases the efficiency of the converter due to higher conduction and switching losses [31]–[33].

Switched Capacitor (SC) and Switched Inductor (SI) are other possible solutions to increase the voltage conversion ratio of the converter. In [34], SI is employed in boost converter to step up the voltage. However, the voltage conversion ratio is not improved by several times and the voltage stress across the switch is equal to the output voltage. To overcome this drawback, several DC-DC converters, e.g. Three-level boost converter, Quadratic Three-level converter, converter using a bootstrap capacitor and inductor, switched capacitor boost converter are proposed [28], [35], [36]. However, the converter voltage conversion ratio is not enhanced by a higher factor even though multiple switches and boosting stages are employed. A high voltage converter is proposed in [37] using several reactive stages. However, it required a large number of inductors, capacitor and diodes.

For overcome the abovementioned drawback, the groundbreaking solution is voltage multipliers to raise the output voltage, which is the most affordable and frugal way to increase the gain of the converter [38]. Non-inverting, as well as inverting boost converter topologies with a combination of the traditional converter with voltage multiplier, are discussed [39]. Later, in [40] Nx inverting configuration of the boost converter is also recommended for photovoltaic DC Link applications. These multiplier boost converter topologies provide a practical solution to intensify the voltage conversion ratio. The multilevel DC-DC converters circuit avail Cockcroft Walton (CW) voltage multiplier which can be a crucial solution for the voltage conversion ratio intensification. Fig. 1(k) and 1(l) show the power circuit of Nx Multilevel Boost Converter (Nx MBC) and Nx Multilevel Buck-Boost Converter (Nx MBBC), respectively [38]–[40]. Reactive elements incorporated in the power converter topology, and operating frequency holds a pivotal role in the designing of the reactive element. Lower magnitudes of reactive components along with high switching frequency serves an acceptable magnitude of the output voltage. However, it also produces a noticeable amount of ripple at the input side.

For clarify the issue of current ripple across the inductor, the value of inductance designed according to application requirement, which may increase the cost, size of the converter and its transient response time. In the original, the configuration of the interleaved structure of positive output multilevel converter for two levels (parallel connected at both input side and load side) is discussed to minimize

the input current ripple and the size of the passive components [39], [41]. However, the only circuitry suggested, and the work extended to another CW multiplier based high gain interleaved DC-DC converter with centralized source using negative and positive multiplier for input ripple cancellation (parallel connected at the input side and series-connected at output side) [39], [41], [42] to attain high voltage conversion ratio with minimum input ripple. Two input boost stage interleaved converters [43] is proposed to attain high voltage conversion ratio with minimum input ripple. However, in [43], two sources and load capacitor with a high voltage rating increases the cost of the converter. Modified Dickson charge pump is used to achieve high step-up voltage by reducing the number of semiconductor devices [44]. However, the converter is limited in the number of stages, and further addition of more number of levels is not possible to achieve high voltage as per requirement. Also, the high rating output capacitor is required to attain a constant output voltage. In [45], the structure of 2x interleaved multilevel converter [39] is extended for higher levels (N), and four different modes of operation are suggested with simulation results for renewable energy applications to boost the voltage with high conversion ratio. In [45], the interleaved multilevel structure is obtained from two same Nx multilevel DC-DC converters [38] connected in parallel at the input side and combined at output side and operated at a higher duty cycle. It reduces the current rating of the components as well as reduces the input current distortion compared to Nx MBC suggested in [38].

In light of the advantages of interleaved structure and voltage multiplier, this article contributes to the following: Detail analysis and investigation of a non-isolated Nx Interleaved Multilevel Boost Converter (Nx-IMBC) with hardware implementation for different operation modes to achieve high output voltage and minimum input ripples. Possible modes of operation are discussed with analysis of CCM and DCM boundary condition. The effect of internal inductor resistance and semiconductor devices is analyzed in detail. The design of reactive components and the selection of semiconductor devices are discussed. The comparison of the suggested converter and recently addressed converter is provided in detail to show the benefits. The performance of Nx-IMBC converter is tested through numerical simulation and hardware implementation of 100W three-level prototypes with or without perturbation in input voltage, output reference voltage and power.

This article is structured as follows: Introduction and several existing derived DC-DC converters, the motivation of converter, and the main contribution are discussed in section-I. The circuit description, modes of operation (CCM and DCM) of hybrid non-isolated and non-inverting Nx-IMBC are discussed in section-II. The effect of inductor internal resistance and semiconductor devices on a voltage conversion ratio of Nx-IMBC, steady-state analysis for CCM and DCM, efficiency and power losses are provided in section III. Various range of operation and waveforms discussed in section IV. The design, current and voltage stress, and selection of semiconductor devices for Nx-IMBC are explained in section-V. Also, comparison of Nx-IMBC with recently addressed converters is provided in section V. Experimental and numerical simulation results of Nx-IMBC are discussed with applications in section-VI. Finally, based on the detailed investigation of obtained experimental and simulation results, the conclusion is provided in section-VII.

II. HYBRID DC-DC NON-ISOLATED AND NON-INVERTING N_X INTERLEAVED MULTILEVEL BOOST CONVERTER (N_X-IMBC)

A. CIRCUIT DESCRIPTION OF N_X-IMBC

Hybrid DC-DC non-isolated and non-inverting Nx-IMBC power circuit is depicted in Fig. 2. Nx-IMBC circuitry combines the features of traditional Interleaved Boost Converter (IBC) and Cockcroft Walton (CW) voltage multiplier. *3N2* capacitors, *4N−2* diodes, two equal rated inductors along with 2 power switches are required to design circuitry of Nx IMBC, where *N* is the number of levels at the output side. Nx-IMBC provides N times conversion ratio *(N/(1−D))* compared to traditional boost converter and same ratio as compared to Nx MBC. Fig. 3(a)-(d) show the graph of the required number of capacitors, diodes, inductor and switches versus the number of levels, respectively.

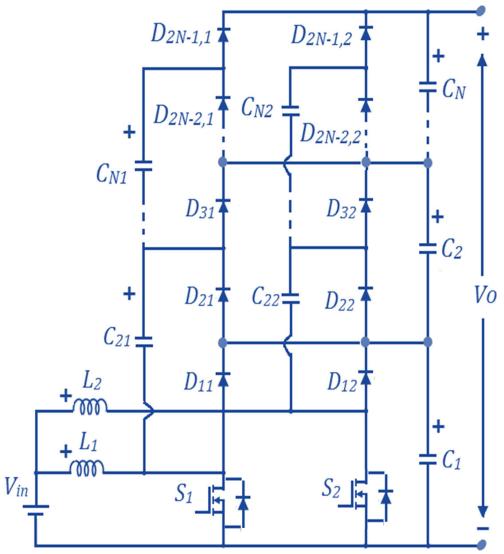

FIGURE 2. The power circuit of Nx IMBC.

The main advantages of Nx-IMBC are that in case if one phase of the converter is failing, then also Nx –IMBC provides the same voltage conversion ratio. Additionally, it is also possible to feed Nx-IMBC with two different sources, which required in several applications like PV–FC feeds DC microgrid.

Others merits of Nx-IMBC topology are

1) The non-inverting output voltage,
2) Non-isolated configuration,

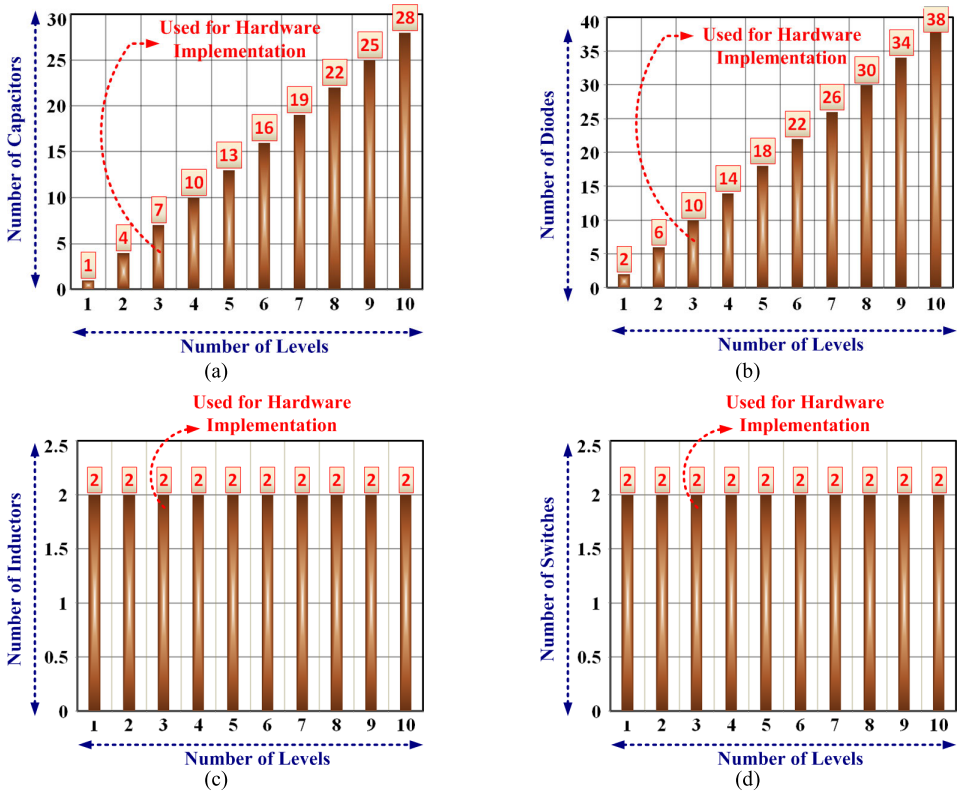

FIGURE 3. Number of components and semiconductor devices versus the number of levels (a) number of capacitors (b) number of diode (c) number of inductor (d) number of switches.

3) N-times high voltage conversion ratio compared to traditional Boost converter (N is the number of levels),
4) Low input current and output voltage ripple,
5) Suitable to feed MLI due to capacitor stack, and
6) Voltage stress across semiconductor devices is low.

Additionally, Nx-IMBC circuitry is simple, and the number of output levels can be easily increased by adding diode-capacitor circuitry to increase the voltage conversion ratio. The output voltage is calculated by adding the voltage across output side capacitors C_1, C_2…, and C_N as follows,

$$V_O = V_{C1} + V_{C2} + \ldots\ldots\ldots\ldots + V_{CN} = \left.\sum_{r=1}^{N} V_{Cr}\right\} \quad (1)$$

B. THE POSSIBLE STATES IN CONTINUOUS CONDUCTION MODE

To explain the states of operation, 3x Interleaved Multilevel Boost Converter (Nx-IMBC with $N = 3$) is assumed with ideal components, capacitors are large enough to provide constant voltage, and the circuit operated in Continuous Conduction Mode (CCM). The proposed converter can exercise in four states of operations.

1) STATE-1: WHEN SWITCHES S_1 AND S_2 ARE ON

When the switches (S_1 and S_2) are ON, inductors L_1 and L_2 magnetized from the input source (V_{in}), and the capacitors C_1, C_2 and C_3 are discharged through the load (R_o). The voltage across the capacitors make diodes D_{21}, D_{22}, D_{41} and D_{42} forward biased and the load side capacitors C_1, C_2 discharged through the path of diodes to charge capacitors C_{21}, C_{22} and C_{31} and C_{32}, respectively. Fig. 4(a) shows the equivalent power circuit when both the switches S_1 and S_2 are ON. In this mode, diodes $D_{11}, D_{12}, D_{31}, D_{32}, D_{51}$ and D_{52} are reversed biased. The voltage across inductors and capacitors are calculated as follows,

$$\left.\begin{aligned} &V_{L1} = V_{L2} = L_1\frac{di_{L1}}{dt} = L_2\frac{di_{L2}}{dt} = V_{in} \\ &V_{C_{21}} = V_{C_{22}} = V_{C_1} \\ &V_{C_{21}} + V_{C_{31}} = V_{C_{22}} + V_{C_{32}} = V_{C_1} + V_{C_2} \\ &V_o = V_{C_1} + V_{C_2} + V_{C_3} \end{aligned}\right\} \quad (2)$$

2) STATE-2: WHEN SWITCH S_1 IS ON, AND SWITCH S_2 IS OFF

The equivalent power circuit when switch S_1 is ON and switch S_2 is OFF is depicted in Fig. 4(b). The inductor L_1 is magnetized from input voltage (V_{in}) and at the same time, the capacitors C_1, C_2 and C_3 charged by inductor L_2 and capacitors C_{22} and C_{32}. The inductor L_2 and capacitors C_{22} and C_{32} also charge capacitors C_{21}, C_{31} of the multiplier cell and provides energy to load (R_o). In this mode, diodes $D_{11}, D_{31}, D_{51}, D_{22}, D_{42}$ are reversed biased, and diodes D_{21}, D_{41}, D_{12}, D_{32} and D_{52} are forward biased. The voltage across

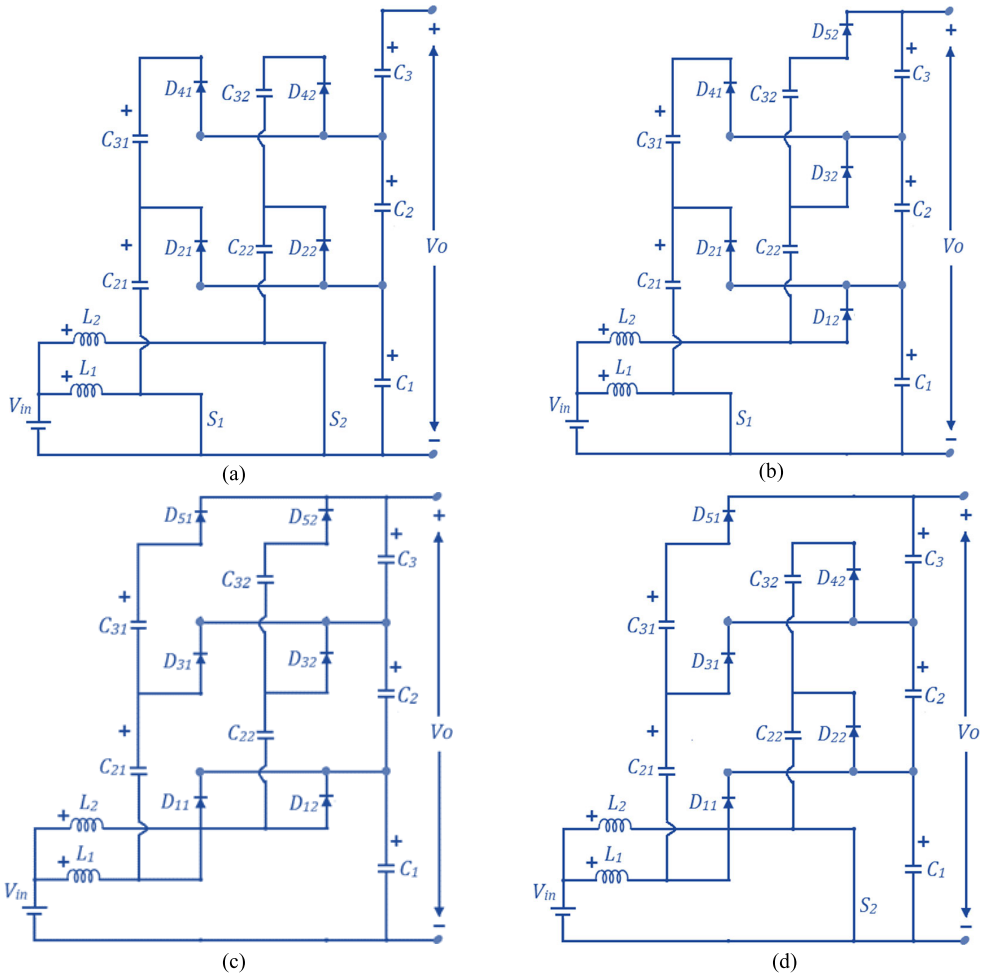

FIGURE 4. Equivalent circuit of Nx IMBC (a) Switches S_1 and S_2 are ON, (b) Switch S_1 is ON and switch S_2 is OFF, (c) Switches S_1 and S_2 are OFF, (d) Switches S_1 is OFF and Switch S_2 is ON.

inductors and capacitors are calculated as follows,

$$\left.\begin{aligned} &V_{L1} = L_1\frac{di_{L1}}{dt} = V_{in} \\ &V_{C_{21}} = V_{C_1}, V_{C_{21}}+V_{C_{31}} = V_{C_1}+V_{C_2} \\ &V_{C_1} = V_{in}-L_2\frac{di_{L2}}{dt} \\ &V_{C_2}+V_{C_1} = V_{in}-L_2\frac{di_{L2}}{dt}+V_{C_{22}} \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} = V_{in}-L_2\frac{di_{L2}}{dt}+V_{C_{22}}+V_{C_{32}} \end{aligned}\right\} \quad (3)$$

3) STATE-3: WHEN SWITCH S_1 AND SWITCH S_2 ARE OFF

The equivalent power circuit when switches S_1 and S_2 are OFF is depicted in Fig. 4(c). In this mode, inductors L_1 and L_2 are demagnetized to charge output side capacitors. Capacitors C_1, C_2 and C_3 are charged by series combination V_{in}, L_1, C_{21}, C_{31} and series combination of V_{in}, L_2, C_{22} and C_{32}. Diodes D_{11}, D_{31}, D_{51}, D_{12}, D_{32}, D_{52} are forward biased, and diodes D_{21}, D_{41}, D_{22}, D_{42} are reversed biased. The voltage across inductors and capacitors are calculated as follows,

$$\left.\begin{aligned} &V_{C_1} = V_{in}-L_1\frac{di_{L1}}{dt} = V_{in}-L_2\frac{di_{L2}}{dt} \\ &V_{C_2}+V_{C_1} = V_{in}-L_1\frac{di_{L1}}{dt}+V_{C_{21}} = V_{in}-L_2\frac{di_{L2}}{dt}+V_{C_{22}} \\ &V_{C_3}+V_{C_2}+V_{C_1} = V_{in}-L_1\frac{di_{L1}}{dt}+V_{C_{21}}+V_{C_{31}} \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} = V_{in}-L_2\frac{di_{L2}}{dt}+V_{C_{22}}+V_{C_{32}} \end{aligned}\right\} \quad (4)$$

4) STATE-4: WHEN SWITCH S_1 IS OFF, AND SWITCH S_2 IS ON

The equivalent circuit of the proposed converter when switch S_1 is OFF and switch S_2 is ON is depicted in Fig. 4(d). The inductor L_2 is magnetized from input voltage (V_{in}) and at the same time, the capacitors C_1, C_2 and C_3 charged by inductor L_1 and capacitors C_{21} and C_{31}. The inductor L_1 and capacitors C_{21} and C_{31} also charge capacitors C_{22}, C_{32} of the multiplier cell and provides energy to load (R_o). In this mode, diodes D_{11}, D_{31}, D_{51}, D_{22}, D_{42} are forward biased, and diodes D_{21},

$D_{41}, D_{12}, D_{32}, D_{52}$ are reversed biased.

$$\left.\begin{aligned} &V_{L2} = L_2\frac{di_{L2}}{dt} = V_{in} \\ &V_{C_{22}} = V_{C_1}, V_{C_{22}}+V_{C_{32}} = V_{C_1}+V_{C_2} \\ &V_{C_1} = V_{in} - L_1\frac{di_{L1}}{dt} \\ &V_{C_2}+V_{C_1} = V_{in} - L_1\frac{di_{L1}}{dt}+V_{C_{21}} \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} = V_{in} - L_1\frac{di_{L1}}{dt}+V_{C_{21}}+V_{C_{31}} \end{aligned}\right\} \quad (5)$$

The CCM inductor current and voltage waveforms for all the state are shown in Fig. 5.

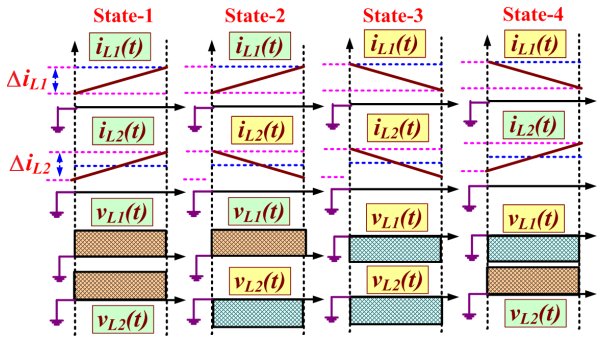

FIGURE 5. CCM inductor current and voltage waveform for all the states.

C. THE POSSIBLE STATES IN DISCONTINUOUS CONDUCTION MODE

When Nx-IMBC circuit operates in DCM, there are three possible states which depend on the switching of the switches S_1 and S_2.

1) STATE-1: WHEN SWITCH S_1 IS ON, SWITCH S_2 IS OFF, AND L_2 CURRENT IS ZERO

The equivalent power circuit for this state is depicted in Fig. 6(a). The inductor L_1 is magnetized from input voltage (V_{in}) and the capacitors C_{21} is charged by the capacitor C_1 through diode D_{21} and switch S_1. Capacitor C_{31} is charged by the capacitor C_2 through diode D_{41} and switch S_1. At the same time, capacitors C_1, C_2, C_3 also discharged through the load (R_o). In this mode, diodes $D_{11}, D_{12}, D_{22}, D_{31}, D_{32}, D_{42}, D_{51}$, and D_{52} are reversed biased and diodes D_{21}, D_{41} are forward biased. The slope of inductor current and capacitors voltage is calculated as follows,

$$\left.\begin{aligned} &\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}, \frac{di_{L2}}{dt} = 0 \\ &V_{C_{21}} = V_{C_1}, V_{C_{21}}+V_{C_{31}} = V_{C_1}+V_{C_2} \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} \end{aligned}\right\} \quad (6)$$

2) STATE-2: WHEN SWITCH S_1 IS OFF, SWITCH S_2 IS ON, AND L_1 CURRENT IS ZERO

The equivalent power circuit for this state is depicted in Fig. 6(b). The inductor L_2 is magnetized from input voltage (V_{in}) and the capacitor C_{22} is charged by the capacitor C_1 through diode D_{22} and switch S_2. Capacitor C_{32} is charged by the capacitor C_2 through diode D_{42} and switch S_2. At the same time, capacitors C_1, C_2, C_3 discharged through the load (R_o). In this mode, diodes $D_{11}, D_{12}, D_{21}, D_{31}, D_{32}, D_{41}, D_{51}$, and D_{52} are reversed biased, and diodes D_{22}, D_{42} are forward biased. The slope of inductor current and capacitors voltage is calculated as follows,

$$\left.\begin{aligned} &\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2}, \frac{di_{L1}}{dt} = 0 \\ &V_{C_{22}} = V_{C_1}, V_{C_{22}}+V_{C_{32}} = V_{C_1}+V_{C_2} \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} \end{aligned}\right\} \quad (7)$$

3) STATE-3: WHEN SWITCHES S_1, S_2 are OFF, L_1 AND L_2 CURRENT IS ZERO

The equivalent power circuit for this state depicted in Fig. 6(c). In this mode, all the diodes are reversed biased and capacitors C_1, C_2, C_3 are discharged through the load (R_o). The slope of inductor current and the output voltage is calculated as follows,

$$\left.\begin{aligned} &\frac{di_{L2}}{dt} = \frac{di_{L1}}{dt} = 0 \\ &V_o = V_{C_3}+V_{C_2}+V_{C_1} \end{aligned}\right\} \quad (8)$$

Inductor current and voltage waveforms for all the state of DCM are shown in Fig. 7.

D. BOUNDARY OF CCM AND DCM

In general, DCM is occurring when the inductor current reaches zero. The condition for CCM and DCM for Nx-IMBC is,

$$\left.\begin{aligned} &DCM \Rightarrow I_{L1} < \Delta i_{L1}(t); I_{L2} < \Delta i_{L2}(t) \\ &CCM \Rightarrow I_{L1} > \Delta i_{L1}(t); I_{L2} > \Delta i_{L2}(t) \end{aligned}\right\} \quad (9)$$

For simple calculation, assume all the components and semiconductor devices are ideal. Consider D is the duty ratio of gate pulses provided to switches S_1 and S_2 (Note: Both switches have an equal duty cycle (D) and switching frequency). The pulse given to switch S_2 is delayed by 50% compared to switch S_1. Therefore, according to circuit topology, the voltage across all the capacitors is the same, and the voltage across the load is calculated as follows,

$$V_o = V_{Nx-IMBC} = N \times V_{C1} = \frac{N \times V_{in}}{1-D} \quad (10)$$

It is noteworthy that, the current flowing through both the inductors is same ($I_{L1} = I_{L2} = I_L$). The condition for DCM is obtained as,

$$\left.\begin{aligned} &I_L = \frac{N^2 \times V_{in}}{2R_o(1-D)_2} < \frac{V_{in}D}{L_1 \times f_s} or \frac{V_{in}D}{L_2 \times f_s} \\ &\frac{fsL_1}{R_o} or \frac{fsL_2}{R_o} < \frac{2D \times (1-D)_2}{N^2}; B < B_{critical}(D); \\ &Boundary\ \text{Surface} = B_{critical}(D) = \frac{2D \times (1-D)_2}{N^2} \end{aligned}\right\} \quad (11)$$

The boundary for DCM and CCM is shown in Fig. 8. Investigated that $B_{critical}(D)$ decreases as the number of levels increased, and $8/27N^2$ is the maximum value of $B_{critical}(D)$ for N level at $D = 1/3$.

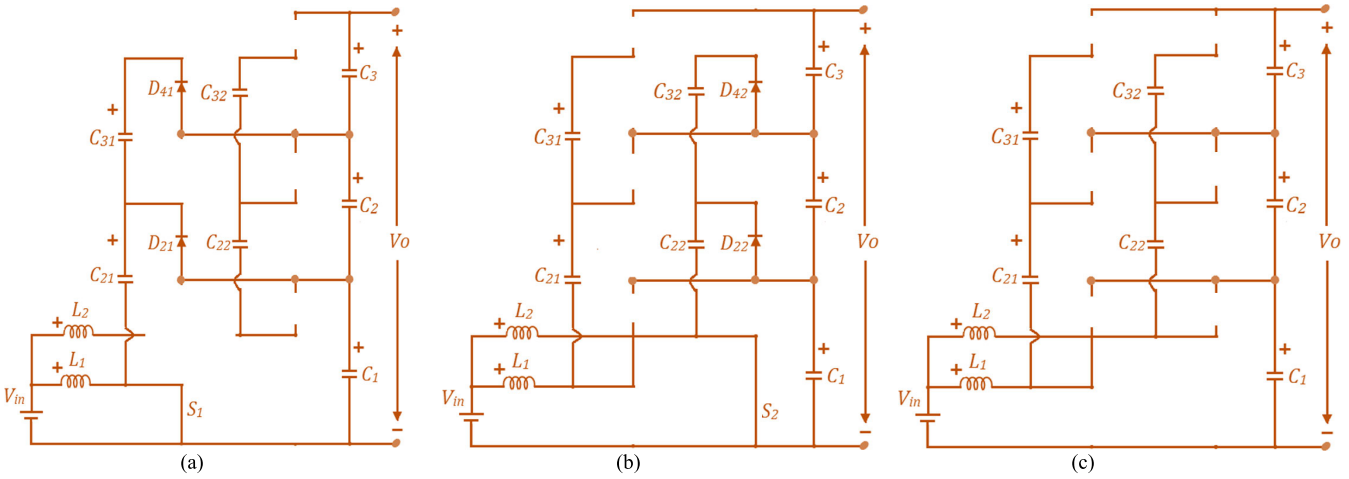

FIGURE 6. Equivalent circuit of DCM states (a) Switches S_1 ON, S_2 is OFF, and L_2 operated in DCM (b) Switches S_1 is OFF, Switch S_2 is ON, and L_1 is operated in DCM (c) Switches S_1 and S_2 are OFF, and L_1 and L_2 are operated in DCM.

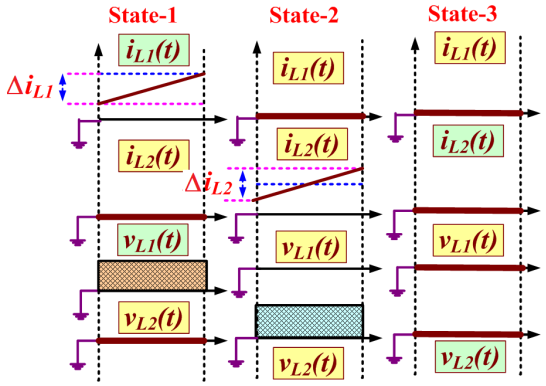

FIGURE 7. DCM inductor current and voltage waveform for all the states.

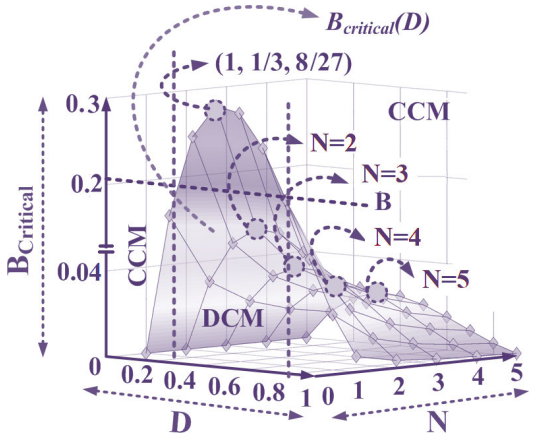

FIGURE 8. The boundary for CCM and DCM.

III. STEADY-STATE ANALYSIS AND EFFECT OF INTERNAL RESISTANCE OF INDUCTOR AND SEMICONDUCTOR DEVICES FOR N_X-IMBC

A. ANALYSIS IN CCM

In real-time applications, the voltage conversion ratio of any DC-DC converter is restricted by parasitic resistance of passive components or devices; specially inductor of the converter. Parasitic R_{L1} and R_{L2} (Equivalent Series Resistance) is considered in series with inductor L_1 and L_2 respectively. The voltage across inductors L_1 and L_2 is calculated when switches S_1 and S_2 are ON and OFF as follow,

$$\left.\begin{aligned} &S_1ON \Rightarrow V_{in} - I_{L1}R_{L1} = L_1\frac{di_{L1}}{dt} \\ &S_2ON \Rightarrow V_{in} - I_{L2}R_{L2} = L_2\frac{di_{L2}}{dt} \\ &S_1OFF \Rightarrow V_{in} - I_{L1}R_{L1} - V_{C_1} = L_1\frac{di_{L1}}{dt} \\ &S_2OFF \Rightarrow V_{in} - I_{L2}R_{L2} - V_{C_1} = L_2\frac{di_{L2}}{dt} \end{aligned}\right\} \quad (12)$$

Note: for simplicity, consider ideal diode ($V_d = 0$) and ideal switch ($V_S = 0$) in Nx- IMBC with load R_o.

$$\left.\begin{aligned} &V_{in} \times I_{in} = I_o \times V_o = \frac{N^2 V_{in} V_{C1}}{(1-D)R_o} \\ &I_{in} = I_{L1} + I_{L2} = \frac{N^2 \times V_{C1}}{(1-D)R_o} \end{aligned}\right\} \quad (13)$$

Inductor volt balanced second method is applied and equations obtained as follow,

$$\left.\begin{aligned} &V_{L1} = D(V_{in} - I_{L1}R_{L1}) + \overline{D}(V_{in} - I_{L1}R_{L1} - V_{C1}) = 0 \\ &V_{L2} = D(V_{in} - I_{L2}R_{L2}) + \overline{D}(V_{in} - I_{L2}R_{L2} - V_{C1}) = 0 \end{aligned}\right\} \quad (14)$$

$$V_{in} = \frac{I_{L1}R_{L1} + I_{L2}R_{L2}}{2} + (1-D)V_{C1} \quad (15)$$

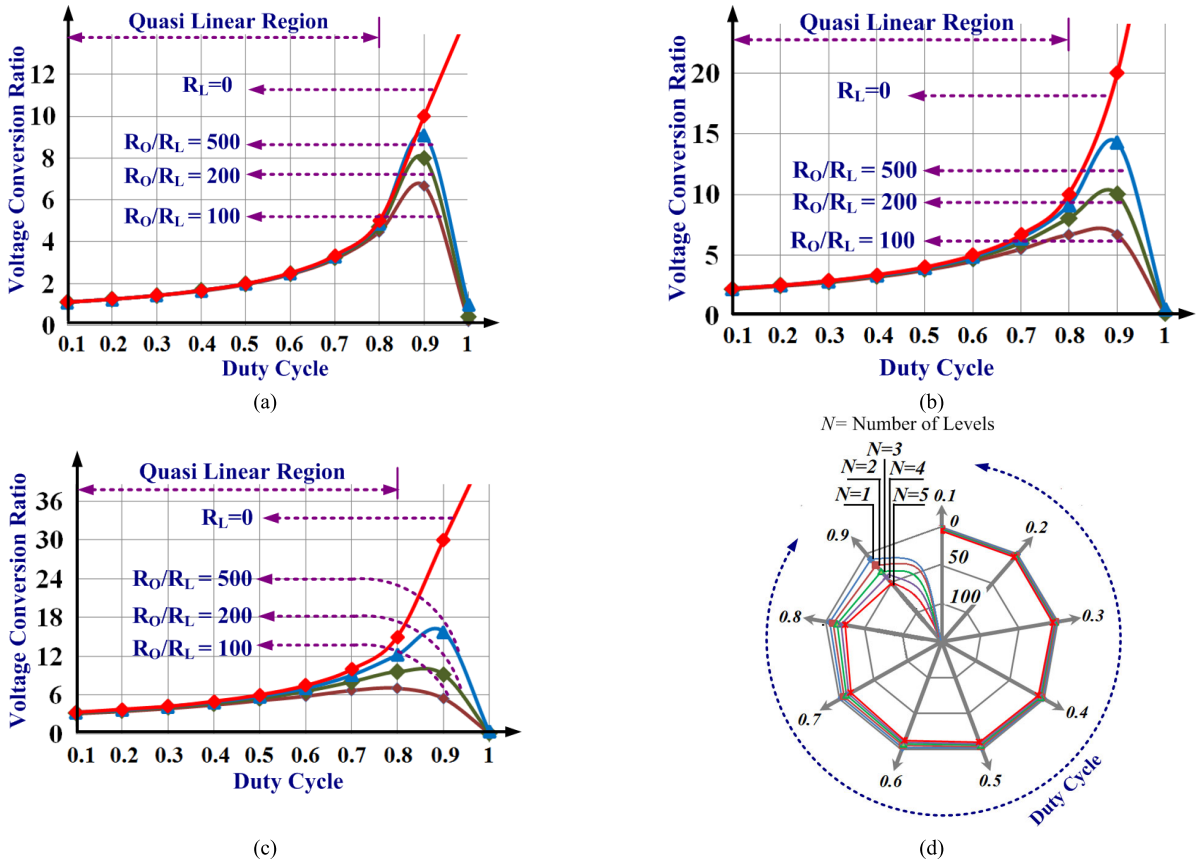

FIGURE 9. Voltage Conversion ratio plot versus the duty cycle for different cases of R_L/R_O (a) N = 1, (b) N = 2, (c) N = 3, (d) voltage conversion ratio plot versus duty cycle for N = 1 to 5 when $R_L = 0$.

Noted that identical rating inductor are used. So, their internal resistance is the same ($R_{L1} = R_{L2} = R_L$). Thus,

$$\left.\begin{aligned} V_{in} &= \frac{(I_{L1} + I_{L2})R_L}{2} + (1-D)V_{C1} \\ V_{in} &= \frac{I_{in}R_L}{2} + (1-D)V_{C1} \end{aligned}\right\} \tag{16}$$

By the above equation, the voltage conversion ratio obtained as,

$$\left.\frac{V_o}{V_{in}} = \frac{1}{\frac{1}{2}\frac{N\times R_L}{(1-D)R_o} + \frac{\overline{D}}{N}} = \frac{N}{(1-D) + \frac{1}{2}\frac{N^2\times R_L}{(1-D)R_o}}\right\} \tag{17}$$

In Fig. 9(a) - 9(c), the voltage conversion ratio is a plot against duty cycle for various cases of R_L/R_o when $N = 1$ *to* 3. In Fig. 9(d), the voltage conversion ratio is a plot against duty cycle for $N = 1$ *to* 5 and $R_L = 0$ (ideal case). Examined that the voltage conversion ratio is linear increases up to duty cycle 80%, and this linear region called a Quasi Linear Region.

To calculate the efficiency of the converter, let us consider voltage V_d and V_s is the drop of each diode and each switch, respectively.

It is examined that capacitor C_1 transfers its energy to charge capacitor C_{21} through diode D_{21} and switch S_1 in state I and II. Also, capacitor C_1 transfers its energy to charge capacitor C_{22} through diode D_{22} and switch S_2 in state I and IV. The voltage across capacitor C_{21} and C_{22} are obtained as follows,

$$\left.\begin{aligned} V_{C21} &= V_{C1} - V_d - V_S \\ V_{C22} &= V_{C1} - V_d - V_S \end{aligned}\right\} \tag{18}$$

The capacitor C_{21} and C_{22} transfer its energy to charged capacitor C_2. The voltage across C_2 is obtained as follows,

$$V_{C2} = V_{C21} - 2V_d = V_{C1} - 3V_d - V_S\} \tag{19}$$

The capacitor C_2 transfers its energy to charge capacitor C_{31} through diode D_{31} and switch S_1 in state I and II. Also, capacitor C_2 transfers its energy to charge capacitor C_{32} through diode D_{32} and switch S_2 in state I and IV. The voltage across capacitor C_{31} and C_{32} is obtained as follows,

$$\left.\begin{aligned} V_{C31} + V_{C21} &= 2V_{C1} - 5V_d - V_S \\ V_{C32} + V_{C22} &= 2V_{C1} - 5V_d - V_S \\ \therefore V_{C31} &= V_{C32} = V_{C1} - 4V_d \end{aligned}\right\} \tag{20}$$

Further, observed that the voltage across capacitors C_{31}, C_{32}, C_{41}, C_{42} …., C_{N1}, and C_{N2} is same and equal to V_{C1}-$4V_d$. The total output voltage is calculated as follows (21), shown at the bottom of the next page.

The efficiency (η) of the Nx-IMBC obtained as follows,

$$\left.\begin{aligned}\eta &= \frac{(1-D)/N}{\frac{1}{2}\frac{N\times R_L}{(1-D)R_o}+\frac{\overline{D}}{N}} - (4N-3)\frac{(1-D)V_d}{NV_{in}} - \frac{(1-D)V_S}{NV_{in}}\\ &\text{if } R_L \to 0, \text{ then } \eta = 1-(4N-3)\frac{(1-D)V_d}{NV_{in}} - \frac{(1-D)V_S}{NV_{in}}\\ &\text{if semiconductor devices are ideal, then}\\ \eta &= \frac{(1-D)/N}{\frac{1}{2}\frac{N\times R_L}{(1-D)R_o}+\frac{(1-D)}{N}}\end{aligned}\right\} \quad (22)$$

The power loss due to semiconductor devices (P_{LS}) and internal resistance of inductor (P_{Li}) of the Nx-IMBC obtained as follows,

$$\left.\begin{aligned}P_{LS} &= P_{in}\left(1-\left(1-(4N-3)\frac{(1-D)V_d}{NV_{in}}-\frac{(1-D)V_S}{NV_{in}}\right)\right)\\ P_{Li} &= P_{in}\left(1-\frac{(1-D)/N}{\frac{1}{2}\frac{N\times R_L}{(1-D)R_o}+(1-D)/N}\right)\end{aligned}\right\} \quad (23)$$

B. ANALYSIS OF DCM

Let's consider, switch S_1 is ON and inductor L_1 is magnetized for the time D_1T_S; switch S_1 is OFF and inductor L_1 is demagnetized for the time D_2T_S; and switch S_1 is OFF and inductor L_1 current is zero for the time D_3T_S. Similarly, at 180° phase shift, switch S_2 is ON and inductor L_2 is magnetized for the time D_1T_S; switch S_2 is OFF and inductor L_2 is demagnetized for the time D_2T_S; and switch S_2 is OFF and inductor L_2 current is zero for the time D_3T_S. The time relations obtained as follows,

$$\left.\begin{aligned}&\textit{One cycle Time} = T_S = \frac{1}{f_S} = DT_S + D_1T_S + D_2T_S\\ &\Rightarrow (D + D_1 + D_2) = 1\end{aligned}\right\} \quad (24)$$

The voltage across inductor L_1 and L_2 for each time-period obtained as follows,

$$\left.\begin{aligned}V_{in} - I_{L1}R_{L1} &= V_{L1}\\ V_{in} - I_{L2}R_{L2} &= V_{L2}\end{aligned}\right\} \textit{ for } D_1T_s \quad (25)$$

$$\left.\begin{aligned}V_{in} - I_{L1}R_{L1} - V_{C1} &= V_{L1}\\ V_{in} - I_{L2}R_{L2} - V_{C1} &= V_{L2}\end{aligned}\right\} \textit{ for } D_2T_S \quad (26)$$

$$\left.\begin{aligned}V_{L1} = 0,\ V_{L2} = 0\end{aligned}\right\} \textit{ for } D_3T_S \quad (27)$$

By inductor volt-second balanced method, the equation obtained as follows,

$$\left.\begin{aligned}(V_{in} - I_{L1}R_{L1})\,D_1 + (V_{in} - I_{L1}R_{L1} - V_{C1})\,D_2 &= 0\\ (V_{in} - I_{L2}R_{L2})\,D_1 + (V_{in} - I_{L2}R_{L2} - V_{C1})\,D_2 &= 0\\ V_{in}\,(D_1+D_2) = \frac{I_{L1}R_{L1}+I_{L2}R_{L2}}{2}\,(D_1+D_2) + (D_2)\,V_{C1}&\end{aligned}\right\} \quad (28)$$

If $R_{L1} = R_{L2} = R_L$ then,

$$\left.\begin{aligned}V_{in}\,(D_1+D_2) &= \frac{(I_{L1}+I_{L2})\,R_L}{2}\,(D_1+D_2) + (D_2)\,V_{C1}\\ \frac{V_{C1}}{V_{in}} &= \left(1-\frac{(I_{L1}+I_{L2})R_L}{2V_{in}}\right)\left(\frac{D_1}{D_2}+1\right)\end{aligned}\right\} \quad (29)$$

For simple calculation, consider all the semiconductor devices are ideal, and capacitors are large enough to provide ripple-free voltage. The voltage across the load calculated as follows,

$$\left.\begin{aligned}\frac{V_o}{V_{in}} &= N\left(1-\frac{(I_{L1}+I_{L2})\,R_L}{2V_{in}}\right)\left(\frac{D_1}{D_2}+1\right)\\ \textit{where, } D_2 &= \frac{D_1NV_{in}}{V_o - V_{in}} = \frac{2L}{R_o}\frac{V_o}{V_{in}D_1}\end{aligned}\right\} \quad (30)$$

If both inductors are identical and ideal then, $L_1 = L_2 = L$ and $R_{L1} = R_{L2} = 0$;

$$\left.\begin{aligned}V_o^2 - \frac{NV_{in}^2D_1^2}{2B} - V_oV_{in} &= 0\\ \textit{where, } B &= \frac{L}{R_oT_s}\end{aligned}\right\} \quad (31)$$

The solution of (31) yields two roots. However, we know that the output of the proposed converter is positive. Therefore positive root is selected, and the voltage conversion ratio obtained as follows,

$$\frac{V_o}{V_{in}} = 0.5\left(1+\left(1+\frac{2ND_1^2}{B}\right)^{\frac{1}{2}}\right) \quad (32)$$

Examined that the voltage conversion ratio is load-dependent and consequent increasing converter output impedance.

$$\left.\begin{aligned}V_o &= \frac{1}{\frac{1}{2}\frac{N\times R_L}{(1-D)R_o}+\frac{\overline{D}}{N}}V_{in} - (4N-3)V_d - V_S\\ &\textit{where,}\\ &\left(\begin{aligned}&\frac{1}{2}\frac{N\times R_L}{(1-D)R_o} \to \text{Effect of Intermal Resistance of Inductor}\\ &(4N-3)V_d \to \text{Effect of diode}\\ &V_S \to \text{Effect of switch}\end{aligned}\right)\end{aligned}\right\} \quad (21)$$

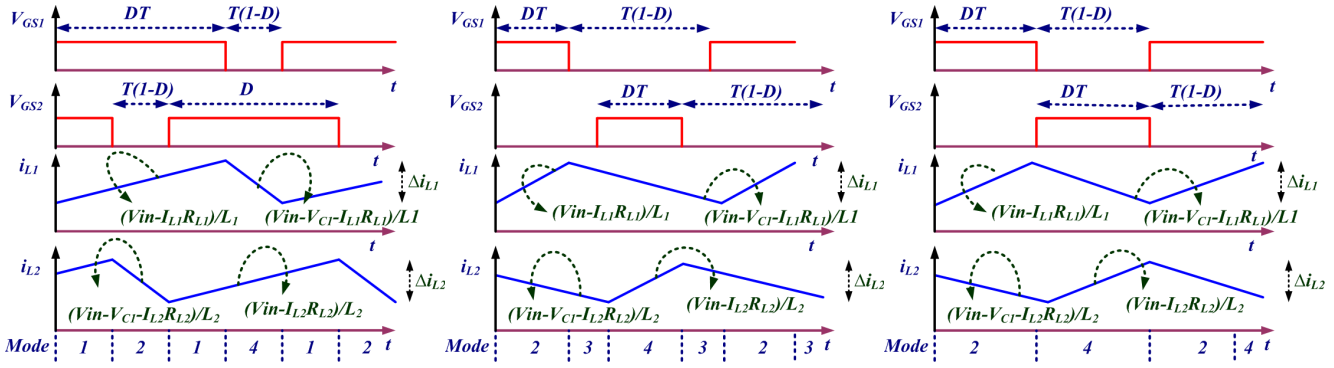

FIGURE 10. Inductor L_1 and L_2 current waveform (a) when the duty cycle is higher than 50%, (b) when the duty cycle is lesser than 50%, (c) when the duty cycle is equal to 50%.

IV. VARIOUS RANGE OF OPERATION AND INDUCTOR CURRENT WAVEFORM

The converter is possible to control in three different range of duty cycle i) duty cycle higher than 50% ii) duty cycle lesser than 50% and iii) duty cycle is equal to 50%. The slope of the inductor (L_1 and L_2) current waveforms are analyzed for three different ranges of duty cycle, as shown in Fig. 10(a)-(c). First, analyzed that the proposed converter operates in states 1, 2 and 4 when the duty cycle is higher than 50%. Second, analyzed that the proposed converter operates in states 2, 3 and 4 when the duty cycle is lesser than 50%. Third, analyzed that the proposed converter operates only in state 2 and 4 when the duty cycle equal to 50%.

V. DESIGN AND COMPARISON OF N_X-IMBC

The slope of the inductor currents is used to calculate the critical inductance such that considered current ripples obtained. The critical inductance and current stress calculated as follows,

$$\left.\begin{aligned} Critical\ L_1 &= \frac{V_{in} - I_{L1}R_{L1}}{\Delta I_{L1}} DT_s \\ Critical\ L_2 &= \frac{V_{in} - I_{L2}R_{L2}}{\Delta I_{L2}} DT_s \\ (I_{L1} = I_{L2}) &> \frac{I_{in}}{2} \end{aligned}\right\} \tag{33}$$

The voltage across all the capacitors is precisely the same if all the diodes are considered ideal. Therefore, due to the balanced voltage structure of voltage multiplier, it is feasible to select all the capacitors with an equal rating. The slope of capacitor voltage is used to calculate the critical capacitance such that considered voltage ripples obtained. The critical capacitance and voltage rating of the capacitor decided as,

$$\left.\begin{aligned} Critical\ C &= \frac{DV_o}{f_s \Delta v_C RN},\ \mathrm{V_C} > \frac{V_o}{N} = \frac{V_{in}}{1-D} \end{aligned}\right\} \tag{34}$$

It is also feasible to select all the diodes with equal rating due to the benefits of voltage multiplier. The voltage and current rating of the diode decided as,

$$\left.\begin{aligned} \mathrm{V}_D > \frac{V_o}{N} = \frac{V_{in}}{1-D},\ I_D > I_L > \frac{I_{in}}{2} \end{aligned}\right\} \tag{35}$$

The drain to source voltage of both switches S_1 and S_2 calculated and examined that each switch voltage is equal to each capacitor voltage. The current flowing through switch is equal to the addition of inductor current and capacitor clamping current. Voltage and current rating of the switch are decided as,

$$\left.\begin{aligned} &(V_{S1} = V_{S2}) > \frac{V_o}{N} = \frac{V_{in}}{1-D} \\ &(i_{S1}(t) = i_{S2}(t)) > i_{in}(t) + Capacitor\ clamping\ current \\ &(i_{S1}(t) = i_{S2}(t)) \gg i_{in}(t), \end{aligned}\right\} \tag{36}$$

In Table-2, Nx-IMBC configuration compared with existing DC-DC converter in terms of voltage conversion ratio, voltage stress, number of the inductor, number of the capacitor, number of diodes, number of switches, input current behavior. It is noteworthy that the Nx-IMBC provides high voltage conversion ratio with the low voltage across switch, input current ripple cancellation, and without using a more significant number of inductors and switches. In Fig. 11, the Nx-IMBC and existing converters are compared in terms of voltage conversion ratio. Notably, Nx-IMBC provides a practical solution to obtain high voltage with reduce input ripple, and low rating components are suitable to design converter.

VI. NUMERICAL SIMULATION AND EXPERIMENTAL RESULTS

Nx-IMBC configuration is simulated with ideal components for three-level (i.e3x IMBC) with the designed parameter to verify its functionality. The designed parameters given in Table 3. Fig. 12(a) shows the output and input voltage of three levels 3x IMBC, and investigated that the voltage conversion ratio converter is 12 at 75% duty cycle. Thus, the required output voltage 120V obtained from a 10V input voltage at a 75% duty cycle. Fig. 12(b) shows the voltage

TABLE 2. Comparison of Nx IMBC and existing DC-DC converter.

Converter	Inductors	Capacitors	Diodes	Switches	Output voltage at D=0.6	Ripples Cancellation	Output capacitor stack	Voltage across switch
Fig.1 (a)	1	1	1	1	$2.50V_{in}$	NO	NO	V_o
Fig. 1(c)	2	1	4	1	$4V_{in}$	NO	NO	V_o
Fig. 1(b)	2	2	3	1	$6.25V_{in}$	NO	NO	V_o
FIg. 1(d)	1	2	2	2	$5V_{in}$	NO	NO	$V_o/2$
Fig. 1(e)	2	2	2	2	$6.25V_{in}$	NO	NO	$0.4V_o$
Fig. 1(f)	2	3	4	3	$9V_{in}$	NO	NO	V_o
FIg. 1(g)	2	3	2	1	$4V_{in}$	NO	NO	$V_o/0.4$
FIg. 1(h)	2	4	4	2	$10V_{in}$	YES	NO	$V_o/4$
FIg. 1(i)	5	6	9	1	$10V_{in}$	NO	NO	$V_o/4$
Fig. 1(j)	2	3	4	2	$5V_{in}$	YES	NO	$V_o/2$
Nx MBC	1	2N-1	2N-1	1	$NV_{in}/0.4$	NO	YES	$V_{in}/0.4$
Nx MBBC	1	2N-1	2N-1	1	$((N-1)+0.6)\ V_{in}/(0.4)$	NO	YES	$V_{in}/0.4$
Nx IMBC	2	3N-2	2(2N-1)	2	$NV_{in}/0.4$	YES	YES	$V_o/4$

TABLE 3. Parameter of numerical simulation test.

Parameter	Value
Input Voltage, Output Voltage	10 V/ 120V
Power, Load	100W, 144Ω
Number of Output Levels	Three
Inductance, Capacitance	150uH, 220uF
Duty Cycle, Switching Frequency	75%, 50kHz

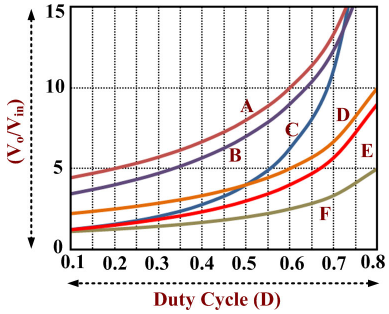

FIGURE 11. Voltage conversion ratio versus duty cycle (A: Fig. 1(h), 1(i), Nx MBC, Nx IMBC; B: Fig. 1(f); C: Fig. 1(b), 1(e); D: Fig. 1(d), 1(j); E: Fig. 1(c), 1(g); F = Fig. 1(a)).

at a different output level. Observed that each level contributes to equal voltage (*Vo*/3, i.e. 40V). Thus, the voltage at the first level is 40V, the voltage at the second level is 80V, and the voltage at the third level is 120V. Fig. 12(c) shows the voltage distribution across output side capacitors (C_1, C_2 and C_3). Investigated that voltage across output side capacitors is equal to *Vo/3* (i.e. 40V). The voltage distribution across all the output side capacitors (C_1, C_2 and C_3) shows that the converter performs satisfactorily. Fig. 12(d) shows the voltage distribution across multiplier capacitors. Investigated that voltage across capacitors of the multiplier is equal to *Vo/3* (i.e. 40V). The voltage distribution across all the capacitors C_{21}, C_{22}, C_{31} and C_{32} shows that the converter performs satisfactorily.

Fig. 13(a) shows the inductor current waveform with the gate pulse of switches. Investigated that 5.2A current is flowing through the inductor (L_1 and L_2) which is nearly half of the input current ($I_{in}/2$). Fig. 13(b) shows the drain to source voltage of switches (V_{DS1} and V_{DS2}) with gate to source voltage of switches (V_{GS1} and V_{GS2}). Observed that the drain to source voltage of switches is equal to *Vo/3* i.e 40V. This drain to source voltage of switch remains same even also of the voltage levels at the output. Output and input current ripples shown in Fig. 13(c). Observed that the input current and output current ripple is 600mA and 2mA, respectively. Thus, 3Nx IMBC provides a low input and output current ripple, and highly desired in photovoltaic application.

The 3x IMBC investigated experimentally, and the result shows a good match with the simulation results. The detail of the hardware components used for the experimental purpose shown in Table 4. The hardware prototype of Nx IMBC is designed for three-level (3x IMBC) and tested at power 100W, and gate pulses are generated through FPGA with a classical PI controller to control the output voltage.

Fig. 14(a) shows the obtained output voltage, input voltage, output current and input current waveform. Examined that output voltage (v_o) 120.17V achieved by feeding input voltage (v_{in}) 10V. The observed input current (i_{in}) and output current (i_o) are 10.63A and 808.5mA, respectively. Fig. 14(b) shows the obtained voltage waveform at various levels of the designed converter. Examined that the voltage at level one, two, and three are 40.13V, 80.19V, and 120.21V, respectively. Separately, the voltage across each output side capacitor also measured and shown in Fig. 14(c). The obtained voltage

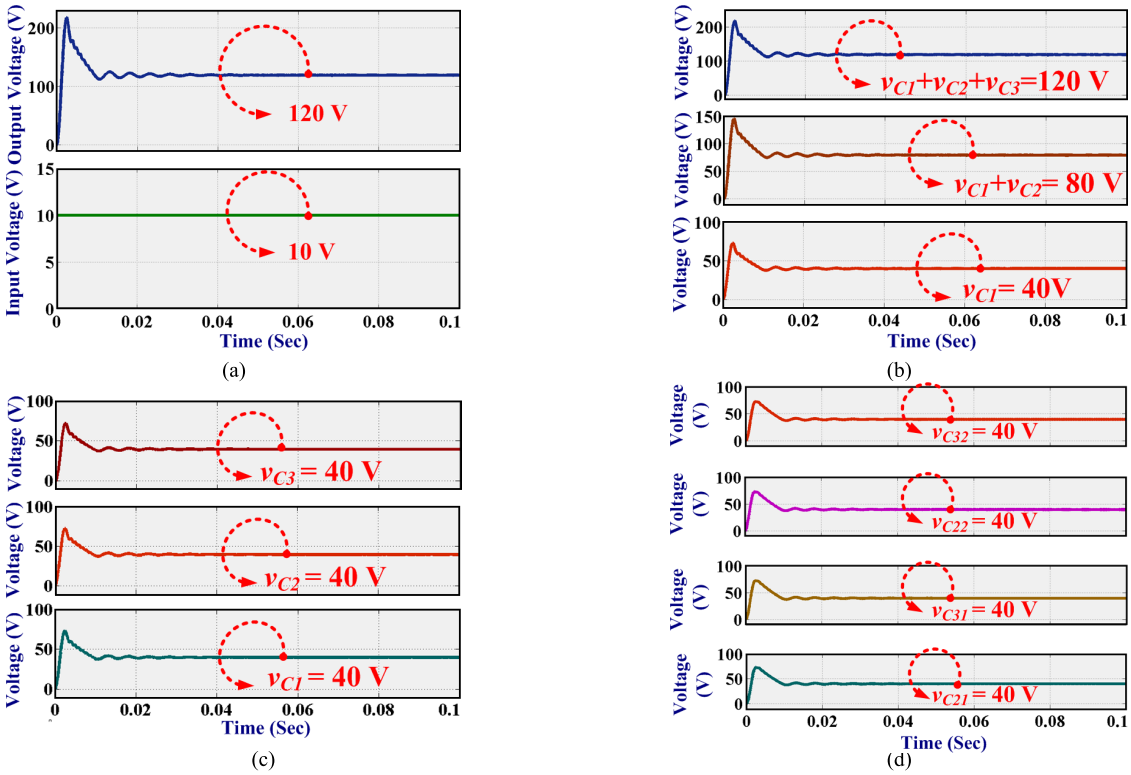

FIGURE 12. Simulation results of 3x IMBC (a) output voltage and input voltage, (b) output voltage at different levels, (c) voltage distribution across capacitors C_1, C_2 and C_3, (d) voltage distribution across capacitors C_{21}, C_{31}, C_{22} and C_{32}.

TABLE 4. Hardware implementation detail.

Components	Value or type	No. of components
Input voltage/output voltage	12V/120V	-
Switch (S_1 and S_2)	IRF540 (0.077 ON sate resistance) (2 pcs)	02
Power Diodes	BYQ28E (10 pcs)	10
Power Inductor	150uH (10A current rating)	02
Capacitors	220uF, 100V (7 pcs)	7
Load	144 Ω, 100W	01
Switching Frequency	50kHz	-

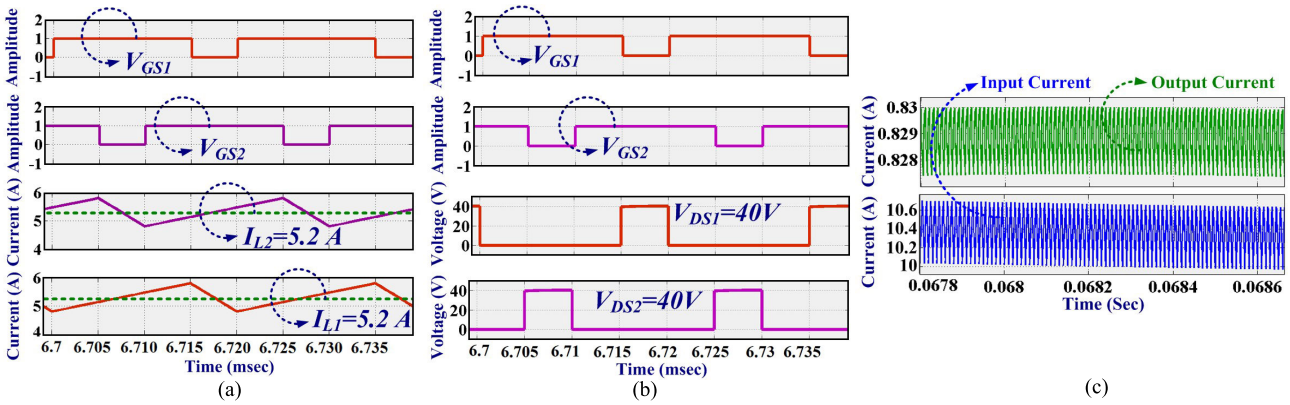

FIGURE 13. Simulation results of 3x IMBC (a) Inductor current waveforms (I_{L1} and I_{L2}) with gate pulse of switches (V_{GS1} and V_{GS2}) (b) Voltage stress across switches (V_{DS1} and V_{DS2}), (c) Input and output current ripples.

across capacitor C_1, C_2, and C_3 are 40.13V, 40.09V, and 40.05V, respectively. The voltage across multiplier capacitors C_{21}, C_{31}, and C_{22}, C_{32} is shown in Fig. 14(d) and Fig. 14(e), respectively. The obtained voltage across capacitor C_{21}, C_{31}, C_{22}, and C_{32} is 40.07V, 40.05V, 40.09V, and 40.08V, respectively. Based on the obtained results, it is clear that voltage

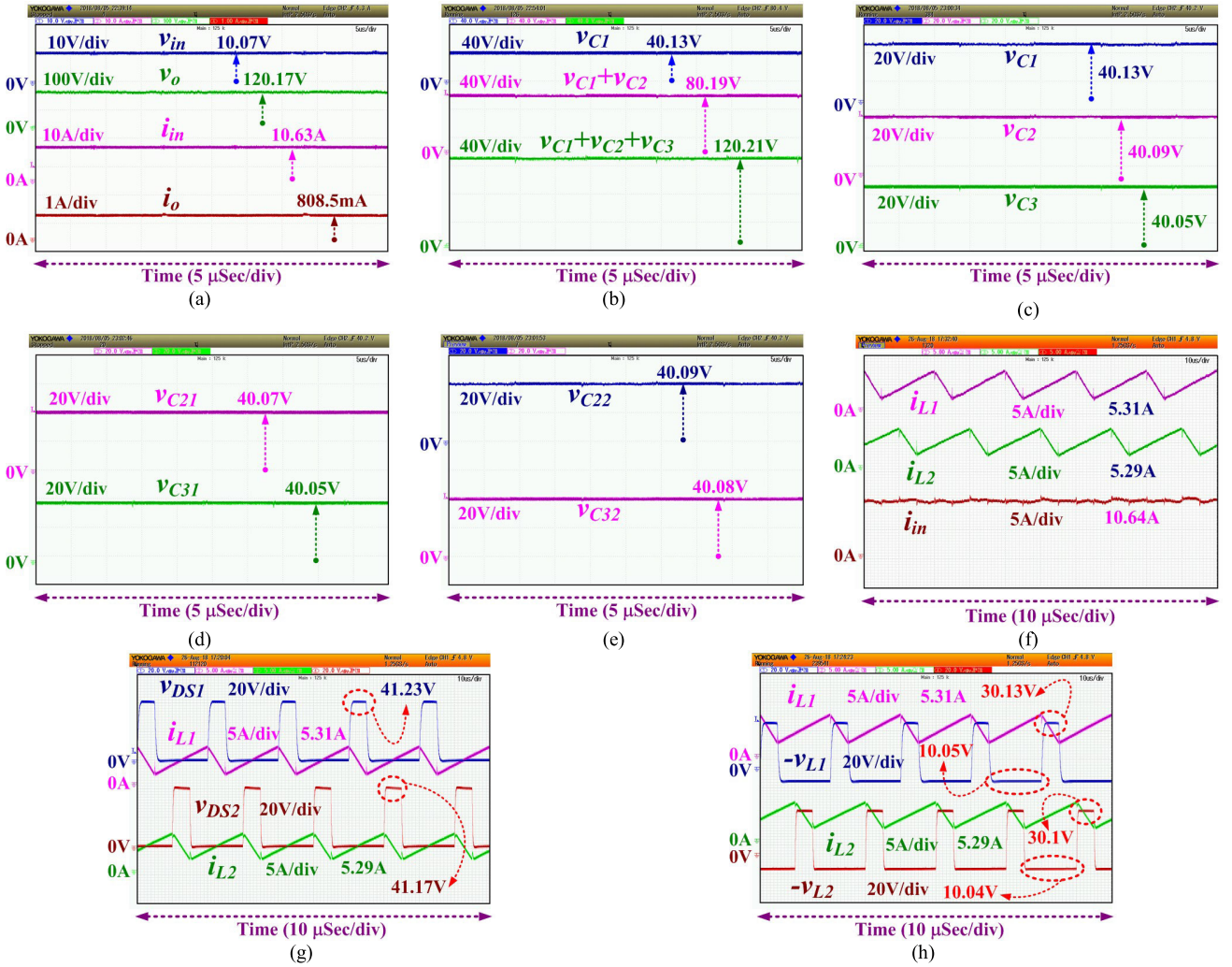

FIGURE 14. Experimental results of 3x IMBC (a) Top to bottom: input voltage (v_{in}), output voltage (v_o), input current (i_{in}), output current (i_o) (b) Top to bottom: level 1 voltage (v_{C1}), Level 2 voltage ($v_{C1}+v_{C2}$), Level 3 voltage ($v_{C1}+v_{C2}+v_{C3}$), (c) Top to bottom: voltage across capacitor C_1 (v_{C1}), voltage across capacitor C_2 (v_{C2}), voltage across capacitor C_3 (v_{C3}), (d) Top to bottom: voltage across capacitor C_{21} (v_{C21}), voltage across capacitor C_{31} (v_{C31}), (e) Top to bottom: voltage across capacitor C_{22} (v_{C22}), voltage across capacitor C_{32} (v_{C32}), (f) Top to bottom: Inductor currents (i_{L1} and i_{L2}) and input current (i_{in}) (g) Top to bottom: voltage across switch S_1 (v_{DS1}), inductor L_1 current (i_{L1}), voltage across switch S_2 (v_{DS2}), inductor L_2 current (i_{L2}), (h) Top to bottom: inductor L_1 current (i_{L1}),), inductor L_1 voltage (v_{L1}), inductor L_2 current (i_{L2}),), inductor L_2 voltage (v_{L2}).

distributions in all the capacitors are equal, and the magnitude is equal to the voltage at the first level of the converter. Fig. 14(f) shows the waveform of inductor current (i_{L1}, i_{L2}) and input current (i_{in}). Noted that both the inductor current are same, but shifted by 180°. The ripple at the input side is nearly cancelled, and 930mA ripple observed in the input current (i_{in}). Confirmed that if both the switches operated at 50% duty cycle, then the ripples in the inductor current is zero. Fig. 14(g) shows the drain to source voltage waveform of switches S_1 and S_2 (v_{DS1} and v_{DS2}). During OFF state of the respective switch, observed that voltage v_{DS1} and v_{DS2} are 41.23V and 41.17V, respectively. Seen that the inductor L_1 and L_2 are charging and discharging when switches S_1 and S_2 turned ON and OFF, respectively. Fig. 14(h) shows the waveform of inductor L_1 and L_2 voltage and current. Observed that the inductor L_1 voltage (v_{L1}) during charging and discharging is 10.05V and 30.13V, respectively. Also, observed that the inductor L_2 voltage (v_{L2}) during charging and discharging is 10.04V and 30.1V, respectively. It is clear that the magnitude of both the inductor L_1 and L_2 voltage waveform the same but shifted by 180°.

The performance of the designed converter also tested under the perturbation from the input side, load side and output voltage reference. Note: State-space modelling skipped from the article; however, the results discussed. Fig. 15(a) shows the waveform of input voltage (v_{in}), inductor L_1 current (i_{L1}), output voltage (v_o) and output current (i_o) when power is abruptly changed from 100W to 120W and 120W to 100W. Fig. 15(b) shows the waveform of the drain to source switch S_1 voltage (v_{DS1}), inductor L_1 current (i_{L1}), output voltage (v_o) and output current (i_o) when power is abruptly changed from 100W to 120W and 120W to 100W.

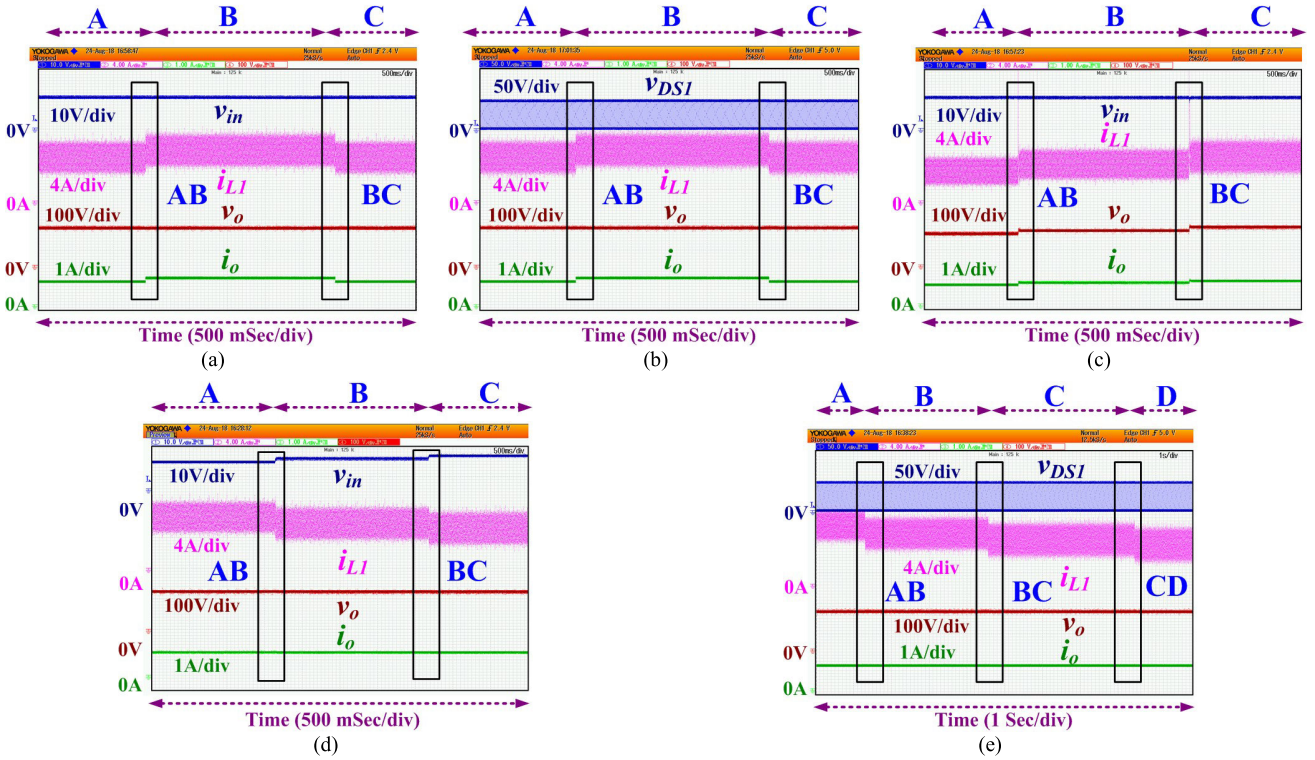

FIGURE 15. Experiment results of 3x IMBC (a) Top to bottom: input voltage (v_{in}), inductor L_1 currents (i_{L1}), output voltage (v_o), output current (i_o) [A, C: Power 100W, B: power 120W, AB: change in power 100 to 120W, BC: change in power 120 to 100W], (b) Top to bottom: voltage across switch S_1 (v_{DS1}), inductor L_1 currents (i_{L1}), output voltage (v_o), and output current (i_o) [A, C: Power 100W, B: power 120W, AB: change in power 100 to 120W, BC: change in power 120 to 100W], (c) Top to bottom: input voltage (v_{in}), inductor L_1 currents (i_{L1}), output voltage (v_o), output current (i_o) [A: output voltage 100V, B: Output voltage 110V, C: Output voltage 120V, AB: change in output voltage 100 to 110 V, BC: change in output voltage 110 to 120], (d) Top to bottom: input voltage (v_{in}), inductor L_1 currents (i_{L1}), output voltage (v_o), output current (i_o) [A: input voltage 10V, B: input voltage 12V, C: input voltage 14V, AB: change in input voltage 10 to 12V, BC: change in input voltage 12 to 14V], (e) Top to bottom: voltage across switch S_1 (v_{DS1}), inductor L_1 currents (i_{L1}), output voltage (v_o), output current (i_o) [A: input voltage 8V, B: input voltage 10V, C: input voltage 12V, D: input voltage 14V, AB: change in input voltage 8 to 10V, BC: change in input voltage 10 to 12V, CD: change in input voltage 12 to 14V].

For convenient, the obtained waveforms sectioned in three sections A, B and C. Section A and C are the obtained waveform when the converter operated at 100W, and section B are the obtained waveform when the converter operated at 120W. Highlighted part AB shows the transients when the power of the converter abruptly changed from 100W to 120W. Highlighted part BC shows the transients of the converter when the power of the converter abruptly changed from 120W to 100W. Notably, the output voltage is maintained; even power abruptly changed with constant input voltage (v_{in}). Due to the constant input voltage (v_{in}) and output voltage (v_o), inductor current (i_{L1}) and output current (i_o) are changed to fulfil the demand for power. There is no change in the drain to source switch voltage (v_{DS1}) even power changed 100W to 120W and 120W to 100W because of constant output voltage (v_o).

Fig. 15(c) shows the waveform of input voltage (v_{in}), inductor L_1 current (i_{L1}), output voltage (v_o) and output current (i_o) when output reference voltage (v_{oref}) is abruptly changed from 100V to 110V and 110V to 120V at constant load. For convenient, the obtained waveforms sectioned in three sections A, B and C. Section A, B, and C shows the obtained waveform when converter output reference (v_{oref}) is set to 100V, 110V, and 120V respectively. Highlighted part AB and BC shows the transients when the power of the converter output reference (v_{oref}) is changed from 100V to 110V and 110V to 120V, respectively. Noticed that expected output voltage achieved even there is no change in input voltage (v_{in}). It is interesting to know that to maintain the equal power at the input and output side, inductor current (i_{L1}) and outputs current a changed according to output voltage reference (v_{oref}).

Fig. 15(d) shows the waveform of input voltage (v_{in}), inductor L_1 current (i_{L1}), output voltage (v_o) and output current (i_o) when the input voltage (v_{in}) abruptly changed from 8V to 10V and 10V to 12V. Section A, B, and C shows the obtained waveform when the converter input voltage (v_{in}) set at 8V, 10V, and 12V, respectively. Highlighted part AB and BC shows the transients when input voltage (v_{in}) converter abruptly changed from 8V to 10V and 10V to 12V, respectively. Notably, constant output voltage (v_{oref}) 120V achieved even changed in input voltage (v_{in}). For maintain the equal power at the input and output side, the inductor current is increased or decreased according to input side voltage (v_1).

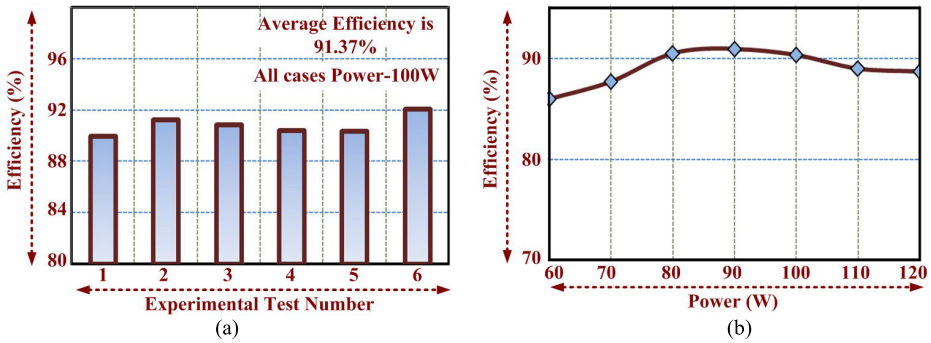

FIGURE 16. Efficiency plots (a) Efficiency during various numbers of experimental tests at 100W, (b) Efficiency versus variation in power level from 60 W to 120W.

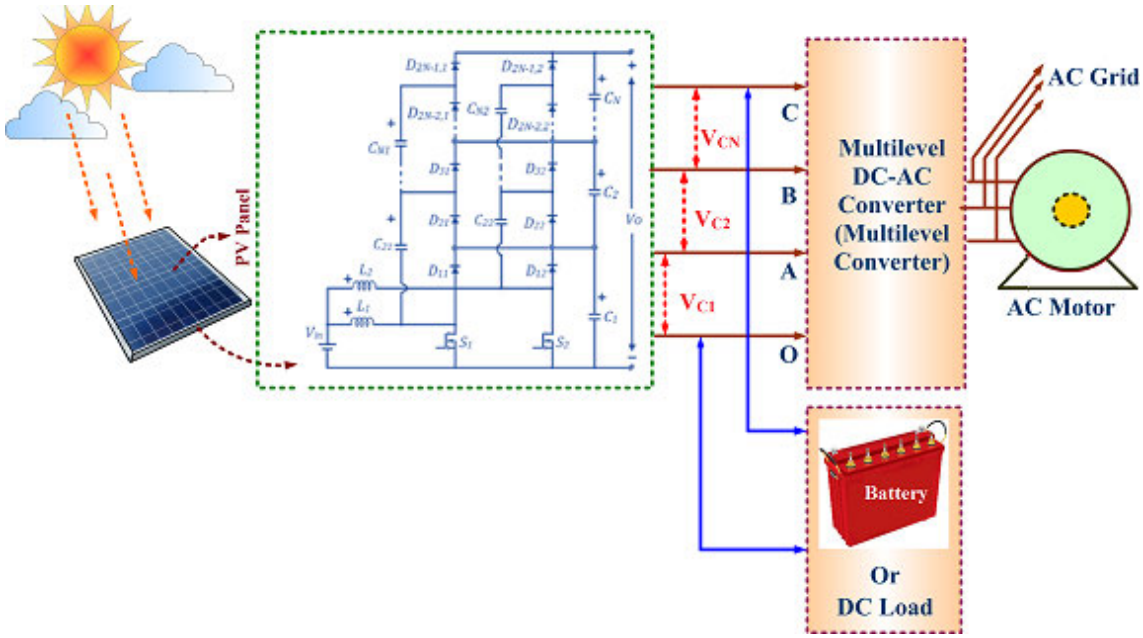

FIGURE 17. Possible application of Nx IMBC in DC-DC-AC system.

Fig. 15(e) shows the waveform of the drain to source switch S_1 voltage (v_{DS1}), inductor L_1 current (i_{L1}), output voltage (v_o) and output current (i_o), when the input voltage (v_{in}) abruptly changed from 8V to 10V, 10V to 12V, and 12 V to 14V. Section A, B, C and D show the obtained waveform when the converter input voltage (v_{in}) set at 8V, 10V, 12V and 14V, respectively. Highlighted part AB, BC and CD shows the transients when input voltage (v_{in}) converter abruptly changed from 8V to 10V, 10V to 12V, and 12V to 14V respectively. Drain to source voltage of switch S_1 (v_{DS1}) and output voltage (v_o) is constant even input voltage changed. For maintain equal power at the input and output side, the inductor current is increased or decreased according to the input voltage (v_1). Various tests conducted, and observed efficiency at 100W shown in Fig. 16(a). It observed that on an average 91.37% efficiency of the 3x IMBC. It noted that the 3x IMBC is slightly improved when compared to the multilevel boost converter (∼89%) at 100W proposed in [38], Interleaved Converter (∼94%) at 150W proposed in [43], and Interleaved converter (∼93.5%) proposed in 150W [44].

The converter is operated at various power levels from 60W to 120W. The observed efficiency at various power levels shown in Fig. 16(b). During power variation, the efficiency of the 3x MBC is in range of 87 to 92%. Majorly, the PV to the grid system, MLI circuitry needs several voltage sources along with several DC-DC converters at the input side. The Nx-IMBC configuration is suitable to feed MLI due to capacitor stack structure at the output side, as shown in Fig. 17. The Nx IMBC provides a solution to feed MLI with single DC-DC converter. Additionally, the Nx-IMBC configuration finds the applications like automotive, renewable appliances, electric vehicles and microgrid were low to high conversion ratio is necessary. Further, it is also possible to increase the phases of the interleaved converter based on the applications,

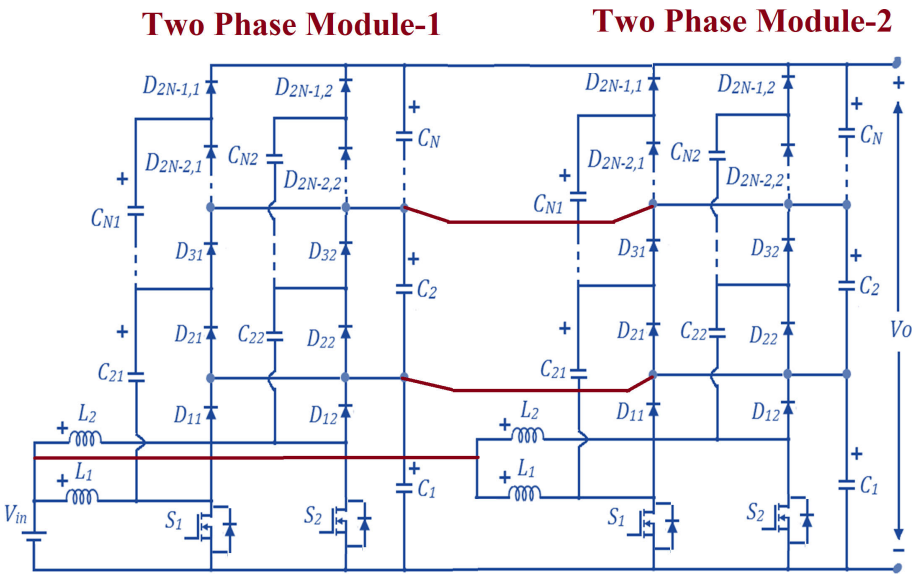

FIGURE 18. Further improvement to increase phases of the interleaved converter (four-phase of Nx IMBC).

e.g. four phases Nx IMBC possible configuration is shown in Fig. 18.

VII. CONCLUSION

The detail investigation and boundary of CCM and DCM with steady-state analysis of hybrid Nx-IMBC are presented. Nx-IMBC converter topology extended the feature of 2x interleaved boost converter and combines the features of the interleaved converter and recently proposed Multilevel Boost Converter (MBC). Nx-IMBC provides higher voltage conversion ratio compared to recently addressed converters with reduced input ripples. The main advantages of Nx IMBC are that in case if one phase of the converter is failing, then also Nx-IMBC provides the same voltage conversion ratio. Additionally, it is also possible to feed Nx-IMBC with two different sources.

Additional merits of the novel converter include:

1. The non-inverting output voltage, and performed as similar as a recently proposed multilevel boost converter.
2. Non-isolated configuration, and avoided bulky transformers.
3. Low input/output current and output voltage ripple.
4. Voltage stress across the switch is low.
5. The number of output side levels raised by adding a diode-capacitor circuit, thereby the voltage conversion ratio increased.

Moreover, the Nx-IMBC converter compared with a new non-isolated DC-DC converter and multilevel converters in terms of switch voltages and number of components. Based on the experimental and simulation result, it is possible to conclude that Nx-IMBC is a promising topology for feeding MLI, photovoltaic applications, automotive appliances, PV drives, and electric vehicles. The experimental shows a good match with simulation results and verifies the validity of the design, feasibility, working of the converter.

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