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A Single-Phase Reduced Component Count Asymmetrical Multilevel Inverter Topology

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***Abstract*—Multilevel inverters (MLIs) have gained wide attention in industry and academia to provide higher voltage levels with lower harmonics, power losses, and cost. This study proposes a new asymmetrical MLI topology with reduced component count (RCC). The proposed topology can be extended in a three-phase structure and both modular and cascaded configurations to generate the required number of voltage levels for high-voltage applications. To minimize the power losses and the voltage stress on the switches, this configuration has the potential to produce negative polarity without an H-bridge configuration, thereby the active switches are reduced to only three switches in the conduction path. Due to the possibility of applying different switching patterns, this paper proposes a new solution by employing particle swarm optimization (PSO) algorithm to determine the optimized DC sources' magnitude. To improve the voltage quality and minimize the total harmonic distortion (THD), the optimal switching angle (OSA) modulation technique is applied to determine the optimum switching angles by PSO algorithm. Moreover, the proposed topology's effectiveness compared to the conventional cascaded H-bridge (CHB) MLI with 15-levels is illustrated by providing comparative results that express fewer power losses. Finally, the proposed topology's feasibility and its optimization approach are validated by a single-phase prototype utilizing 15- and 25-levels.**

***Index Terms*—Multilevel Inverter (MLI), Optimal Switching Angle (OSA), Particle Swarm Optimization (PSO), Reduced Component Count (RCC), Total Harmonic Distortion (THD).**

I. Introduction

MULTILEVEL inverters (MLIs) have been used as a solution for voltage rating limitation of power semiconductors while improving the output power and voltage qualities. With the advent of MLIs, there is a decrease in voltage stress across power switches, switching losses, total harmonic distortion (THD), expensive and bulky filters, electromagnetic interference, and better output characteristics than the conventional two-level inverters. MLIs have important roles in various advanced power conversion applications, like renewable energy systems (standalone and grid-connected), battery energy storage systems, variable frequency drives, electric vehicle drives, uninterruptible power supplies, etc. The most well-known conventional MLIs have three basic topologies, which are diode clamped (DC-MLI), flying capacitor (FC-MLI), and cascaded H-bridge (CHB-MLI) [1], [2].

The conventional MLIs required a high number of components to generate a staircase waveform. Reduced component count (RCC) MLI topologies are a solution for the drawbacks of the conventional MLIs. According to the generated output voltage polarities, RCC-MLIs are classified into two groups. The first group is a combination of the main structure and a series H-bridge unit, where the main section generates output voltage steps with positive polarity. On the other hand, using the H-bridge section allows for generating the negative voltage polarity [3]–[5]. The second group is RCC-MLIs with the main structure capable of providing both the positive and negative polarities [6]–[9]. The second group suits the most low- and medium-voltage applications, due to the lower voltage stress on the H-bridge switches that narrows down the applicability in high-voltage applications. In addition to the on-state switches in the main structure, the existence of two on-state switches in the H-bridge section leads to more power losses for the first group [10]. Increasing voltage quality by multiple DC sources leads to two definitions of symmetrical (equal) and asymmetrical (unequal) DC sources presented in the literature. To obtain higher levels for asymmetrical MLIs, some methods like binary, trinary, and other algorithms are available [11]–[13]. The MLI topology proposed in [14] has lower conduction losses than the CHB-MLI. Further, the numbers of switching patterns for different current paths do not increase at high-voltage levels. The MLIs proposed in [15], [16] are asymmetrical, which have the disadvantage of high total blocking voltage (TBV) due to their H-bridge sections. An abundance of switching patterns may increase reliability and fault-tolerance capability, change the current path, and keep the system normal after a fault occurs [17], [18]. Some RCC-MLI topologies have been briefly reviewed in [19]–[27].

Besides different topologies and configurations of power switches, different modulation strategies have been introduced as well. Some of them are more usable in industrial applications like selective harmonic elimination (SHE), space vector modulation (SVM), optimal switching angle (OSA) modulation at low frequencies [28]–[33], which can be applied with artificial intelligence algorithms to optimize the output voltage/current. It is an excellent solution to decrease the

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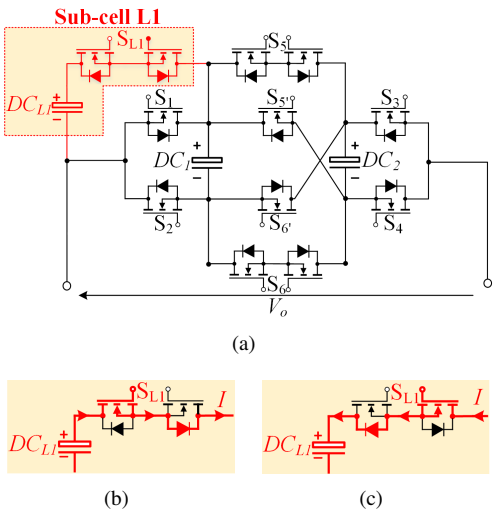


Fig. 1. Circuit diagram of the proposed single-phase MLI topology (a) 15-level inverter of the generalized proposed topology with a sub-cell (L1), (b) and (c) Current directions in the sub-cell (L1).

control of computational burden [34]. Among these modulation strategies, fundamental-frequency modulation methods can provide better performance than high-frequency methods. Lower switching losses and more control on THD, and the amplitudes of output harmonics are the benefits of these methods.

This paper proposes a new asymmetrical reduced component count MLI topology with multiple DC sources and the ability to generate both the positive and negative voltage levels without the help of an additional series H-bridge section. The proposed MLI topology reduces the number of on-state switches to three active switches in each module's current loop to decrease the power losses and increase the total efficiency. It can be extended easily in a three-phase structure and both modular and cascaded connections too. By utilizing the PSO algorithm, an optimization procedure is proposed to determine the optimized voltage magnitudes of DC sources instead of using the standard algorithms (binary, trinary, and other algorithms) and mathematical operations. The paper is organized as follows: Section II presents the proposed MLI topology and its operating principles, Section III illustrates the employed OSA modulation strategy, Section IV discusses loss calculations in the proposed and the conventional CHB-MLI, Section V depicts a comprehensive comparative study, Section VI is focused on simulation and experimental results of the proposed MLI topology prototype, and finally, Section VII draws the conclusion.

II. Operating Principles of The Proposed MLI

A. Circuit Configuration

A general schematic of the proposed topology is presented in Fig. 1(a), which consists of the main structure and a sub-cell. This configuration is a single-phase topology and is based on unequal DC sources. The proposed configuration can overcome the drawback of power losses and the cost of modular extension better in comparison with the topology proposed in [14]. By adding a sub-cell of one bidirectional power switches and one DC source, it is possible to increase the number of voltage levels. Fig. 1(b) and (c) show how the bidirectional switch in series with the DC source (DC_{L1}) can prevent short circuits by blocking current polarities. In this arrangement, there are only three active power semiconductors to generate the desired voltage level. So, the main advantage of the proposed topology is a reduction of conduction losses. The other benefits of the proposed configuration can be expressed as a reduction in component count that leading a decrease in control complexity and cost since it has no bulky passive elements like capacitors to be utilized to maintain the voltage levels. A 15-level inverter can be achieved by adding a sub-cell to the main structure. So, the structure consists of three voltage sources (DC_1, DC_2, and DC_{L1}), six unidirectional switches (S_1, S_2, S_3, S_4, $S_{5'}$, and $S_{6'}$) and three bidirectional switches (S_{L1}, S_5, and S_6). Furthermore, combining two sub-cells would result in a 25-level inverter. Assuming that the number of DC sources is n_{DC}, the number of required power switches N_{SW} and gate-drivers N_{Driver} can be defined for the proposed topology for $n_{DC} \geq 3$ as follows:

$$N_{SW} = 2n_{DC} + 6 \quad (1)$$

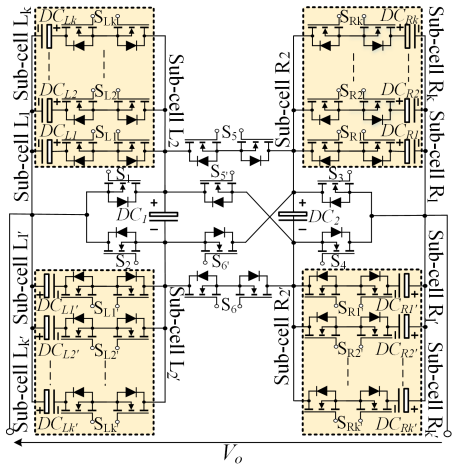
$$N_{Driver} = n_{DC} + 6 \quad (2)$$

TABLE I
Switching States of the Proposed 15-Level Inverter in Fig. 1

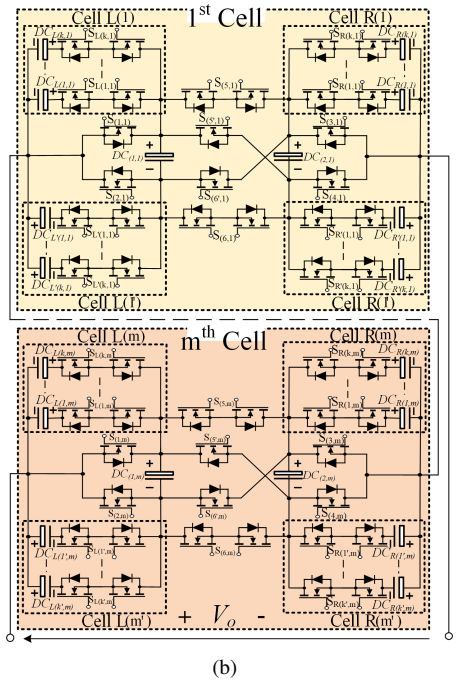
State	S_{L1}	S_1	S_2	S_3	S_4	S_5	$S_{5'}$	S_6	$S_{6'}$	V_{out}	Voltage Level
1	0	1	0	0	1	0	0	0	1	$+DC_1 + DC_2$	$+7V_{DC}$
2	1	0	0	0	1	0	0	0	1	$+DC_1 + DC_2 - DC_{L1}$	$+6V_{DC}$
3	0	1	0	0	1	1	0	0	0	$+DC_2$	$+5V_{DC}$
	0	0	1	0	1	0	0	0	1		
4	1	0	0	0	1	1	0	0	0	$+DC_2 - DC_{L1}$	$+4V_{DC}$
5	0	0	1	0	1	1	0	0	0	$-DC_1 + DC_2$	$+3V_{DC}$
6	0	1	0	1	0	0	0	0	1	$+DC_1$	$+2V_{DC}$
	0	1	0	0	1	0	0	1	0		
7	1	0	0	1	0	0	0	0	1	$+DC_1 - DC_{L1}$	$+V_{DC}$
	1	0	0	0	1	0	0	1	0		
8	0	1	0	1	0	1	0	0	0	0	0
	0	1	0	0	1	0	1	0	0		
	0	0	1	0	1	0	0	1	0		
9	0	0	1	1	0	0	0	0	1	$-DC_{L1}$	$-V_{DC}$
	1	0	0	1	0	1	0	0	0		
	1	0	0	0	1	0	1	0	0		
10	0	0	1	0	1	0	1	0	0	$-DC_1$	$-2V_{DC}$
	0	0	1	1	0	1	0	0	0		
11	0	1	0	1	0	0	0	1	0	$+DC_1 - DC_2$	$-3V_{DC}$
12	1	0	0	1	0	0	0	1	0	$+DC_1 - DC_2 - DC_{L1}$	$-4V_{DC}$
13	0	0	1	1	0	0	0	1	0	$-DC_2$	$-5V_{DC}$
	0	1	0	1	0	0	1	0	0		
14	1	0	0	1	0	0	1	0	0	$-DC_2 - DC_1$	$-6V_{DC}$
15	0	0	1	1	0	0	1	0	0	$-DC_1 - DC_2$	$-7V_{DC}$

B. Operating Principles

The possible switching states of the proposed 15-level inverter are listed in Table I. To achieve all the possible voltage levels (positive and negative), the DC sources' magnitudes should be considered as $DC_1 = 2V_{DC}$, $DC_2 = 5V_{DC}$, and $DC_{L1} = V_{DC}$. According to Table I, there are twenty-four switching patterns to produce 15 steps in the output voltage. A large number of switching patterns lead to numerous available current paths. In all cases for the modular extension, only



(a)



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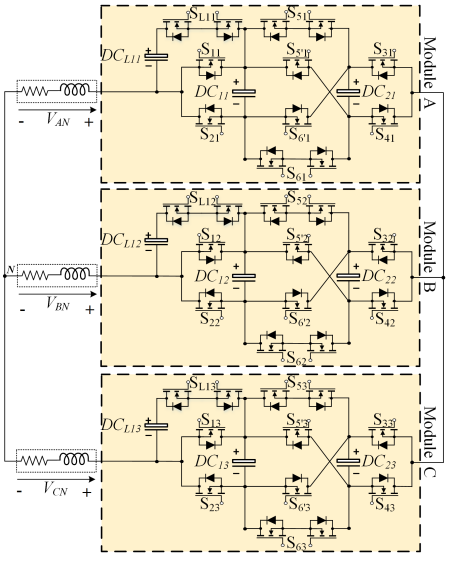


(c)

Fig. 2. Proposed MLI topology, (a) Single-phase modular extension, (b) Cascaded extension, and (c) Three-phase configuration.

three on-state power switches are used as conducting routes to generate any voltage levels.

C. Module Extension

One of the merits of the proposed MLI structure is its capability to be extended in modular and cascaded connections to generate higher voltage levels. This particular feature has many benefits, and it is instrumental in high voltage applications, where there are many limitations on blocking voltage of each switch. A modular extension is provided easily by adding a sub-cell comprised of one bidirectional switch and one DC source. By adding a sub-cell to the mentioned structure in Fig. 1, it is possible to generate ten more levels in the output voltage and provide a 25-levels inverter. The cascaded extension can be provided by a series connection of these modules. These sub-cells can be added in parallel with side switches (S_1, S_2, S_3, and S_4) to generate more voltage levels. These sub-cells are labeled as (L, L', R, and R'). Fig. 2(a) presents a modular extension of the proposed MLI topology. This structure is synthesized by connecting more sub-cells in parallel to produce more voltage levels. At each module, only three switches are required to conduct the current and generate any voltage level. The topology followed in Fig. 2(b) is known as a cascaded extension comprising m series cells. Each of the cells in modular configuration consists of k number of sub-cells ($1 < 2 < ... < j < ... < k$). The switches ($S_1$, S_2, S_{Lk}, and $S_{Lk'}$) are on the left side, the switches (S_3, S_4, S_{Rk}, and $S_{Rk'}$) are on the right side, and (S_5, $S_{5'}$, S_6, and $S_{6'}$) are in the center. They will not be turned on at the same time to avoid short circuit of (DC_1, DC_{Lk}, and $DC_{Lk'}$), (DC_2, DC_{Rk}, and $DC_{Rk'}$), and (DC_1 and DC_2) respectively. Likewise, an extension of the proposed MLI topology is possible for a three-phase configuration. In Fig. 2(c), a combination of three single-phase 15-level inverters (module A, module B, and module C) of the proposed topology makes a three-phase MLI that are in series with loads in each phase. The same as single-phase, it is possible to derive both modular and cascaded extensions of the three-phase configuration too.

D. Blocking Voltage and DC Voltage Sources Magnitude

In asymmetrical MLIs, the DC sources' magnitudes are considered different to produce more output voltage levels than the symmetrical MLIs. A comprehensive mathematical formulation is provided for the standard algorithms to determine the optimum DC sources' magnitudes in many publications. A maximum voltage magnitude that a switch has to block in off-state is defined as the switch's blocking voltage. The sum of these voltage magnitudes of each switch in a converter is called TBV. This paper proposes a new solution to form the largest combination of input DC sources to achieve the maximum voltage levels rather than employing mathematical formulation or calculation algorithms. This approach will reduce TBV significantly. Table II presents the blocking voltage of switches for a 15-level inverter. The value of each switch's blocking voltage is considered a dependent and absolute parameter due to the employment of DC sources magnitude in both the positive and negative polarities arrangement for the optimization

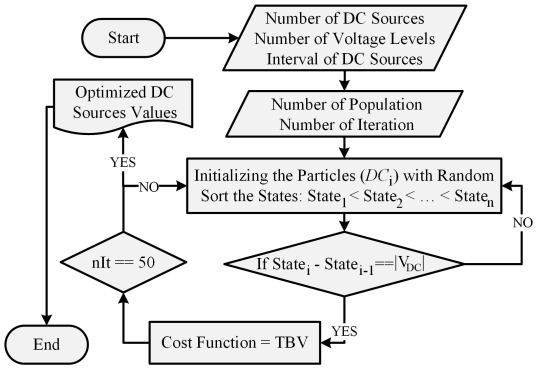


Fig. 3. Flow chart of the utilized optimization procedure for obtaining the optimized DC sources values using particle swarm optimization.

algorithm. For the proposed topology with modular extension, TBV of the individual switches can be expressed as:

$$V_{S1} = max(DC_{Lk}, DC_1, (DC_1 - DC_{Lk'})) \tag{3}$$

$$V_{S2} = max(DC_{Lk'}, DC_1, (DC_1 - DC_{Lk})) \tag{4}$$

$$V_{S3} = max(DC_{Rk}, DC_2, (DC_2 - DC_{Rk'})) \tag{5}$$

$$V_{S4} = max(DC_{Rk'}, DC_2, (DC_2 - DC_{Rk})) \tag{6}$$

$$V_{S5} = V_{S6} = max(DC_1, DC_2) \tag{7}$$

$$V_{S5'} = V_{S6'} = DC_1 + DC_2 \tag{8}$$

$$V_{SLk} = max(DC_{Lk}, DC_{Lk} - DC_1, DC_{Lk} - DC_{Lj}, DC_{Lk} + DC_{Lk'}) \tag{9}$$

$$V_{SLk'} = max(DC_{Lk'}, DC_{Lk'} - DC_1, DC_{Lk'} - D_{Lj'}, DC_{Lk'} + DC_{Lk}) \tag{10}$$

$$V_{SRk} = max(DC_{Rk}, DC_{Rk} - DC_2, DC_{Rk} - DC_{Rj}, DC_{Rk} + DC_{Rk'}) \tag{11}$$

$$V_{SRk'} = max(DC_{Rk'}, DC_{Rk'} - DC_2, DC_{Rk'} - DC_{Rj'}, DC_{Rk'} + DC_{Rk}). \tag{12}$$

DC sources are considered variable in both positive and negative ranges. In this way, the maximum value of TBV can be calculated for each switch. Finally, the TBV of the whole system can be calculated as follows:

TABLE II
SWITCH BLOCKING VOLTAGE OF THE PROPOSED 15-LEVEL INVERTER

Switch	Blocking Voltage Magnitude
S_1	$max(DC_{L1}, DC_1, DC_1 - DC_{L1})$
S_2	DC_1
S_3	DC_2
S_4	DC_2
S_5	$max(DC_1, DC_2)$
$S_{5'}$	$DC_1 + DC_2$
S_6	$max(DC_1, DC_2)$
$S_{6'}$	$DC_1 + DC_2$
S_{L1}	$max(DC_{L1}, DC_{L1} - DC_1)$

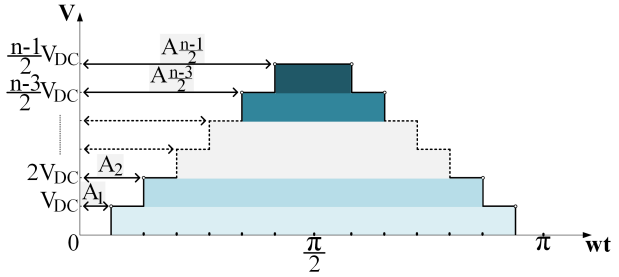


Fig. 4. Voltage waveform and switching angles of each level for an n-level inverter.

$$TBV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + 2V_{S5} + 2V_{S5'} + V_{SLi} + V_{SRi} + V_{SLi'} + V_{SRi'}. \tag{13}$$

Fig. 3 presents the optimization procedure to determine the magnitudes of the DC sources. At the beginning of this flowchart, the number of DC sources and the maximum number of the voltage level states are given. The maximum number of the possible voltage levels state can be obtained by considering the proposed topology's available arrangements. After that, the definition of the DC sources' intervals is the next step. For instance, intervals of the proposed n-level inverter are equal to $[\frac{-n}{2}, \frac{+n}{2}]$, and n is the number of voltage levels. The absolute value of each switch's blocking voltage for the 15-level proposed configuration is considered in Table II. So, all the states of the DC sources' arrangement can be analyzed by keeping both the positive and the negative values (different polarities). According to the obtained results, iteration and population numbers are considered 50, suitable for this optimization. Each DC sources' arrangement is known as a state to achieve the proposed topology's desired output voltage. The output voltage value organizes all the switching states' arrangements (Table I). Suppose the difference between consecutive levels will not be equal to $|V_{DC}|$ (the nominal DC voltage), THD increases, and consequently, the quality of the output decreases. So, this constraint should be observed for all the states. This optimization procedure leads to a reduction in TBV, which is considered as a cost function for this algorithm. At the end of this algorithm, the DC sources' optimized magnitudes are obtained for the proposed topology. Different MLI topologies can employ the optimization procedure of the proposed algorithm.

III. MODULATION STRATEGY

In this paper, the optimal switching angle modulation technique is used to order the power switches. This technique works based on selecting the optimized switching angles to improve the output voltage quality. By using this technique, a reduction in switching losses and THD are achieved. Fig. 4 presents the selected switching angles at the first quarter cycle of the voltage waveform to make a symmetrical configuration with off-line calculations for an n-level inverter. In this way, there is no DC terms and even harmonics in the output voltage. The output voltage function based on Fourier analysis is as follows:

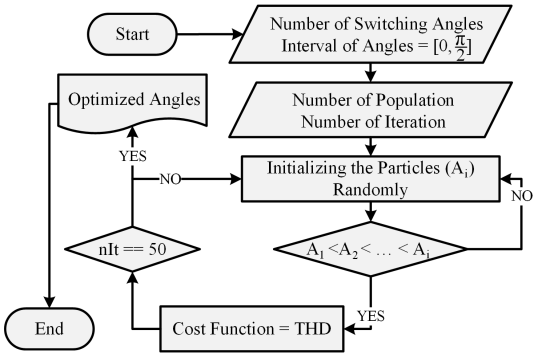


Fig. 5. Flow chart of the utilized optimization procedure to find the optimized angles using particle swarm optimization.

$$\begin{cases} V_{L1} = \sum\limits_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_1) \\ V_{L2} = \sum\limits_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_2) \\ ... \\ V_{L\frac{(n-1)}{2}} = \sum\limits_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_{\frac{(n-1)}{2}}) \end{cases} \tag{14}$$

$$V_{out} = V_{L1} + V_{L2} + ... + V_{L\frac{(n-1)}{2}} \tag{15}$$

The vector of the phase voltage is V_{out}, V_{Li} is the voltage for i^{th} level, and $A_1°$, $A_2°$, and $A°_{(\frac{n-1}{2})}$ are the switching angles of first, second and $(\frac{n-1}{2})^{th}$ voltage levels respectively.

The value's difference of two consecutive levels is equal to $|V_{DC}|$. The optimization procedure of the mentioned modulation technique is presented in Fig. 5. Particle swarm optimization (PSO) algorithm is employed for this optimization procedure to minimize THD by selecting optimized switching angles.

At the beginning of this algorithm, the number of switching angles is determined based on the number of output voltage steps. This parameter is equal to $\frac{n-1}{2}$ (there is one angle at each level, as shown in Fig. 4). Intervals of the switching angles are considered $[0\ \ \frac{\pi}{2}]$. The number of populations n_{POP} and the number of iterations n_{It} are equal to 50. The constraints of switching angles value are $A_1°<A_2°<...<A_n°$, which defines the condition for calculation of a Fourier series and consequent THD evaluation. The THD is considered as a cost function, and the mentioned algorithm has to minimize it as well. There are twelve switching angles for the proposed 25-level inverter. The optimized switching angles by this technique are presented in Table III (the angles are in degrees).

TABLE III
OPTIMIZED SWITCHING ANGLES FOR 25-LEVEL INVERTER

Angle(degree)	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	THD_V
OSA (PSO)	2.5	7.2	11.7	16.8	21.8	26.8	32.0	38.0	44.5	51.2	59.7	71.0	3.2%
Ref [13]	2.6	5.4	12.1	17.1	21.7	26.9	32.6	38.5	44.8	51.9	60.7	72.7	3.4%

The obtained THD from the OSA modulation technique in this study is better than the obtained optimum results in [13].

IV. LOSS CALCULATIONS

Three groups of power losses exist in power converters: conduction, switching and blocking state (leakage) losses. Blocking state losses are neglected because they are small [10]. The prototype of the proposed MLI topology consists of power MOSFETs. The conduction losses for these switches can be calculated using a MOSFET-approximation with the drain-source on-state resistance $(R_{DS,on})$. MOSFET conduction losses $(P_{c,M})$ are the integration of the instantaneous power losses over a switching period (T_{sw}), which gives an average value, as follows:

$$P_{c,M} = \frac{1}{T_{sw}} \int_0^{T_{sw}} R_{DS,on}.i(t)^2_{DS}.dt = R_{DS,on}.I^2_{DS,rms} \tag{16}$$

where i_{DS} is the drain-source current and $I_{DS,rms}$ is the root mean square value of the MOSFET on-state current.

The anti-parallel diode can be estimated using a diode-approximation with a series connection of DC voltage source that represents the diode on-state in zero-current voltage. In addition, a diode on-state resistance (R_D) is estimated to calculate the anti-parallel diode conduction losses $(P_{c,D})$, as follows:

$$\begin{aligned} P_{c,D} &= \frac{1}{T_{sw}} \int_0^{T_{sw}} (V_D + R_D.i_F(t)).i_F(t).dt \\ &= V_D.I_{F,avg} + R_D.I^2_{F,rms} \end{aligned} \tag{17}$$

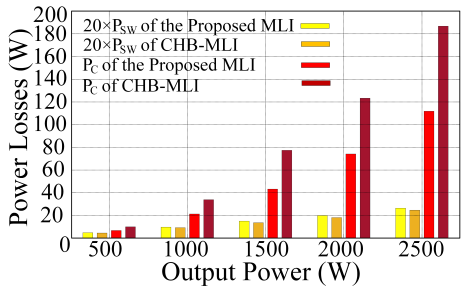
where V_D is diode forward voltage, i_F is current through the diode, $I_{F,avg}$ is the average value of diode current, and $I_{F,rms}$ is the root mean square value of the diode current.

Switching losses consist of turn-on and turn-off switching sequences, which depends upon rise and fall times, the number of active switches, and switching frequency. The switching losses are analyzed for a typical switch, and then it will be extended for the proposed topology. The switching energy losses during the turn-on state in the MOSFET $(E_{on,M})$ with taking the reverse recovery of the free-wheeling diode into account can be calculated as follows:

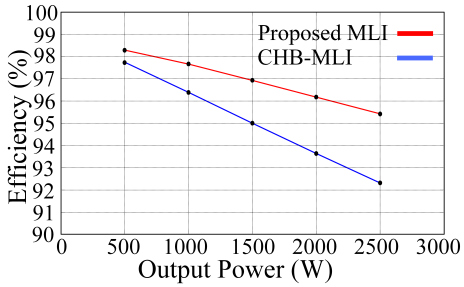
$$\begin{aligned} E_{on,M} &= \int_0^{T_{ri}+T_{fv}} v_{DS}(t).i_{DS}(t).dt \\ &= V_{DS}.I_{DS,on}.\frac{T_{ri}+T_{fv}}{2} + Q_{rr}.V_{DS} \end{aligned} \tag{18}$$

where T_{ri} is the current rise-time of the switch, T_{vf} is the voltage fall-time of the switch, v_{DS} is the drain-source voltage, $I_{DS,on}$ is the drain-source current in on-state and Q_{rr} is the reverse recovery charge. It should be considered that at low switching frequencies the switching losses are very small.

The switching losses during the turn-off state $(E_{off,M})$ is as follows:



(a)



(b)

Fig. 6. Efficiency analysis of the proposed topology and the conventional CHB-MLI topologies with 15-level output voltage, (a) Conduction and switching losses distribution, (b) Simulated efficiency at different output powers.

$$E_{off,M} = \int_0^{T_{rv}+T_{fi}} v_{DS}(t).i_{DS}(t).dt = V_{DS}.I_{DS,off}.\frac{T_{rv}+T_{fi}}{2} \quad (19)$$

where T_{rv} is the voltage rise-time of the switch, T_{fi} is the current fall-time of the switch, and $I_{DS,off}$ is the drain-source current in off-state. Turn-on and turn-off energy of the diode that consists mostly of the reverse-recovery energy is normally neglected.

Finally, power losses and efficiency equations can be calculated as follows:

$$P_{sw} = (E_{off,M} + E_{on,M}).F_{sw} \quad (20)$$

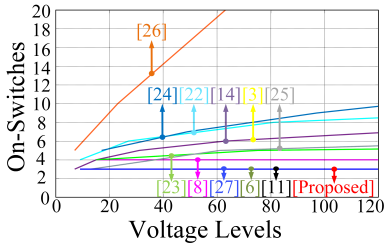
$$P_{loss} = P_{c,M} + P_{c,D} + P_{sw} \quad (21)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}.100\% \quad (22)$$

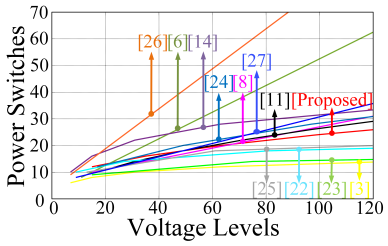
Here P_{sw} is the switching losses, P_{loss} is the total power losses, P_{out} is the output power, and F_{sw} is the fundamental switching frequency. The aforementioned losses are obtained numerically for the proposed MLI topology and CHB-MLI according to the power MOSFETs specification that is presented in Table IV [10].

TABLE IV
UTILIZED POWER MOSFET SPECIFICATIONS

Parameter	Value
$R_{DS,on}$	0.027 Ω
R_D	0.05 Ω
V_D	1.8 V
$T_{ri} \cong T_{rv}$	55 ns
$T_{fi} \cong T_{fv}$	39 ns
Q_{rr}	5 μC
Junction Temperature	25 °C



(a)



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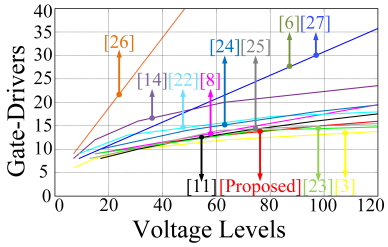
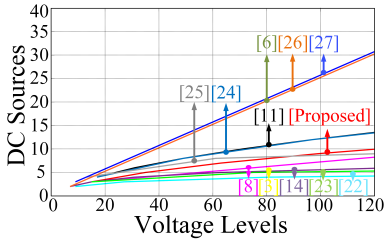


(c)



(d)

Fig. 7. Comparison of different topologies (a) On-state power switches, (b) Power switches, (c) Gate-drivers, (d) DC sources, against the voltage levels.

Table V presents some details of the component count for the proposed topology and the conventional CHB-MLI. In Fig. 6(a), the theoretical calculation of the conduction and the switching losses are depicted for 15-level inverters at different output powers and V_{rms} of the output voltage magnitude is equal to 0.71 pu. The binary manner is used in CHB-MLI topology. Both of these topologies have twelve power switches and three DC sources. In this figure, the switching losses are multiplied by 20 to be observable. It can be seen that conduction losses have the most contribution to the total power loss. In Fig. 6(b), the theoretical efficiency for a 15-level proposed topology and CHB-MLI topology is presented. It can be seen, the proposed MLI topology and CHB-MLI efficiencies are about 98.3% and 97.4% respectively for 500

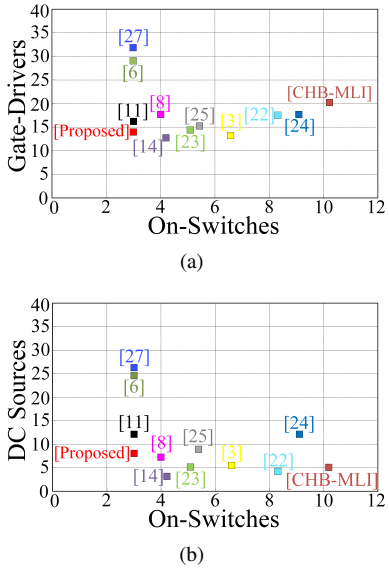


Fig. 8. Comparison of different topologies with the same number of switching patterns (a) Gate-drivers and (b) DC sources, against the on-state power switches.

W output power, and it is about 95.4% and 92.2% respectively for 2.5 kW output power. It is clear, the proposed MLI topology has lower power losses and higher efficiency than the conventional CHB-MLI.

V. Comparison of Topologies

To analyze the proposed topology's effectiveness, various comparisons have been made with the number of output voltage levels, on-state switches, switching patterns, power switches, gate-drivers, and DC sources with recent topologies. In the first section comparing diagrams, four different features are assessed, and Fig. 7 shows the relevant charts. Fig. 7(a) shows a graphical representation of the number of on-state switches versus the voltages levels of the proposed MLI topology and other MLI topologies. It can be observed the number of on-state switches of the proposed topology with a modular extension for any level is equal to three. The references [6] and [11] have the same value as the proposed topology, but reference [8] has four on-state switches. This feature leads to fewer component counts in the current path, and finally, fewer conduction losses. As demonstrated in Fig. 7(b), the proposed topology has fewer power switches against the reference [6] and [14]. Based on Fig. 7(c), the reference [14] has many gate-drivers that consists of isolated DC sources and optocouplers.

TABLE V
Comparison of the Proposed MLI with CHB-MLI [2]

Voltage Level	Components	CHB-MLI	Proposed MLI
15	Power MOSFETs	12	12
	Optocouplers	12	9
	Isolated Aux DC Sources	9	7
	Power DC Sources	3	3
	DC Source Varieties	3	3
	On-State Switches	6	3

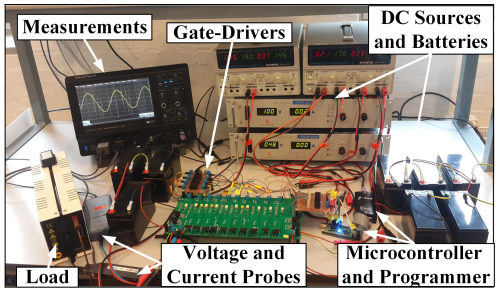


Fig. 9. Laboratory setup for the proposed MLI.

In the proposed topology, bidirectional switches are used that have a common source-emitter. It leads to employing fewer gate-drivers. Fig. 7(d) presents the proposed topology has a reduction in DC sources against [6] and [11] topologies. Reduction in power switches, gate-drivers, and DC sources improves the complexity of control, total cost, volume, and weight.

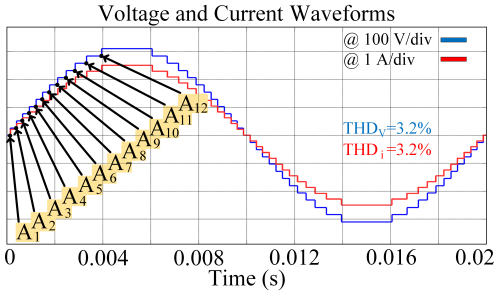
Investigating the number of switching patterns regarding the reliability and the protection point of view is critical when a fault has occurred. The number of gate-drivers and DC sources are compared against the number of on-state power switches in Fig. 8, and the number of switching patterns are equal to 100 for all the topologies. It can be seen the proposed MLI topology has the minimum number of gate-drivers and DC sources against on-state power switches simultaneously, with the same number of switching patterns, which can change the current path. The number of isolated auxiliary power sources presented in Table V justifies the proposed topology's additional advantage. In the case of 15 voltage levels, the proposed MLI contains 12 power MOSFETs. At the same time, it requires only seven auxiliary isolated DC sources for the drivers' power supply. These results from the fact that ten out of twelve MOSFETs feature common-source connections in five pairs, as could be appreciated from Fig. 1. Moreover, these pairs of MOSFETs could be driven using a single 2-channel low-side driver to reduce converter realization complexity. These features reduce the number and cost of components in auxiliary circuits of the proposed MLI.

VI. Simulation and Experimental Results

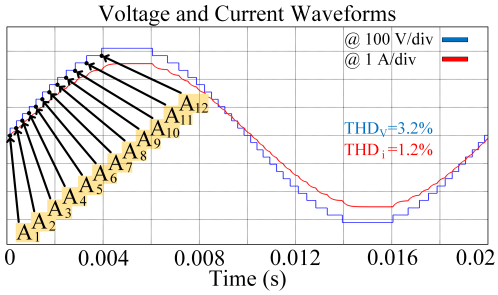
To demonstrate the proposed topology, it has been implemented in MATLAB/SIMULINK as well as the prototype.

TABLE VI
Hardware Specifications

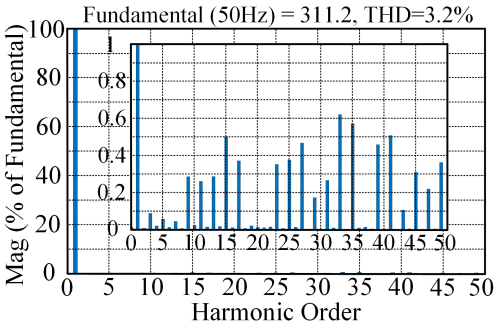
Components	Specifications
Microcontroller	ARM (NXP-LPC 1768)
MOSFET	IRFP460
Optocoupler	TLP250
DC/DC Converter	R12P22005D
Battery	RS PRO, 12V Lead, 7Ah
Input Voltage (15-Level)	DC_1= 84V, DC_2= 210V, DC_{L1}= 42V
Input Voltage (25-Level)	DC_1= 52V, DC_2= 260V, DC_{L1}= 26V, $DC_{R_1'}$= 130V
Load	100Ω <R< 500Ω
Output Frequency	50Hz



(a)



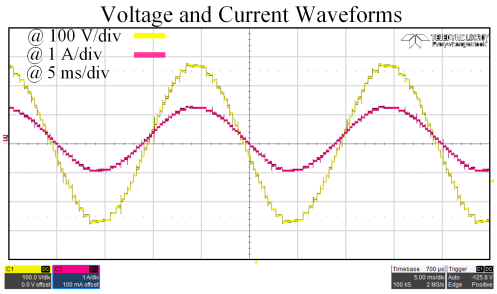
(b)



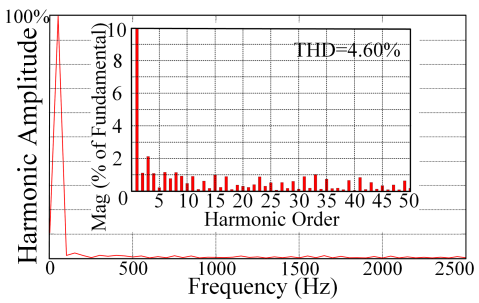
(c)

Fig. 10. Simulation results of 25-level MLI with optimized switching angles, (a) Output voltage and current waveforms for resistance load, (b) Output voltage and current waveforms for resistive-inductor load, (c) Simulated spectrum of low order harmonics in the output voltage.

Specifications of the hardware prototype are given in Table VI. In this experiment, batteries are utilized as bidirectional DC sources to generate output voltage levels. ARM microcontroller (NXP-LPC 1768) is employed to generate the switching sequences. The experimental setup of the MLI topology prototype is depicted in Fig. 9. Simulation results of the proposed topology using a 25-level inverter with optimized twelve switching angles based on Table III are presented in Fig. 10. The stepped waveforms of the output voltage and current are presented in Fig. 10(a) for a resistance load equal to 120 Ω. Both the THD_V and THD_i of the output are equal to 3.2% and V_{rms} is equal to 0.72 pu. In Fig. 10(b), the stepped waveforms of the output voltage and current for a resistive-inductor load that comprises 120 Ω and 20 mH are presented. The THD_V and THD_i of the output are equal to 3.2% and 1.2% respectively, and V_{rms} is equal to 0.72 pu too. Also, the harmonic spectrum of the output voltage is presented in Fig. 10(c). The ratio of the value for the DC voltage sources of the proposed 25-level are $DC_1 = 2V_{DC}$, $DC_2 = 10V_{DC}$, $DC_{L1} = V_{DC}$, and $DC_{R1'} = 5V_{DC}$. Various values are

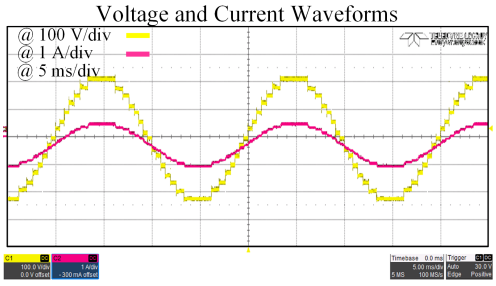


(a)

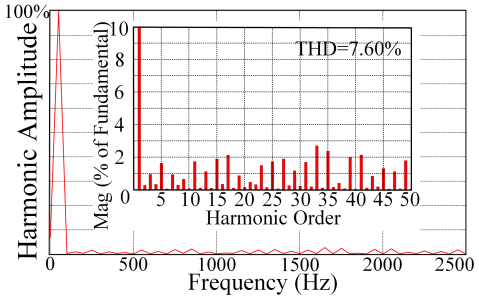


(b)

Fig. 11. Experimental results of the proposed 25-level inverter, (a) Output voltage and current waveforms, (b) Harmonic spectrum.



(a)

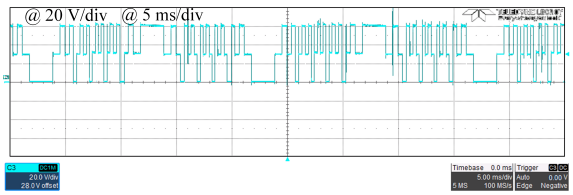


(b)

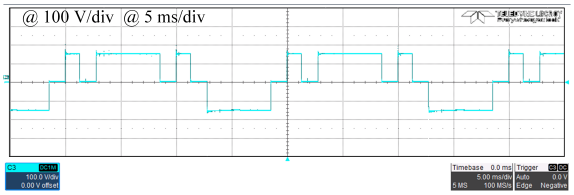
Fig. 12. Experimental results of the proposed 15-level inverter, (a) Output voltage and current waveforms, (b) Harmonic spectrum.

obtained for the ratio of the DC sources. These values are achieved using the optimization procedure given in Fig. 3. The switching angles of both the simulation and experimental are optimized, as shown in Table III.

Fig. 11(a) and (b) show experimental results of the output voltage and current waveforms with resistance load for 25-level proposed MLI. In Fig. 11(a), V_{rms} is equal to 0.72 pu, and the nominal DC voltage $|V_{DC}|$ of the output voltage



(a)



(b)

Fig. 13. Experimental waveforms of voltage across switches for 25-level inverter, (a) S_{L1}, (b) $S_{R1'}$.

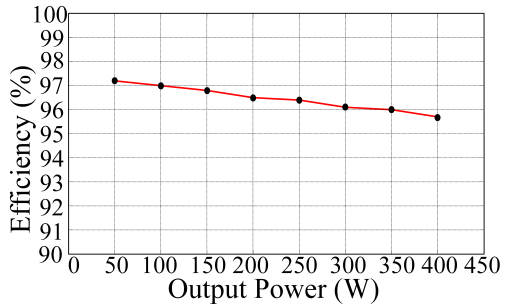


Fig. 14. Measured efficiency of the proposed 15-level inverter topology.

should have the same amplitude that is equal to 26 V. Two sub-cells are considered for the proposed 25-level inverter. The harmonic spectrum of the output voltage is presented in Fig. 11(b). Details of the harmonic orders and their magnitudes are obtained using an oscilloscope WaveSurfer 3024 (the output voltage waveform is sampled with 100 MS/s ratio). The obtained samples were transferred to MATLAB software to form the output waveform and measure the harmonic orders.

Fig. 12(a) and (b) present the experimental results of the obtained 15-level output voltage and current waveforms with resistivity load. In Fig. 12(a), the nominal DC voltage $|V_{DC}|$ of the output voltage has the same amplitude of 42 V, and V_{rms} is equal to 0.71 pu. Only one sub-cell is considered for the proposed 15-level inverter. The harmonic spectrum of the output voltage is presented in Fig. 12(b). Due to the time-delays of components, some even harmonic orders are generated in the harmonic spectrum for both 15- and 25-level inverters.

Measured blocking voltages of S_{L1} and $S_{R1'}$ bidirectional switches for the proposed 25-level inverter are shown in Fig. 13. These bidirectional switches avoid short circuit of the DC sources. Fig. 14 shows the experimental efficiency versus the output power for the proposed topology with 15-levels. As the output power rises, losses of the whole system will decrease. The efficiency for 50 W output power is a bit more than 97%, and 400 W output power is a bit less than 96%. Switching angles of all results for the proposed topology are optimized based on the optimization procedure of Fig. 5.

Evaluation parameters of the proposed topology for modular extension are presented in Table VII. Some parameters, like the required components, switching patterns, voltage levels, TBV, and varieties, are presented. An improved THD_V is obtained using the OSA modulation strategy for various voltage levels, and it is presented in Table VII.

TABLE VII
MODULAR EXTENSION OF THE PROPOSED MLI TOPOLOGY

Level	DC Sources	Unidirectional Switches	Bidirectional Switches	Gate-Drivers	Switching Patterns	TBV	DC Source Varieties	THD_V	$V_{rms,pu}$
15	3	6	3	9	24	36	3	5.3%	0.71
25	4	6	4	10	36	63	4	3.2%	0.72
35	5	6	5	11	48	121	4	2.5%	0.71
49	6	6	6	12	64	176	4	1.9%	0.71
63	7	6	7	13	80	214	5	1.1%	0.71
81	8	6	8	14	100	302	6	...<1%	0.71
99	9	6	9	15	120	412	6	...<1%	0.71
121	10	6	10	16	144	533	6	...<1%	0.71

VII. CONCLUSION

In this paper, a novel asymmetrical MLI with a reduced component count is proposed to be used for renewable energy generation. The proposed topology can be easily extended to a three-phase structure and both modular and cascaded connections. It can be used in high voltage applications to lower stresses on the power switches. The significant advantage of the proposed MLI is the ability to generate negative voltage levels without a series H-bridge module that gives a reduction in power losses. Only three on-state power switches are required to generated different voltage levels in a module. An optimization procedure is used to determine the magnitude of the DC sources by employing the PSO algorithm to reduce the total blocking voltage instead of common approaches or algorithms. The proposed optimization approach is one of the desired features allowing for considering all the possible combinations of the input DC sources in the output voltage levels. Besides, it is flexible to be applied to any MLI topologies. Moreover, the OSA modulation technique was used at low switching frequency with the optimized switching angles by the PSO algorithm. The obtained optimized switching angles provide the best THD among those in recent papers. Considering power losses, the proposed topology has a reduced number of required switches, gate-drivers, and DC sources for a specific number of voltage levels compared to other MLI topologies. A detailed comparison of the proposed topology with other existing MLI topologies using several indices is performed. It can be concluded that the proposed topology has superior performance and fewer losses compare to published topologies. Abilities of the proposed topology are verified by simulations and experiments with 15- and 25-level inverters.

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