



Aalborg Universitet

AALBORG UNIVERSITY  
DENMARK

## Implications of Short-Circuit Degradation on the Aging Process in Accelerated Cycling Tests of SiC MOSFETs

Du, He; Baker, Nick; Iannuzzo, Francesco

*Published in:*

2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)

*DOI (link to publication from Publisher):*

[10.1109/ISPSD46842.2020.9170133](https://doi.org/10.1109/ISPSD46842.2020.9170133)

*Publication date:*

2020

*Document Version*

Accepted author manuscript, peer reviewed version

[Link to publication from Aalborg University](#)

*Citation for published version (APA):*

Du, H., Baker, N., & Iannuzzo, F. (2020). Implications of Short-Circuit Degradation on the Aging Process in Accelerated Cycling Tests of SiC MOSFETs. In *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (pp. 202-205). Article 9170133 IEEE.

<https://doi.org/10.1109/ISPSD46842.2020.9170133>

### General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal -

### Take down policy

If you believe that this document breaches copyright please contact us at [vbn@aub.aau.dk](mailto:vbn@aub.aau.dk) providing details, and we will remove access to the work immediately and investigate your claim.

# Implications of Short-Circuit Degradation on the Aging Process in Accelerated Cycling Tests of SiC MOSFETs

He Du, Nick Baker, Francesco Iannuzzo  
Department of Energy Technology  
Aalborg University  
Aalborg, 9220, Denmark  
hdu@et.aau.dk

**Abstract**— The purpose of this paper is to investigate the impact of repetitive short circuit events on the remaining useful lifetime of 1.0-kV/ 22-A SiC MOSFETs. Mixed accelerated power cycling tests, together with the different number of short-circuit repetitions, have been performed to provide a concrete estimation of short-circuit impact. The experimental results of short circuit waveforms show an increasing gate leakage current with the increasing number of repetitions. Due to the higher on-state voltage, induced by short circuit degradation, the devices withstand higher temperature swing during power cycling test compared to their initial condition, which accelerates the aging process and is related to the number of repetitive short circuits.

**Keywords**—Silicon Carbide (SiC) power MOSFET; reliability; short-circuit; power cycling;

## I. INTRODUCTION

Silicon Carbide (SiC) MOSFETs are becoming a more efficient alternative to silicon IGBTs beyond 600 V [1]. Under short circuit conditions, SiC MOSFETs may have 5-10 times the peak current density of Silicon IGBTs due to the smaller die area and thinner N- drift layer. This higher instantaneous power, combined with smaller thermal capacitance, results in a lower short-circuit withstand time [2]. Since short-circuit withstand time is an important parameter of the power semiconductor device which enables robust performance in many power electronic applications, several fast short-circuit detection techniques have now been demonstrated, which allow SiC MOSFETs to withstand short circuit events without device destruction [3] [4].

Previous works have focused on performing either power-cycling [5] or short-circuit tests [6], separately to investigate the reliability of SiC MOSFETs. The difference in short-circuit robustness between healthy and degraded devices has also been studied [7]. However, thanks to the development of fast short-circuit protection, the device may undergo many times of non-destructive short circuits along its whole lifetime [8]. Therefore, the impact of repetitive short circuit events on the remaining useful lifetime of SiC MOSFETs needs to be considered.

In this paper, a power cycling test without short-circuit

stress is performed first as a reference. Then three different number of short-circuit repetitions are introduced into three power cycling tests with the same temperature condition to investigate the impact of repetitions.

## II. TEST SETUP AND APPROACH

### A. Test Setup

The Device Under Test (DUT) is a commercial 1000-V/ 22-A, 120 m $\Omega$  SiC MOSFET, manufactured by CREE with 3<sup>rd</sup> planar technology and separate driver source pin.

The schematic and appearance of the power cycling test are shown in Fig. 1 and Fig. 2, separately. The DC source supply (Delta Elektronika SM 70-45 D) provides a constant current  $I_{load}$ . A power module from IXYS with two 1200-V/ 85-A IGBTs is used as the main switches. The DUT1 and DUT2 operate in a complementary mode with 0.5 ms overlap during the test. Independent gate drivers with adjustable output voltage (CREE CRD-001) are used for both IGBTs and DUTs. Their signals are controlled by an ARM mbed LPC1768, which also streams real-time data to PC.

The on-state drain-source voltage of both DUT1 and DUT2 ( $V_{DS,on}$ ) are monitored during each cycle. When the DUT switches off, a small current ( $I_1 = I_2 = 20$  mA) injects through the body diode to estimate the junction temperature ( $T_j$ ) and ensure that the package-related degradation does not

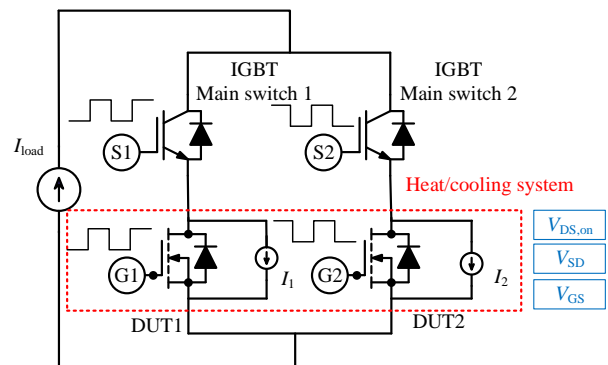


Fig. 1. Schematic of power cycling test.

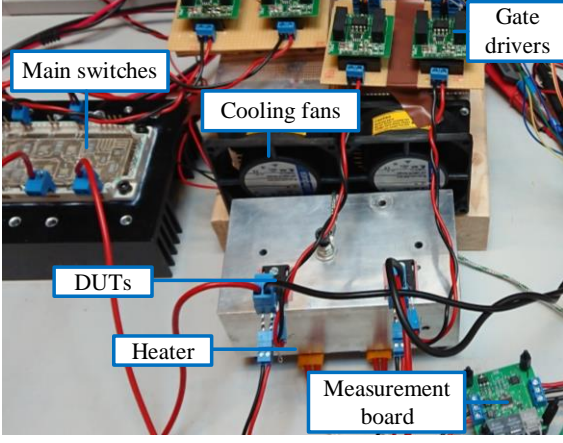


Fig. 2. Power cycling test setup appearance.

affect the measurement. Since the MOS-channel may conduct current at zero bias, leading to an inaccurate relationship between the  $T_j$  and body diode voltage ( $V_{SD}$ ), the off-state gate source voltage is set to  $-4$  V at both initial calibration stage and power cycling tests. A controllable heater and forced air cooling system are used to control the mean junction temperature. The selected power cycling condition is from  $70$  °C ( $T_{j\_min}$ ) to  $130$  °C ( $T_{j\_max}$ ) by adjusting the  $I_{load}$  and external heater. The turn-on/off time ( $t_{on}/t_{off}$ ) is  $2$  s /  $2$  s and the positive gate-source voltage ( $V_{GS}$ ) is set to  $15$  V for each test.

The repetitive short-circuit tests are performed with a 2.4-kV/ 10-kA Non-Destructive Tester (NDT) described in [9], and the schematic is shown in Fig. 3. To ensure the repetitive condition and avoid short circuit destruction such as thermal runaway, the short-circuit energy needs to be lower than the critical energy. Therefore, according to previous work [10], the drain-source voltage ( $V_{DS}$ ) is set to  $600$  V and  $V_{GS}$  is  $+15$  V/ $-4$  V with  $20$   $\Omega$  external gate resistance. The short-circuit pulse time duration is equal to  $2.2$   $\mu$ s, and the case temperature is  $25$  °C. During each short-circuit repetition, the drain current ( $I_D$ ),  $V_{DS}$  and  $V_{GS}$  are recorded.

### B. Test Approach

The experimental approach flow chart can be seen in Fig. 4. At first, static characteristics are measured to select the

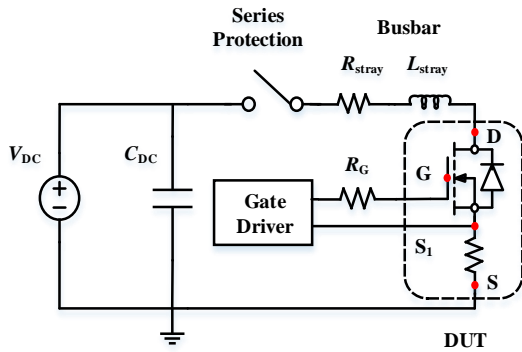


Fig. 3. Schematic of repetitive short-circuit test.

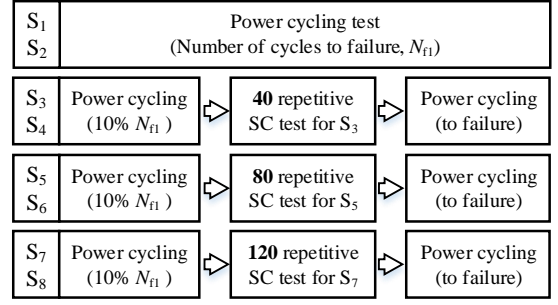


Fig. 4. Flow chart of mixed accelerated power cycling test combined with different degrees of short-circuit degradation.

matched devices as DUTs, named from  $S_1$  to  $S_8$ . Then, two devices ( $S_1$  and  $S_2$ ) are used to perform a power cycling test without any short-circuit stress and the number of cycles to failure ( $N_f$ ) is recorded. In step 3, three new devices ( $S_3$ ,  $S_5$ , and  $S_7$ ) are power-cycled up to  $10\% \cdot N_f$  cycles, at which point a short-circuit stress of 40, 80, and 120 short circuits are applied separately. As a reference, three other devices ( $S_4$ ,  $S_6$ , and  $S_8$ ) are performed without short circuit stress, respectively, and their other function is to keep the settings consistent (i.e.  $I_{load}$ ) when the power cycling tests continue to perform after  $10\% \cdot N_f$  cycles. In addition, the relationship between  $V_{SD}$  and  $T_j$  is recalibrated after the repetitive short-circuit tests.

### III. EXPERIMENTAL RESULTS

The test results of  $S_1$  and  $S_2$  without short-circuit stress are shown in Fig. 5. During each power cycle, the maximum junction temperature ( $T_{j\_max}$ ), minimum junction temperature ( $T_{j\_min}$ ) and on-state drain-source voltage ( $V_{DS,on}$ ) are recorded. With the number of cycles increasing, both devices exhibit an increasing trend of  $V_{DS,on}$  and  $T_{j\_max}$  after 20 k cycles. The device  $S_2$  failed at 30.4 k cycles, which is considered to be  $N_f$ .

Therefore, the power cycling of the device  $S_3$ ,  $S_5$  and  $S_7$  stopped after 3 k cycles ( $10\% \cdot N_f$ ) in the following tests, respectively, and different number of short-circuit repetitions were applied at this point.

The short-circuit waveforms, including  $V_{DS}$ ,  $I_D$ , and  $V_{GS}$ ,

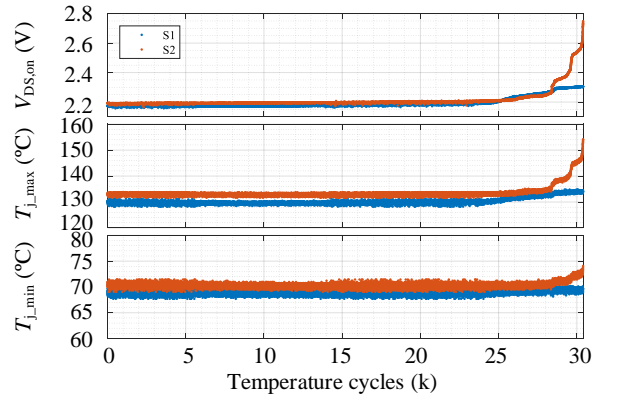


Fig. 5. Power cycling test for device  $S_1$  and  $S_2$  without short-circuit stress ( $I_{load} = 14.6$  A,  $t_{on}/t_{off} = 2$  s).

are recorded by oscilloscopes. The results of the first and last short-circuit repetition are shown in Fig. 6. All the devices have consistent short circuit waveforms in the beginning. However, since the device S<sub>3</sub>, S<sub>5</sub>, and S<sub>7</sub> withstood 40, 80, and 120 short-circuit repetitions, separately, they have different degrees of degradation, showing as lower peak short-circuit current and gate-source voltage at the last repetition.

If the gate-source voltage at 2 μs, which is close to the end of the pulse, is extracted as a degradation indicator, the gate leakage current at 2 μs can be calculated by the quotient of the voltage drop across the external gate resistor. Fig. 7 shows that the gate leakage current increases gradually with the number of short-circuit repetitions. This phenomenon can be explained by gate oxide degradation [11].

To ensure accurate temperature estimation, the relationship between the V<sub>SD</sub> and T<sub>j</sub> is recalibrated again after the repetitive short-circuit tests, as can be seen in Fig. 8. All three devices show a significant variation owing to gate degradation. In contrast, the device S<sub>4</sub>, S<sub>6</sub>, and S<sub>8</sub> without short-circuit stress remain the same values after the power cycling tests as shown in Fig. 9.

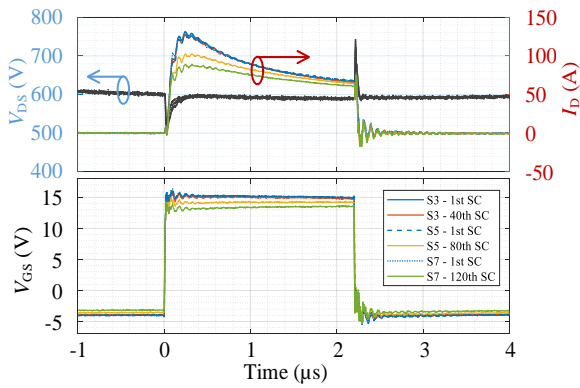


Fig. 6. Short-circuit waveforms ( $V_{DS}$ ,  $I_D$  and  $V_{GS}$ ) of the device S<sub>3</sub>, S<sub>5</sub> and S<sub>7</sub> (only the first and last repetition are presented).

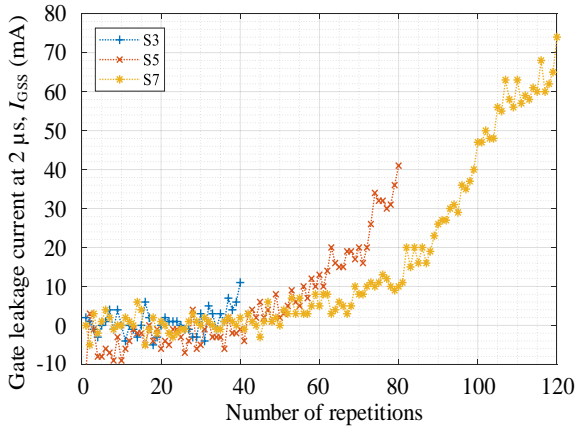


Fig. 7. Repetitive short-circuit tests for the device S<sub>3</sub>, S<sub>5</sub> and S<sub>7</sub> ( $V_{DS} = 600$  V,  $t_{SC} = 2.2$  μs,  $V_{GS} = +15/-4$  V). Calculated gate leakage current at 2 μs during short-circuit test increases with the number of repetitions.

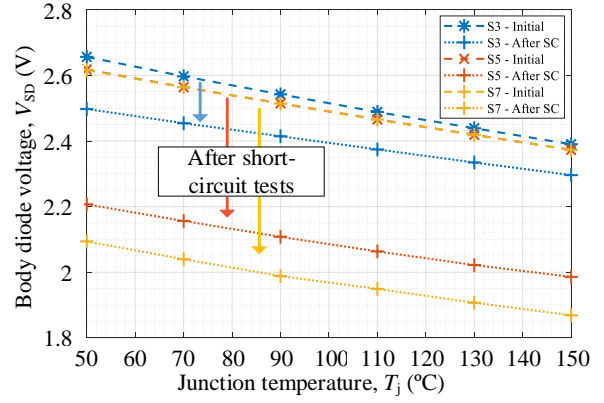


Fig. 8. Relationship between body diode voltage ( $V_{SD}$ ) and junction temperature ( $T_j$ ) of the device S<sub>3</sub>, S<sub>5</sub> and S<sub>7</sub> ( $I_D = 20$  mA) before the power cycling and after short-circuit tests.

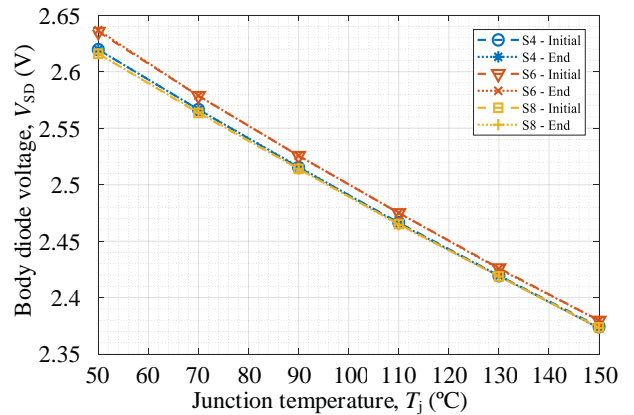


Fig. 9. Relationship between body diode voltage ( $V_{SD}$ ) and junction temperature ( $T_j$ ) of the device S<sub>4</sub>, S<sub>6</sub> and S<sub>8</sub> ( $I_D = 20$  mA) before and after the power cycling tests.

Thereafter, power cycling tests continued after different degrees of short-circuit degradation. Although the output positive voltage of the gate drivers still keep 15 V as before, the measured gate-source voltage for the device S<sub>3</sub>, S<sub>5</sub>, and S<sub>7</sub> reduce to 14.2 V, 11.8 V, and 11.1 V, respectively. Therefore, the on-state drain-source voltage ( $V_{DS,on}$ ) increases suddenly as shown in Fig. 10.

With the larger number of short-circuit repetitions, the device has a higher  $V_{DS,on}$  and the increased conduction loss leads to a further higher maximum junction temperature ( $T_{j,max}$ ) and junction temperature swing ( $\Delta T_j$ ) in Fig. 11. The more severe temperature condition exacerbates the aging process and the device S<sub>3</sub>, S<sub>5</sub> and S<sub>7</sub> fail after 4.88 k, 5.25 k, and 6.3 k cycles, respectively. In contrast, the other three devices without undergoing any short-circuit stress show stable  $V_{DS,on}$  and  $\Delta T_j$  until the tests are stopped.

Compared to the experimental results from the device S<sub>1</sub>, the number of cycles to failure reduces significantly with short-circuit repetitions. When the gate leakage current

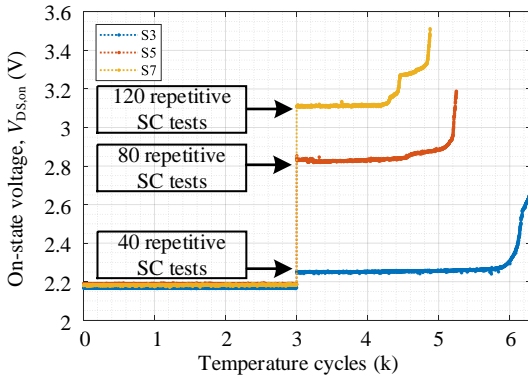


Fig. 10. On-state drain-source voltage ( $V_{DS,on}$ ) variation during power cycling test for the device  $S_3$ ,  $S_5$  and  $S_7$  with different degrees of short-circuit stress.

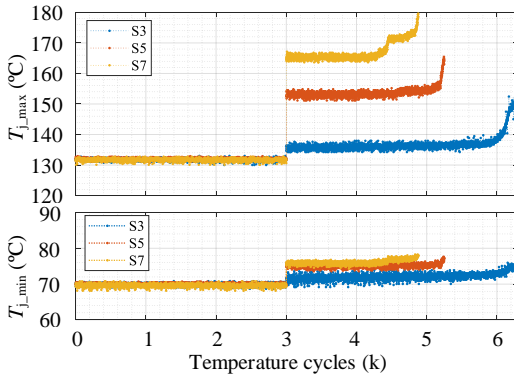


Fig. 11. Maximum and minimum junction temperature variation during power cycling test for the device  $S_3$ ,  $S_5$  and  $S_7$  with different degrees of short-circuit stress.

becomes non-negligible, the impact of short-circuit events can be transferred to a higher accelerated condition.

#### IV. CONCLUSIONS

The paper presents the impact of short-circuit degradation on the remaining useful lifetime of 1000-V/ 22A SiC MOSFETs with a third planar technology. Mixed accelerated aging test, together with different number of short-circuit repetitions have been performed. After repetitive short-circuit tests, different degrees of gate degradation are observed. Experimental results show that the larger number of short

circuits leads to a much higher  $V_{DS,on}$  and  $\Delta T_j$  during the power cycling tests, resulting in a less remaining useful lifetime.

#### ACKNOWLEDGMENT

This work is funded by the Advanced Power Electronic Technology and Tools (APETT) project from the Innovation Fund Denmark.

#### REFERENCES

- [1] X. She, A. Q. Huang, and B. Ozpineci, "Review of Silicon Carbide Power Devices and," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.
- [2] J. Sun, H. Xu, X. Wu, and K. Sheng, "Comparison and analysis of short circuit capability of 1200V single-chip SiC MOSFET and Si IGBT," 2016 Int. Forum Wide Bandgap Semicond. China, IFWS 2016 - Conf. Proc., vol. 3, pp. 42–45, 2017.
- [3] Y. Shi, R. Xie, L. Wang, Y. Shi, and H. Li, "Short-circuit protection of 1200V SiC MOSFET T-type module in PV inverter application," *ECCE 2016 - IEEE Energy Convers. Congr. Expo. Proc.*, pp. 1–5, 2016.
- [4] D. P. Sadik et al., "Short-Circuit Protection Circuits for Silicon-Carbide Power Transistors," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, 2016.
- [5] E. Ugur, S. Member, F. Yang, S. Member, S. Pu, and S. Member, "Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2858–2867, 2019.
- [6] J. Sun, J. Wei, Z. Zheng, Y. Wang, and K. J. Chen, "Short Circuit Capability and Short Circuit Induced VTH Instability of a 1.2kV SiC Power MOSFET," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 7, no. 3, pp. 1539–1546, 2019.
- [7] P. Diaz Reigosa, H. Luo, and F. Iannuzzo Ge, "Implications of Ageing through Power Cycling on the Short Circuit Robustness of 1.2-kV SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11182–11190, 2019.
- [8] B. Maxime, O. Remy, C. Thibault, B. Pierre, O. Sebastian, and T. Dominique, "Electrical performances and reliability of commercial SiC MOSFETs at high temperature and in SC conditions," 2015 17th Eur. Conf. Power Electron. Appl. EPE-ECCE Eur. 2015, 2015.
- [9] P. D. Reigosa, F. Iannuzzo, H. Luo, and F. Blaabjerg, "A short-circuit safe operation area identification criterion for SiC MOSFET power modules," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2880–2887, 2017.
- [10] H. Du, P. D. Reigosa, L. Ceccarelli, and F. Iannuzzo, "Impact of Repetitive Short-Circuit Tests on the Normal Operation of SiC MOSFETs Considering Case Temperature Influence," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 195–205, 2020.
- [11] F. Boige, F. Richardeau, D. Trémouilles, S. Lefebvre, and G. Guibaud, "Investigation on damaged planar-oxide of 1200 V SiC power MOSFETs in non-destructive short-circuit operation," *Microelectron. Reliab.*, vol. 76–77, pp. 500–506, 2017.