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Effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs and its failure analysis

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Abstract – When the SiC MOSFET works in the normal operating conditions, its remaining useful lifetime used to be estimated based on the monitored parameters and the lifetime model derived from accelerated tests. In this case, the degradation caused by abnormal events has not been considered. Therefore, it makes sense to investigate the effect of short-circuit degradation on the remaining useful lifetime of SiC MOSFETs. A different number of repetitive short-circuit events have been introduced into the accelerated power cycling tests to assess the impact. The experimental results indicate a gate degradation with the increasing number of short-circuit repetitions, which leads to higher conduction loss and earlier failure. Further failure analysis is achieved by performing lock-in thermography, scanning electron microscopy, and focused ion beam.

1. Introduction

Silicon Carbide (SiC) MOSFETs have widely emerged in the market, offering higher efficiency and power density [1]. To meet the safety requirements, the short-circuit reliability of SiC MOSFETs is becoming a critical concern as it endures a high voltage, high current, and high transient junction temperature at the same time [2]. Many efforts have been devoted to short-circuit robustness, revealing a shorter short-circuit withstand time [3]. To avoid device destruction induced by short-circuit events, faster desaturation fault detection and short circuit protection has been proposed, which allows the SiC MOSFET to withstand many times of low-energy non-destructive short-circuit events during its whole lifetime [4].

Through different accelerated ageing tests (such as power cycling, temperature cycling), the lifetime models of SiC MOSFETs can be obtained. Then, together with condition monitoring parameters (for example, on-state drain-source voltage, junction-case thermal impedance), the Remaining Useful Lifetime (RUL) of the devices can be estimated under normal operating conditions [5]. However, it is worth noting that the impact of short-circuit events on the RUL was neglected before. By taking into account this aspect, it will be possible to achieve a more accurate RUL estimation.

This paper aims to investigate the effect of short-circuit degradation on the RUL in power cycling tests by introducing a different number of short-circuit events. In Section 2, the test approach and platforms are described. The experimental results are presented in Section 3. Then Section 4 presents failure analysis and further discussion. Finally, concluding remarks are given.

2. Mixed power cycling tests with short-circuit stress

Power cycling test tends to detect the bond wires lift-off, which is a common failure mode at the packaging level and it is caused by the Coefficient of Thermal Expansion (CTE) mismatch between the bond wire and SiC material. In order to identify the ageing process in the tests, the on-state drain-source voltage ($V_{DS,on}$), consists of the chip and package-related voltage, is used as an ageing indicator [6]. Hence, the power cycling tests combined with a different number of repetitive short-circuit tests are performed to assess the short-circuit degradation effect on the $V_{DS,on}$ and the number of cycles to failure (N_f). The Device Under Test (DUT) is a commercial 1000-V/ 22-A SiC MOSFET with 3rd planar technology from Wolfspeed. The experimental approach can be seen in Fig. 1.

First of all, fresh devices with matched static characteristics are chose and named from S_1 to S_8. A power cycling test without any short-circuit stress is performed for device S_1 and S_2 to understand its end of the lifetime. The number of cycles to failure (N_{f1}) is recorded when either device first shows an extremely high $V_{DS,on}$ or open circuit failure mode to mitigate the impact of the deviation. Then the number of cycles equal to 10%·N_{f1} is selected as the point to introduce short-circuit events since the devices remain consistent characteristics at the early of the test and the impact of power cycling ageing on the short-circuit performance is negligible [7]. Thereafter, another three sets of power cycling tests are run. For the device S_3, S_5, and S_7, a different number of repetitive short circuits (40, 80, and 120) are applied at the selected point (10%·N_{f1}), respectively. To ensure the power cycling tests keep the same setting conditions after 10%·N_{f1}, the device S_4, S_6, and S_8 are run without short

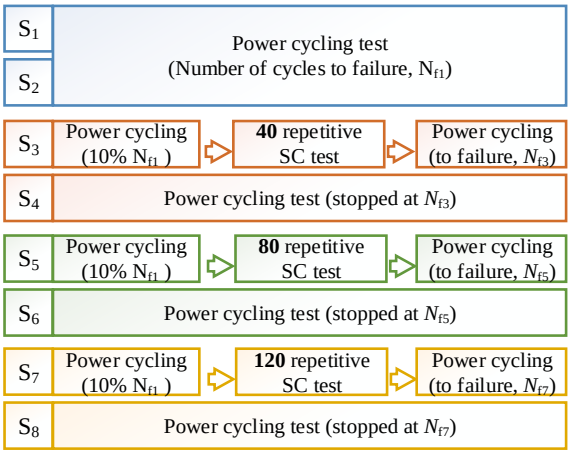

Fig. 1. Experimental approach of the power cycling test combined with different numbers of short-circuit repetitions.

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circuit stress as a reference.

During DC-based power cycling tests, the devices are heated periodically by conduction power loss (P_{con}) and cooled down when the devices turn off. Their junction temperature conditions are controlled by adjusting turn-on and turn-off time duration (t_{on}/t_{off}), constant load current (I_{load}), together with controllable heater and forced air cooling system. The schematic of the power cycling test is shown in Fig. 2. A DC source supply (DELTA SM 70-45 D) provides the required I_{load} and two main switches (1200-V 85-A IGBTs from IXYS) operate in a complementary mode with 0.5 ms overlap during the test. Each DUT, in series with one of the main switches, has the same control signal and separated gate driver (CREE CRD-001) with adjustable output voltage. The ARM microcontroller development board (MBED-LPC1768) generates control signals and streams real-time test data to PC. The gate-source voltage (V_{GS}) is monitored with the oscilloscope during the whole test.

During the conduction period of the DUT, its $V_{DS,on}$ is recorded as an ageing indicator. When the DUT turns off, the body diode's voltage drop (V_{SD}) is measured by injecting a small current (I_1 = I_2 = 20 mA), which makes the impact of package-related ageing on the V_{SD} negligible. Since the relationship between the V_{SD} and junction temperature (T_j) does not change over ageing, the V_{SD} can be used to estimate the T_j [8]. It should be noted that the V_{SD} is affected by the off-state V_{GS} value as the MOS-channel still conducts current at zero gate bias or small negative bias [9]. Thus, a negative V_{GS} of -4 V is applied at the initial calibration stage to enable an accurate estimation.

The power cycling test condition is selected as below. By adjusting the I_{load} and cooling system, the initial maximum junction temperature (T_{j_max}) and minimum junction temperature (T_{j_min}) are set to 130 ºC and 70 ºC, respectively. Then the I_{load} and the case temperature controlled by the cooling system are kept constant during the test. The t_{on}/t_{off} is 2 s/2 s and the gate resistance is equal to 20 Ω. The V_{GS} of the device S_1, S_3, S_5, and S_7 is set to +15 V/ -4 V. For the other devices (i.e. S_2, S_4, S_6, and S_8), a slight lower V_{GS} is used to ensure the same junction temperature condition.

The repetitive short circuit events are performed with a Non-Destructive Tester, which has been described in [10]. To prevent thermal runaway failure, the applied short-circuit energy must be lower than the critical energy of the device (E_{SCmax}). Therefore, the short-circuit condition at 25 ºC case temperature is selected based on previous work in [11], whose E_{SCmax} is 0.15 J. The short-circuit pulse time duration (t_{SC}) is set to 2.2 µs since its maximum short-circuit withstanding time (t_{SC_max}) is 4 µs (i.e. t_{SC}/t_{SC_max} = 0.55). The drain-source voltage (V_{DS}) is 600 V and the V_{GS} keeps +15 V/ -4 V with 20 Ω external gate resistance. The case temperature is 25 ºC. During each short circuit repetition, the waveform of drain current waveform (I_D), V_{DS} and V_{GS} are measured with the oscilloscope.

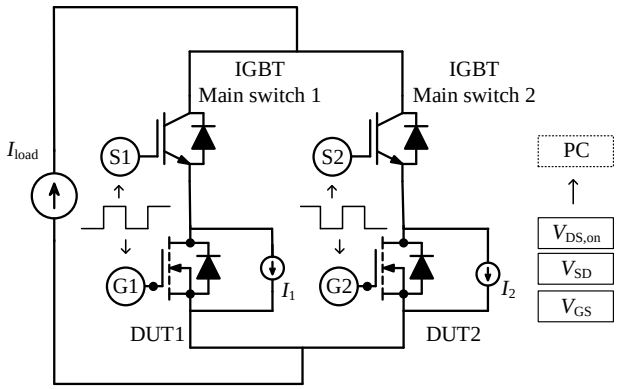


Fig. 2. Schematic of DC-based power cycling test.

3. Experimental results

Fig. 3 shows the evolution of the on-state voltage ($V_{DS,on}$), T_{j_max} and T_{j_min} with the number of cycles for the device S_1 and S_2. The $V_{DS,on}$ of both devices have similar increasing trend till 28 k cycles and the device S_2 failed after 30.4 k cycles, which is regarded as the number of cycles to failure without short circuit stress (N_{f1}). Therefore, the power cycling tests for the device S_3, S_5, and S_7 stop after 3 k cycles (10%·N_{f1}) and at that point, different number of short-circuit repetitions (40, 80 and 120 times) are performed, respectively.

Fig. 4 presents the first and last time short circuit waveforms of the device S_3, S_5, and S_7, including V_{DS}, I_D and V_{GS}. Comparing to the same results at the first short-circuit repetition, the last repetition shows an obvious difference, reflecting on the lower V_{GS} and peak I_D.

The V_{GS} at end of the short-circuit time duration, i.e. t = 2 µs, can be used as an indicator to evaluate the short-circuit degradation process [11]. Then the gate leakage current at 2 µs (I_{GSS}) during the short-circuit test can be estimated by the voltage drop on the external gate resistor (20 Ω). The left axis of Fig. 5

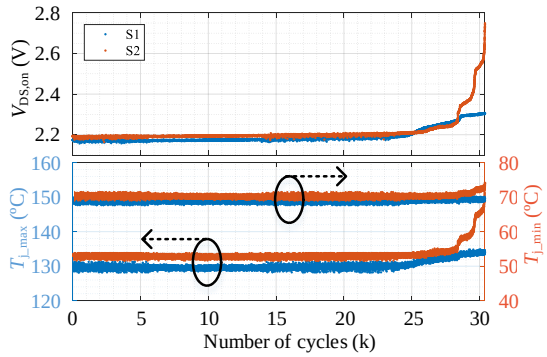


Fig. 3. Power cycling test for device S_1 and S_2 without short circuit stress.

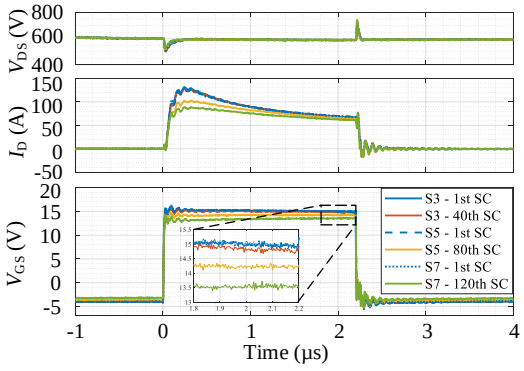


Fig. 4. First and the last repetition short circuit waveform (V_{DS}, I_D and V_{GS}) of the device S_3, S_5 and S_7.

shows the increasing I_{GSS} with the number of repetitions. The short-circuit energy (E_{SC}) of each repetition is also calculated and shown in the right axis of Fig. 5. All devices keep nearly the same E_{SC} (0.114 J) at the beginning, which is below the critical energy (i.e. E_{SC}/E_{SCmax} = 0.76). It shows that the different degrees of degradation is mainly affected by the number of repetitions rather than the first time or initial E_{SC}. These results can be explained by gate degradation, which includes the damages in gate oxide or SiO_2 dielectric [12].

After short-circuit events, the relationship between V_{SD} and T_j is calibrated again. Among them, the devices without short circuit stress (i.e. S_4, S_6 and S_8) keep the same values as before. Because of the increased I_{GSS}, the device after short circuit stress

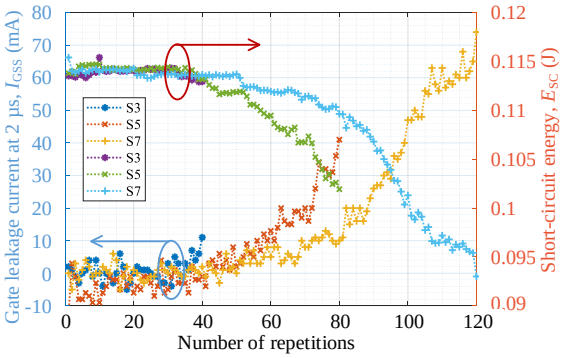


Fig. 5. Estimated gate leakage current at 2 µs (I_{GSS}) increases and short-circuit energy (E_{SC}) decreases with the number of short-circuit repetitions.

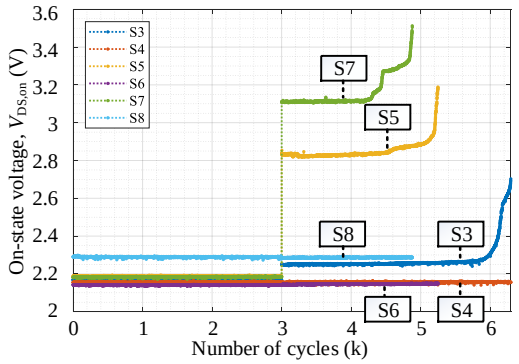


Fig. 6. On-state drain-source voltage ($V_{DS,on}$) variation with the number of cycles for the devices from S_3 to S_8.

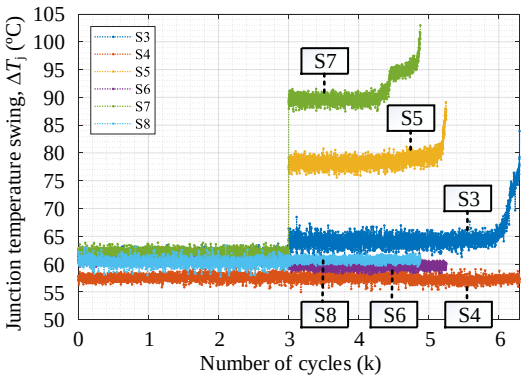


Fig. 7. Junction temperature swing (ΔT_j) variation with the number of cycles for the devices from S_3 to S_8.

(i.e. S_3, S_5 and S_7) is set to -4 V V_{GS} again and a clear variation appears. Thereafter, the power cycling tests continue to run until failure as mentioned above in Section 2. Fig. 6 shows the $V_{DS,on}$ evolution of the device S_3 - S_8. All three reference devices without short circuit stress remain the same $V_{DS,on}$ as before while the other three devices with short-circuit stress show increased value. Due to the non-negligible I_{GSS}, the oscilloscope-measured V_{GS} of the device S_3, S_5 and S_7 drop from 15 V to 14.2 V, 11.8 V and 11.1 V, respectively even though the positive output voltage of their gate drivers still keep 15 V. This factor mainly contributes to the higher $V_{DS,on}$ and higher conduction loss, which results in a higher junction temperature swing further as shown in Fig. 7. This implication of short-circuit stress on the power cycling condition has been explained in [13].

With the higher junction temperature swing (ΔT_j), the device S_3, S_5 and S_7 fail after 6.3 k, 5.25 k and 4.88 k cycles, separately while the other three reference devices show stable $V_{DS,on}$ and ΔT_j until the tests are stopped. This result indicates that the number of cycles to failure is affected by the number of short-circuit repetitions (i.e. the degree of gate degradation). Fig. 8 presents the relationship between the number of cycles to failure and the quotient of total short-circuit energy and critical energy (E_{total}/E_{SCmax}), and it can be fitted as the dotted line. Therefore, if several times of non-destructive short circuits happen in the applications, a revised RUL estimation based on the short-circuit energy and updated T_j might be needed.

4. Failure analysis and discussion

To obtain further insight into the effect of short-circuit degradation, deeper failure analysis is achieved for the devices S_5 and S_6. First, the devices are de-capsulated by laser ablation and high-temperature acid etching to remove the moulded material and then the ultrasonic cleaning is used for both devices. The bonding wires of the device S_5 are found to have been removed from the top side of the chip, as shown in Fig. 9 (a) and (b). However, the Al wires of the device S_6 remain bonded on the chip surface in Fig. 9 (c) and (d). A likely explanation may be that the bonding wires of the device S_5 has already lifted off before de-capsulation, which agrees with its open circuit failure mode. On the other hand, the V_{DS} of the

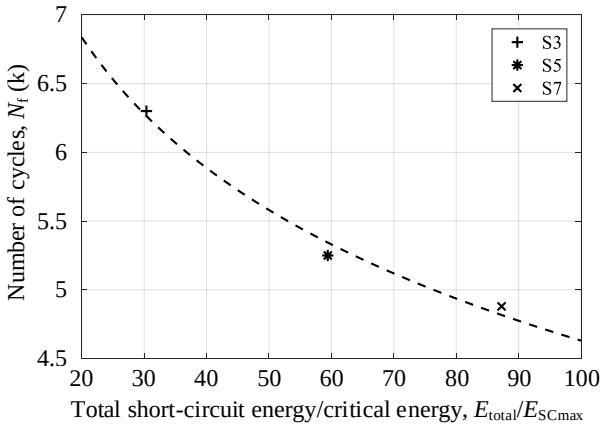


Fig. 8. Relationship between the number of cycles to failure (N_f) and the quotient of total short-circuit energy and its critical energy (E_{total}/E_{SCmax}).

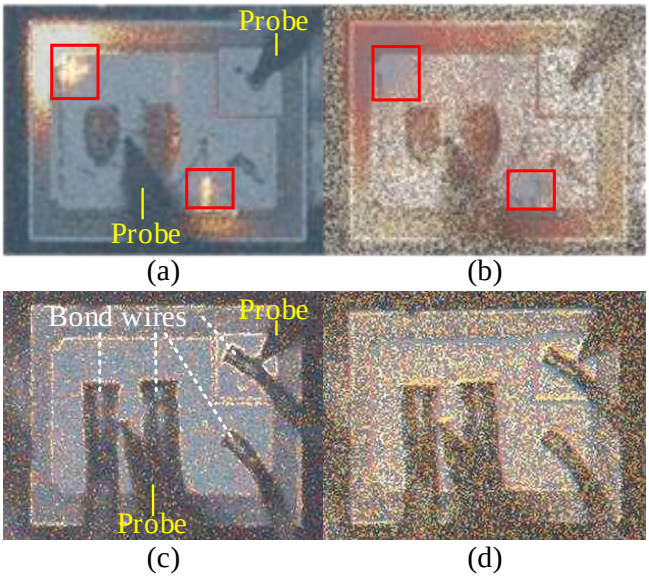


Fig. 9. Lock-in thermography with applied gate-source voltages: (a) amplitude and (b) phase image of the device S_5; (c) amplitude and

device S_6 keeps stable, indicating well connection and negligible impact of de-capsulation process and ultrasonic cleaning on the bonding wires.

After that, the lock-in thermography measurements are performed to locate the damaged areas. The high-resolution lock-in thermography system from DCG Systems is equipped with a high-performance InSb 320 M infrared camera, which makes it possible to detect low power dissipation. A periodical square-pulse voltage is applied on the gate pad through probe while the drain and source are short connected to the ground. To avoid introducing artificial damage, the gate leakage current limitation is set.

With respect to the device S_5, the measured gate leakage current achieves at 1 mA when the V_{GS} is equal to 0.84 V and two degraded regions have been observed as shown in Fig. 9 (a) and (b); the reason why these two regions are located in the periphery needs to be further studied. In contrast, the device S_6 shows negligible gate leakage current (I_{GSS} = 0.17 nA) when the V_{GS} is applied to 15 V, which indicates no gate damage as shown in Fig. 9 (c) and (d).

Thereafter, a Focused Ion Beam (FIB) at the degraded locations of the device S_5 is performed by the ThermoScientific Helios G4 PFIB UXe system to obtain the vertical cross-section. Fig. 10 shows the magnified Scanning Electron Microscopy (SEM) image and a dielectric SiO_2 crack exists in one of the cells. This crack may be caused by an etching artefact close to it. On the other hand, whether there is a damage in the gate oxide between the polysilicon and the SiC substrate, whose thickness is around 50 nm, cannot be seen, unfortunately, since the FIB limits SEM resolution.

However, this dielectric SiO_2 crack might have reached the polysilicon gate along with the direction vertical to the figure. This kind of crack is also found in [12] [14] and well supported in [15] with the Energy-Dispersive Spectroscopy (EDS) results, which indicates that the thermal stress on SiO_2 dielectric causes the crack. Then, a conductive path between the polysilicon gate and the Al source can be built and leads to a significant I_{GSS}.

Besides, a large difference in the Al grains size between the top and bottom locations is observed in Fig. 11. This

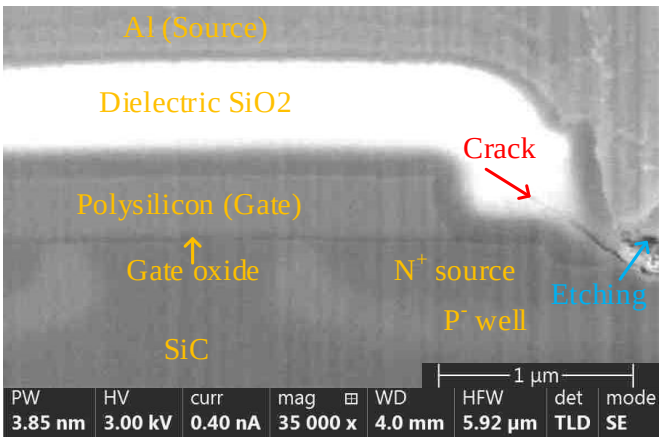
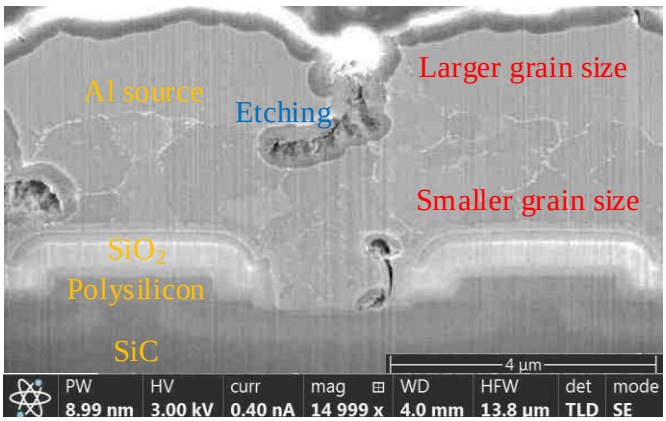


Fig. 10. Magnified cross-sectional SEM image of the damaged cell from the device S_5. The red arrow identifies the crack.



inhomogeneity of Al grains size is similar to the Al metallization reconstruction in [16] and it might come from the vertical temperature gradient, which in turn induces microstructural evolution along the temperature gradient. Further research is needed to investigate whether it comes from short-circuit stress or power cycling stress. The degradation of Al metallization, which is characterized by the grain size reduction, can be explained by the dislocation-based plasticity in [17]. Then the multiplication of grain boundaries and even the appearance of intergranular cracks may cause an increase of Al metallization resistance.

5. Conclusions

This paper investigates the effect of short-circuit degradation on the RUL of the 1000-V 22-A SiC MOSFETs with 3rd planar technology from Wolfspeed. The experimental results of mixed power cycling tests show that a larger number of short-circuit repetitions induce higher I_{GSS}, which leads to the higher $V_{DS,on}$ and P_{con}. Owing to the higher ΔT_j, the device fails much earlier and further failure analysis still demonstrates the bonding wires lift-off, which is in agreement with the open-circuit failure mode. After the FIB, a dielectric SiO_2 crack is observed with SEM. This may form a conductive path between the gate and source, which results in the higher I_{GSS}. The inhomogeneity of Al grains size might be caused by a strong vertical temperature gradient during the tests and attributed to the dislocation-based plasticity.

Acknowledgements

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