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dq-Frame Impedance Modeling of Three-phase Grid-tied Voltage Source Converters Equipped With Advanced PLLs

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***Abstract*—With the increased prevalence of power converters in power systems, especially three-phase voltage source converters (VSCs), the stability analysis of power electronics-based power systems has received much attention recently. To this end, different impedance models, such as the *dq*-domain, sequence-domain, and phasor-domain impedance models among others, have been developed for three-phase VSCs in recent years. A common trend in all these impedance models, which have no noticeable practical advantage compared to each other, is considering a standard synchronous reference frame PLL (SRF-PLL) for the synchronization of the VSC with the power grid. The standard SRF-PLL, however, has a limited filtering ability and, therefore, may not be very practical in most applications. To deal with this shortcoming of the SRF-PLL, a great number of advanced three-phase PLLs have been proposed in the literature. These advanced PLLs may have different feedback/feedforward loops and filters in their structures, which make including their dynamics in the available impedance models complicated. Bridging this gap in research is the objective of this paper. To this end, it is demonstrated that advanced three-phase PLLs have an alternative representation, which can be easily included in the available *dq*-frame impedance model. Several case studies are presented to verify this idea.**

***Index Terms*—*dq* frame, filters, impedance model, phase-locked loop (PLL), stability, synchronization, synchronous reference frame (SRF), three-phase systems, voltage source converter (VSC), weak grids.**

I. Introduction

With recent development in power electronics technology and signal processing devices, three-phase power converters are more and more employed in the generation, transmission, and distribution power systems [1]. For instance, on the generation side, they are widely used for grid interfacing renewable energy sources, such as photo-voltaic and wind systems, which have received much attention recently because of the adverse environmental effects of conventional fossil fuel power plants. The three-phase power converters are also building blocks in applications like high-voltage dc transmission and flexible ac transmission systems on the transmission side of power systems.

Among different technologies of power converters, voltage source converters (VSCs) are particularly popular thanks to their high efficiency [2], [3]. The grid-tied VSCs are often controlled as a current source, which means they are regulated to inject a controlled current to the grid.

With the increased utilization of power electronic converters, especially three-phase current-controlled VSCs, analyzing stability issues in power electronics-based power systems has received considerable attention. Two pioneering research papers in this area are [4] and [5]. Inspired by the impedance-based stability criterion in designing switching regulators [6], it has been shown in [4] that the stability of a grid-tied VSC can be evaluated by applying the Nyquist stability criterion to the ratio of the grid impedance to the VSC output impedance. In [5], the *dq*-frame impedance modeling of a grid-tied VSC has been presented, which was later refined in [7]. The VSC output impedance is represented by 2×2 matrices in these works. Therefore, the generalized Nyquist stability criterion is adopted for analyzing the interaction between the VSC output impedance and the grid impedance. One of the main contributions of [5] and [7] is probably considering the dynamics of the phase-locked loop (PLL) during the impedance modeling. It is demonstrated in these works that the PLL, which is often used for the synchronization of the VSC with the power grid, causes a negative resistor behavior in the VSC output impedance. This negative resistor, which may adversely affect the VSC stability under weak grids, is affected by the PLL bandwidth and the VSC power rating.

In [8], it is discussed that the *dq*-frame impedance modeling of VSCs has some drawbacks, such as the tight coupling of its *d*- and *q*-axis elements and the difficulty of its physical interpretation among others. To deal with these limitations, the sequence-domain impedance modeling of grid-tied VSCs in the stationary reference frame is proposed in [9], which involves the harmonic linearization, i.e., the linearization of the nonlinear system around a periodic trajectory [8]. According to this impedance model, the positive- and negative-sequence output impedance of the three-phase VSC are decoupled in a balanced system and, therefore, can be determined using a

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single measurement.

In [10] and [11], it is proved that the positive- and negative-sequence impedance of the converter are not completely decoupled. In fact, because of the PLL of the VSC, there are couplings between the positive- and negative-sequence impedance of the three-phase VSC, even when the system is balanced. It is shown in [10] and [11] that neglecting these couplings may result in some inaccuracies in evaluating the VSC stability.

In [12], a relationship between the VSC impedance models in different domains is established. To be more exact, it is demonstrated in [12] that the modified sequence-domain impedance model [10] and the *dq*-frame impedance model [7] are mathematically equivalent. It means that the VSC stability analysis using both of these models will give the same result. It also means that they can be obtained from each other by applying a linear transform. It is also demonstrated in [12] that applying a model-order reduction to these two models results in the original sequence-domain impedance model [9].

In addition to the above models, some other impedance models for VSCs may also be found in the literature. In [13], for example, a phasor-based impedance model is presented, which is equivalent to the *dq*-domain and modified sequence-domain impedance models. In [14], the direct derivation of the VSC impedance model in the stationary reference frame using a complex space vector method is proposed, which is slightly different from the modified sequence-domain model.

In all these impedance models, which have no noticeable practical advantage compared to each other, often a standard synchronous reference frame PLL (SRF-PLL) is considered for the grid synchronization of three-phase VSCs. In many applications (e.g., in microgrids and weak grid scenarios), however, using the standard SRF-PLL may not be very practical as the grid voltage may be imbalanced and highly contaminated by harmonics, interharmonics, and dc offset, and the standard SRF-PLL has a limited ability to filter these disturbances. To deal with this limitation of the standard SRF-PLL, a great number of advanced three-phase PLLs have been designed and proposed in the literature [15]. These PLLs have a great diversity and may include different types of filters and feedback/feedforward loops in different reference frames in their structures. Therefore, including their dynamics in the VSC impedance model can be very complicated, especially for those who are not experienced in the field. Bridging this gap in research is the main objective of this paper. To this end, it is demonstrated in this paper that advanced three-phase PLLs have an alternative representation, which can be simply obtained and included in the *dq*-frame impedance model presented in [7]. Notice that the impedance modeling in the *dq* frame does not limit the usefulness of this idea because, as mentioned before, different impedance models are mathematically equivalent to the *dq*-frame one and, therefore, can be simply obtained from it by applying linear transformations. To facilitate understanding of the proposed idea, some case studies and examples are presented.

The rest of the paper is organized as follows. In Section II, an overview of the *dq*-frame impedance modeling of a three-phase current-controlled VSC with a general PLL structure is presented. It will also be discussed in the same section that available advanced three-phase PLLs have an alternative representation in this general form, which can be obtained by following a straightforward procedure. To better understand this idea, three case studies are presented in Sections III. Some discussions are presented in Section IV. Section V concludes this paper.

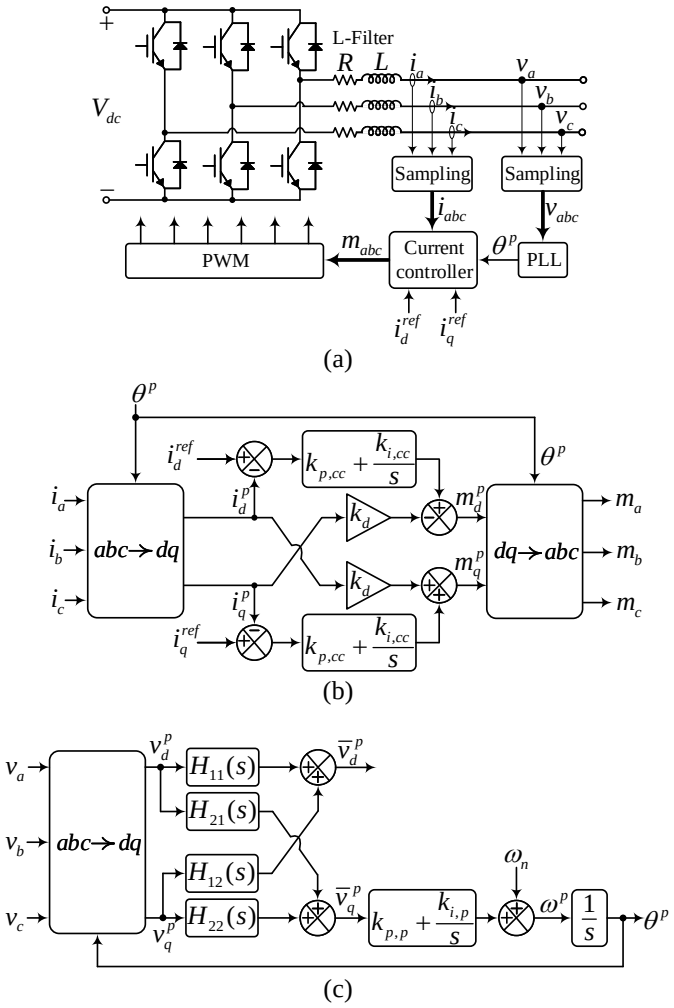

Fig. 1. (a) A three-phase VSC for grid-tied applications. (b) Current controller of the VSC. (c) PLL of the VSC.

II. Overview of *dq*-Frame Impedance Modeling

A. Assumptions

Fig. 1(a) illustrates the block diagram representation of a three-phase VSC for grid-tied applications, where its current controller and PLL are as shown in Fig. 1(b) and (c), respectively. In this structure, v_{abc}, i_{abc}, and V_{dc} are the grid voltage, the VSC output current, and the dc-link voltage, respectively. m_{abc} are the reference signals for the PWM. L and R are the inductance and resistance of the *L*-filter, respectively. $k_{p,cc}$ and $k_{i,cc}$ [$k_{p,p}$ and $k_{i,p}$] are the proportional and integral gains of the proportional-integral (PI) regulator of the current controller [PLL], respectively. θ^p and ω^p are the output phase angle and angular frequency of the PLL, respectively. i_d^{ref} and i_q^{ref} are

the d-axis and q-axis reference currents, respectively. k_d is the decoupling term. $H_{11}(s)$, $H_{12}(s)$, $H_{21}(s)$, and $H_{22}(s)$ are some generic transfer functions in the PLL structure.

In what follows, an overview of the *dq*-frame impedance modeling of this VSC is presented [7]. Before presenting the overview, some assumptions are made. As the main objective of this paper is demonstrating the procedure for including the dynamics of advanced three-phase PLLs in the VSC's *dq*-frame impedance model, and the PLL dynamics mostly affect the VSC output impedance in the low-frequency range, the PWM and computational delays, which have a small effect in the low-frequency range, are ignored [13]. A constant dc-link voltage is also assumed throughout this paper, which means the dynamics of the dc-link voltage controller of the VSC are neglected. The grid voltage frequency is also assumed to be fixed at its nominal value, i.e., ω_n.

B. Relationship Between Variables in Grid and PLL dq Frames

An important point to keep in mind is that the VSC has two *dq* frames: the PLL (current controller) *dq* frame and the grid *dq* frame, which are indicated by the superscripts p and g, respectively. Equation (1) defines the VSC signals in these two *dq* frames, where the uppercase denotes the working point and $\sim$ indicates a small perturbation.

$$\begin{array}{ccc} i_d^g = I_d + \tilde{i}_d^g & m_d^g = M_d + \tilde{m}_d^g & v_d^g = V_d + \tilde{v}_d^g \\ i_q^g = I_q + \tilde{i}_q^g \ , & m_q^g = M_q + \tilde{m}_q^g \ , & v_q^g = V_q + \tilde{v}_q^g \\ \hline i_d^p = I_d + \tilde{i}_d^p & m_d^p = M_d + \tilde{m}_d^p & v_d^p = V_d + \tilde{v}_d^p \\ i_q^p = I_q + \tilde{i}_q^p \ , & m_q^p = M_q + \tilde{m}_q^p \ , & v_q^p = V_q + \tilde{v}_q^p \end{array} \tag{1}$$

Notice that a given signal has the same working point in both *dq* frames. Notice also that the working point of the voltage in the q-axis, i.e., V_q, is equal to zero. This fact can be concluded from the PLL structure in Fig. 1(c).

If we consider the phase displacement between two rotating frames as $\Delta\theta = \theta^p - \theta^g$, where θ^p and θ^g are the rotating angles of the PLL and grid *dq* frames, respectively, and consider the Park's transformation as (2), the signals in these two frames can be related to each other as expressed in (3), where x is an arbitrary signal.

$$T_{abc\to dq} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} x_d^p \\ x_q^p \end{bmatrix} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \begin{bmatrix} x_d^g \\ x_q^g \end{bmatrix}. \tag{3}$$

In the working point, the phase displacement is zero, i.e., two *dq* frames are aligned. By considering a small perturbation in the phase displacement between two frames, we have

$$\begin{aligned} \begin{bmatrix} X_d + \tilde{x}_d^p \\ X_q + \tilde{x}_q^p \end{bmatrix} &= \begin{bmatrix} \cos(\Delta\tilde{\theta}) & \sin(\Delta\tilde{\theta}) \\ -\sin(\Delta\tilde{\theta}) & \cos(\Delta\tilde{\theta}) \end{bmatrix} \begin{bmatrix} X_d + \tilde{x}_d^g \\ X_q + \tilde{x}_q^g \end{bmatrix} \\ &\approx \begin{bmatrix} 1 & \Delta\tilde{\theta} \\ -\Delta\tilde{\theta} & 1 \end{bmatrix} \begin{bmatrix} X_d + \tilde{x}_d^g \\ X_q + \tilde{x}_q^g \end{bmatrix} \approx \begin{bmatrix} X_d + \tilde{x}_d^g + X_q\Delta\tilde{\theta} \\ X_q + \tilde{x}_q^g - X_d\Delta\tilde{\theta} \end{bmatrix} \end{aligned} \tag{4}$$

which is corresponding to

$$\begin{bmatrix} \tilde{x}_d^p \\ \tilde{x}_q^p \end{bmatrix} \approx \begin{bmatrix} \tilde{x}_d^g \\ \tilde{x}_q^g \end{bmatrix} + \begin{bmatrix} +X_q\Delta\tilde{\theta} \\ -X_d\Delta\tilde{\theta} \end{bmatrix}. \tag{5}$$

Notice that the term $\Delta\tilde{\theta}$ in the above equation, according to the PLL structure in Fig. 1(c), is equal to

$$\begin{aligned} \Delta\tilde{\theta}(s) &= \overbrace{\frac{k_{p,p}s + k_{i,p}}{s^2}}^{G_b(s)} \left\{ H_{21}(s)\tilde{v}_d^p(s) + H_{22}(s)\tilde{v}_q^p(s) \right\} \\ &\approx G_b(s) \Big\{ H_{21}(s) \left[\tilde{v}_d^g(s) + V_q\Delta\tilde{\theta}(s) \right] \\ &\quad + H_{22}(s) \left[\tilde{v}_q^g(s) - V_d\Delta\tilde{\theta}(s) \right] \Big\} \end{aligned} \tag{6}$$

or equivalently

$$\begin{aligned} \Delta\tilde{\theta}(s) \approx & \overbrace{\frac{G_b(s)H_{21}(s)}{1 + G_b(s)\left[H_{22}(s)V_d - H_{21}(s)V_q\right]}}^{G_{PLL1}(s)} \tilde{v}_d^g(s) \\ & + \underbrace{\frac{G_b(s)H_{22}(s)}{1 + G_b(s)\left[H_{22}(s)V_d - H_{21}(s)V_q\right]}}_{G_{PLL2}(s)} \tilde{v}_q^g(s). \end{aligned} \tag{7}$$

Considering (5) and (7), the following relationships between the signals in the two *dq* frames can be found [7]:

$$\begin{bmatrix} \tilde{m}_d^g(s) \\ \tilde{m}_q^g(s) \end{bmatrix} \approx \begin{bmatrix} \tilde{m}_d^p(s) \\ \tilde{m}_q^p(s) \end{bmatrix} + \overbrace{\begin{bmatrix} -M_qG_{PLL1}(s) & -M_qG_{PLL2}(s) \\ M_dG_{PLL1}(s) & M_dG_{PLL2}(s) \end{bmatrix}}^{\boldsymbol{G^m_{PLL}}(s)} \begin{bmatrix} \tilde{v}_d^g(s) \\ \tilde{v}_q^g(s) \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} \tilde{i}_d^p(s) \\ \tilde{i}_q^p(s) \end{bmatrix} \approx \begin{bmatrix} \tilde{i}_d^g(s) \\ \tilde{i}_q^g(s) \end{bmatrix} + \overbrace{\begin{bmatrix} I_qG_{PLL1}(s) & I_qG_{PLL2}(s) \\ -I_dG_{PLL1}(s) & -I_dG_{PLL2}(s) \end{bmatrix}}^{\boldsymbol{G^i_{PLL}}(s)} \begin{bmatrix} \tilde{v}_d^g(s) \\ \tilde{v}_q^g(s) \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} \tilde{v}_d^p(s) \\ \tilde{v}_q^p(s) \end{bmatrix} \approx \overbrace{\begin{bmatrix} 1 + V_qG_{PLL1}(s) & V_qG_{PLL2}(s) \\ -V_dG_{PLL1}(s) & 1 - V_dG_{PLL2}(s) \end{bmatrix}}^{\boldsymbol{G^v_{PLL}}(s)} \begin{bmatrix} \tilde{v}_d^g(s) \\ \tilde{v}_q^g(s) \end{bmatrix}. \tag{10}$$

C. VSC Impedance Modeling

The averaged model of the VSC in the *abc* frame can be expressed as

$$Ri_{abc}(t) + L\frac{di_{abc}(t)}{dt} = \frac{V_{dc}}{2}m_{abc}(t) - v_{abc}(t). \tag{11}$$

Transferring (11) to the grid *dq* frame results in

$$\begin{aligned} & R \begin{bmatrix} i_d^g(t) \\ i_q^g(t) \end{bmatrix} + L \begin{bmatrix} \frac{di_d^g(t)}{dt} \\ \frac{di_q^g(t)}{dt} \end{bmatrix} + \begin{bmatrix} 0 & -L\omega^g \\ L\omega^g & 0 \end{bmatrix} \begin{bmatrix} i_d^g(t) \\ i_q^g(t) \end{bmatrix} \\ & = \frac{V_{dc}}{2} \begin{bmatrix} m_d^g(t) \\ m_q^g(t) \end{bmatrix} - \begin{bmatrix} v_d^g(t) \\ v_q^g(t) \end{bmatrix}. \end{aligned} \tag{12}$$

Considering the definitions (1), the above equation can expressed in the Laplace domain as

$$\overbrace{\begin{bmatrix} R + Ls & -L\omega^g \\ +L\omega^g & R + Ls \end{bmatrix}}^{\boldsymbol{G_z}(s)} \begin{bmatrix} \tilde{i}_d^g(s) \\ \tilde{i}_q^g(s) \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} \tilde{m}_d^g(s) \\ \tilde{m}_q^g(s) \end{bmatrix} - \begin{bmatrix} \tilde{v}_d^g(s) \\ \tilde{v}_q^g(s) \end{bmatrix}. \tag{13}$$

By substituting (8) into (13) and considering the current controller in Fig. 1(b), we have

$$\begin{aligned}\boldsymbol{G_z}(s)\begin{bmatrix}\tilde{i}_d^g(s)\\ \tilde{i}_q^g(s)\end{bmatrix} &\approx \frac{V_{dc}}{2}\begin{bmatrix}\tilde{m}_d^p(s)\\ \tilde{m}_q^p(s)\end{bmatrix}\\ &\quad-\left(\boldsymbol{I}-\frac{V_{dc}}{2}\boldsymbol{G_{PLL}^m}(s)\right)\begin{bmatrix}\tilde{v}_d^g(s)\\ \tilde{v}_q^g(s)\end{bmatrix}\\ &=-\frac{V_{dc}}{2}\left(\boldsymbol{G_{cc}}(s)-\boldsymbol{G_{dec}}\right)\begin{bmatrix}\tilde{i}_d^p(s)\\ \tilde{i}_q^p(s)\end{bmatrix}\\ &\quad-\left(\boldsymbol{I}-\frac{V_{dc}}{2}\boldsymbol{G_{PLL}^m}(s)\right)\begin{bmatrix}\tilde{v}_d^g(s)\\ \tilde{v}_q^g(s)\end{bmatrix}\end{aligned}\tag{14}$$

where $\boldsymbol{I}$ is the identity matrix, $\boldsymbol{G_{cc}}(s)=\frac{k_{p,cc}s+k_{i,cc}}{s}\boldsymbol{I}$, and $\boldsymbol{G_{dec}}=\begin{bmatrix}0 & -k_d\\ k_d & 0\end{bmatrix}$.

Substituting (9) into (14) gives the *dq*-frame impedance of the VSC as (15), at the bottom of the page.

III. Impedance Modeling of VSC Equipped With Advanced PLLs

Eq. (15), as mentioned before, is the output impedance of the VSC in the *dq* frame, which has been obtained for the PLL structure shown in Fig. 1(c). Most of advanced three-phase PLLs, however, have different structures from Fig. 1(c). To be more exact, they may have different kinds of adaptive or nonadaptive filters and feedback/feedforward loops in different reference frames in their structure, which make the VSC impedance modeling complicated, especially for those who are not experienced in the field. This paper, as mentioned before, aims to address this difficulty. The key idea is that, roughly speaking, all advanced three-phase PLLs, regardless of their structure, have an alternative representation that is the same as Fig. 1(c) from the structural point of view. It can be proved that this alternative representation of advanced three-phase PLLs, which is referred to as the standard-form counterpart (SFC), is mathematically equivalent to the original structure from the small-signal point of view. Therefore, for obtaining the *dq*-frame output impedance of VSC equipped with an advanced PLL, one just needs to find its SFC. To better understand this idea, three case studies are presented in what follows.

A. Case Study 1

A great number of advanced three-phase PLLs have a structure as shown in Fig. 2 [16], in which $\hat{v}_\alpha$ and $\hat{v}_\beta$ are the estimation of the fundamental component of v_α and v_β, respectively, $q\hat{v}_\alpha$ and $q\hat{v}_\beta$ are the quadrature (90° phase-shifted) versions of $\hat{v}_\alpha$ and $\hat{v}_\beta$, respectively, and $\hat{v}_{\alpha\beta}^+$ denotes the estimation of the grid voltage fundamental-frequency positive sequence (FFPS) component in the $\alpha\beta$ frame. In such PLLs (Fig. 2), a prefiltering stage between $abc\rightarrow\alpha\beta$ and $\alpha\beta\rightarrow dq$ transformations exists. This prefiltering stage, which is frequency-adaptive, is directly coupled with the SRF-PLL control loop through a feedback loop. The main responsibility of this stage is extracting the FFPS component of the grid voltage in the $\alpha\beta$ frame. If it is required, it may also extract the fundamental-frequency negative sequence (FFNS) component of the grid voltage and even its harmonic components.

The prefiltering stage in Fig. 2 includes two identical real (as opposed to complex) filters and a so-called $\alpha\beta$-frame positive sequence calculator (PSC$_{\alpha\beta}$). Each filter adaptively extracts the fundamental component of its input signal and its 90° phase-shifted version. These filters can be realized in different ways. The methods based on the all-pass filter [17], second-order generalized integrator (SOGI) [18], [19], third-order generalized integrator (TOGI) [20], [21], fourth-order generalized integrator (FOGI) [22], [23], third-order scalar filter [24], enhanced PLL (EPLL) structure [25], and the series/parallel connection of these filters [26], [27] and their mixed application [28] are just few examples among others. For a detailed review of possible options, refer to [15], [16], and [29].

The outputs of the two filters in Fig. 2 are fed to the PSC$_{\alpha\beta}$, which calculates the grid voltage FFPS component according to the instantaneous symmetrical component (ISC) theory in the $\alpha\beta$ frame, as expressed below [19]:

$$\begin{aligned}\hat{v}_\alpha^+ &= \tfrac{1}{2}\left(\hat{v}_\alpha - q\hat{v}_\beta\right)\\ \hat{v}_\beta^+ &= \tfrac{1}{2}\left(\hat{v}_\beta + q\hat{v}_\alpha\right).\end{aligned}\tag{16}$$

1) Obtaining SFC: The two filters in Fig. 2 are frequency-adaptive. Therefore, strictly speaking, their input and output signals cannot be related to each other using transfer functions. However, because the grid frequency was assumed to be fixed at its nominal value (see Section II-A) and because the small-signal impedance modeling of the VSC is intended here, the feedback signal ω^p to the prefiltering stage can be assumed (quasi-) constant. In this case, each filter in Fig. 2 can be characterized by two transfer functions, as expressed below:

$$\begin{aligned}\frac{\hat{v}_\alpha(s)}{v_\alpha(s)} &= \frac{\hat{v}_\beta(s)}{v_\beta(s)} = H_D(s)\\ \frac{q\hat{v}_\alpha(s)}{v_\alpha(s)} &= \frac{q\hat{v}_\beta(s)}{v_\beta(s)} = H_Q(s).\end{aligned}\tag{17}$$

Using (16) and (17), the output signals of the PSC$_{\alpha\beta}$ in the Laplace domain can be expressed as

$$\begin{aligned}\hat{v}_\alpha^+(s)+j\hat{v}_\beta^+(s) &= \frac{1}{2}\left(\hat{v}_\alpha(s)-q\hat{v}_\beta(s)\right)+j\frac{1}{2}\left(\hat{v}_\beta(s)+q\hat{v}_\alpha(s)\right)\\ &= \frac{H_D(s)+jH_Q(s)}{2}\left(v_\alpha(s)+jv_\beta(s)\right).\end{aligned}\tag{18}$$

It is known that transferring a filter from the $\alpha\beta$ frame to the *dq* frame is corresponding to a frequency shift (equal to the angular speed of the *dq* frame) in the transfer function of the filter [30], [31]. As the angular speed of the *dq* frame in Fig.

$$\boldsymbol{Z_{dq}}(s)\approx\left(\boldsymbol{I}-\frac{V_{dc}}{2}\boldsymbol{G_{PLL}^m}(s)+\frac{V_{dc}}{2}\left(\boldsymbol{G_{cc}}(s)-\boldsymbol{G_{dec}}\right)\boldsymbol{G_{PLL}^i}(s)\right)^{-1}\left(\boldsymbol{G_z}(s)+\frac{V_{dc}}{2}\left(\boldsymbol{G_{cc}}(s)-\boldsymbol{G_{dec}}\right)\right).\tag{15}$$

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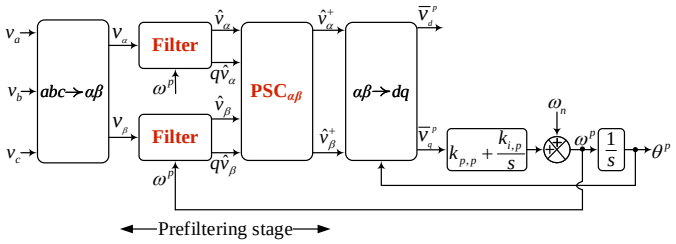

Fig. 2. A popular form of advanced three-phase PLLs characterized by a prefilter in the $\alpha\beta$ frame.

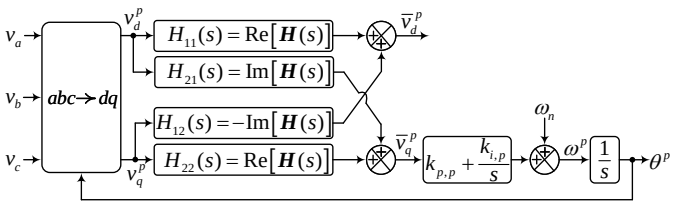

Fig. 3. SFC of PLL structures in Fig. 2 and 9.

2 is ω^p, the result of transferring (18) to the dq frame is

$$\bar{v}_d^p(s)+j\bar{v}_q^p(s) = \underbrace{\frac{H_D(s+j\omega^p)+jH_Q(s+j\omega^p)}{2}}_{\boldsymbol{H}(s)}\left(v_d^p(s)+jv_q^p(s)\right). \quad (19)$$

In the above equation, $\boldsymbol{H}(s)$ is a complex-coefficient transfer function[1], which can be divided into its real and imaginary parts, i.e., $\boldsymbol{H}(s) = \mathrm{Re}[\boldsymbol{H}(s)] + j\,\mathrm{Im}[\boldsymbol{H}(s)]$. Therefore, in the matrix form, (19) is corresponding to

$$\begin{bmatrix}\bar{v}_d^p(s)\\ \bar{v}_q^p(s)\end{bmatrix} = \begin{bmatrix}\overbrace{\mathrm{Re}[\boldsymbol{H}(s)]}^{H_{11}(s)} & \overbrace{-\mathrm{Im}[\boldsymbol{H}(s)]}^{H_{12}(s)}\\ \underbrace{\mathrm{Im}[\boldsymbol{H}(s)]}_{H_{21}(s)} & \underbrace{\mathrm{Re}[\boldsymbol{H}(s)]}_{H_{22}(s)}\end{bmatrix}\begin{bmatrix}v_d^p(s)\\ v_q^p(s)\end{bmatrix}. \quad (20)$$

Considering (20), the SFC of Fig. 2 can be obtained as depicted in Fig. 3. Notice that the coefficients of the transfer function $\boldsymbol{H}(s)$ in (20) may include ω^p, which needs to be replaced by its nominal value, i.e., ω_n.

For reader's convenience, the procedure of obtaining the SFC of Fig. 2, which is shown in Fig. 3, is summarized in what follows:

- Step 1: Assume the frequency feedback signal ω^p to the two filters in Fig. 2 as a constant, and obtain the characteristic transfer functions of these filters, as expressed in (17).
- Step 2: Obtain the transfer function $\boldsymbol{H}(s)$ as expressed in (19).
- Step 3: Replace ω^p by ω_n in the transfer function $\boldsymbol{H}(s)$, divide $\boldsymbol{H}(s)$ into its real and imaginary parts, and obtain H_{11}, H_{12}, H_{21}, and H_{22}, as expressed in (20).
- Step 4: Obtain the SFC of Fig. 2, as shown in Fig. 3.

2) Example: Here, as an example, the TOGI proposed in [21] is considered for implementing the two filters in Fig. 2.

[1]In special cases, it may be a real-coefficient transfer function.

Fig. 4 shows the block diagram of the resulting PLL, which is referred to as the dual TOGI-based PLL (DTOGI-PLL). The TOGI, which is highlighted by a dashed box in this structure, is an extension of the SOGI. To be more exact, the TOGI is realized by adding an integrator in parallel with the SOGI. This additional integrator makes the SOGI immune to the disturbance effect of a possible input dc component and, at the same time, provides an estimation of this component.

The SFC of the DTOGI-PLL is as shown in Fig. 3. The transfer functions H_{11}, H_{12}, H_{21}, and H_{22} in this representation can be readily obtained as expressed in (21) and (22) at the bottom of the next page by following the step-by-step procedure summarized at the end of the previous section.

3) Verification: The SFC of the DTOGI-PLL is supposed to be an alternative mathematically-equivalent representation of the DTOGI-PLL from the small-signal point of view. This section aims to evaluate this issue. To this end, the following tests are considered.

- Test 1: 0.25 p.u. voltage sag in phase *A* happens.
- Test 2: 0.05 p.u. dc component to phase *A* is added.
- Test 3: 10° phase jump happens.

Both simulation and experimental results of these tests are presented. The simulation results are obtained using Matlab/Simulink, and the experimental ones are based on the dSPACE 1006 platform. A Chroma 61845 grid simulator generates the three-phase grid voltage signals in the experimental verification.

Fig. 5 and 6 are the simulation and experimental results. Notice that, to save space, only the experimental results of Test 1 and 2 are shown here. Notice also that the experimental results only include the estimated frequency because the phase angle of the three-phase grid voltage signals is unknown. The main observation from the simulation and experimental results, which are completely in agreement, is that the DTOGI-PLL and its SFC have very close outputs and, therefore, are equivalent systems from the small-signal point of view.

The above tests were small-signal tests. In this stage, it may be interesting to compare the DTOGI-PLL and its SFC in response to a more severe disturbance. To this end, a quite large phase jump (30° phase jump) test is considered, which its results are shown in Fig. 7. A small difference between the results of the DTOGI-PLL and its SFC is observed. Understanding the reason behind this difference requires a brief explanation of the coupling between different variables in the PLL systems. In all PLLs, including the DTOGI-PLL, the phase and frequency variables are estimated in a common loop. It means that a phase jump results in some spurious transients in the estimated frequency (refer to [32] for more details). The magnitude of these transients is proportional to the magnitude of phase jump. In other words, a large phase jump causes large spurious transients in the estimated frequency. In obtaining the SFC of the DTOGI-FLL, however, it was assumed that the estimated frequency, which is fed back to the prefilter, is a constant. The inaccuracy caused by this assumption under large phase jumps is the main reason behind the difference between the results of the DTOGI-PLL and its SFC in Fig. 7.

As mentioned before, the dq-frame output impedance of a current-controlled VSC equipped with an advanced PLL can

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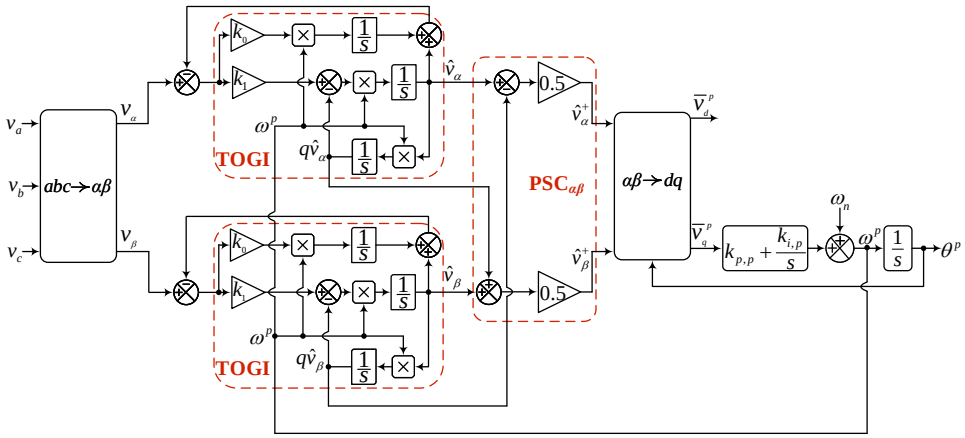

Fig. 4. Block diagram of the DTOGI-PLL. k_0 and k_1 are the control gains of the TOGI.

TABLE I
PLLs' CONTROL PARAMETERS

	Value of PLL's control parameters
DTOGI-PLL	$k_{p,p} = 0.443$ rad/s, $k_{i,p} = 16.873$ rad/s^2, $k_1 = \sqrt{2}$, $k_0 = 0.2$
3phEPLL	$k_{p,p} = 0.626$ rad/s, $k_{i,p} = 33.747$ rad/s^2, $\mu = 2\omega_n = 628.32$ rad/s
mSRF-PLL	$k_{p,p} = 0.684$ rad/s, $k_{i,p} = 48.625$ rad/s^2, $k_v = 142.17$ rad/s, $k_0 = 71.09$ rad/s
ROGI-PLL	$k_{p,p} = 1.064$ rad/s, $k_{i,p} = 57.61$ rad/s^2, $k_1 = 222.14$ rad/s, $\omega_l = 54.16$ rad/s

TABLE II
VSC PARAMETERS

Description	**Value**
Grid line-ground peak voltage	$120\sqrt{2}$
Input dc voltage (V_{dc})	600 V
Inductance of the VSC output filter (L)	1 mH
Resistance of the VSC output filter (R)	0 Ω
d-channel reference current (i_d^{ref})	200 A
q-channel reference current (i_q^{ref})	0 A
Grid angular frequency (ω^g)	$2\pi 50$ rad/s
Proportional gain of the current controller ($k_{p,cc}$)	0.04 Ω
Integrator gain of the current controller ($k_{i,cc}$)	5 Ω/s
Decoupling term (k_d)	0 Ω

be accurately obtained using the analytic equations reviewed in Section II if we have the SFC of that PLL. The correctness of this idea is verified for the case of the DTOGI-PLL here. To this end, the DTOGI-PLL is considered for the grid synchronization of the current-controlled VSC in Fig. 1(a). The analytical *dq*-frame output impedance of the VSC is then obtained using the SFC of the DTOGI-PLL and the analytical expressions in Section II. Finally, this analytical prediction is compared with the output impedance obtained using the frequency sweep simulation of the current-controlled VSC. The method presented in [33] is used for obtaining the *dq* impedance sweep. Fig. 8 shows the obtained results. Regardless of a small error in the very-low-frequency range of Z_{dq} (Fig. 8(b)), it is observed the analytic equation and frequency sweep simulation have well-matched results.

It is worth mentioning here that Z_{dq} (Fig. 8(b)) has a very small magnitude compared to the other elements of the impedance matrix in the low-frequency range, which makes its measurement using frequency sweep more sensitive to numerical issues. That is the main reason behind the small error in the very-low-frequency range of Fig. 8(b).

B. Case Study 2

Many advanced three-phase PLLs in the literature have a structure similar to Fig. 9 [15], [34], in which $\hat{v}_a$, $\hat{v}_b$, and $\hat{v}_c$ are the estimation of the fundamental component of v_a, v_b, and v_c, respectively, $q\hat{v}_a$, $q\hat{v}_b$, and $q\hat{v}_c$ are the quadrature (90° phase-shifted) versions of v_a, v_b, and v_c, respectively, and $\hat{v}^+_{abc}$ denotes the estimation of the grid voltage FFPS component in the abc frame. The prefiltering stage in this structure, as shown in Fig. 9, is implemented in the *abc* frame and includes three filters and a positive sequence calculator in the *abc* frame (PSC$_{abc}$). Each filter extracts the fundamental component of a phase signal and its quadrature (90° phase-shifted) version. The outputs of these filters are fed to the PSC$_{abc}$, which

$$H_{11}(s) = H_{22}(s) = \frac{k_1\omega_n s^5+(k_1^2+k_0k_1)\omega_n^2 s^4+5k_1\omega_n^3 s^3+(3k_1^2+4k_0k_1)\omega_n^4 s^2+4k_1\omega_n^5 s+2k_1^2\omega_n^6}{2s^6+4(k_0+k_1)\omega_n s^5+2(k_0^2+2k_0k_1+k_1^2+5)\omega_n^2 s^4+(16k_0+12k_1)\omega_n^3 s^3+(8k_0^2+12k_0k_1+4k_1^2+8)\omega_n^4 s^2+8k_1\omega_n^5 s+2k_1^2\omega_n^6} \quad (21)$$

$$H_{21}(s) = -H_{12}(s) = \frac{(k_1^2+k_0k_1)\omega_n^3 s^3+(k_1^2+4k_0k_1)\omega_n^5 s}{2s^6+4(k_0+k_1)\omega_n s^5+2(k_0^2+2k_0k_1+k_1^2+5)\omega_n^2 s^4+(16k_0+12k_1)\omega_n^3 s^3+(8k_0^2+12k_0k_1+4k_1^2+8)\omega_n^4 s^2+8k_1\omega_n^5 s+2k_1^2\omega_n^6} \quad (22)$$

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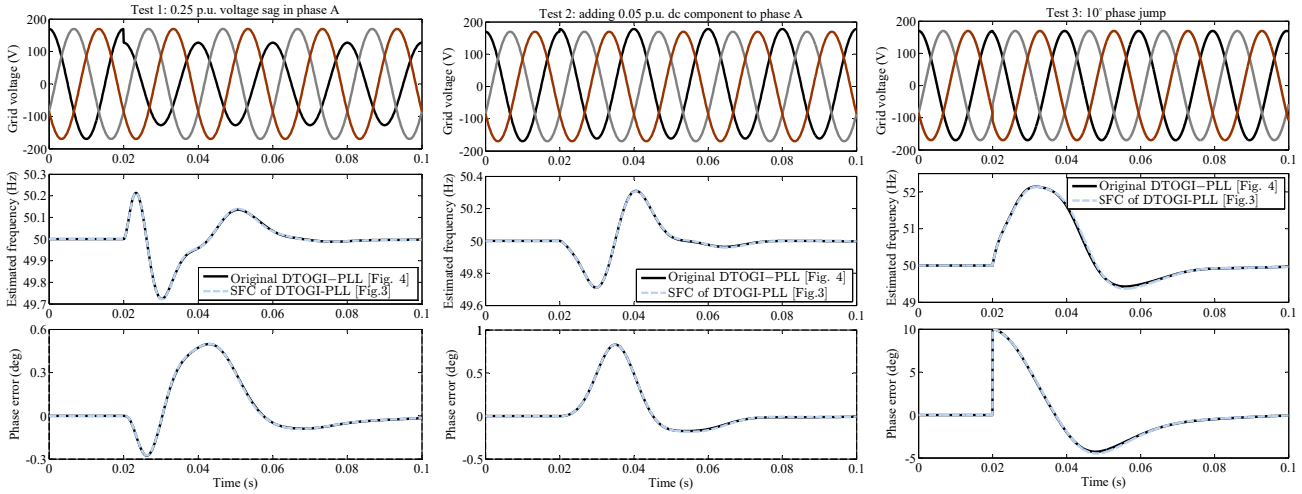

Fig. 5. Numerical comparison between the DTOGI-PLL [Fig. 4] and its SFC [Fig. 3]. (a) Test 1. (b) Test 2. (c) Test 3. The control parameters of the DTOGI-PLL can be found in Table I. The transfer functions H_{11}, H_{12}, H_{21}, and H_{22} in the SFC of the DTOGI-PLL are as expressed in (21) and (22). The nominal amplitude and nominal frequency of the grid voltage throughout this paper are $120\sqrt{2}$ and 50 Hz, respectively. Both the DTOGI-PLL and its SFC are discretized with a sampling frequency of 20 kHz.

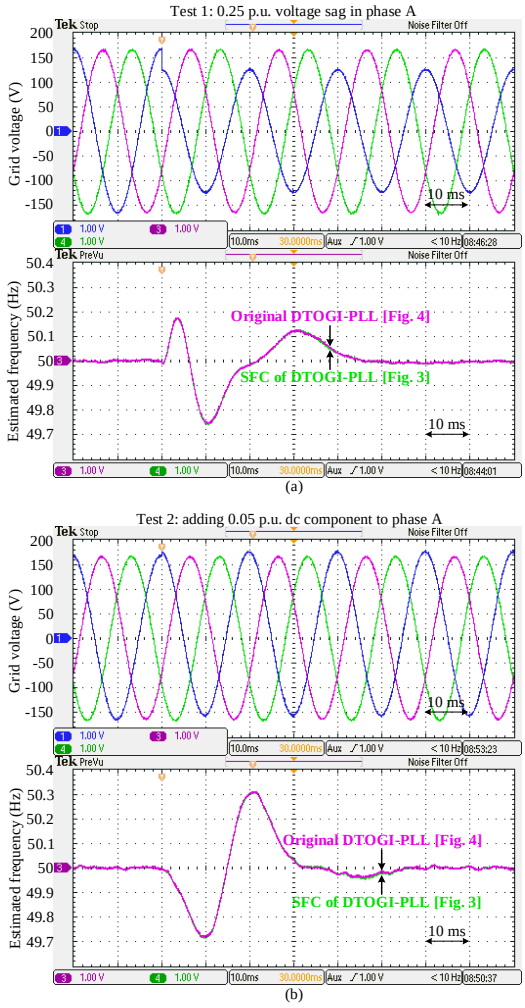

Fig. 6. Experimental comparison between the DTOGI-PLL [Fig. 4] and its SFC [Fig. 3]. (a) Test 1. (b) Test 2.

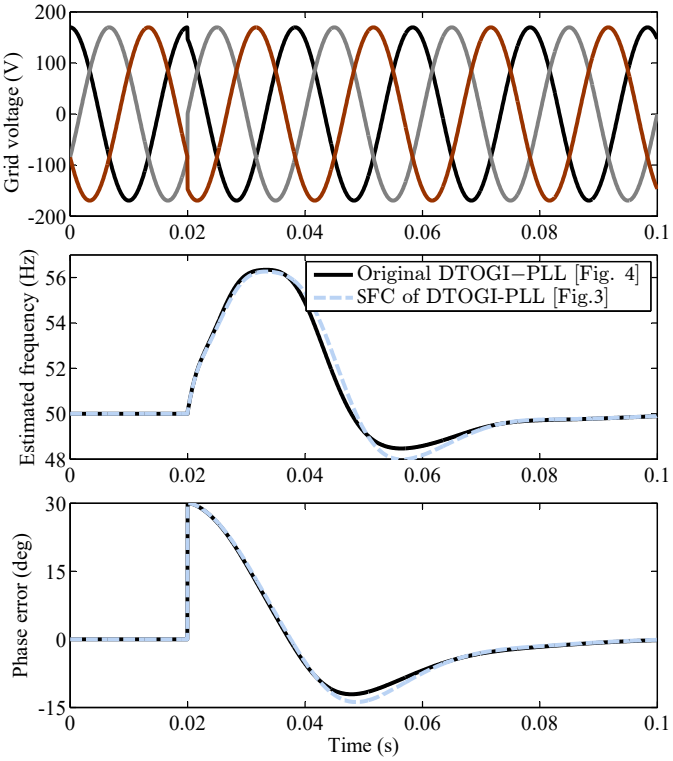

Fig. 7. A transient response comparison between the DTOGI-PLL [Fig. 4] and its SFC [Fig. 3] in response to a 30° phase jump.

calculates the FFPS component of the grid voltage in the *abc* frame based on the ISC theory, as expressed below:

$$\begin{aligned}\hat{v}_a^+ &= \tfrac{1}{3}\hat{v}_a - \tfrac{1}{6}\left(\hat{v}_b + \hat{v}_c\right) - \tfrac{1}{2\sqrt{3}}\left(q\hat{v}_b - q\hat{v}_c\right)\\ \hat{v}_b^+ &= \tfrac{1}{3}\hat{v}_b - \tfrac{1}{6}\left(\hat{v}_c + \hat{v}_a\right) - \tfrac{1}{2\sqrt{3}}\left(q\hat{v}_c - q\hat{v}_a\right)\\ \hat{v}_c^+ &= \tfrac{1}{3}\hat{v}_c - \tfrac{1}{6}\left(\hat{v}_a + \hat{v}_b\right) - \tfrac{1}{2\sqrt{3}}\left(q\hat{v}_a - q\hat{v}_b\right).\end{aligned} \tag{23}$$

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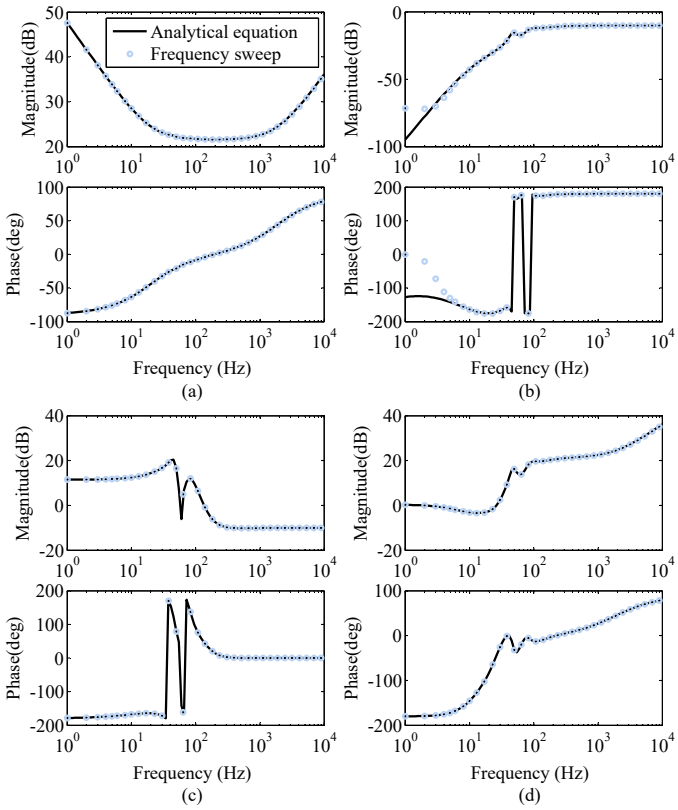

Fig. 8. *dq*-frame output impedance of the current-controlled VSC in Fig. 1(a) with the DTOGI-PLL for the grid synchronization. (a) Z_{dd}. (b) Z_{dq}. (c) Z_{qd}. (d) Z_{qq}. The solid lines are the analytically obtained output impedance, and circles are the results of the frequency sweep simulation. The values of the DTOGI-PLL and VSC parameters can be found in Tables I and II, respectively. Average converter model is considered in the frequency sweep simulation.

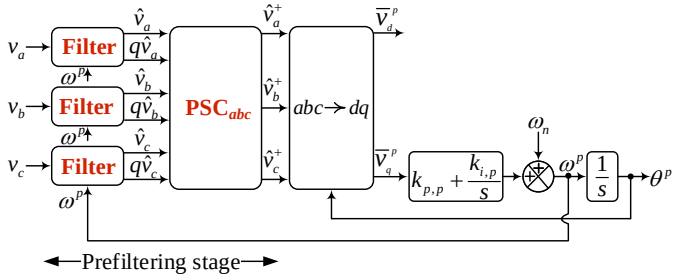

Fig. 9. A popular form of advanced three-phase PLLs characterized by a prefilter in the abc frame.

1) Obtaining SFC: As far as the phase angle estimation of the FFPS component of the grid voltage is concerned, as it is the case here, Fig. 9 and Fig. 2 are the same PLLs.[2] The reason is that, roughly speaking, the input signals in Fig. 2 and 9 are subjected to the same course of actions, but in a different order, before transferring to the *dq* frame. It implies that the SFC of Fig. 9 will be the same as that of Fig. 2 [see Fig. 3] and, therefore, it can be obtained by following the same procedure (refer to the end of Section III-A1). An example is presented in what follows to make this fact more clear.

[2]The difference between the PLL structures shown in Fig. 2 and 9 lies in the ability of estimating the zero sequence component. Without using any extra filter, the PLL structure in Fig. 9 can be easily extended to provide an accurate estimation of the zero sequence component of the grid voltage. It is, however, not the case for the PLL structure in Fig. 2.

2) Example: Fig. 10(a) illustrates an advanced three-phase PLL, which uses three EPLLs as the filter for extracting the fundamental component of the three-phase input signals and their quadrature version [25]. This structure is briefly referred to as the 3phEPLL here. The EPLL can be self-adaptive or it can receive an estimation of the grid frequency from the SRF-PLL. The latter case is considered here. By changing the order of operations on the three-phase input signals before transferring them to the *dq*, an alternative representation of the 3phEPLL can be obtained as depicted in Fig. 10(b). Now, using this structure, the step-by-step procedure summarized at the end of Section III-A1 can be followed for obtaining the SFC of the 3phEPLL. Notice that the SFC of 3phEPLL will be as shown in Fig. 3.

Here, a minor challenge can be finding the input-output transfer functions of the EPLL, as it involves the calculations of sine and cosine functions in its structure [see the dashed box in Fig. 10(a)]. This challenge has already been addressed in the literature. According to the guidelines presented in [35], if the feedback signal ω^p is assumed to be constant, the characteristic transfer functions of the EPLL in Fig. 10(b) can be obtained as

$$\begin{aligned} H_D(s) &= \frac{\hat{v}_\alpha(s)}{v_\alpha(s)} = \frac{\hat{v}_\beta(s)}{v_\beta(s)} = \frac{\mu s}{s^2+\mu s+(\omega^p)^2} \\ H_Q(s) &= \frac{q\hat{v}_\alpha(s)}{v_\alpha(s)} = \frac{q\hat{v}_\beta(s)}{v_\beta(s)} = \frac{\mu\omega^p}{s^2+\mu s+(\omega^p)^2}. \end{aligned} \tag{24}$$

Using (24) and the step-by-step procedure in Section III-A1, the transfer functions H_{11}, H_{12}, H_{21}, and H_{22} in the SFC of the 3phEPLL can be obtained as

$$\begin{aligned} &H_{11}(s) = H_{22}(s) \\ &= \frac{\mu s^3+\mu^2 s^2+4\mu\omega_n^2 s+2\mu^2\omega_n^2}{2s^4+4\mu s^3+(2\mu^2+8\omega_n^2)s^2+8\mu\omega_n^2 s+2\mu^2\omega_n^2} \end{aligned} \tag{25}$$

$$\begin{aligned} &H_{21}(s) = -H_{12}(s) \\ &= \frac{\mu^2\omega_n s}{2s^4+4\mu s^3+(2\mu^2+8\omega_n^2)s^2+8\mu\omega_n^2 s+2\mu^2\omega_n^2}. \end{aligned} \tag{26}$$

3) Verification: Here, a comparison between the 3phEPLL and its SFC in response to the same tests as those defined in Section III-A3 is carried out. The comparative simulation and experimental results can be observed in Figs. 11 and 12, respectively. It is observed that the simulation and experimental results are completely in agreement, which confirms the 3phEPLL and its SFC are equivalent from the small-signal point of view.

To further support the small-signal equivalence of the 3phEPLL and its SFC, the 3phEPLL is considered for the grid synchronization of the current-controlled VSC in Fig. 1(a), and its *dq*-frame output impedance is obtained using the frequency sweep simulation. These simulation results are then compared with the analytical *dq*-frame impedance model of the VSC (see Section II), which is obtained using the SFC of the 3phEPLL. The obtained results can be observed in Fig. 13. It can be observed that, regardless of a small error in the low-frequency range of Z_{dq} [Fig. 13(b)], the frequency sweep simulation and

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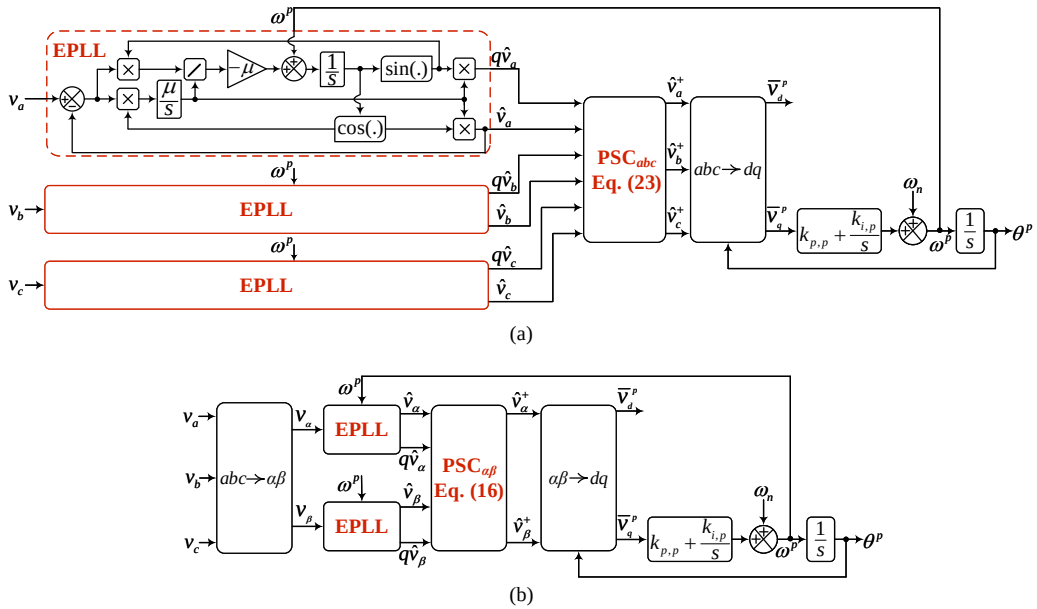

Fig. 10. (a) Block diagram of the 3phEPLL. (b) Alternative representation of the 3phEPLL.

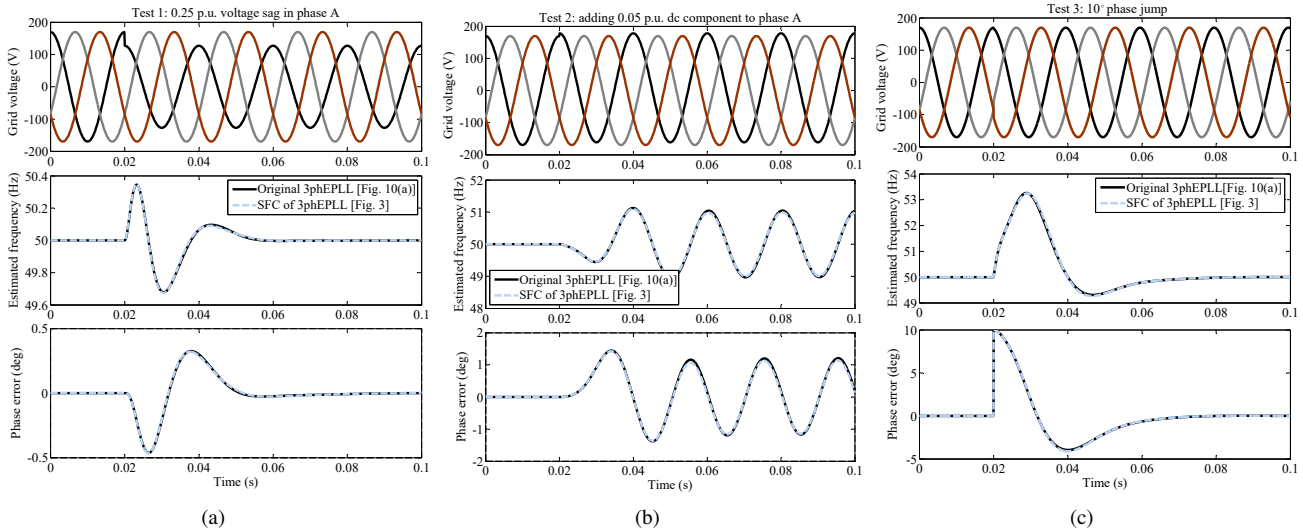

Fig. 11. Numerical comparison between the 3phEPLL [Fig. 10(a)] and its SFC [Fig. 3]. (a) Test 1. (b) Test 2. (c) Test 3. The control parameters of the 3phEPLL can be found in Table I. The transfer functions H_{11}, H_{12}, H_{21}, and H_{22} in the SFC of the 3phEPLL are as expressed in (25) and (26).

analytical prediction have well-matched results.

C. Case Study 3

We often know the SRF-PLL, which is the basic building block of almost all advanced three-phase PLLs, as shown in Fig. 14(a). The SRF-PLL, however, has an alternative mathematically-equivalent representation, which can be observed in Fig. 14(b) [36]. The key feature of this representation is generating the error between the grid voltage three-phase signals and their FFPS component, which can be used for detecting the grid voltage disturbance components (dc offset, harmonics, interharmonics, and FFNS component) and mitigating their adverse effects on the SRF-PLL performance, as shown in Fig. 15 [36]. Some interesting points about this PLL structure are as follows:

- The filter block in Fig. 15 works in parallel with the SRF-PLL.
- The filter block may itself include N parallel sub-filters, where each one is tuned to a concerned disturbance frequency. These sub-filters are not necessarily ordinary filters. They can, for example, be some other SRF-PLLs tuned to concerned harmonic frequencies [37].
- Contrary to the PLL structures in Fig. 2 and 9, where the filters are adapted to frequency changes through a frequency feedback loop to avoid phase and amplitude errors in the PLL output under frequency drifts, the filter block in Fig. 15 is not necessary to be frequency-adaptive. The reason is that this filter, from the point of view of estimating the FFPS component, is located within the control loop and, therefore, does not cause

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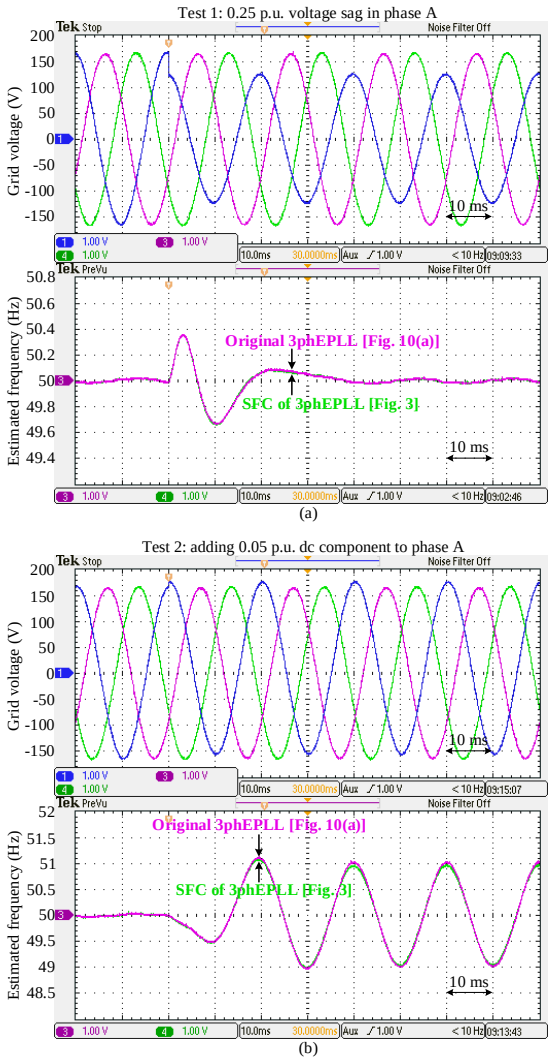

Fig. 12. Experimental comparison between the 3phEPLL [Fig. 10(a)] and its SFC [Fig. 3]. (a) Test 1. (b) Test 2.

phase and amplitude errors in the PLL output under off-nominal frequencies. However, if the presence of harmonic disturbances under off-nominal frequencies is expected, using adaptive filters is recommended.

By considering the fact that Fig. 14(a) is the SFC of Fig. 14(b), one may easily obtain the SFC of Fig. 15 by transferring the dynamics of its filter block to the *dq* frame. To better understand this procedure, a simple example is presented in what follows.

It is known that the presence of the dc offset in the grid voltage may have adverse effects on the PLL and, therefore, grid-connected power converter performance.[3] In [21], it is demonstrated that this problem can be easily addressed by considering the filter block in Fig. 15 as a simple integrator. Fig. 16(a) shows this idea, which is called the modified SRF-PLL (mSRF-PLL).

[3]The presence of the dc offset in the grid voltage causes fundamental-frequency oscillatory errors in the output phase angle of the PLL, which may cause a dc injection by the converter to the grid [38].

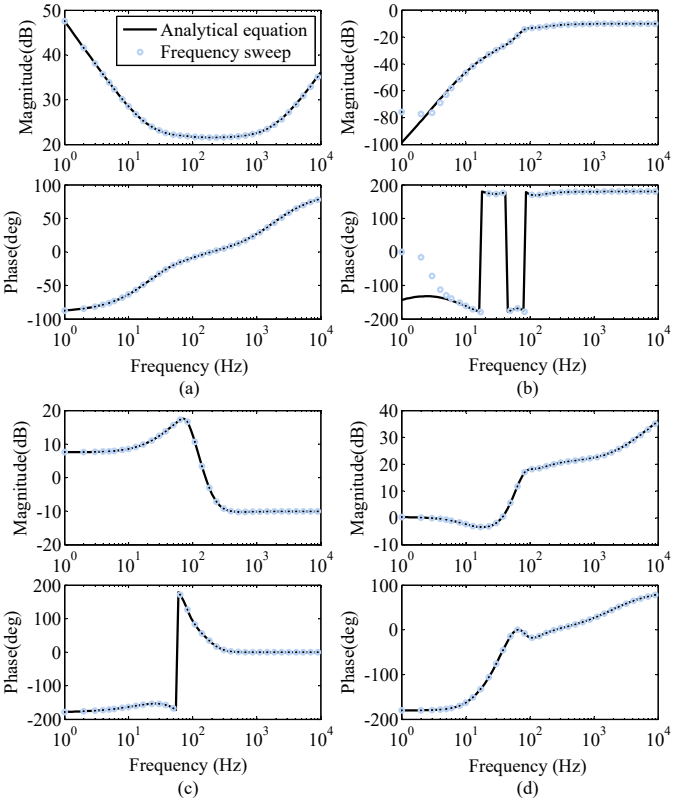

Fig. 13. *dq*-frame output impedance of the current-controlled VSC in Fig. 1(a) with the 3phEPLL for the grid synchronization. (a) Z_{dd}. (b) Z_{dq}. (c) Z_{qd}. (d) Z_{qq}. The solid lines are the analytically obtained output impedance, and circles are the results of the frequency sweep simulation. The values of the 3phEPLL and VSC parameters can be found in Tables I and II, respectively. Average converter model is considered in the frequency sweep simulation.

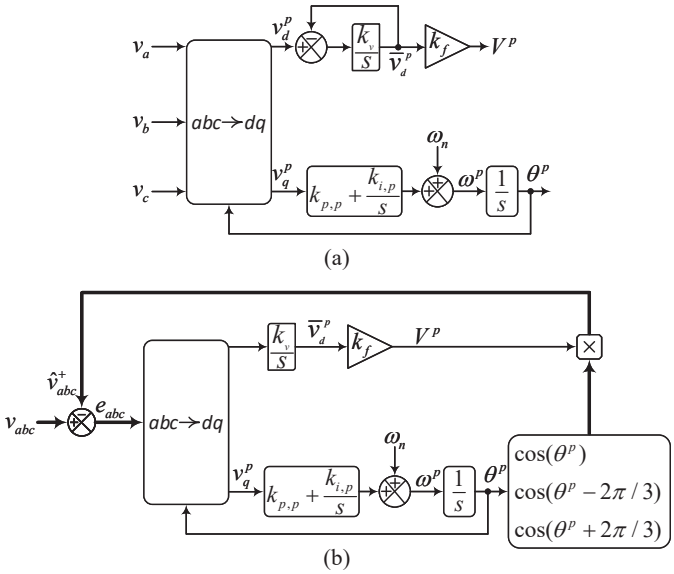

Fig. 14. (a) SRF-PLL. (b) Alternative representation. V^p is the estimated amplitude. k_f is a scaling factor, which depends on the Park's Transformation. Here, it is equal to $k_f = \sqrt{2/3}$.

For obtaining the SFC of the mSRF-PLL, all elements before the Park's transformation need to be transferred to the *dq* frame. Recall that Fig. 14(a) is the SFC of Fig. 14(b).

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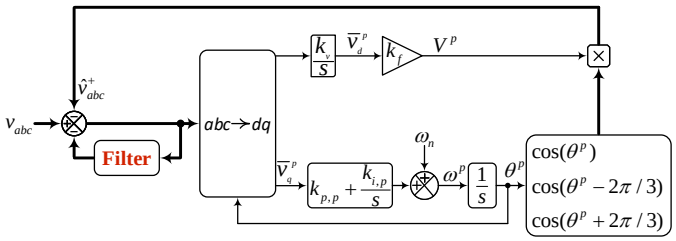

Fig. 15. A popular form of advanced three-phase PLLs characterized by a parallel filter.

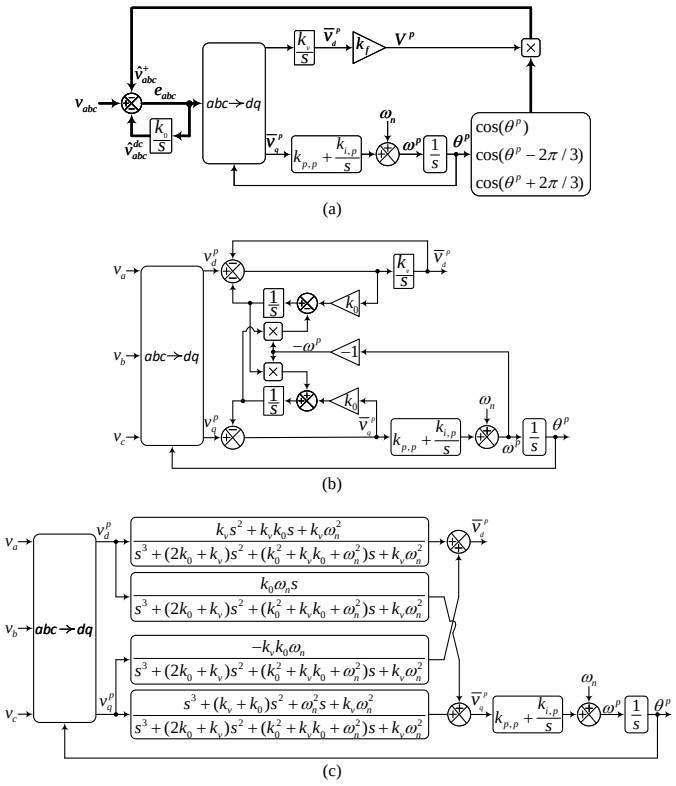

Fig. 16. (a) Block diagram of the mSRF-PLL. (b) Alternative representation of the mSRF-PLL, which is obtained by transferring the filtering stage before its Park's transformation to the *dq* frame. (c) SFC of mSRF-PLL.

Considering this fact and the guidelines presented in Section III-A1, an alternative mathematically-equivalent representation of Fig. 16(a) can be obtained as depicted in Fig. 16(b). Notice that the integrator in the *abc* frame, i.e., k_0/s, turns to a reduced-order generalized integrator (ROGI) with the center frequency at $-\omega^p$ in the *dq* frame, i.e., $k_0/(s+j\omega^p)$. By fixing the center frequency at $-\omega_n$ and applying some simple mathematical manipulations, the SFC of the mSRF-PLL can be obtained as shown in Fig. 16(c).

Figs. 17 and 18 are the comparative simulation and experimental results of the mSRF-PLL and its SFC in response to the tests defined in Section III-A3. These results demonstrate that they are equivalent from the small-signal point of view. Fig. 19, which compares the *dq*-frame output impedance of the VSC in Fig. 1(a) obtained using frequency sweep simulation with the analytically calculated one, further supports this equivalence. Notice that in the frequency sweep simulation, the actual mSRF-PLL is used for the grid synchronization of the VSC, and the analytical prediction is based on the SFC of the mSRF-PLL.

IV. Discussion

A. Complex-Coefficient Filters

The prefiltering stages in Figs. 2 and 9, as it was discussed before, involve using a PSC, which calculates the FFPS component of the grid voltage from the outputs of filters in the $\alpha\beta$ or *abc* frame. Each filter in these PLLs operates only on a single signal and extracts its fundamental component and its quadrature version. Such a filter is often called a *real* filter. Another type of filter, which is highly popular in designing PLLs, is the *complex-coefficient* filter (CCF) [15], [39]. A CCF, which operates simultaneously on two orthogonal signals (axes), has an asymmetrical frequency-response around zero Hz and, consequently, a sequence-selective (frequency-selective) property. Thanks to this property, a complex-coefficient prefilter does not require a PSC. The key points about obtaining the SFC of a PLL with a complex-coefficient prefilter are as follows:

- A CCF-based prefilter is often implemented in the $\alpha\beta$ frame [39]. In this case, the procedure for obtaining the SFC of the PLL is the same as what discussed before in Section III-A1.
- Implementing CCF-based prefilters in mixed $\alpha\beta/dq$ frames or abc/dq frames have also been reported in the literature [40], [41]. In this case, one needs to obtain the pure $\alpha\beta$ frame counterpart of the prefilter before performing the procedure presented in Section III-A1 for obtaining the SFC of the PLL.

B. Presence of Lag Filter in the Frequency Feedback

In the PLL structures shown in Fig. 2 and 9, which were studied in Sections III-A and III-B, respectively, the estimated frequency is directly fed back to the prefiltering stage. Sometimes, however, a lag filter may also be included in the frequency feedback loop [42], [43]. There are two main reasons for using such a filter. The first one is mitigating the dynamic coupling between the SRF-PLL and its prefilter and improving the stability margin, and the second one is providing additional degrees of freedom for better tuning of the control parameters and achieving a better speed/accuracy trade-off. Using such a lag filter in the frequency feedback loop, however, may make obtaining the SFC of the PLL a bit complicated. Through a simple example in what follows, this section aims to show how this difficulty can be tackled.

In Fig. 20(a), it is observed that the prefiltering stage is a simple first-order complex bandpass filter (CBF), which is constructed by using a ROGI in a unity feedback loop [39]. The center frequency of the ROGI and, therefore, the CBF is adapted to frequency changes through a frequency feedback loop. This feedback loop contains a lag filter with the transfer function $L(s)$. It is assumed that the lag filter has a unity dc gain. For obtaining the SFC of this PLL, as discussed in Section III-A1, the dynamics of its prefilter need to be

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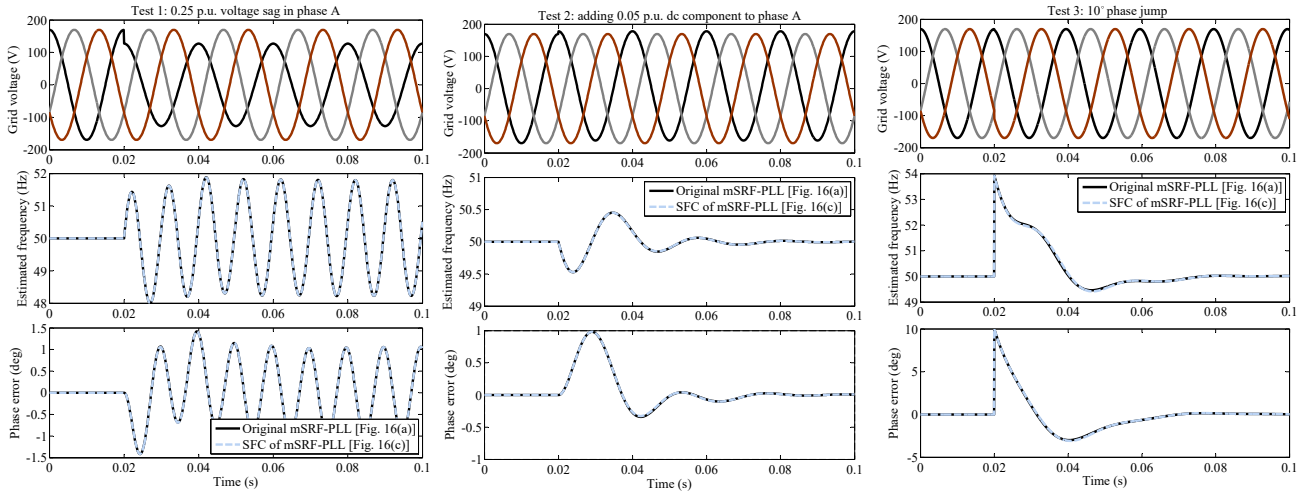

Fig. 17. Numerical comparison between the mSRF-PLL [Fig. 16(a)] and its SFC [Fig. 16(c)]. (a) Test 1. (b) Test 2. (c) Test 3. The control parameters of the mSRF-PLL can be found in Table I.

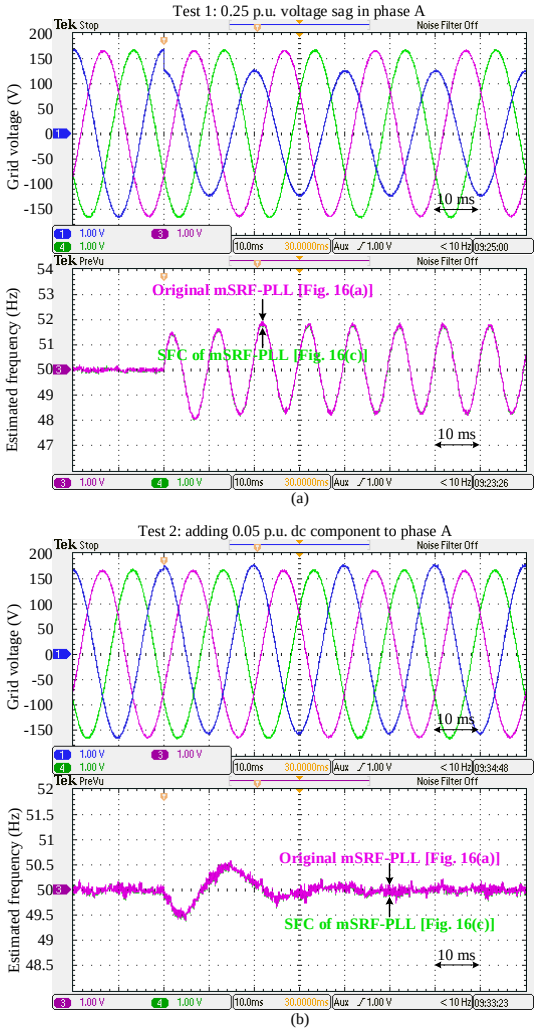

Fig. 18. Experimental comparison between the mSRF-PLL [Fig. 16(a)] and its SFC [Fig. 16(c)]. (a) Test 1. (b) Test 2.

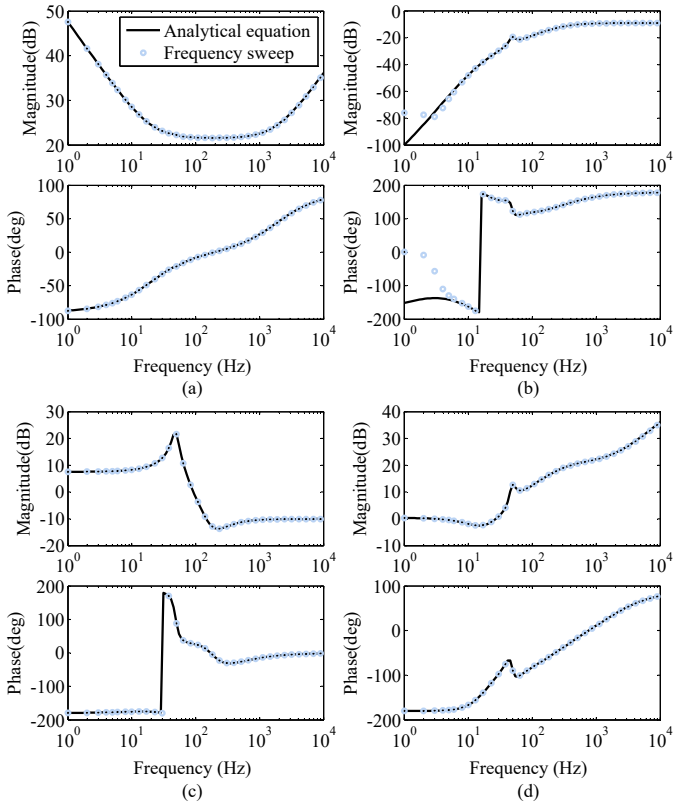

Fig. 19. dq-frame output impedance of the current-controlled VSC in Fig. 1(a) with the mSRF-PLL for the grid synchronization. (a) Z_{dd}. (b) Z_{dq}. (c) Z_{qd}. (d) Z_{qq}. The solid lines are the analytically obtained output impedance, and circles are the results of the frequency sweep simulation. The values of the mSRF-PLL and VSC parameters can be found in Tables I and II, respectively. Average converter model is considered in the frequency sweep simulation.

transferred to the dq frame. As mentioned before, such a transfer is corresponding to a frequency shift equal to ω^p in the frequency response of the prefilter. Therefore, the center frequency of the CBF changes from $\bar{\omega}^p$ in the $\alpha\beta$ frame to $\bar{\omega}^p - \omega^p$ in the dq frame [see Fig. 20(b)]. It is observed that the

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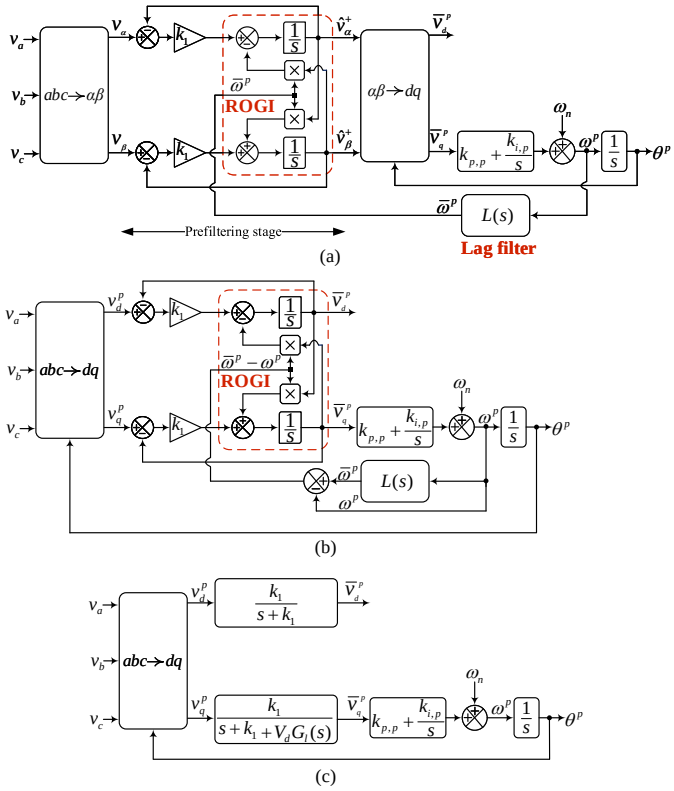

Fig. 20. (a) Block diagram of the ROGI-PLL. (b) Alternative representation. (c) SFC of the ROGI-PLL. $G_l(s) = \frac{(1-L(s))(k_{p,p}s+k_{i,p})}{s}$.

presence of the lag filter in the frequency feedback loop causes some nonlinearities, which cannot be ignored; otherwise, it causes a considerable inaccuracy. It implies that obtaining the SFC of the PLL in the presence of a lag filter in its frequency feedback loop involves linearization.

From Fig. 20(b), the time derivatives of the signals $\bar{v}_d^p$ and $\bar{v}_q^p$ can be expressed as

$$\frac{d\bar{v}_d^p}{dt} = k_1(v_d^p - \bar{v}_d^p) - \overbrace{(\bar{\omega}^p - \omega^p)\bar{v}_q^p}^{\text{nonlinear term}} \tag{27a}$$

$$\frac{d\bar{v}_q^p}{dt} = k_1(v_q^p - \bar{v}_q^p) + \underbrace{(\bar{\omega}^p - \omega^p)\bar{v}_d^p}_{\text{nonlinear term}}. \tag{27b}$$

The nonlinearity of (27a) and (27b) are because of the highlighted terms. We know that the working points of the signals $\bar{v}_d^p$ and $\bar{v}_q^p$ are the same as those of the signals v_d^p and v_q^p, i.e., V_d and V_q, respectively, where $V_q = 0$. We also know that the working point of the frequency error term $\bar{\omega}^p - \omega^p$ is equal to zero. Considering these, (27a) and (27b) can be approximated by

$$\frac{d\bar{v}_d^p}{dt} \approx k_1(v_d^p - \bar{v}_d^p) \tag{28a}$$

$$\frac{d\bar{v}_q^p}{dt} \approx k_1(v_q^p - \bar{v}_q^p) + V_d(\bar{\omega}^p - \omega^p) \tag{28b}$$

where, according to Fig. 20(b), the frequency error term $\bar{\omega}^p - \omega^p$ in the Laplace domain is equal to

$$\bar{\omega}^p(s) - \omega^p(s) = -\frac{\overbrace{(1-L(s))(k_{p,p}s+k_{i,p})}^{G_l(s)}}{s}\bar{v}_q^p(s). \tag{29}$$

Using (29), (28) can be expressed in the Laplace domain as

$$\bar{v}_d^p(s) \approx \frac{k_1}{s+k_1}v_d^p(s) \tag{30a}$$

$$\bar{v}_q^p(s) \approx \frac{k_1}{s+k_1+V_dG_l(s)}v_q^p(s). \tag{30b}$$

Using (30), the SFC of the ROGI-PLL can be obtained as depicted in Fig. 20(c).

Figs. 21 and 22, which are the comparative simulation and experimental results of the ROGI-PLL and its SFC in response to the tests defined in Section III-A3, confirm that they are equivalent from the small-signal point of view.

C. Hidden Lag Filter in Frequency Feedback Loop

The lag filter in the frequency feedback loop may sometimes be hidden as the frequency may be tapped from a different point than the standard one. This section aims to clarify this fact.

The input of the voltage-controlled oscillator (VCO) is the standard point of tapping the frequency in the PLL structure. It is, however, not the only option. In fact, one may also tape the frequency from the output of the integrator of the PI controller [15], [25], [44]. For example, in Fig. 23(a), this alternative point is used for recording the frequency and feeding back to the prefiltering stage. It can be proved that feeding back the frequency from this point is mathematically equivalent to take the frequency from the standard point and pass it through a first-order low-pass filter (LPF) with the cutoff frequency $k_{i,p}/k_{p,p}$, as shown in Fig. 23(b).

V. Conclusion

The main aim of this paper was to demonstrate the procedure for including the dynamics of advanced PLLs in the *dq*-frame impedance model of a three-phase grid-connected VSC. To this end, an overview of the *dq*-frame impedance modeling of a three-phase grid-tied VSC with a PLL as shown in Fig. 1(c) was presented. It was then discussed that all advanced three-phase PLLs have an alternative representation as Fig. 1(c), called the standard-form counterpart (SFC). It means that the *dq*-frame output impedance of a VSC equipped with an advanced PLL can be easily obtained by finding the SFC of its PLL. To gain a deeper insight into this idea, three case studies were presented. In each case, a class of advanced PLLs was introduced, obtaining their SFC was explained, an example was presented, and some verification results were presented. Finally, some discussions about some more specific cases that one may encounter during the procedure for obtaining the SFC of advanced PLLs were presented.

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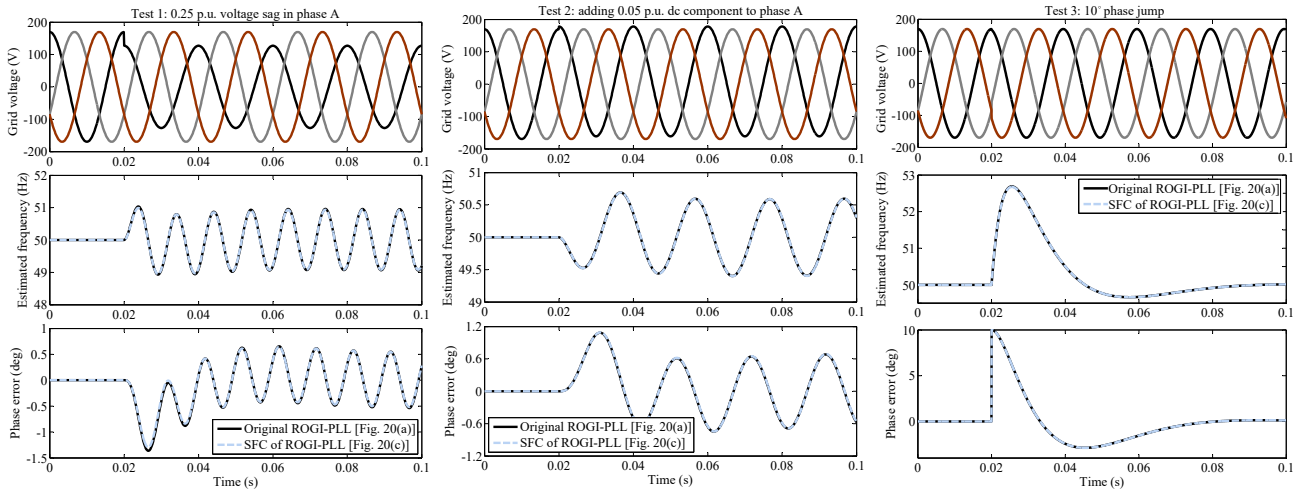

Fig. 21. Numerical comparison between the ROGI-PLL [Fig. 20(a)] and its SFC [Fig. 20(c)]. (a) Test 1. (b) Test 2. (c) Test 3. The lag filter in the frequency feedback loop of the ROGI-PLL is considered to be a first-order LPF with the cutoff frequency ω_l. The control parameters of the ROGI-PLL can be found in Table I.

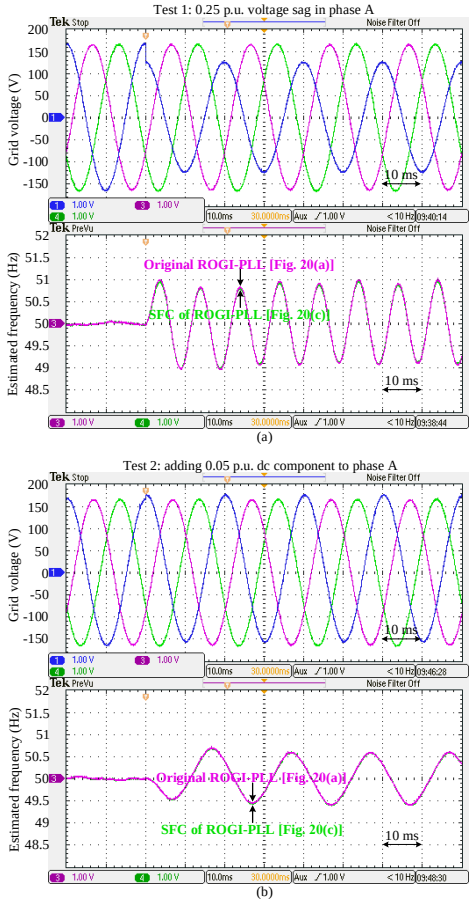

Fig. 22. Experimental comparison between the ROGI-PLL [Fig. 20(a)] and its SFC [Fig. 20(c)]. (a) Test 1. (b) Test 2.

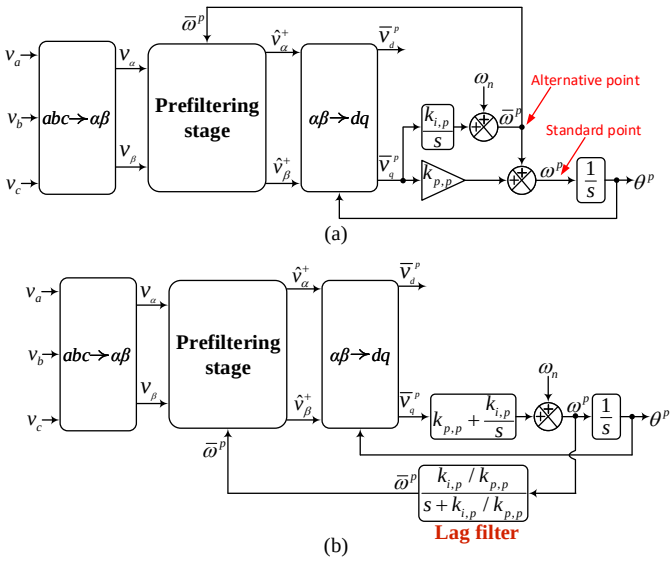

Fig. 23. (a) PLL uses the output of the integrator of the PI controller for recording the frequency and feeding back to its prefilter. (b) Alternative mathematically-equivalent representation.

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