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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2020.3018535

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Active Power Cycling Test Bench for SiC Power MOSFETs - Principles, Design and Implementation

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***Abstract*—One way to achieve the best in class reliability is the implementation of a Design for Reliability methodology into the design process in order to estimate the lifetime of each individual critical component, based on proper reliability models for failure modes. The main drawback of the above-mentioned approach is that it relies on handbook-based reliability models, which usually are only accurate for particular components. This fact causes the necessity to develop a testing procedure for SiC power MOSFET, to determine its reliability model parameters. Such model could be further implemented in the Design for Reliability methodology for the high performance power supply design process. In this paper, a cost effective and industrial friendly laboratory setup for Active Power Cycling of SiC power MOSFETs in SOT-227b housing is presented. By this example, various control strategies for accelerated lifetime testing, degradation indicators for wear out condition monitoring and junction temperature estimation methods are compared on their impact on test results and complexity in either laboratory setup and its maintenance procedure. Technical issues related to the start-up of Active Power Cycling test and failure detection algorithm are discussed. Finally, test results for SiC power MOSFETs subjected to over 63355 power cycles are presented.**

***Index Terms*—Semiconductor device reliability, Power MOSFETs, Reliability engineering**

I. Introduction

Power electronics is widely used in many industries - e.g. electric drives as part of transmission lines in factories or the mining industry, DC-DC converters as the output stage in battery charger systems, AC-DC converters as active rectifiers in modern high performance power supplies, etc. [1]. So the reliability of the whole complex industrial system is highly dependent on the reliability of the power electronic converters used in such a system.

The Design for Reliability (DfR) methodology is widely used to increase the reliability of all sort of complex systems and is based on a simple idea - the reliability of each component should be assessed for pre-defined stress levels to estimate Mean Time To Failure (MTTF) of the whole system (e.g. power electronic converter [2], [3]) or subsystem (e.g. single DC-DC converter from a PV farm [4]). It consists of the following steps [5], [6]:

1) mission profile and environmental parameters definition,
2) system-level mission profile evaluation,
3) circuit modelling,
4) stressors levels evaluation for critical components,
5) reliability evaluation for critical components,
6) system-level reliability assessment.

A good example of a power electronic converter which has to meet high reliability requirements is a water-cooled power supply for plasma processing applications. Plasma processing techniques are widely used for e.g. integrated circuit or LCD screen manufacturing. A typical manufacturing process may consists of $50 - 300$ different steps. In each step of the process, a different mixture of gases is injected into a plasma chamber to build up a nanometer-thin layer. If only a single step were interrupted, e.g. by power converter failure, the sputtered layer would be distorted, which might significantly change the properties of the whole stack-up. In such case, the manufactured batch of product would be wasted, causing significant financial losses. Thus, demand for high reliability of the equipment used in a manufacturing process is easy to understand. In this case, the DfR methodology could be used as follows. First, the expected mission profile has to be defined - output voltage/current/power, on time, off time, application (e.g. substrate bias [7], magnetron sputtering [8], etching [9]), etc. Then, environmental parameters have to be included - e.g. ambient temperature, coolant temperature, relative humidity, mains voltage, etc. Based on these data, a mission profile for the whole system and its subsystems is defined - e.g. power demand and cooling capabilities. Those curves are the input data in the next step of the DfR methodology - circuit modelling, which has to be performed to determine e.g. power losses and exact stress levels for the chosen critical components. In the next step, the MTTF for component should be estimated based on the calculated stress levels and known Probability Density Function (PDF). Lastly, the overall lifetime of power semiconductors, subsystems and the whole system should be calculated. One drawback of this approach is that for each critical component, e.g. power semiconductors, there are numerous different failure

Manuscript received April 07, 2020; revised June 30, 2020; accepted August 05, 2020. This work was supported in part by the Polish Ministry of Science and Higher Education Department under first edition of "Doktorat wdrozeniowy" programme.

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modes and each of them are accelerated by various stressors. Therefore, PDF parameters for each failure mode should be presented as a function of stress level for better accuracy [10]. Another problem is that the parameters of PDF of each failure mode are unique for each component as they depend on the structure of the component (e.g. thickness and length of wire bonds) and manufacturing process (e.g. cooling ramp) of the power semiconductor itself. Typically, PDFs are defined during the reliability testing - a timely analysis to wear out - of a pristine device. For this purpose Accelerated Lifetime Testing (ALT) is used, to accelerate the aging of devices and to obtain reliability data in a short time.

The experiments presented above have main obstacles related to the DfR methodology - proper lifetime estimation requires detailed knowledge about used components. Unfortunately, such data as PDFs are difficult to obtain for customers. This fact provides a motivation to start studying an easy and low-cost reliability model parameter evaluation.

The main advantages of SiC power MOSFETs over Si devices are their $300-400$ times lower on-state channel resistance ($R_{DS_{on}}$) and significantly lower parasitic capacitance, which allows for operation at higher switching frequencies [11]. A third advantage of SiC MOSFETs over Si equivalents is their higher maximum junction temperature (T_J) [12]. These properties make the SiC power device perfect to fit for specialized, high performance power supplies for industrial applications. An excellent example of such a non-typical power converter is the above-mentioned power supply for plasma processing systems.

For this purpose, a reliability model parameter identification for $1200\ V,\ 70\ A$ SiC power MOSFETs has been initiated, as this device technology is becoming increasingly popular in the power electronics industry, due to the recent qualification of SiC power modules for the automotive industry [13].

This paper presents a comparison of different strategies for ALT of encapsulated semiconductor devices and technical issues related to the start-up of such tests in the scope of complexity of laboratory setups themselves and their impact on test results. In addition, the current status of reliability modeling of Si and wide-band gap power MOSFETs is presented. Based on this evaluation, Active Power Cycling (APC) of SiC power MOSFETs in $SOT-227b$ housing is defined as an interesting new research case study.

In section II the methodology of accelerated testing is presented with a detailed comparison of power cycling and thermal cycling, using different end-of-life criteria and challenges related to the interpretation of ALT results. Moreover, the impact of different heating profiles on the test results is also discussed. Afterwards, in section III, technical issues related to the preparation of ALT for semiconductor devices are presented. As a result, the practical realisation of different control strategies, junction temperature estimation methods and health indicator measurement procedures are discussed. The presented evaluation was performed during the preparation of a laboratory setup for APC of SiC power MOSFETs in an $SOT-227b$ housing. The main technical aspects of this laboratory setup are presented in section III. In addition, the impact of methodical and technical aspects on overall cost of laboratory setup and testing procedure are presented across these sections. In section IV, test results are presented - how electrical parameters of tested MOSFETs changed over time, how many samples failed during testing and what was the root-cause of the failures detected. Finally, in section V conclusions are given and summary of all the results presented.

II. Accelerated Life Test Methodology

In the case of encapsulated power semiconductors (power MOSFETs, diodes, IGBTs, etc.) the main stressors are maximum junction temperature [14], temperature swing during a single thermal cycle [15], blocking voltage [16], relative humidity [17] and gate voltage [18]. Each of these stressors accelerate at least one of the following failure modes, which are typical for encapsulated power semiconductors: solder delamination, solder joint fatigue, bond wire lift-off [19], bond wire heel-cracking [20], brittle cracking [21], corrosion [22], gate oxide time dependent breakdown [23], single event effects [24], etc. Various researchers have shown that such failures can be modeled with a proper PDF [25]. One of the known examples of such an approach is the usage of a Weibull model to describe fatigue of solder interconnection [26] or time-dependent dielectric breakdown in SiC power semiconductors [27]. Typically, researchers have used Thermal Cycling (TC) and Power Cycling (PC), referred also as *passive* and *active* cycling respectively, for reliability evaluation of power semiconductors [28] - [29]. These studies showed that several challenges in power cycling have to be resolved in order to obtain reliable and accurate test results, which are suitable for lifetime estimation of power semiconductors. These challenges may be divided into two groups: methodical and technical. In this section, only methodical challenges are presented - the technical topics are more broadly discussed in section III.

A. Thermal and Power Cycling

There are two main approaches for power cycling of semiconductor devices. The first one is to keep temperature swing constant over the test progress, to investigate the physical basis of fatigue failures - crack expansion rate, progress of delamination or grain growth in the solder joint [30] - [31]. The main idea behind such an approach is to monitor pre-defined electrical, physical or chemical parameters, also called health indicators, in order to make an indirect lifetime estimation of the tested device. Furthermore, such test results may be used to implement the physical laws of fatigue into FEM-models and to adjust those models to reality [32].

A standard approach is to consider the tested semiconductor as a black box and to develop an empirical model. In such a case, the power level is kept constant during test instead of temperature swing. As Device Under the Test (DUT) degrades, the thermal impedance increases, causing higher peak junction temperature during pulse time, which additionally accelerates the degradation mechanism. Therefore, when the test was performed without the self-acceleration mechanism, the lifetime of the power module was approximately three times longer, as presented in [28] - [33].

Such a large difference is caused by a significant distinction in physics of failure induced during TC and APC. In case of thermal cycles, due to the technical limitations of thermal chambers, the temperature slope is quite low - it varies from 50 $\frac{^\circ C}{min}$ to 70 $\frac{^\circ C}{min}$. In contrast, the temperature slope during power cycles is limited only by the thermal capacitance of the heatsink used for the cooling of DUTs, which may result in a theoretical thermal gradient over 1.8 $\frac{^\circ C}{ms}$. Therefore, mechanical stress in the tested structure, induced by differences in the thermal expansion coefficients between SiC structure, solder joint and bond wire, is much higher in the case of APC [34].

The next issue is to determine a proper heating phase (On-time pulse) and cooling phase duration (Off-time pulse). An example of a power and temperature envelope during a single cycle is shown in Fig. 1. A typical approach is to decrease the annealing and tempering time (also called "dwell time") to shorten the overall cycle period and, as a result, shorten the whole test duration. Unfortunately, the mechanical tensions present inside the tested power semiconductor slowly relaxes during the dwell time. In such a case, an excessive reduction of dwell time may result in shortening the lifetime of the tested sample, as was presented in [35], through extended impact of the mechanical tensions on the semiconductor structure. As a result, thermal cycles or mild-slope power cycles with long dwell-time are preferable for e.g. solder delamination and grain growth, unlike short power cycles, which mostly introduce bonding-related failure modes. These facts stress the importance of testing power semiconductors in conditions close to real application.

Summarizing the discussion, the APC test becomes a better representation of real-life applications. In a typical power electronic converter, there will be no compensation of self-acceleration of degradation mechanisms within power semiconductors - a power supply works with a specific load and has to deliver the desired amount of power to it, without considering which operation conditions the power electronic components within. It is important to remember, that in real applications not only does the MOSFET degrade, but also the thermal interface between module and heatsink. This phenomenon will additionally increase the junction temperature swing for the same dissipated power level. The above-mentioned facts suggest that APC is a more suitable approach for establishing an empirical reliability model of power semiconductors than TC.

B. End-Of-Life Criteria

The next fundamental decision with a significant impact on both the design of accelerated lifetime test and the chosen end-of-life (EOL) criteria. Typical degradation indicators for SiC power MOSFETs are: gate leakage current ($I_{GS_{lk}}$), drain leakage current ($I_{DS_{lk}}$), threshold voltage ($V_{GS_{th}}$), channel resistance ($R_{DS_{on}}$), body diode forward voltage drop (V_{fwd}) and thermal impedance ($Z_{TH_{jc}}$) [36]. All of these parameters are useful; however, none of them is universal as each of the listed health indicators is related to a different degradation mechanism. Thus, a proper health indicator should be defined during the design of ALT which is suitable for the failure mode under examination.

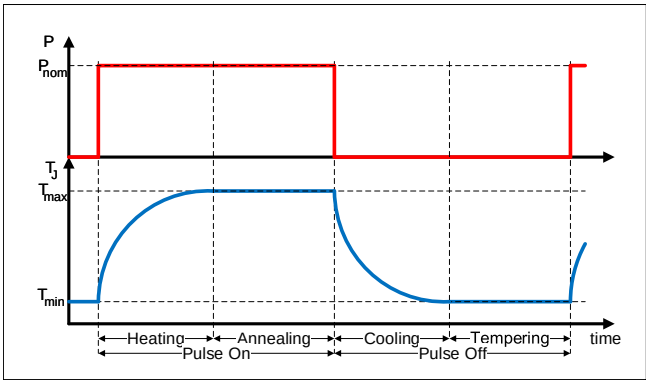

Fig. 1. Typical heating cycle for accelerated lifetime testing procedure with distinguished particular cycle steps.

As presented in [37], gate leakage current and drain leakage current may not change at all in the lifespan of the tested semiconductor, while there are significant changes in channel resistance or body diode voltage. On the other hand, multiple studies [38], [39] have shown that both $I_{GS_{lk}}$ and $I_{DS_{lk}}$ have a spike just before the power MOSFET has a fatal failure. Both of these indicators are strictly related to the state of the semiconductor chip itself, as the gate leakage current increases sharply when the gate oxide fails. Similarly, drain-source leakage current spikes after the failure of a single MOSFET cell inside the chip. Another health indicator, which describes the state of the gate oxide is the threshold voltage. In contrast to gate leakage current, this parameter changes slowly over the lifespan of the power MOSFET, according to the gate oxide degradation progress.

A well-known health indicator used in APC testing of power modules is thermal impedance. This parameter changes as solder between either semiconductor chip and Direct Bonded Copper (DBC) or DBC and baseplate delaminates, due to degradation of the soldering between them [40].

The electrical parameters commonly used for evaluation of aging in bond wires are channel on-state resistance and body diode voltage drop [36]. These two indicators seem to be equivalent, but such hypothesis might be misleading. As presented in Fig. 2, $R_{DS_{on}}$ measured at the terminals of encapsulated power MOSFET consists of components like: solder resistance (R_S), bond wires resistance (R_B), drain and source terminal resistance (R_T), channel resistance (R_{Ch}), accumulation region resistance (R_A), JFET region resistance (R_{JFET}), drift region resistance (R_D) and $N+$ region resistance (R_{Subs}) [37]. As MOSFETs R_{ch} is dependent on gate threshold voltage ($V_{GS_{th}}$) and R_A is dependent on flat-band voltage (V_{FB}), $R_{DS_{on}}$ increases according to the degradation of the gate oxide, as both threshold voltage and accumulation region resistance suffer degradation due to the drift in the interface charge. In contrast, V_{fwd} measured at the source-drain terminals is not gate threshold voltage dependent, but contains still interconnection resistance. Because of this, it should remain constant throughout all APC test, until the bond wire fails.

Typical EOL criteria for the presented health indicators are summarized in Table I. Various researchers have proved

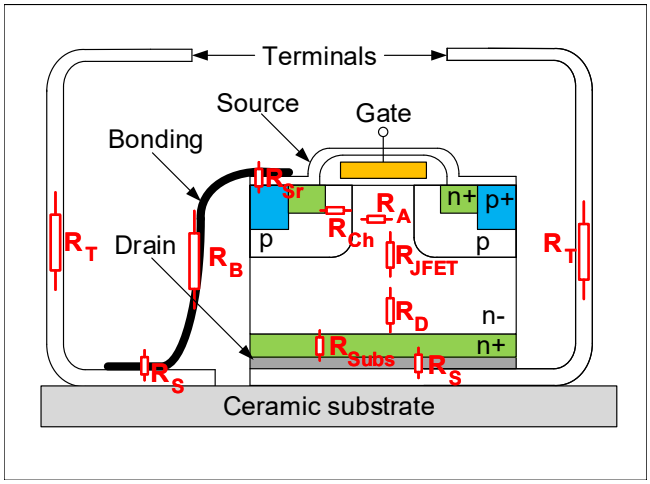

Fig. 2. Simplified diagram of encapsulated power MOSFET with marked chosen physical components of on-state channel resistance.

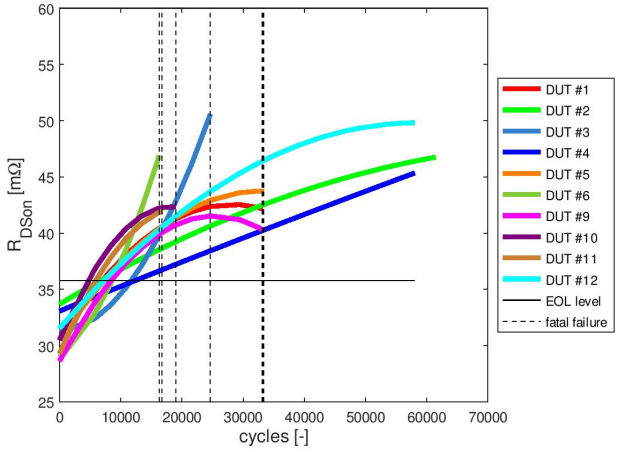

Fig. 3. Interpolated values of 12 SiC power MOSFETs, typical on-state channel resistance during APC test. Visible oscillations and decrease in on-state channel resistance before failure are caused by measurements dispersion and they are within confidence boundaries.

TABLE I
END OF LIFE CRITERIA FOR SIC POWER MOSFETS

Parameter	$I_{GS_{lk}}$	$I_{DS_{lk}}$	$V_{GS_{th}}$	$Z_{TH_{jc}}$	$R_{DS_{on}}$	V_{fwd}
Threshold	$+100\%$	$+100\%$	$\pm 20\%$	$+20\%$	$+20\%$	$+2\%$

that such drift from nominal values corresponds to significant degradation of the tested semiconductor device. This approach will shorten the duration of ALT, but has a significant drawback - it does not provide any information about *how long* the damaged sample will work before a fatal failure. This is not critical in the case of accelerated tests designed for scientific purposes like investigation of the physical basis of fatigue failures; nevertheless, it becomes significant in the case of building an empirical reliability model for commercial purposes. According to the conduced tests (see Figs. 3 - 4, Table II), the tested samples reached EOL criteria after only 8395 power cycles, while the first recorded fatal failure happened after 16283 cycles. This knowledge provides vast possibilities to be exploited - e.g. by warning the end-user of the power electronic converter about incoming failures. A detailed description of testing conditions, $R_{DS_{on}}$ measurement procedure and test results are presented in section IV.

TABLE II
TEST RESULTS FOR SIC POWER MOSFETS OPERATING WITH $105°C$ TEMPERATURE SWING

Sample number	Cycle count	Failure description
$6B$	16283	Drain-Source shorted
$11B$	16756	Gate-Source shorted, Drain-Source open
$10B$	18975	Drain-Source shorted
$3B$	24643	Drain-Source shorted
$9B$	33100	Gate-Source shorted ($\sim 4\ \Omega$), Drain-Source shorted ($\sim 3.5\ \Omega$)
$1B$	33163	Drain-Source shorted
$5B$	33359	Drain-Source shorted

C. Extrapolation of lifetime model

The last methodical question is whether the lifetime model extracted from ALT allows an accurate reliability estimation

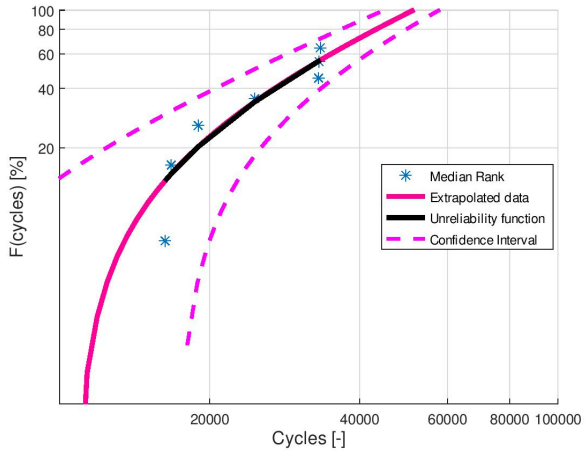

Fig. 4. Graphical representation of ALT results for SiC power MOSFETs subjected to $105°C$ temperature swing. Median ranks of recorded failures allowed for linear regression (black line) and extrapolation of unreliability function (pink line). The dashed pink lines represent 5% confidence interval.

in the whole range of expected stress levels to be conducted. It is interesting how the lifetime estimation accuracy varies for the following issues:

- Low temperature swing - below $40°C$.
  As presented in [41], strong experimental evidence suggests that the degradation process accelerates toward EOL. Therefore, it is possible to define *linear* and *non-linear* ageing phases for thermomechanical failure modes. Although low ΔT temperature swings do not significantly contribute to lifetime consumption during the linear stage of the ageing process, this impact is no longer negligible whenever solder crack initiates or the bond-wire starts to lift-off and the power semiconductor reaches its lifetime non-linear stage. In addition, in the linear ageing phase of the power semiconductor, some of the materials used for manufacturing remain in the

elastic region. When these materials reach the plastic region, their hysteresis stress-strain plots are shifted, which results in their deformation after subjecting the power semiconductor to thermomechanical stress. Therefore, the power semiconductor reaches the non-linear ageing phase. In this case, it is expected that a reliability model extracted from ALT results may introduce an underestimation of the power MOSFET useful lifetime for low temperature swing.

- Different t_{ON}/t_{OFF} ratio and duration of the power cycle or different power profile.
  As mentioned in section II-A, the heating profile has a significant impact on the test results due to the change in the leading failure mode. In this case, the reliability model would only be correct for very specific heating profiles - the same as used during ALT. This leads to the following questions: How to extrapolate lifetime estimation for different heating profiles (e.g. different duty cycle and period)? What would the lifetime estimation error be if this relationship between the duty cycle of the heating profile and power MOSFET reliability were ignored?
- Switching losses instead of conduction losses.
  In typical applications (e.g. AC-DC converter, DC-DC converter) the power MOSFET is subjected to high switching losses and a small part of conduction losses, which might also impact on lifetime estimation accuracy.

These questions are fundamental for practical applications of reliability modelling, as long-term tests are expensive and time-consuming. Unfortunately, this makes it extremely difficult to prepare multiple tests, each optimized for different failure modes, due to lack of economic justification. To overcome this challenge, these failure modes (solder delamination, solder joint fatigue, bond wire lift-off, bond wire heel-cracking, brittle cracking) shall be considered as one - *fatigue-like failure mode*. By implication, the laboratory setup described in this paper was designed and optimized to induce these types of failures.

III. ALT LABORATORY SETUP FOR ENCAPSULATED DISCRETE SIC POWER MOSFETS

A. Power MOSFET junction temperature estimation methods for ALT testing

One of the main technical issues in ALT is an accurate junction temperature measurement method suitable for APC. Both direct and indirect measurement methods were successfully utilized in [42], [43]. The impact of junction temperature measurement accuracy on power semiconductor lifetime estimation becomes visible after analysis of the CIPS2008 model of PC-induced failures in Si power IGBTs [44]. As presented in [45], 5% temperature measurement error for $80°C$ temperature swing may introduce over 31% relative error in lifetime estimation expressed in number of cycles. In case of encapsulated power MOSFETs, a practical realization of accurate junction temperature measurement is especially challenging, as the utilization of any direct method is impossible.

The main disadvantage of the indirect temperature methods is a rather small change of the measured signal with temperature [46]. This fact significantly increases the complexity and price of equipment used for T_J estimation based on Thermo-Sensitive Electrical Parameters (TSEP) monitoring. In addition, power MOSFETs TSEP (e.g. $R_{DS_{on}}$, $V_{GS_{THLD}}$, $I_{DS_{lkg}}$, etc.) changes as chip and bond wire degradation progresses. This fact is especially unfortunate as an accurate T_J estimation would require a periodic calibration procedure, which would significantly increase the maintenance cost of an accelerated life test.

For these reasons, a different approach has been chosen for the presented laboratory setup. Junction temperature is estimated based on monitored baseplate temperature (T_C), dissipated power (P_L) and known initial thermal impedance between junction and case $Z_{TH_{J-C}}$. As stated previously, thermal impedance changes over time due to degradation of soldering between either chip and DBC or DBC and baseplate. Therefore, this method allows to determine only the initial conditions - e.g amplitude of junction temperature swing for fresh samples. This approach is allowed as the presented APC test is designed for empirical reliability model extraction and the self-acceleration the of the degradation mechanism is a desired phenomenon. Thus, discussed test will result in the useful lifetime of SiC power MOSFETs (defined as number of power cycles) as a function of initial amplitude of T_J swing. The estimated junction temperature can be expressed as:

$$T_J = P_L \cdot Z_{TH_{J-C}} + T_C \tag{1}$$

The main drawback of the model-based junction temperature estimation method is the relationship between thermal model parameters, environmental conditions and the placement of the reference temperature sensor [47]. One possibility to overcome this flaw and increase T_J estimation accuracy is measurement and identification of $Z_{TH_{J-C}}$ parameters (e.g. with a particle swarm optimization algorithm [48]) for a sample placed in the ALT laboratory setup. Then, if it is desired to monitor T_J during the test, this calibration procedure has to be repeated periodically to maintain estimation accuracy at a satisfactory level. This however increases the maintenance cost of the ALT procedure. Another possible solution for accurate T_J monitoring for ALT of power semiconductors, is the preparation of a complex, time-dependent thermal impedance model, which covers variations of lumped parameters caused by degradation or operating conditions, as presented in [49]. These flexible RC parameters can be extracted with Finite Element Modelling (FEM) and be verified or calibrated with proper experiments. The main drawback of this method is the amount of time and effort spent on identification of thermal model parameters, which increases the investment cost of ALT test. An alternate approach is to prepare a reliability model based on *case temperature* instead of *estimated junction temperature*; however, such an approach difficults any attempts of reliability-oriented comparative study between different types of power MOSFETs. Therefore, it would only be useful for internal purposes of industrial consumer of power electronics - e.g. to estimate the useful lifetime of an SiC power MOSFET based on actual stress levels present in a target application. The main benefit of this simplified approach is simplicity - as far as environmental parameters remain constant and case temperature is measured in the same way in ALT laboratory

setup and target application, the developed reliability model will be correct.

B. Control and health monitoring methods for large-scale ALT testing

Another issue is scaling up the batch size to decrease the confidence boundaries of the reliability model obtained while maintaining the simplicity and low overall cost of the laboratory setup. Each of the technical solutions discussed below was evaluated in the scope of Design to Cost (DtC) methodology [50]. At the first step, the following cost factors were identified: investment expenses, material cost and maintenance cost. The first group consists of expensive laboratory equipment, essential for the aforementioned test setup, like high power DC supply, measurement equipment (e.g. source meter unit, curve tracer, high resolution voltage meter, etc.) or heat exchanger. The second group consists of single use or reusable materials required for the test (e.g. power MOSFETs themselves, electronic controllers of dissipated power, heatsinks and a housing or rack system) and manpower spent on the start-up of the ALT test. The final cost component is maintenance, which is related to time and manpower required to keep the test running.

All samples in ALT can be connected in parallel or in series. In the case of high current devices, parallel connection is not an optimal solution as it requires the usage of extremely high current to heat up the tested devices properly. As an example of the designed APC test bench, the current efficiency of a power source supplying 40 samples of 70 A SiC MOSFETs at the same time, would have to be at least 2.2 kA. Practical realization of such a laboratory setup would require the usage of multiple high power DC sources, which would significantly increase the investment costs.

Another problem related to parallel connection is current sharing between the samples tested. In the case of SiC power MOSFETs, on-state channel resistance is $30-40$ $m\Omega$, which is very close to the resistance of wires and cables connecting DUTs. In this case, any asymmetry in galvanic connection between samples can cause unequal current sharing. Such phenomena can be avoided by a proper control strategy, like active current equalizing or sequential switching of the semiconductors tested. The first approach requires the usage of multiple precise current transducers, which significantly increases the cost of the laboratory setup. The second solution, as presented in Fig. 5, allows the current efficiency of the power source for the laboratory setup to be decreased to $56-74$ A, as only one DUT is supplied at the same time. The main drawback of this approach is the extension of the cycle period by a factor of the batch size, which makes the whole test impractical. E.g. for base cycle period 20 s, 50000 power cycles performed in sequential switching of DUTs would take ~ 15 months.

Series connection of the samples tested naturally solves the issues described above. The main drawback of this approach is a heavy self-acceleration of the fatigue mechanism in the weakest link. As the SiC power MOSFET degrades, channel resistance increases, which causes higher power to

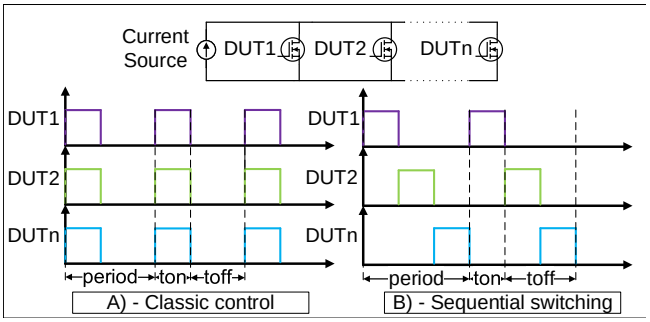

Fig. 5. Comparison of classic control mode (a) and sequential switching (b) for APC.

be dissipated at the most damaged DUT. To avoid this mechanism, the voltage across the tested samples has to be actively equalized. A test performed without such voltage equalizing is called a Current Cycling test (CC) and allows for accurate modelling of the degradation of power semiconductor devices subjected to thermal cycling caused by conduction losses. However, because of low gate charge and parasitic capacitance, SiC power MOSFETs are typically used in high frequency switching application - e.g. resonant converters, in which SiC devices are mostly subjected to switching losses. Unfortunately, in most applications the level of switching losses are not solely related to the health of the SiC power MOSFET itself, but also varies from the degradation of driver circuit, environmental conditions, load, etc. Therefore, the results of an APC test performed with V_{DS} equalizing have higher applicability. Both voltage (for series connection) and current (for parallel connection) equalizing may be performed by actively adjusting the gate voltage, but a precise drain-source voltage measurement is more economical to implement.

In the next step, the health indicators discussed in section II-B were critically evaluated in the scope of a DtC methodology. The main challenge related to $I_{GS_{lk}}$, $I_{DS_{lk}}$, $V_{GS_{th}}$ or $Z_{TH_{jc}}$ monitoring, also referred in this paper as *complex health indicators*, is rather impractical in the realization of the measurement procedure for a large number of tested samples. Accurate and valuable measurements require the usage of sophisticated (e.g. curve tracer) or custom made (e.g. setup for thermal impedance measurement) equipment and disassembling the samples from the laboratory setup. The usage of a curve tracer, which may cost approximately 90000 €, depending on the configuration, instead of a source meter unit or a high precision current source with High Precision Voltage Meter may significantly increase the investment cost of ALT. Such complicated health indicator measurement procedures could significantly increase the maintenance cost in large-scale ALT. In contrast to the health indicators mentioned above, $R_{DS_{on}}$ and V_{fwd} measurement circuits can be implemented directly in a test bench for APC, which makes these health indicators more suitable for large-scale tests.

The impact of a chosen health monitoring strategy on the overall maintenance cost of ALT test is presented in Fig. 6. For the cost estimation it was assumed that a four wire measurement of $R_{DS_{on}}$ and V_{fwd} takes approximately 1 min for a single sample, while dismounting the tested MOSFET

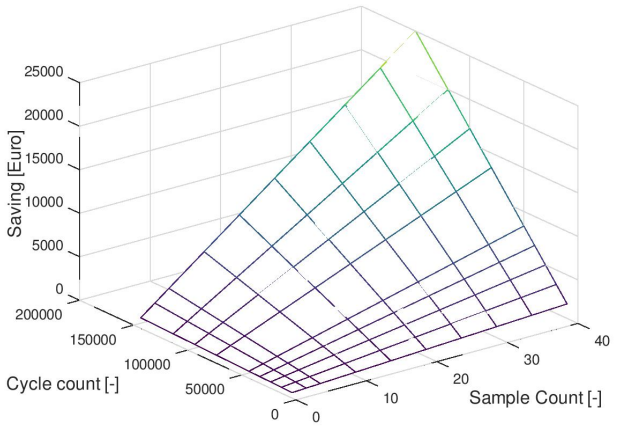

Fig. 6. Model of maintenance cost difference for simple and complex health measurement in the scope of samples of MOSFETs tested and test duration (cycles).

TABLE III
SiC POWER MOSFET ELECTRICAL PARAMETERS

Electrical Parameter	I_{DS}	V_{DSS}	$R_{DS_{on}}$	$R_{TH_{JH}}$	$T_{J_{MAX}}$
Nominal Value	68 A	1200 V	34 $m\Omega$	0.6 $\frac{K}{W}$	175 $°C$

from the laboratory setup, measurement of the desired complex health indicator and remounting it back in the laboratory setup takes at least 6 $mins$. In the model discussed, it is assumed that the health measurement procedure is performed at least once per 2000 cycles and the cost of a working hour is 100 €. The simulations presented show that although the health monitoring strategy has no significant impact on the overall maintenance cost for small test batches ($\leq$ 10 samples) or short tests ($\leq$ 70000 cycles), for large test batches a proper decision on the monitored health indicator may allow for savings reaching 25000 €.

The next technical issue is the definition of a proper active heating method for the samples tested. Based on the electrical parameters of the SiC MOSFETs tested (see Table III), the minimum DC current required to heat up the structure by $80°C$ is 62 A, which barely fits inside the transistor's Safe Operating Area (SOA). As the maximum rated current for tested samples is 68 A at $T_C = 25°C$, a test conducted with a higher temperature swing (e.g. $105°C$), would imply operation besides SOA - especially for higher ambient temperatures (e.g. $30°C$ or $50°C$). Unfortunately, operation beside SOA may distort the test result, by false accelerating fatigue-like failure modes [51], which makes this approach sub-optimal.

Another possible solution for increasing the power dissipated at those MOSFETs to the desired level, e.g. 200 W, is to introduce high frequency switching losses. Hard switching allows for working within the safe operating area, while sustaining the desired temperature swing. The main drawback of this approach is the high complexity of the laboratory setup, as accurate measurement of switching losses requires phased, fast, high-resolution voltage and current measurements [52].

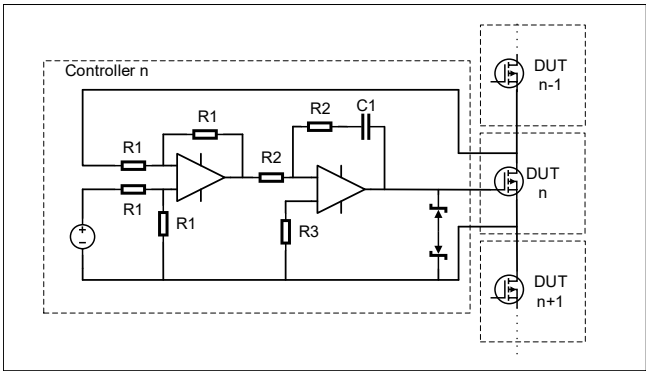

Fig. 7. Schematic diagram of gate voltage controller circuit.

Practical realization of such a measurement circuit requires the usage of expensive ultra-fast acquisition systems [53], which significantly increases the cost of the APC test procedure. Hard switching may also distort the test results by introducing new failure modes, e.g. parasitic BJT transistor turn-on [54] or power MOSFET self turn-on [55].

Based on the presented evaluation, heating up devices by limited DC current ($\sim$ 22.5 A), conducted through transistors operating in the linear mode, was defined as an optimal and most economical solution. A similar approach is described in the AQG-324 standard [56], which obliges the designer of an ALT setup for IGBTs to assure operation within the saturation area only. By analogy, tested power MOSFETs operating conditions have to remain within the linear region during the test. This functional requirement is related to a modern planar MOSFET structure, as they are designed as parallel connection of hundreds of single-cell MOSFET transitors. If the device is fully saturated, the transistor's drain current may have a negative or a positive temperature coefficient, depending on actual V_{GS} value, which may lead to thermal instability [57]. In case of a power MOSFET operating in the linear region, it will have a negative thermal coefficient.

For precise V_{DS} voltage regulation, a proper control circuit with low temperature drift was designed. To increase the EMC immunity and safety of the laboratory setup, galvanic isolation of the power supply of each gate voltage controller circuit was provided. Each controller was equipped with a voltage measurement and display in order to facilitate the test monitoring. A schematic view of a gate voltage controller is presented in Fig. 7. The elements used in this circuit are as follows: $R1 = 56$ $[k\Omega]$, $R2 = 10$ $[k\Omega]$, $R3 = 0$ $[\Omega]$, $C1 = 47$ $[nF]$.

The specification of the presented laboratory setup and operating conditions for the samples tested are summed up in Table IV and Table V respectively. As mentioned in section II, the main concern in ALT methodology is junction temperature control accuracy and repeatability. In the laboratory setup presented, there are two possible sources of T_J inaccuracy - power ripples ($P_{OUT_{Acc}}$) caused by the power supply itself and drain-source voltage dispersion between neighboring samples ($V_{DS_{(n)-(n+1)}}$) caused by tolerances of passive and active elements in the drain-source voltage controllers. The first was measured with an MDO 3040 digital oscilloscope and a

TABLE IV
ELECTRICAL PARAMETERS OF LABORATORY SETUP FOR APC

Batch Size 40 $[pcs]$	V_{OUT} 260 $[V]$	I_{DS} 22.5 $[A]$	P_{OUT} 5.8 $[kW]$
Sampleset Size 10 $[pcs]$	$V_{OUT_{Acc}}$ 12 $[V]$	$I_{DS_{Acc}}$ 1 $[A]$	$P_{OUT_{Acc}}$ 12 $[W]$
$V_{DS_{(n)-(n+1)}}$ 300 $[mV]$	$P_{L_{(n)-(n+1)}}$ 2.68 $[W]$	$T_{J_{Acc}}$ 0.18 $[°C]$	$T_{J_{(n)-(n+1)}}$ 1.6 $[°C]$

TABLE V
OPERATING CONDITIONS OF TESTED SEMICONDUCTOR DEVICES

Sample set no.	V_{DS} $[V]$	P_L $[W]$	ΔT_J $[°C]$	$T_{J_{LOW}}$ $[°C]$	$T_{J_{HIGH}}$ $[°C]$
A	6.7	150.5	90.5	30	120.5
B	7.8	175	105.3	50	155.3
C	5.6	126	76.5	50	126.5
D	5.6	126	76.5	30	106.5

$TA-042$ differential probe, with 2% basic accuracy, while the second was measured with both a differential probe and a high precision voltmeter - $FLUKE289$, with 0.025% basic accuracy. Despite the high voltage and current levels (V_{OUT}, I_{DS}), overall voltage and current ripples across MOSFET cascade ($V_{OUT_{Acc}}$, $I_{DS_{Acc}}$) are very low and introduces minor power fluctuations - approximately $12\ W$, which causes an $0.18°C$ error in the junction temperature control ($T_{J_{Acc}}$). Drain-source voltage dispersion measured with the differential probe is below $300\ mV$, which results in $6.75\ W$ power loss deviation between DUT_n and DUT_{n+1}. This deviation causes $\sim 4\ °C$ junction temperature variation ($T_{J_{(n)-(n+1)}}$) between samples. Unfortunately, as the noise itself recorded a with $TA-042$ differential probe was $240\ mV$, which results in 0.8 signal to noise ratio. On the other hand, measurements performed with the $FLUKE\ 289$ showed that the worst-case V_{DS} difference between samples is $96\ mV$ for sampleset A, $119\ mV$ for sampleset B, $32\ mV$ for sampleset C and $34\ mV$ for sampleset D, resulting in $\sim 1.3°C$, $\sim 1.6°C$, $\sim 0.43°C$ and $\sim 0.46°C$ respectively. Therefore, this deviation is considered negligible, as in the previous case. An example record of baseplate temperature, acquired for a single DUT, is presented in Fig. 8. The curve grouping shown in Fig. 8 and the fact that peak case temperature value for each DUT remained constant during the test (see Fig. 9) showed that pulse-by-pulse control repeatability is satisfactory.

The last key parameter of this drain-source voltage controller is its stability over time. Periodical V_{DS} measurements performed for each sample at the very beginning of the ALT test, after 16928 cycles and later, showed that power MOSFETs operating conditions remained at the same level, within $\pm 20\ mV$ confidence boundaries, which is acceptable.

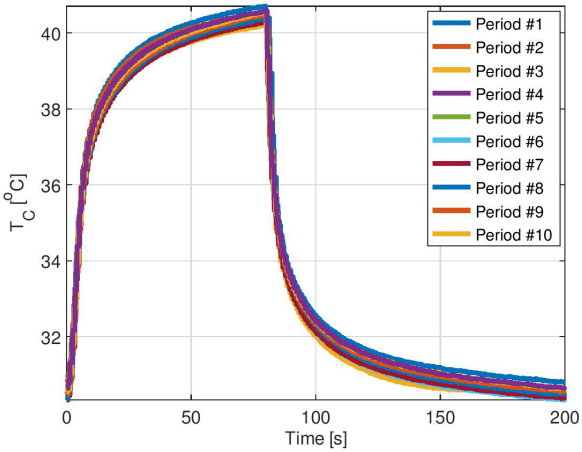

Fig. 8. Measured baseplate temperature record for 10 following power cycles performed by single DUT. Discretised temperature reading is presented on Y axis, while timestamp is presented on X axis.

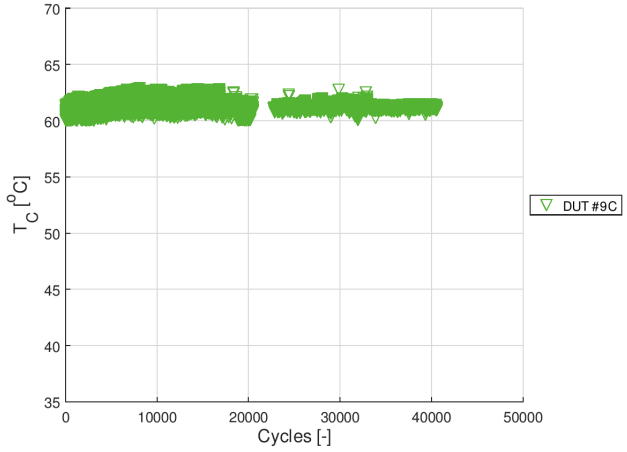

Fig. 9. Case temperature record example - measured for sample $\#9C$ stressed with $50°C-126.6°C$ junction temperature swing. The presented record is shorter than the test duration itself, as the recorded data was partially lost.

C. Failure detection algorithm for ALT testing

The last technical challenge related to the design of the ALT laboratory setup is failure detection. As discussed earlier, the test should be conducted until all samples fail; therefore, it was necessary to design an emergency circuit, capable of shutting down the heating current within milliseconds in order to avoid complete destruction of the SiC chip. This allows for further analysis of a failed MOSFET - e.g. decapsulation or X-RAY photography. For this purpose, a voltage and current monitoring circuit, presented in Fig. 10, was designed. An emergency algorithm based on both measurements determines the condition of the laboratory setup, and whether there is a heating pulse, short circuit or open circuit. Four different threshold levels for the voltage and current measured were defined:

- Current threshold low (I_{low}) - $I_{nominal} \cdot 5\%$,
- Current threshold high (I_{high}) - $I_{nominal} \cdot 90\%$,
- Voltage threshold low (V_{low}) - $V_{nominal} - V_{DS_{min}}$,

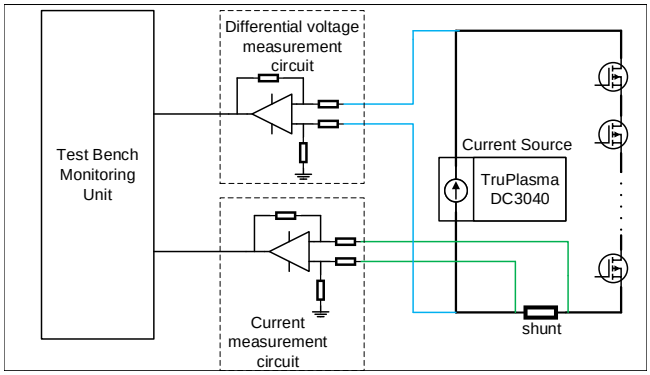

Fig. 10. Schematic of supervisory circuit for failure detection.

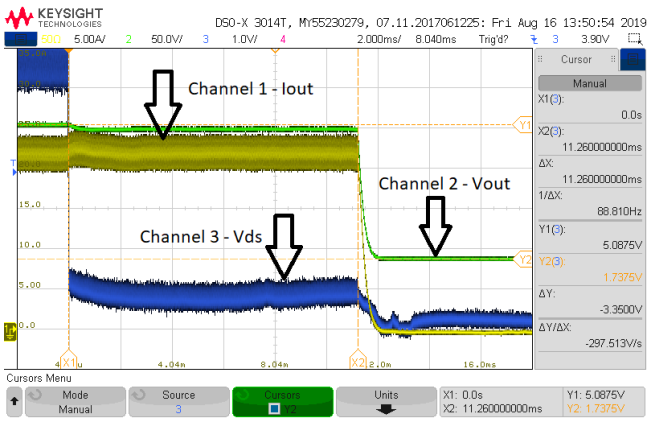

Fig. 11. Test of MOSFET failure detection circuit: Channel 1 - operating current (I_{OUT}), Channel 2 - voltage at MOSFET cascade (V_{OUT}), Channel 3 - voltage at shorted sample ($V_{DS_{8D}}$).

- Voltage threshold high (V_{high}) - $V_{nominal} \cdot 120\%$,

where $I_{nominal}$ is the nominal RMS current value during a cycle, $V_{nominal}$ is the nominal RMS voltage across the MOSFET cascade during a cycle and $V_{DS_{min}}$ is the minimum voltage drop in single DUT during the test. In the discussed emergency detection algorithm, actual voltage (V_{act}) and current (I_{act}) are constantly compared to these threshold levels, to detect three possible states: short-circuit (SC), open-circuit (OC) and correct operation (CO). The logical relationships used for this purpose are presented by (2) - (4). In Fig. 11, an actual failure detection is presented. Both output current (channel 1 - yellow) and voltage (channel 2 - green) across the tested samples decrease exponentially after failure detection. As each voltage controller circuit is equipped with a parallel RC circuit, balancing voltage across MOSFETs, it is assured that neither failure has a negative impact on the rest of the tested samples.

$$I_{act} \geq I_{high} \wedge V_{act} \leq V_{low} \implies SC = 1 \tag{2}$$

$$V_{act} \geq V_{high} \wedge I_{act} \leq I_{low} \implies OC = 1 \tag{3}$$

$$SC \neq 1 \wedge OC \neq 1 \implies CO \tag{4}$$

The presented failure detection circuit may also be used for further automatization of the ALT procedure or integration of the laboratory setup in a larger infrastructure, compliant with $Industry$ 4.0 concepts [58]. In this paper, the most basic version of the laboratory setup for ALT of power SiC MOSFETs is presented. Therefore, each failure stops the test until the operator manually removes the failed sample and resets the alarm, which takes ~ 15 min.

An overview and corresponding block diagram of the discussed laboratory setup are presented in Fig. 12 and Fig. 13 respectively. Various researchers have presented their proposals for laboratory setups for APC [59], TC [60] or Temperature and Power Cycling (TPC) [61]. A common feature for all these laboratory setups is the small batch size for each test - sample size varied from 1 to 10 samples [62], [63]. In contrast to the above, the laboratory setup presented allowed for simultaneous test of 4 different batches, which resulted in a total capacity of 40 samples. Also, previous research was mainly focused on high voltage IGBT modules and low power discrete semiconductors in common packages - e.g. $TO-220$, $TO-247$ [64], [65], [29]. The laboratory setup presented here, optimized to be cost effective, large scale APC test of discrete semiconductors in industry grade housing $SOT-227b$, complements the above mentioned state-of-the-art well.

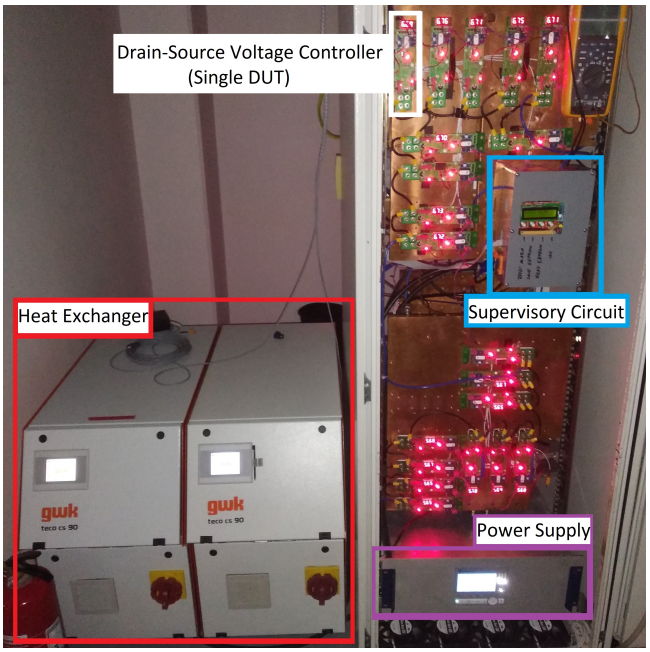

Fig. 12. Overview of APC laboratory setup and its main components.

IV. Test Results

The results of periodic health indicators measurements for tested power semiconductor devices are presented in Figs. 14 - 19.

In the case of the power MOSFETs, which were subjected to low thermal stress (ΔT swing from $30°C$ to $106.5°C$ per cycle), the health indicator measurement showed that the test had barely any impact on DUTs. As is presented in Fig. 14 and Fig. 17, all recorded measurements were very close to nominal values, and - by implication - neither health indicator exceeded typical EOL criteria. In contrast to the sample set D,

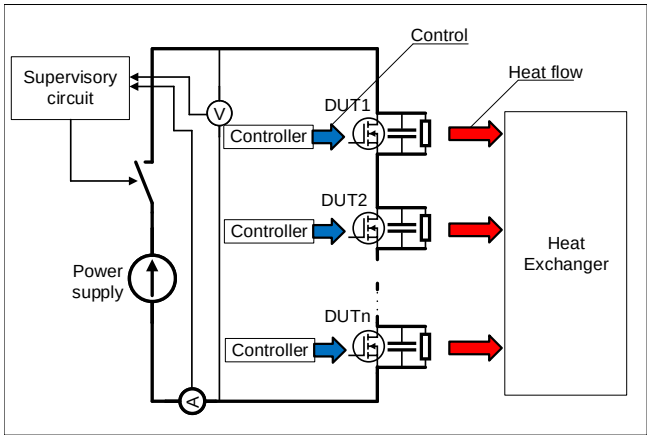

Fig. 13. Simplified block diagram of presented laboratory setup for APC test.

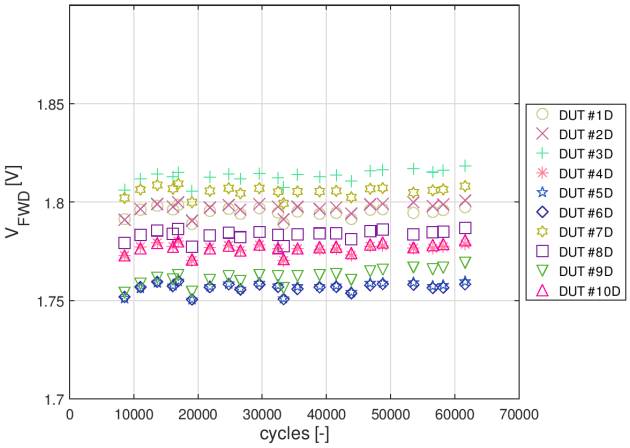

Fig. 14. Body diode forward voltage drop measurement for sample set D - $\Delta T_J = 76.5°C$, $T_{J_{LOW}} = 30°C$, $T_{J_{HIGH}} = 106.5°C$

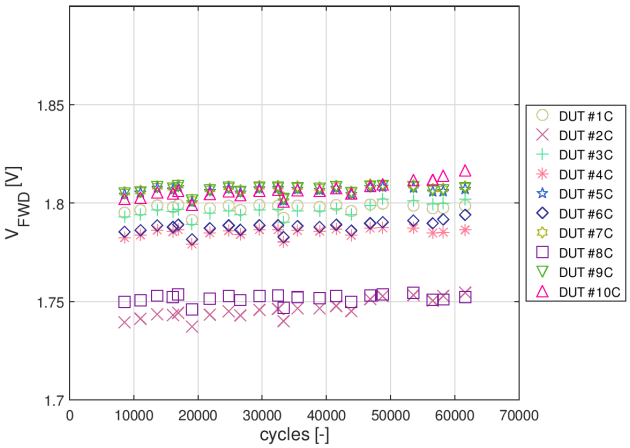

Fig. 15. Body diode forward voltage drop measurement for sample set C - $\Delta T_J = 76.5°C$, $T_{J_{LOW}} = 50°C$, $T_{J_{HIGH}} = 126.5°C$

periodic $R_{DS_{on}}$ measurement for power MOSFETs subjected to $50°C - 126.6°C$ junction temperature swing, showed a slowly progressive degradation. Samples #2, #3, #6 and #10

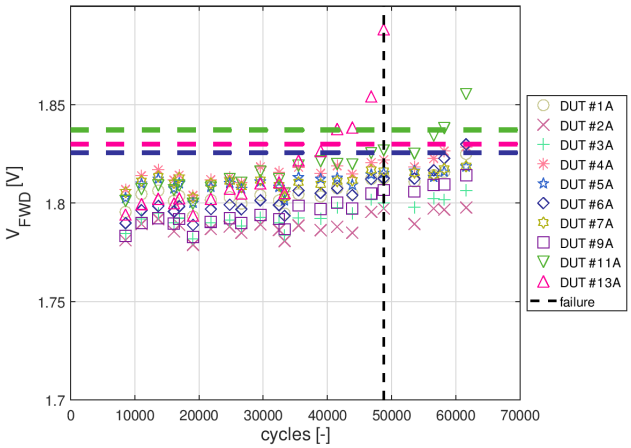

Fig. 16. Body diode forward voltage drop measurement for sample set A - $\Delta T_J = 90.5°C$, $T_{J_{LOW}} = 30°C$, $T_{J_{HIGH}} = 120.5°C$

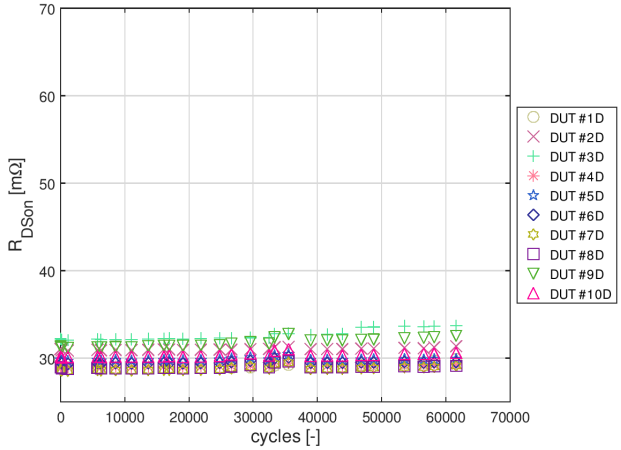

Fig. 17. On-state channel resistance measurement for sample set D - $\Delta T_J = 76.5°C$, $T_{J_{LOW}} = 30°C$, $T_{J_{HIGH}} = 106.5°C$

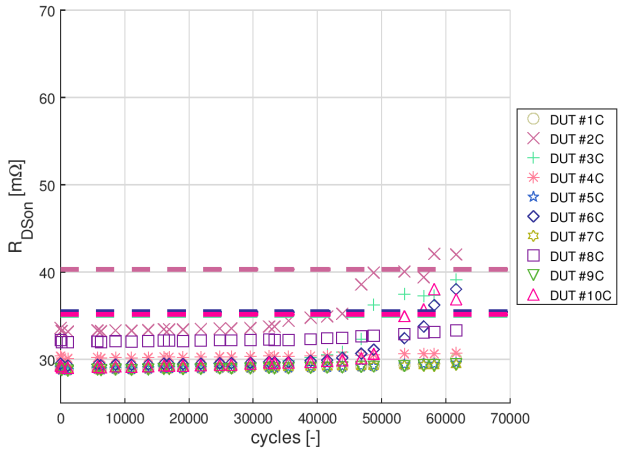

Fig. 18. On-state channel resistance measurement for sample set C - $\Delta T_J = 76.5°C$, $T_{J_{LOW}} = 50°C$, $T_{J_{HIGH}} = 126.5°C$

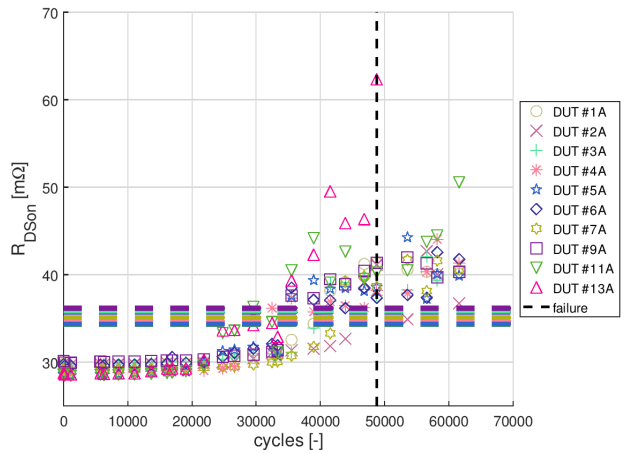

Fig. 19. On-state channel resistance measurement for sample set A - $\Delta T_J = 90.5°C$, $T_{J_{LOW}} = 30°C$, $T_{J_{HIGH}} = 120.5°C$

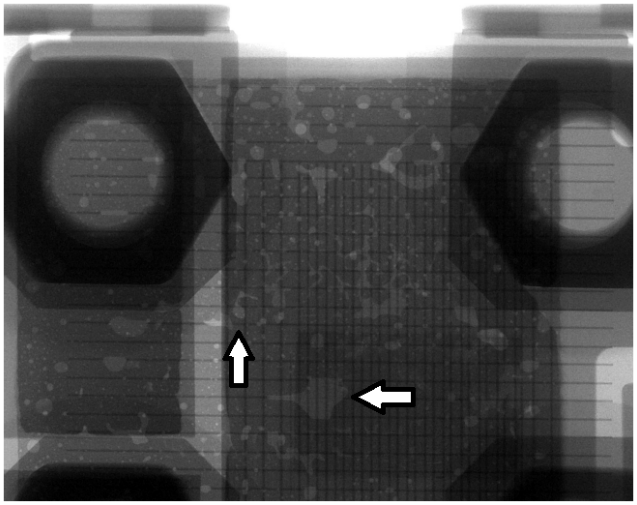

Fig. 20. Top view of a SiC power MOSFET example subjected to X-Ray analysis. Visible small cavities (white arrows) were verified as typical of the manufacturing process - they were not induced by the APC test.

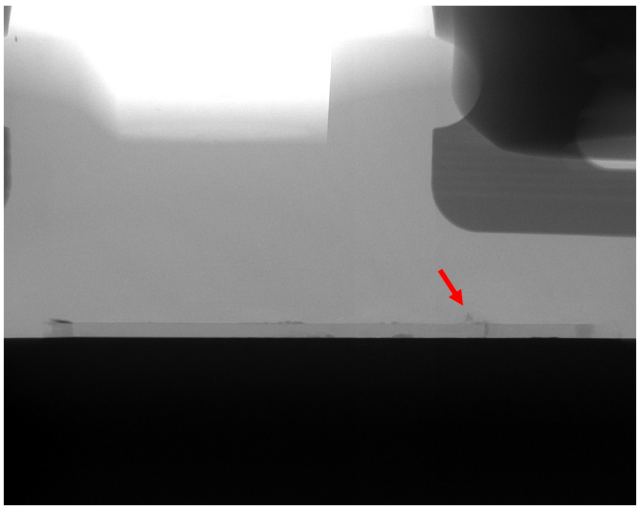

Fig. 21. Close up on side X-Ray image of a failed sample. Visible crack in SiC chip, located beneath terminal, marked with red arrow. Due to localization, the crack is invisible in the top view X-Ray, presented in Fig. 20.

even reached their $R_{DS_{on}}$-based EOL criteria. A comparison of V_{fwd} and $R_{DS_{on}}$ records, presented in Figs. 15 and 18 respectively, shows that only the on-state channel resistance changed during the studied test and the body diode forward voltage drop remained at nominal level.

A deeper analysis of Figs. 16 - 19, shows a clear drift of electrical parameters for power MOSFETs, which were subjected to moderate thermal stress ($90.5°C$ junction temperature swing). There was a single fatal failure for this batch (sample $\#13A$) after 48793 cycles. All the samples tested reached $R_{DS_{on}}$-based EOL criteria and three samples V_{fwd}-based EOL criteria too (samples $\#6A$, $\#11A$ and $\#13A$). This suggests a rapidly progressing degradation or even lift off of the bond wires in the tested semiconductor devices.

As presented in section II-B, 7 out of 10 samples stressed with $105.3°C$ junction temperature swing failed during the discussed APC test. All the samples tested reached $R_{DS_{on}}$ based EOL critera below 20000 thermal cycles, as shown in Fig. 3 (section II). The decapsulation process combined with shear strength test and X-Ray analysis showed that each failed sample had all bond wires lift-off, while the soldering beneath the chip remained intact (see Fig. 20). As it was confronted with the supplier, cavities in the soldering beneath the semiconductor chip, visible in X-Ray images, were within an acceptable range - typical of their manufacturing process. This suggests that those cavities were not a result of the APC test. In addition to the above-mentioned, X-Ray scanning revealed also a crack in the SiC chip structure, presented in Fig. 21. A closer analysis of the X-Ray images and post-decapsulation pictures have shown that the SiC chip was damaged in 50% of the failed samples. Each time the crack was located close to the gate region (right side of Fig. 23), which suggests that all samples were damaged due to the same failure mode.

As the decapsulation process is highly invasive, due to the corrosive properties of the acids used to dissolve the moulding, it was performed in two stages. First, a short acid bath allowed the lifted bond wires to be exposed (see Fig. 22), which confirmed the hypothesis that the observed growth of $R_{DS_{on}}$ and V_{fwd} was caused by the degradation of the bond wire connection. Second, a longer acid bath revealed the SiC chip and distinct black markings from the lifted bonding wires. Unfortunately, during the decapsulation process the chip broke along crack found during X-Ray analysis, as shown in Fig. 23. The crack location suggests that bond wires located closer to the source terminals (right side of Fig. 23) lifted off earlier than those located close to the drain- and gate- terminals. With each lifted bond wire, the current was conducted through a smaller surface, resulting in local overheating and significant mechanical stress in the SiC chip and - eventually - cracking. As presented in Fig. 23, each lifted bond wire left a characteristic black mark - an result of the chemical reaction between the solvent used in the decapsulation process (H_2SO_4) and either remains of solder

or the intermetal dielectric layer. Unfortunately, metallurgical analysis was impossible to perform due to the highly invasive nature of the decapsulation process. A comparison of the degraded power MOSFET (Fig. 23) and fresh sample (Fig. 24) supports the first hypothesis, as each bond wire was surrounded with a characteristic black sediment. Also, all bond wires were lifted off.

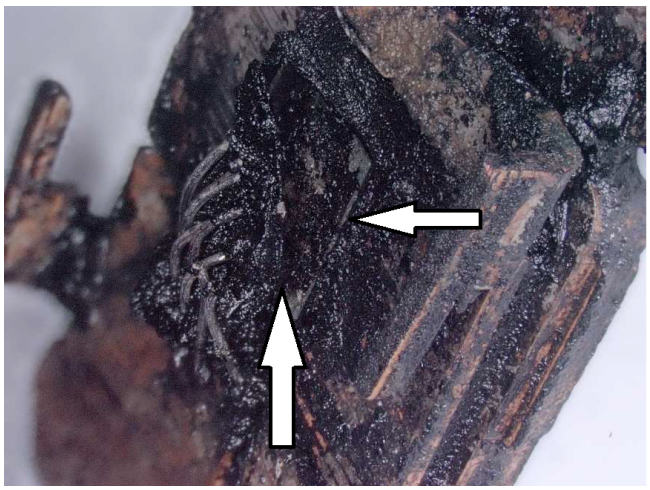

Fig. 22. Close-up image of decapsulated example of an SiC power MOSFET. Apparent lifted bonding wires are marked with white arrows.

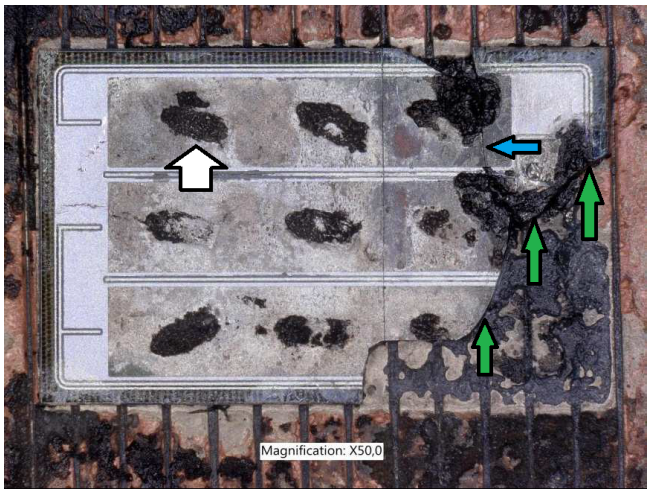

Fig. 23. Top view of decapsulated sample after long acid bath. Visible black markings are left by lifted bonding wires (white arrow). Thin crack in SiC chip (blue arrow) is the result of a hotspot caused by non-laminar current flow across the SiC chip. The chip itself was partially damaged during the decapsulation process. It broke along the crack line (green arrows).

The test results presented showed that over 63355 power cycles had barely any impact on the samples, whose junction temperature changed from $30°C$ to $120.5°C$ during each cycle. Neither health indicator changed from nominal values for all samples in test batch D. In contrast to sample set D, devices subjected to the same junction temperature swing ($76.5°C$), but for a higher base temperature ($T_{J_{LOW}} = 50°C$) showed some indications of a progressing degradation. Samples subjected to moderate stress level ($\Delta T_J = 90.5°C$) showed rapidly progressing degradation after approximately

Fig. 24. Top view of fresh sample subjected to decapsulation process.

35000 cycles. For this sample set, a single failure was recorded - after e.g. 48793 power cycles. In the case of DUTs subjected to heavy stress ($105.3°C$ junction temperature swing), 7 out of 10 samples failed during the test. Each failed sample (from test batch A and B) was subjected to X-Ray analysis and the decapsulation process. This investigation enabled it to be confirmed that failure mode for each analyzed sample was within the scope of *fatigue-like failure mode* definition. Each failed DUT had all the bond wires lifted off, while the soldering between chip and baseplate remained intact, which clearly showed that for this particular type of SiC power MOSFET in $SOT-227b$ housing, the weakest link are the bond wires.

V. Conclusions

Although fatigue-like failure modes are similar for both Si and SiC devices (e.g. bond wire lift-off, solder delamination), ALT of SiC power MOSFETs introduces different technical challenges than testing procedures designed for Si devices. As an example, SiC devices requires significantly lower losses to introduce the desired T_J swing, as they usually have higher thermal impedance than Si devices. On the other hand, health monitoring of the samples tested is far more challenging for SiC devices, as the main health indicator - $R_{DS_{on}}$ - is very low for such devices (e.g. $\sim$ 35 $m\Omega$). In contrast, $R_{DS_{on}}$ for Si devices is usually $5-10$ times higher than for SiC devices. Finally, a key difference between the ALT of SiC and Si devices is the rate of gate oxide layer degradation and its impact on the overall health of the samples tested. Therefore, for SiC power MOSFETs, at least two different health indicators ($R_{DS_{on}}$, V_{fwd}) have to be monitored to perform adequate assessment of bond wire conditions.

Design to Cost analysis showed that in fact maintenance is a major factor in the overall cost of Accelerated Lifetime Testing of SiC power MOSFETs. Therefore, great focus should be placed on optimization of the maintenance procedure during the design of the laboratory setup for such ALT. As shown, series connection of samples tested and utilization of $R_{DS_{on}}$

and V_{fwd} as health indicators allow health monitoring measurements to be performed on-site, without dismounting the tested samples, which greatly decreases the time spent on the maintenance procedure and resulting in significantly lower maintenance costs. In addition, the optimized design of the laboratory setup and careful definition of health indicators or EOL criteria allowed the need for the use of sophisticated measurement equipment (e.g. curve tracer or fast acquisition systems) to be avoided, which significantly decreased the investment cost related to the start-up of APC test. As presented in section III-B, the proposed approach allow for savings reaching 90000 € in investment costs and 25000 € in maintenance costs.

Beside the technical aspects, the proposed testing method also makes ALT testing more industry friendly. The test bench presented allows for simultaneous testing of 40 devices, which is a significant improvement in comparison to typical laboratory setups for ALT testing. Moreover, it is possible to distinguish 4 separate batches among 40 simultaneously tested samples, each subjected to different operating conditions. In this paper, similar failure modes (bond wire lift-off, bond wire heel cracking, solder joint fatigue, solder delamination) are grouped and considered as a single *fatigue-like failure mode*. This approach is much more suitable for some industrial customers of power electronics (e.g. power converter manufacturers) than typical Physics of Failure, as it is easier to implement and more cost effective. For example, to evaluate PDF parameters for each of the above mentioned failure modes, reliability engineers would have to design at least four different Accelerated Lifetime Tests for three stress level combinations for each test, according to (5).

$$N_T = N_{FM} \cdot N_S \tag{5}$$

In this equation, N_T is the number of required tests, N_{FM} is the number of failure modes for which a PDF model is required, and N_S is the number of stressors suitable for all tested failure modes. The definition of a single *fatigue-like failure mode* allows for significant reduction of the required amount of test, as N_{FM} is reduced to 1. Closer analysis of failed samples showed that both the proposed ALT methodology and the presented laboratory setup heavily accelerate the failure modes which are within scope of the definition of *fatigue-like failure mode*.

The results have shown accurate and repeatable control of power dissipated at the tested samples, which has resulted in a high repeatability of the DUTs baseplate temperature and demonstrated that the designed laboratory setup fulfills the main requirements for the Accelerated Lifetime Testing methodology. In addition, a supervisory circuit and a failure detection algorithm, for minimizing the damage inside failed DUTs, is presented. The test results showed satisfactory performance, allowing the current flowing through the tested power MOSFETs to be shut down within $11.3\ ms$. To sum up, the supervisory circuit presented successfully protected the tested samples, which failed in the APC test, which further allowed for detailed failure mechanism analysis.

Finally, the presented test results showed that discrete SiC power MOSFETs in $SOT-227b$ are not susceptible to power cycles in which the junction temperature does not exceed $106.5°C$ and junction temperature swing does not exceed $76.5°C$. In contrast, power cycles with a $105.3°C$ T_J swing cause rapidly accelerating degradation of bond wire connections, and results in a significant shortening of the useful lifetime of the SiC power MOSFET.

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