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A UPFC for Voltage Regulation in LV Distribution Feeders with a DC-Link Ripple Voltage Suppression Technique

M. Mejbaul Haque, *Student Member, IEEE*, M. S. Ali, Peter Wolfs, *Senior Member, IEEE,* Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—The large scale integration of distributed photovoltaic (PV) generation causes several power quality issues in low voltage (LV) distribution networks. Network voltage profile variations severely affect the LV distribution networks. The four leg unified power flow controller (4L-UPFC) has series and shunt converters that can address the power quality issues. However, instantaneous power theory (IPT) shows that second order (2ω) harmonic voltage (2ωHV) appears at the dc-link capacitor of the 4L-UPFC during any unbalanced operations. This paper proposes control strategies for series and shunt converters that will simultaneously regulate the load voltages of a distribution feeder while suppressing the 2ωHV term on the dc-link of the UPFC. A controlled negative sequence (NS) current from the shunt converter is used to suppress the 2ωHV term on the dc-link. The active suppression of the 2ωHV term allows electrolytic capacitors to be replaced with small long life ceramic or film capacitors and this does not require additional passive compensation. Stability analysis of the control loops demonstrates the overall stability of the converter system. The proposed control methods have been implemented on a Texas DSP (F28377D). An experimental demonstration on a laboratory scale prototype shows the proposed control methods can effectively regulate the load voltages at LV distribution feeders and suppress the 2ωHV on the dc-link of UPFC during unbalanced loads and supply conditions.**

***Index Terms*—Distribution networks, 2ωHV, stability analysis, 4L-UPFC, voltage regulation.**

I. Introduction

THE expansion of small-scale PV units results in significant power quality issues in LV distribution networks [1]. The International Energy Agency (IEA) has estimated that the global cumulative installed PV system capacity will reach 1.3 TW by 2023 [2]. The total capacity of PV installations in Australia has reached 13.9 GW as of September 2019 [3]. This rapid proliferation of residential PV units causes significant reverse power flow problems in LV feeders [4, 5]. As the PV penetration increases, the reverse power flow phenomenon appears more frequently and causes voltage rise along the LV distribution feeders. This might cause violations of specified voltage boundary limits. Moreover, overvoltage restricts the active power injections into a LV distribution network [6]. As the generation changes, fast regulatory action with intelligent control is required to manage the voltage profile and to accommodate further PV units [6]. Due to the erratic changes in voltage profile, the usual operation of the traditional voltage regulatory devices such as on load tap changers (OLTCs), static voltage regulators (SVRs) and switched capacitors (SCs) is interrupted. For example, OLTCs operate more frequently to respond to the variations in network voltage profile than under usual conditions [7]. Reactive power control is an option, however, due to the high R/X ratio in LV feeders, this is not an effective solution for voltage regulation compared to active power. Active power curtailment can prevent the voltage rise, however this reduces the solar utilization capacity [8]. The coordinated control in [9] are useful for voltage regulation if the operation conflicts between OLTCs, SVRs and SCs are resolved. Due to these limitations of the methods, a 4L-UPFC topology is examined as a voltage regulator for LV distribution networks. The basic structure of the 4L-UPFC is shown in Fig. 1. The structure is similar to the unified power quality conditioner (UPQC) and this is in fact considered as a UPQC-L system [10]. In recent years, 4L-UPFCs have been used in many industrial applications, including hybrid electric vehicles [11], and electric arc furnaces (EAF) for arc stability [12].

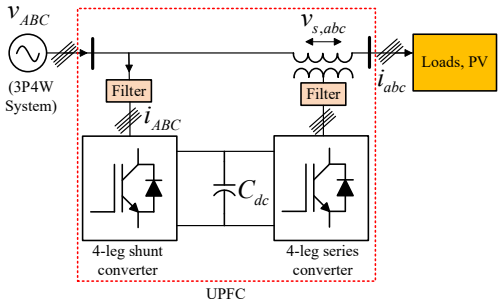

Fig. 1. General schematic of a typical 4L-UPFC [13].

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The 4L-UPFCs are gaining increased attention as voltage regulators in LV feeders due to their faster response time compared to OLTCs and switched capacitors [13, 14]. However, IPT reveals that the 4L-UPFC produces 2ωHV across the dc-link capacitor during any unbalanced operation of the LV distribution feeders [15]. The 2ωHV component increases the voltage stress on the inverter power semiconductors and increases the current stress upon the DC bus capacitors. This needs to be removed [16, 17]. Therefore, the selection of a dc-link capacitor and appropriate control strategies for a 4L-UPFC are extremely important to eliminate 2ωHV fluctuations. An electrolytic capacitor is a common choice, however this is bulky and expensive, has low ripple current capability per unit capacitance and has a shorter lifetime [16-19]. It is also reported that it occupies 35-40% of the whole system volume and weight while contributing 23% to the total system cost [18]. Converter designs that replace electrolytic filter capacitors with higher reliability devices such as polypropylene or ceramic capacitors are drawing more attention [16, 20, 21]. However, the replacement of electrolytic capacitors with alternative capacitor types of a few tens of microfarads will cause larger 2ωHV fluctuations which requires a 4L-UPFC to compensate with improved control strategies.

A number of 2ωHV suppression methods based on instantaneous power control have been developed for grid connected three phase PWM inverters [22-31]. In [30], the positive sequence (PS) and negative sequence (NS) currents were regulated in a positive synchronously rotating frame (PSRF) that caused larger control loop tracking errors due to limited control bandwidth. A dual current controller was proposed in [24] to regulate PS and NS currents independently with separate rotating frames. However, the line impedance was not taken into consideration in calculating the output power. This method used 120 Hz notch filters which reduces loop bandwidth because the additional phase delay requires a reduction in loop gain to retain a sufficient stability margin [26]. The input-output power control methods in [25] and [28] used the instantaneous active and reactive power at the terminals of the rectifier to calculate current references. To avoid the tracking errors and notch filters for the extraction of PS and NS currents, resonant controllers were used in [25] and [28]. The system dynamic performance can be affected by the above methods and the controllers are not easy to tune. The instantaneous power control method based on an output power control strategy in [22] is robust to generalized asymmetries. In [22] and [31], the extraction of PS and NS voltages was performed with the assumption that the line impedance is balanced. In addition, sequential decomposers were used for the extraction of PS and NS voltages and currents. The instantaneous power control method in [26] can deal with 2ωHV fluctuations even when the line impedance is unbalanced. To avoid the use of sequential decomposers, this method used proportional plus integral resonant (PI-R) controllers [32]. Recently, a reduced dc-link capacitor based PWM converter has been proposed in [29] that requires an extra compensation circuit for 2ωHV suppression which adds to control complexity. A very limited literature exists on the application and control of series and shunt converters of 4L-UPFCs in LV distribution networks. A 4L-UPFC has been proposed in [33] to regulate load voltages by controlling the series converter, however that lacks the full range of compensation capabilities and control for dc-link voltages.

The major contribution of the paper is to propose improved sequence based control strategies for the series and shunt converters of the 4L-UPFC. It also extends the sequence based approach for voltage regulation in the earlier work [13] and supplements the concept of the positive and negative sequence current extraction method for the shunt converter to control the 2ωHV fluctuations. The details of control methodologies are explained and the stability analysis of the control loops is presented in the paper. The salient feature of the proposed sequence based control framework avoids the sequential component decomposers and resonant controllers for extraction of the sequence current components. The proposed sequence based control approach does not require an extra circuit to compensate for 2ωHV fluctuations. The paper is organized as follows. Section II presents instantaneous power flow analysis for the 4L-UPFC. The average and oscillatory power equations which form the basis of sequence based control for shunt converter are shown. In section III, the design guidelines for the selection of the dc-link capacitor is discussed for two harmonic cases. The control methods of series and shunt converters are discussed in section IV for voltage regulation and 2ωHV suppression respectively. The proposed novel method of extracting positive and negative sequence currents to control the 2ωHV fluctuations is discussed in IV-C. Section V discusses the input and output filter design and stability analysis of the control loops. A simulation model of the 4L-UPFC is developed and tested at standard test conditions which are presented in Section VI. The experimental setup is shown in section VII. Section VIII presents the experimental results to show the performance of the 4L-UPFC for voltage regulation and 2ωHV suppression at the dc-link. Finally, Section IX concludes the paper.

II. Instantaneous Power Flow Analysis for 4L-UPFC

The detailed diagram of the 4L-UPFC under investigation is shown in Fig. 2. The series converter injects controllable phase voltages via series injection transformers for voltage regulation and balancing. The shunt converter supplies or absorbs the real power demanded by the four-leg series converter. According to IPT, the total instantaneous real power of the series and shunt converters can be derived from Fig. 2. This is separated into average power, $\overline{p}$ and oscillatory power, $\tilde{p}$ parts respectively which are expressed by (1) and (2) [15]. During any unbalanced operation, the series converter injects compensating voltages. The voltages and line currents can have PS, NS and zero sequence (ZS) components.

$$\begin{aligned} p_s(t) &= i_a(t)\times v_{Aa}(t) + i_b(t)\times v_{Bb}(t) + i_c(t)\times v_{Cc}(t) \\ &= \overline{p}_s(t) + \tilde{p}_s(t) \end{aligned} \tag{1}$$

$$\begin{aligned} p_p(t) &= i_{Ap}(t)\times v_{AN}(t) + i_{Bp}(t)\times v_{BN}(t) + i_{Cp}(t)\times v_{CN}(t) \\ &= \overline{p}_p(t) + \tilde{p}_p(t) \end{aligned} \tag{2}$$

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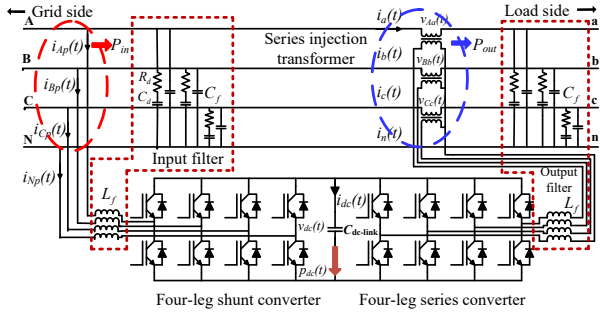

Fig. 2. Three phase distribution level 4L-UPFC under investigation.

As a result, the resulting average and oscillatory real powers, $\bar{p}_s(t)$ and $\tilde{p}_s(t)$ of the series converter are calculated using (1) as follows:

$$\bar{p}_s(t) = 3V_{s+}I_{s+}\cos(\varphi_{vs+} - \varphi_{is+}) + 3V_{s-}I_{s-} \cdot\cos(\varphi_{vs-} - \varphi_{is-}) + 3V_{s0}I_{s0}\cos(\varphi_{vs0} - \varphi_{is0}) \quad (3)$$

$$\tilde{p}_s(t) = -3V_{s+}I_{s-}\cos(2\omega t + \varphi_{vs+} + \varphi_{is+}) - 3V_{s-}I_{s+} \cdot\cos(2\omega t + \varphi_{vs-} + \varphi_{is-}) - 3V_{s0}I_{s0}\cos(2\omega t + \varphi_{vs0} + \varphi_{is0}) \quad (4)$$

In (1)-(4), the voltages, currents and phases of the series converter are represented by suffix "s" while these parameters are represented by suffix "p" for the parallel/shunt converter. Also, the sequence components of voltages and currents are represented by +, - and 0 suffixes for PS, NS and ZS respectively. Now, the series injected power must be balanced by shunt converter output power to avoid 2ωHV fluctuation at the dc-link [15, 27]. The power balance is achieved by controlling the shunt converter input currents that will have PS, NS and ZS components to ensure a full range of compensation. The average and oscillatory powers, $\bar{p}_p(t)$ and $\tilde{p}_p(t)$ of the shunt converter have to be obtained using (2) as follows:

$$\bar{p}_p(t) = 3V_{p+}I_{p+}\cos(\varphi_{vp+} - \varphi_{ip+}) + 3V_{p-}I_{p-} \cdot\cos(\varphi_{vp-} - \varphi_{ip-}) + 3V_{p0}I_{p0}\cos(\varphi_{vp0} - \varphi_{ip0}) \quad (5)$$

$$\tilde{p}_p(t) = -3V_{p+}I_{p-}\cos(2\omega t + \varphi_{vp+} + \varphi_{ip+}) - 3V_{p-}I_{p+} \cdot\cos(2\omega t + \varphi_{ps-} + \varphi_{ps-}) - 3V_{p0}I_{p0}\cos(2\omega t + \varphi_{vp0} + \varphi_{ip0}) \quad (6)$$

In practical applications, shunt converter input voltages have a dominant PS component, $V_{p+}\angle\varphi_{vp+}$ but this is not necessarily completely balanced. In this situation, if $V_{p+} >> V_{p-}$ the shunt converter real average and oscillatory powers would become:

$$\bar{p}_p(t) = 3V_{p+}I_{p+}\cos(\varphi_{vp+} - \varphi_{ip+}) \quad (7)$$

$$\tilde{p}_p(t) = -3V_{p+}I_{p-}\cos(2\omega t + \varphi_{vp+} + \varphi_{ip+}) \quad (8)$$

Equations (7) and (8) show that the average power, $\bar{p}_p(t)$ delivered by the shunt converter can be controlled by the PS current, whereas the oscillatory power, $\tilde{p}_p(t)$ fluctuates at 2ω (100 Hz) frequency. This causes 2ωHV fluctuations at the dc-link of the 4L-UPFC. The 2ωHV fluctuations on the dc-link are removed by a small controlled NS current with an appropriate magnitude and phase.

III. Design Guidelines for DC-Link Capacitor

Traditional converters utilize large electrolytic capacitors to achieve sufficient current carrying ability and capacitor lifetimes. This results in low equivalent series resistance (ESR) and low ripple voltages [27, 34, 35]. In this paper, much smaller film capacitors with negligible ESR are used. During the steady state, the variation in energy storage, E_c due to currents at the dc-link capacitor is given by (9) where V_u and V_l are the upper and lower dc-link voltages respectively.

$$E_c = \frac{1}{2}\times C_{dc-link}\times(V_u^2 - V_l^2) \quad (9)$$

A. Case I: Unbalanced 3-phase supply with no harmonics

If the 4L-UPFC in Fig. 2 is supplied by a three phase unbalanced voltage with fundamental frequency, then 2ωHV fluctuation at the dc-link capacitor is determined by (8). The energy storage at the dc-link capacitor due to 2ω oscillatory power in (8) is the area under the one-half cycle of the power waveform. For specified upper and lower voltage limits, the capacitor size is calculated as follows, [22]:

$$C_{dc-link} = \frac{6v_{p+}i_{p-}}{\omega(v_u^2 - v_l^2)} \quad (10)$$

Equation (10) reveals that a proportional relationship exists between the dc-link capacitor size and the NS current of the shunt converter. Some design choices are:

- A minimally sized dc-link capacitor with a controlled shunt converter NS current to suppress 2ωHV.
- A design with a larger dc-link capacitor that can carry the oscillatory power and allow shunt compensation currents up to the converter's rated limit.
- A compromise design with a dc-link capacitor that is sized to allow a controlled amount of NS compensation and harmonic currents.

B. Case II: Unbalanced 3-phase with balanced harmonic current

If the shunt converter has to provide compensation currents for harmonics, an additional oscillatory power, $\tilde{p}_p(t)$ will appear on the dc-link. In this paper, the analysis is carried out for a balanced odd harmonic case. This may have PS (n = 7, 13, 19, 25…), NS (n = 5, 11, 17, 23….) and ZS (n = 3, 9, 15, 21….) current components respectively. As the average power for these harmonic current components is zero, the generalized oscillatory power, $\tilde{p}_p(t)$ produced by the shunt converter can be given by (11)-(13) using (2) as follows:

$$\tilde{p}_{p+}(t) = \sum_{n=7,13,19}^{\infty} 3V_{mp+}I_{nh+}\cos((m-n)\omega t + \varphi_{vp+} - \varphi_{inh+}) \quad (11)$$

$$\tilde{p}_{p-}(t) = -\sum_{n=5,11,17}^{\infty} 3V_{mp+}I_{nh-}\cos((m+n)\omega t + \varphi_{vp+} + \varphi_{inh-}) \quad (12)$$

$$\tilde{p}_{p0}(t) = \sum_{n=3,9,15}^{\infty} 3V_{mp0}I_{nh0}\cos((m-n)\omega t + \varphi_{vp0} - \varphi_{inh0}) - \sum_{n=3,9,15}^{\infty} 3V_{mp0}I_{nh0}\cos((m+n)\omega t + \varphi_{vp0} + \varphi_{inh0}) \quad (13)$$

As ZS voltage, V_{mp0} is usually small compared to the PS and NS voltages at fundamental frequency, $m = 1$, the oscillatory power, $\tilde{p}_{p0}(t)$ is very small and can be neglected. After simplification, the total oscillatory power, $\tilde{p}_{pt}(t)$ at the dc-link becomes:

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$$\tilde{p}_{pt}(t) = \sum_{n=7,13,19}^{\infty} 3V_{mp+}I_{nh+}\cos((m-n)\omega t + \varphi_{vp+} - \varphi_{inh+}) - \sum_{n=1,5,11}^{\infty} 3V_{mp+}I_{nh-}\cos((m+n)\omega t + \varphi_{vp+} + \varphi_{inh-}) \quad (14)$$

In this case, the dc-link capacitor size can be estimated using (11) and (12) respectively that can be calculated by (15)-(16). The dc-link capacitor depends on upper and lower dc-link voltage limits, v_u and v_l, PS r.m.s voltage magnitude, v_{mp+}, PS and NS harmonic current, $i_{mnh\pm}$ and the harmonic order, n

$$C_{dc-link} = \frac{12v_{mp+}i_{nh+}}{\omega(n-1)(v_u^2 - v_l^2)} \text{ for m = 1 and n = 7, 13...} \quad (15)$$

$$C_{dc-link} = \frac{12v_{mp+}i_{nh-}}{\omega(n+1)(v_u^2 - v_l^2)} \text{ for m = 1 and n = 1, 5...} \quad (16)$$

IV. Proposed Control Methodologies

A. Phase locked loop (PLL) reference set

The proposed control strategies utilize six reference waveforms produced from a PLL which are defined in (17). The PLL angle, θ_{PLL} is calculated using the grid side voltage vectors.

$$\begin{cases} R_aS = \sin(\theta_{PLL}) \\ R_aC = \sin(\theta_{PLL}+90°) = \cos(\theta_{PLL}) \\ R_cS = \sin(\theta_{PLL}+120°) \\ R_cC = \sin(\theta_{PLL}+210°) = \cos(\theta_{PLL}+120°) \\ R_bS = \sin(\theta_{PLL}+240°) = \sin(\theta_{PLL}-120°) \\ R_bC = \sin(\theta_{PLL}+330°) = \cos(\theta_{PLL}-120°) \end{cases} \quad (17)$$

B. Control strategies of series converter

In this paper, the series converter is controlled in PSRF and negative sequence reference frame (NSRF) controllers provide voltage regulation as presented in Fig. 3. The series converter is controlled to force the output load voltages to follow the positive sequence sinusoidal reference voltages, v_{ref}. The error voltages, $v_e = v_{ref} - v_{load}$ in abc coordinates are transformed into stationary a dq0 PSRF and a dq NSRF for the extraction of positive, zero and negative sequence voltage error vectors. These dc voltage errors are independently regulated by the PI controllers and the residual error voltages are then transformed into rotating abc coordinates. These are normalized by the dc link voltage and fed through the series converter that regulates the load voltages. The zero sequence voltage controller was added within the PSRF to regulate the zero sequence voltage component. In this control system, a time delay T_d (1.5 times the switching period of the PWM modulator) is considered to reflect the sampling and calculation delays in the discrete time PWM controller. To remove the high frequency ripples in the load voltages, a second order output filter $H(s)$ is considered in the forward path of the control system. The filter characteristic and detailed stability analysis of the control loop is discussed in Section V. The positive and zero sequence voltage extraction was performed in the dq0 PSRF using (18), whereas the negative sequence voltage extraction was achieved in the dq NSRF using (19).

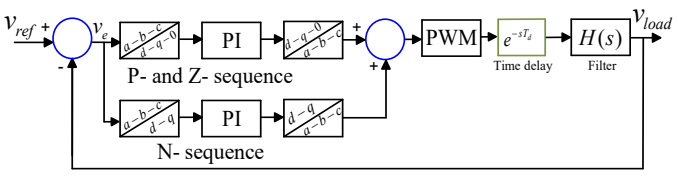

Fig. 3. Series converter ac load voltage control system.

$$\begin{bmatrix} V_{d+} \\ V_{q+} \\ V_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin\theta_{PLL} & \sin(\theta_{PLL}-\frac{2\pi}{3}) & \sin(\theta_{PLL}+\frac{2\pi}{3}) \\ \cos\theta_{PLL} & \cos(\theta_{PLL}-\frac{2\pi}{3}) & \cos(\theta_{PLL}+\frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_{e,a} \\ v_{e,b} \\ v_{e,c} \end{bmatrix} \quad (18)$$

$$\begin{bmatrix} V_{d-} \\ V_{q-} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} -\sin\theta_{PLL} & -\sin(\theta_{PLL}+\frac{2\pi}{3}) & -\sin(\theta_{PLL}-\frac{2\pi}{3}) \\ \cos\theta_{PLL} & \cos(\theta_{PLL}+\frac{2\pi}{3}) & \cos(\theta_{PLL}-\frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} v_{e,a} \\ v_{e,b} \\ v_{e,c} \end{bmatrix} \quad (19)$$

C. Control strategies of shunt converter

The conventional methods use a stationary α, β reference frame to construct an instantaneous power control method [25, 26, 29, 31] that produces harmonics in the line currents. For example, the direct control of 2ω oscillatory power in the stationary α, β frame generates fundamental and third harmonic line currents [36]. In this paper, improved control strategies of the shunt converter for 2ωHV suppression are implemented using PS and NS framework approaches to avoid generation of harmonic currents. A complete diagram of the proposed control strategy for the shunt converter is shown in Fig. 4 which has three subsystems: PS current extraction system to control average power in Fig. 5, a NS current extraction system to suppress 2ωHV in Fig. 6(a) and a current regulator of the shunt converter in Fig. 7. The PS current is used to meet the real power requirement of the series converter and these arise when the PS network voltages need to be raised or lowered. The NS current is used to suppress the 2ωHV oscillations on the dc-link. It is assumed that the instantaneous voltage across the dc-link capacitor of the proposed 4L-UPFC in Fig. 2 consists of average and 2ωHV components as follows:

$$\begin{cases} v_{dc}(t) = V_{dc} + \tilde{v}_{dc}\sin(2\omega t + \varphi) \\ v_{dc}(t) = V_{dc} + \tilde{v}_{dc}\sin(2\omega t)\cos(\varphi) + \tilde{v}_{dc}\cos(2\omega t)\sin(\varphi) \end{cases} \quad (20)$$

The positive sequence current extraction system in Fig. 5 has three subsystems: a PI regulator, a fast overvoltage proportional controller and a feedforward control system.

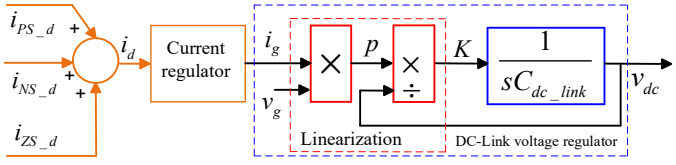

Fig. 4. Complete diagram of shunt converter current control system with dc-link voltage regulator.

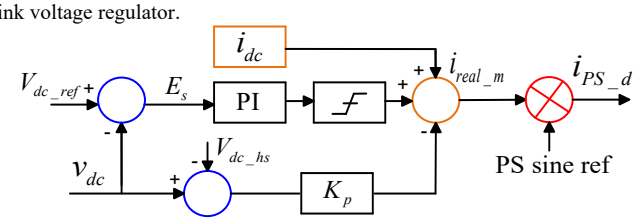

Fig. 5. Positive sequence current extraction method.

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The feedforward current demand I_{dc} is estimated based on the instantaneous power of the series and shunt converters of the 4L-UPFC. This is estimated by the instantaneous power difference between the series and shunt converters and the input PS voltage. The dc-link voltage control loop compares the average dc-link voltage, V_{dc} with the reference dc-link voltage, V_{dc_ref}. The PI controller responds to the error, E_s in the average dc-link voltage and forces it to zero. The overvoltage proportional control compares V_{dc} with the high speed reference dc-link voltage, V_{dc_hs} and uses a proportional controller which may demand short bursts of PS current to limit the voltage excursions during transients that persist for a few milliseconds. The overvoltage control system is a protection limit for the dc-link capacitor voltage regulator. If there is an overvoltage in the dc-link capacitor, the control system reduces it rapidly by controlling the PS current of the shunt converter. These three subsystems produce a total PS magnitude demand signal, i_{real_m} that is multiplied by a three phase PS sine reference set to calculate the total PS current demands, i_{PS_d} as per (21) to satisfactorily control average power of the four-leg shunt converter as seen from (7).

$$i_{PS\_d} = i_{real\_m} \times R_a S + i_{real\_m} \times R_b S + i_{real\_m} \times R_c S \quad (21)$$

Fig. 6(a) shows the negative sequence current extraction system. The instantaneous dc-link capacitor voltage, v_{dc} is directly used to generate the NS current demand for suppressing 2ωHV fluctuation on the dc-link. The extraction of the dc-link voltage magnitude at 2ω is performed by sine and cosine synchronous detectors with associated 10 ms moving average filters using (17). The outputs of the sine and cosine synchronous detectors, $\tilde{v}_{dc}/2\times\cos(\varphi)$ and $\tilde{v}_{dc}/2\times\sin(\varphi)$, are forced to zero by the actions of the PI controllers. The residual oscillatory power components, S_k and C_k in phase with $\sin(\theta_{PLL})$ and $\cos(\theta_{PLL})$ respectively are cancelled by injecting a sinusoidal NS current, i_{NS_d} represented by (22) into the phase current demand. Fig. 6(b) shows the neutral current control system of the 4L-UPFC. For any unbalanced load operation, there will be the neutral current i_N flowing to the upstream side of the 4L-UPFC device and this needs to be compensated. The neutral current flowing to the upstream of the 4L-UPFC is calculated by the grid side phase currents which are forced to follow the zero reference neutral current by the action of a PI regulator.

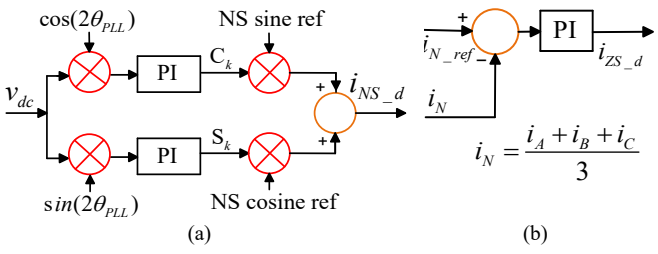

Fig. 6. (a) Negative sequence current extraction method for 2ωHV control, and (b) neutral current control method.

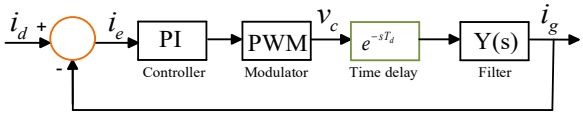

Fig. 7. Current regulator of the shunt converter.

The PS, NS and ZS current demand produces the total three phase current demand i_d represented by (23) that is driving the shunt converter.

$$i_{NS\_d} = S_k \times R_a C + C_k \times R_a S + S_k \times R_c C + C_k \times R_c S + S_k \times R_b C + C_k \times R_b S \quad (22)$$

$$i_d = i_{PS\_d} + i_{NS\_d} + i_{ZS\_d} \quad (23)$$

A closed loop current regulator as shown in Fig. 7 is used to control the shunt converter current. The three phase grid currents, i_g are measured and compared with i_d to calculate the current error, i_e. The PI controller drives the error to get the target voltages for the shunt converter to regulate the currents. The voltage generated by the PI controllers is normalized by the dc-link voltage. This is fed through the three dimensional space vector modulator (3D-SVM) [37] to generate modulated PWM pulses to trigger the shunt converter's IGBTs. The shunt converter voltage v_c and input filter transfer admittance $Y(s)$ produce the controlled grid current i_g. The nonlinear system in the dotted area in Fig. 4 has been linearized to calculate an effective linearized gain, K relating positive sequence current demand to average dc-link current into the dc-link capacitor. In the linearization process, the controlled grid currents and the grid voltages are used to calculate the power, p and the linearized gain, K (W/A) is calculated using p and v_{dc}.

D. *Decoupling of multiple control loops*

The proposed control strategies for the series and shunt converters of the 4L-UPFC are effectively decoupled at the dc-link. The series converter is controlled in a dq0 reference frame for load voltage regulation as shown in Fig. 3. The shunt converter uses the nested control structure shown in Fig. 4. The inner most control loop is a wide bandwidth current regulator which allows the converter to be controlled as a generalized current source. The outer control loops present an aggregated current demand which is the linear superposition of the demands of the lower bandwidth outer loops such as the dc-link voltage regulator and any shunt current demands for phase balancing.

V. Filter Designs and Stability Analysis

A. *Filter design with passive damping*

The basic diagram of the grid connected current controlled voltage source inverter with a LC filter is shown in Fig. 8. The L_f and C_f are the converter side filter inductor and capacitor, v_c is converter voltage and L_g denotes the grid side inductor. The LC filter inductor provides continuous current but has a degree of current ripple and the capacitor can absorb some of these current ripples and produce continuous voltages. The grid is modelled by an equivalent inductor, L_g and an ideal voltage source, v_g. Damping is provided to improve the stability of the

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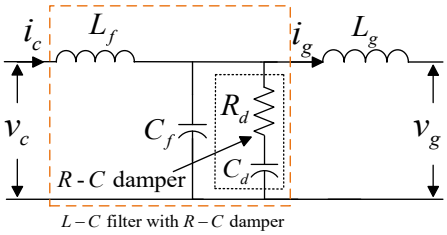


Fig. 8. Schematic diagram of LC filter with R-C damper (dotted box).

current regulator by suppressing the resonance peak caused by the converter side filter and grid side parameters [38-42]. The suppression of the resonance is performed by either passive damping with an additional *R* or *R-C* damper circuit [41] or active damping [40] or methods such as state variable feedback [42]. As active damping requires a higher number of sensors that have additional cost or a state estimation approach which increases the control complexity [41], this work considers passive damping provided by R_d and C_d as shown in Fig. 8. The grid side current, i_g is taken as a feedback which improves the stability of the current controller compared to converter side current feedback [38]. The filter admittance $Y(s)$ for grid current control can be derived as in (24).

$$Y(s)=\frac{I_g(s)}{V_c(s)}=\frac{sR_dC_d+1}{s^4L_fL_gC_fR_dC_d+s^3L_gL_f(C_f+C_d)+s^2R_dC_d(L_g+L_f)+s(L_g+L_f)} \tag{24}$$

B. Stability analysis of the control systems

1) Shunt converter current regulator

The plant model of the current regulator in Fig. 7 can be developed in (25) using (24) and a time delay ($T_d=1.5\times T_{sw}$) for the digital PWM modulator.

$$G_{pi}(s)=e^{-sT_d}\times Y(s)$$
$$=\frac{(sR_dC_d+1)\times e^{-sT_d}}{s^4L_fL_gC_fR_dC_d+s^3L_gL_f(C_f+C_d)+s^2R_dC_d(L_g+L_f)+s(L_g+L_f)} \tag{25}$$

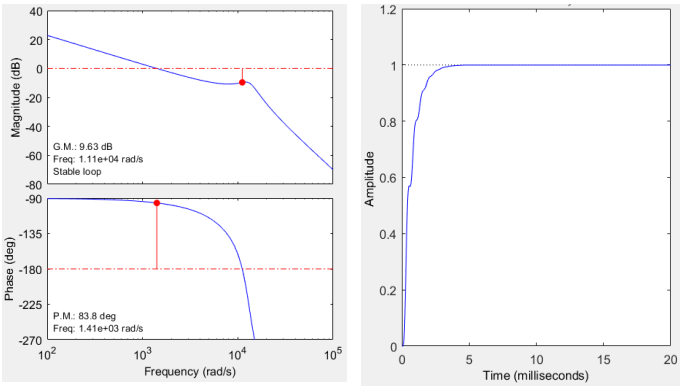
The filter and grid parameters are listed in Table I. The open loop transfer function of the current regulator with control parameters (K_{pi} = 5 and K_{ii} = 2) is expressed as in (26) using (25).

$$G_{i\_ol}(s)=G_{ci}(s)\times G_{pi}(s)=(K_{pi}+\frac{K_{ii}}{s})\times G_{pi}(s) \tag{26}$$

The stability of the control loops is analyzed using the Matlab Control System Designer Toolbox. The stability of the current regulator is shown in Fig. 9 using a Bode diagram and step response analysis. The open loop Bode diagram in Fig. 9(a) shows that the system is stable with no resonant gain overshoot and a -3dB bandwidth of 1.41 $\times 10^3$ rad/s. The current control system is well regulated and maintains sufficient gain and phase margin. The step response of the closed loop control system (control to output) in Fig. 9(b) shows that the system is well damped and stable. Therefore, the stability analysis confirms that the second order *LC* filter with passive damping is not susceptible to resonance and improves the stability of the overall converter system.

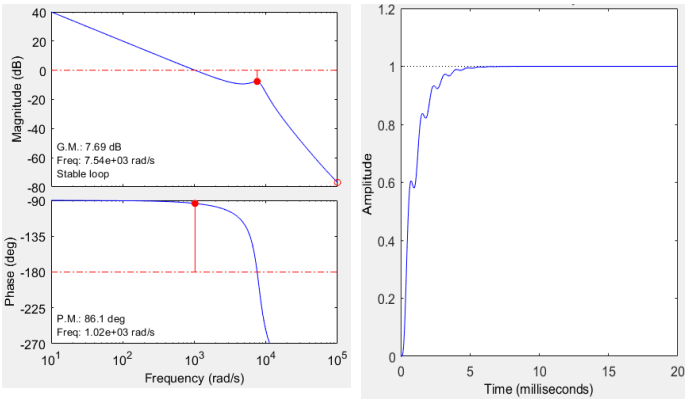
2) Series converter ac load voltage control system

The plant model of the load voltage regulation system for the series converter in Fig. 3 can be derived as in (28). The similar



(a) (b)

Fig. 9. Stability analysis of the current regulator: (a) Bode plot of open loop system, and (b) step response of closed loop system (control to output).



(a) (b)

Fig. 10. Stability analysis of the series converter ac load voltage control system: (a) Bode plot of open loop system, and (b) step response of closed loop system.

filter network as indicated by the dotted box in Fig. 8 is used at the load end of the 4L-UPFC device as shown in Fig. 2. The transfer function $H(s)$ of the filter for regulated load voltage is derived in (27) and the plant model of the load voltage regulation system is presented in (28).

$$H(s)=\frac{(sR_dC_d+1)}{s^3L_fC_fR_dC_d+s^2(L_fC_d+L_fC_f)+sR_dC_d+1} \tag{27}$$

$$G_{p\_vl}(s)=e^{-sT_d}\times H(s)$$
$$=\frac{(sR_dC_d+1)\times e^{-sT_d}}{s^3L_fC_fR_dC_d+s^2(L_fC_d+L_fC_f)+sR_dC_d+1} \tag{28}$$

The open loop transfer function of the voltage regulation system with control parameters (K_{pvl} = 0.1 and K_{ivl} = 10000) is derived as in (29).

$$G_{vl\_ol}(s)=G_{c\_vl}(s)\times G_{p\_vl}(s)=(K_{pvl}+\frac{K_{ivl}}{s})\times G_{p\_vl}(s) \tag{29}$$

The stability analysis of the series converter load voltage regulation system with the filter dynamics is presented in Fig. 10 by a Bode diagram and step response analysis. The open loop Bode diagram in Fig. 10(a) shows that the system is stable and has a 7.69 dB gain margin and 86.1° phase margin. The step response of the closed loop control system (control to output) in Fig. 10(b) shows that the system is also stable.

3) DC link capacitor voltage regulator

The control system for the dc-link capacitor voltage regulator is shown in Fig. 4. The open and closed loop transfer functions

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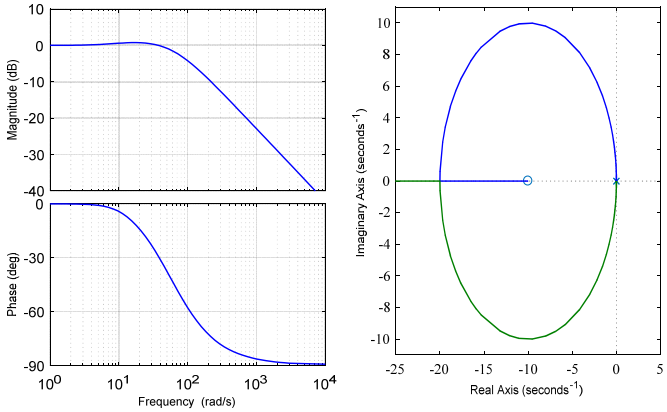

Fig. 11. Stability analysis of the dc-link capacitor voltage control system: (a) Bode diagram of closed loop system, and (b) root locus of open loop system.

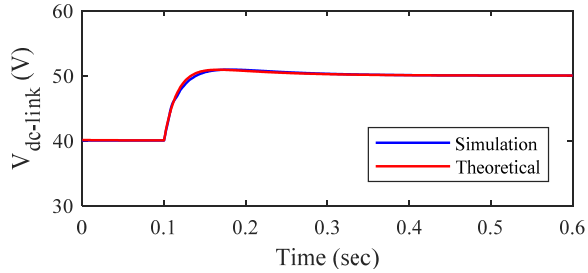

Fig. 12. Step response of the dc-link capacitor voltage control system.

of the dc-link capacitor voltage regulator in (30) are derived by the linearization at the selected dc-link voltage operating point. A 66 μF film capacitor is used as a dc-link and the effective linearized gain, K is calculated to be 0.795 W/V for a 40 V dc-link. A proportional gain, $K_{p\_dc} = 0.006$ and an integral gain, $K_{i\_dc} = 0.06$ has been used to regulate the dc-link voltage.

$$\begin{cases} G_{dc\_ol}(s) = \dfrac{sKK_{p\_dc} + KK_{i\_dc}}{s^2 C_{dc\_link}} \\ G_{dc\_cl}(s) = \dfrac{G_{dc\_ol}(s)}{1 + G_{dc\_ol}(s)} = \dfrac{sKK_{p\_dc} + KK_{i\_dc}}{s^2 C_{dc\_link} + sKK_{p\_dc} + KK_{i\_dc}} \end{cases} \quad (30)$$

The closed loop Bode diagram of the dc-link capacitor voltage control system is shown in Fig. 11(a) and shows that the control system is stable with a small (0.78 dB) gain overshoot at 18 rad/s and a -3dB bandwidth of 81.6 rad/s. The root locus analysis in Fig. 11(b) shows that all poles are in the left half of the s-plane. Fig. 12 shows the step response of the dc-link capacitor voltage control system. At t = 0.1 sec, a step change of the dc-link voltage from 40 to 50 V is applied to see the dc-link voltage controller response. Fig. 12 shows that the simulated step response closely follows the theoretical result.

4) Dynamic response of load voltage regulator

Fig. 13 shows the dynamic response of the series converter load voltage regulation system. The series converter voltage control system controls the load voltages to follow the reference voltages of 21.21 V (peak) with a balanced load of 30 Ω in each phase. The supply voltages are 21.21 V (peak) except phase "c" (blue) where this is intentionally lowered to 18 V peak to have unbalanced supply systems. Fig. 13(a)-(c) show regulated load voltages, shunt converter input voltages and injection voltages. It shows that, from t = 0 to t = 20 ms, the load voltage is well

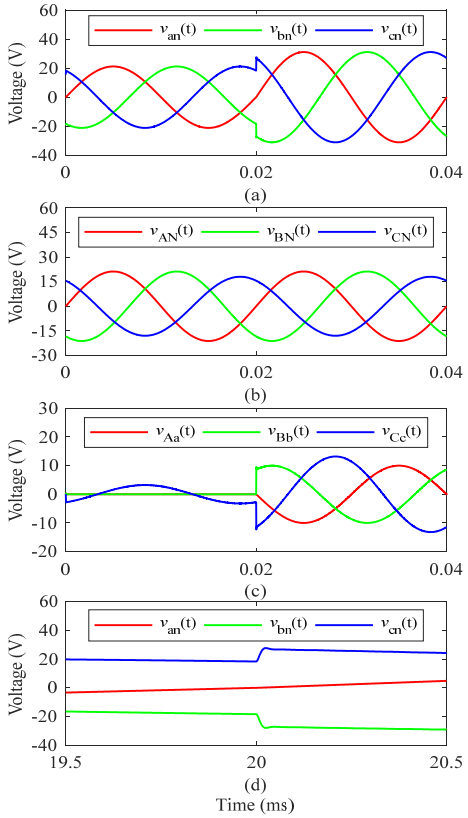

Fig. 13. Dynamic response of the voltage control system: (a) load voltages (v_{an}, v_{bn} and v_{cn}), (b) shunt converter input voltages (v_{AN}, v_{BN} and v_{CN}), (c) series injection voltages (v_{Aa}, v_{Bb}, and v_{Cc}), and (d) response of voltage controllers.

regulated at 21.21 V and the phase "c" injects a compensating voltage of 3.21 V to regulate load voltages. When there is a dynamic change in reference voltages from 21.21 V to 31.21 V at t = 20 ms, the controllers start to inject compensating voltages to follow the reference voltages at 31.21 V as seen in Fig. 13(a) and (c). Fig. 13(d) shows the step response of the load voltage controllers for the dynamic changes in reference voltages. The result shows that the controllers respond rapidly to track any dynamic changes in reference voltages. The series converter ac voltage control loop is designed to be faster than the dc-link capacitor voltage regulator. Therefore, it rejects the 100 disturbance (100 Hz ripple voltage) from the dc-link of the UPFC by the loop gain. The dynamics of dc-link capacitor voltage control loop are decoupled and is not affected by the dynamics of series converter ac load voltage control loop and shunt converter current control loop.

VI. Modelling and Simulation Results

Typical 500 meter long Australian distribution feeders are used to build the simulation model of the 4L-UPFC system. The feeders consist of a 7/3.75 mm all aluminum conductor with an equivalent impedance of (0.452+j0.270) Ω/km [13] as indicated within the dotted lines in Fig. 14.

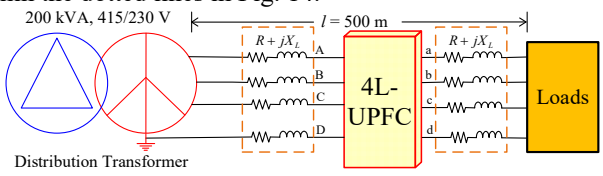

Fig. 14. Simulation model of 4L-UPFC used in LV distribution networks [13].

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The 4L-UPFC based voltage regulator is connected at the middle of the feeders between the transformer and loads. A 100 kVA, 415/240 Vrms distribution transformer that has a per-unit series impedance of 0.01+j0.03 Ω is used to supply the feeders. For the simulation studies, each phase of the distribution feeder is loaded by a 50 Arms 0.95 pf lagging load and an additional 20 Arms unity pf load is connected at Phase "b" that is switched on at 10 ms. A very small 10 μF capacitor is used as the dc-link capacitor. The input voltage to the UPFC device is purposefully made unbalanced as seen at the phase "c" voltage which is 10 Vrms lower than the other phase voltages. The voltage is well regulated at 240 Vrms at the output side of the UPFC as seen in Fig. 15(b) and the series injection voltage at phase "c" is always higher as shown in Fig. 15(c). The series converter of the 4L-UPFC adds a combination of PS, NS and ZS voltages to control

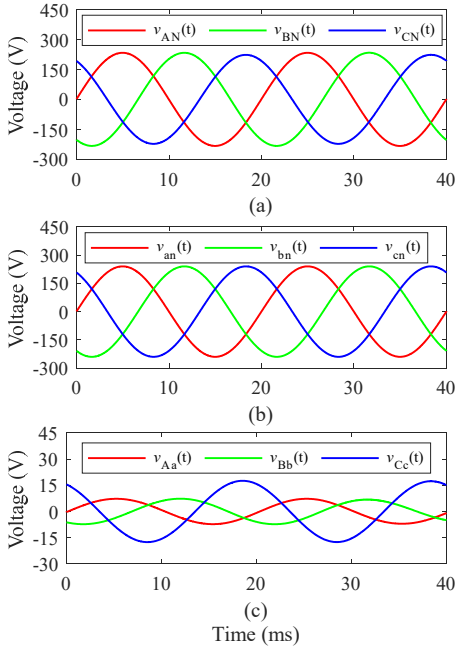

Fig. 15. Simulation results with 2ωHV control: (a) regulated load voltages (v_{an}, v_{bn} and v_{cn}), (b) shunt converter input voltages (v_{AN}, v_{BN} and v_{CN}), and (c) series injection voltages (v_{Aa}, v_{Bb}, and v_{Cc}).

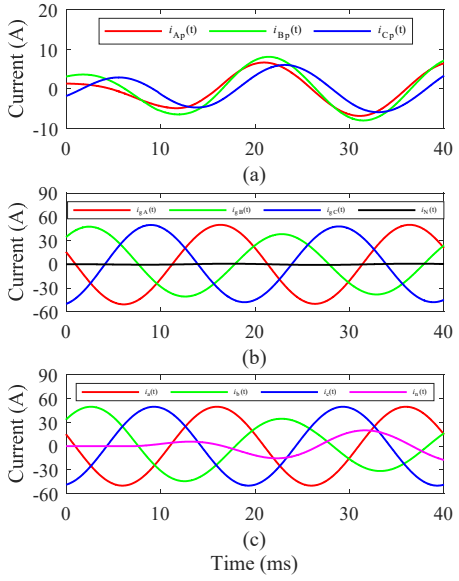

Fig. 16. Simulation results: (a) shunt converter input currents (i_{Ap}, i_{Bp}, and i_{Cp}), (b) grid currents (i_{gA}, i_{gB}, i_{gC} and i_N), and (c) output currents (i_a, i_b, i_c and i_n).

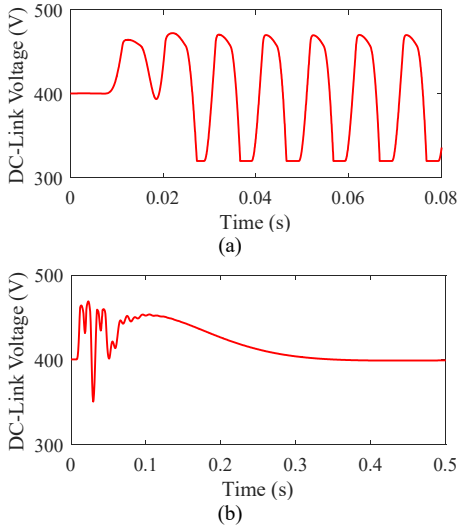

Fig. 17. DC-link voltage of 4L-UPFC: (a) before 2ωHV control applied, and (b) after 2ωHV control applied.

the voltages at the output load end. The simulation results of the shunt converter, grid and load currents are shown in Fig. 16. When a 20 Arms additional load commences its operation in phase "b" at t = 10 ms, the phase "b" current reduces in magnitude as seen in Fig. 16(b) and (c). Prior to t = 10 ms, the shunt converter currents are balanced as this draws balanced compensation currents from the grid. The grid and load currents are also completely balanced and no current flows through the neutral conductor. However, when the 20 Arms additional load commences its operation in phase "b" at t = 10 ms, then all currents become unbalanced. The shunt converter starts to draw a combination of PS, NS and ZS currents. The neutral current/zero sequence current controller is applied to draw a compensation current that forces the neutral current in the grid side to nearly zero as shown in Fig. 16(b).

The dynamic performance of dc-link voltage of the proposed 4L-UPFC with and without a 2ωHV control system is presented in Fig. 17(a)-(b). Fig. 17(a) shows that the dc-link capacitor voltage is well regulated at 400 V dc prior to the additional load in phase "b" starts operation. However, the dc-link voltage produces 2ω (100 Hz) a ripple voltage as the distribution network becomes unbalanced by the additional load in phase "b" at t = 10 ms. However, the 2ω ripple voltage component disappears from the dc-link capacitor in the steady state as shown in Fig. 17(b).

VII. Experimental Setup

A small-scale three-phase distribution level 4L-UPFC prototype was built. The experiments were conducted at approximately one tenth of the nominal LV distribution system voltage to comply with laboratory occupational health and safety requirements. Fig. 18(a)-(c) show the 4L-UPFC development board, experimental system and schematic respectively. Three IGBT modules were used to produce a total of eight phase legs for the series and shunt converters. Each module has three phase legs with bootstrap gate drivers. A 66 µF film capacitor was used as a dc-link capacitor in the experimental system. The detailed specification of the parameters for 4L-UPFC system is shown in Table I.

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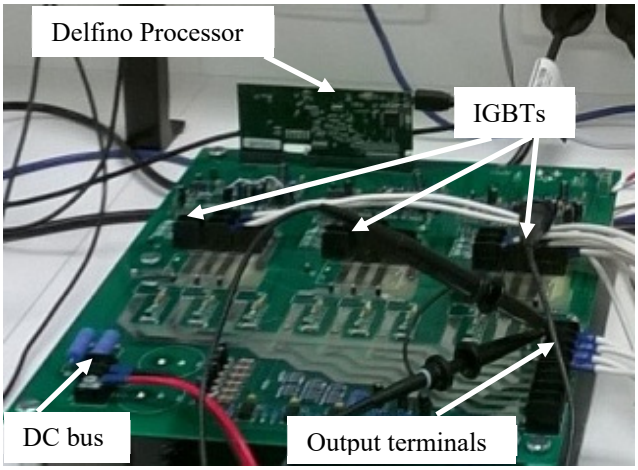
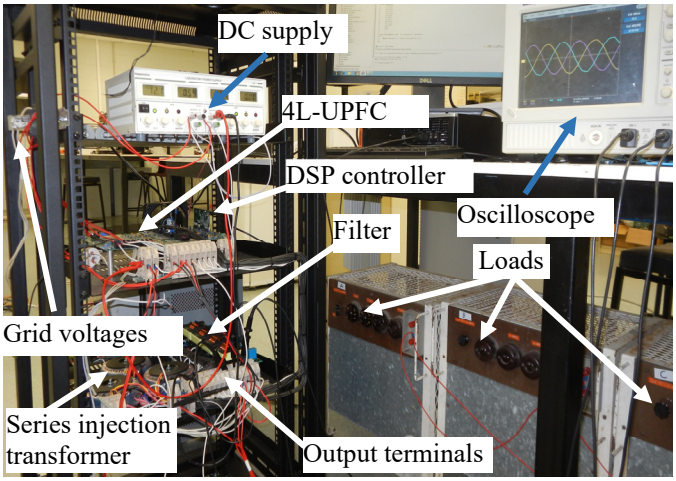


(a)



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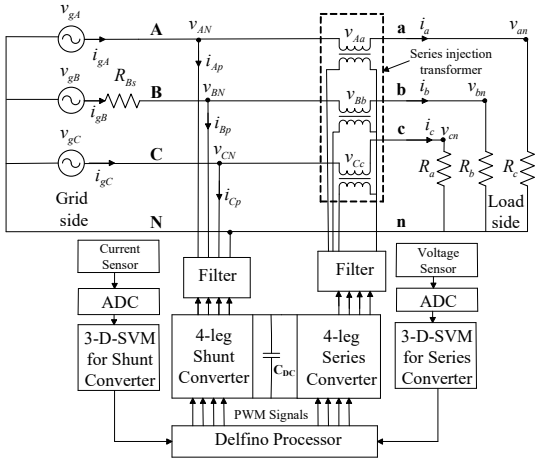


(c)

Fig. 18. Experimental setup: (a) pictorial view of 4L-UPFC development board, (b) experimental test platform, and (c) schematic diagram of 4L-UPFC.

VIII. Experimental Results

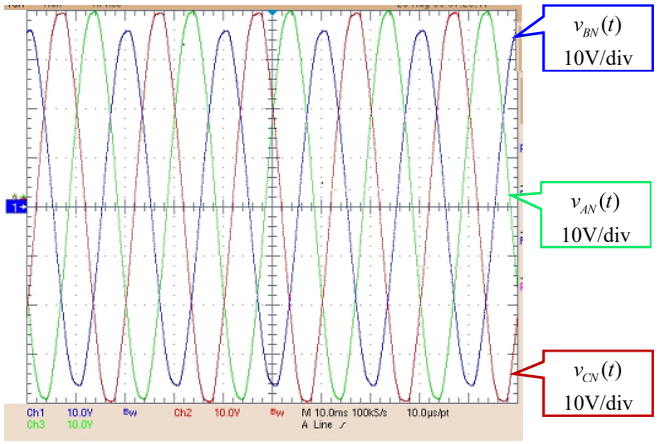
The effectiveness of the proposed control methods for series and shunt converter of the 4L-UPFC is experimentally demonstrated in this section. The experimental results are presented for the following cases, namely (i) voltage regulation and (ii) voltage regulation and 2ωHV suppression.

TABLE I
Specification of 4L-UPFC Experimental System

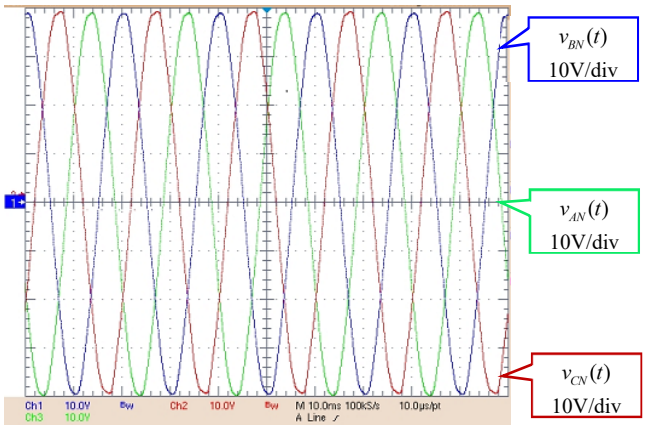
Parameters	Values
IGBT Modules	STGIPL14K60 (15 A, 600 V)
Series injection transformer	240 V:24 V (rms)
Grid voltage, v_g	28 V (rms)
Filter inductor, L_f	2 mH
Filter capacitor, C_f	5 μF
Damping resistor, R_d	27 Ω
Damping capacitor, C_d	5 μF
Grid impedance, L_g	1.6 mH
Switching frequency, f_{sw}	20 kHz
Time delay, T_d	75 μs
Grid voltage frequency, f	50 Hz
Nominal load, R	30 Ω
DC-link capacitor, $C_{dc\text{-}link}$	66 μF
DC-link voltage, $V_{dc\text{-}link}$	40 V
DSP Controller	F28377D
Series resistor, R_{bs}	2.35 Ω

A. Performance of 4L-UPFC for voltage regulation

In the first phase of the experimental demonstration, only the series converter of the 4L-UPFC is taken into consideration to verify the correct operation of the series converter ac voltage control system. The loads are balanced; however, the shunt converter input voltages were purposefully made unbalanced by adding a 2.35 Ω resistor, R_{bs} at phase "b" that lowers the phase "b" (blue) supply voltage magnitude as shown in Fig. 19(a). The regulated load voltages are shown in Fig. 19(b).



(a)



(b)

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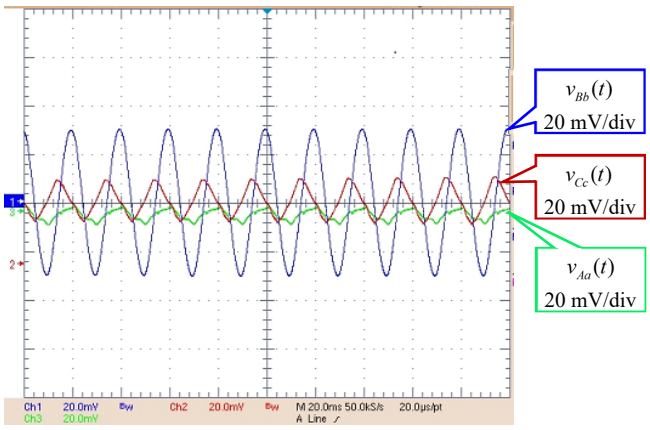

(c)

Fig. 19. Experimental results: (a) shunt converter input voltages (v_{AN}, v_{BN} and v_{CN}), (10V/div, 10ms/div), (b) regulated load voltages (v_{an}, v_{bn} and v_{cn}), (10V/div, 10ms/div), and (c) series injection voltages (v_{Aa}, v_{Bb}, and v_{Cc}), (20 mV/div, 20ms/div).

The results confirm the proper operation of the series converter as the output load voltages are well balanced. The series injection voltages are unequal in magnitude and phase as shown in Fig. 19(c). These are attenuated by a factor of 100. As phase "b" provides the compensating voltage, the voltage at phase "b" is higher than any other phases as seen in Fig. 19(c).

B. Performance of 4L-UPFC for voltage regulation and 2ωHV suppression

The series and shunt converters are both active while 2ωHV control in Fig. 6(a) is altered to active and inactive states. In this case, an unbalanced three-phase Y-connected resistive load (R_a = 15 Ω, R_b = 5 Ω, R_c= 220 Ω) is considered [29]. The supply voltages are unbalanced by introducing a small resistor in phase "b" as shown in the schematic at Fig. 18(c). To obtain a sufficient contrast, the oscilloscope data for voltages and currents are plotted in Matlab. Table II outlines the steady state performance of the 4L-UPFC.

TABLE II
SEQUENCE COMPONENTS OF VOLTAGE AND CURRENTS AT DIFFERENT POINTS OF THE EXPERIMENTAL SYSTEM

Sequence parameters	With 2ωHV control (Fig. 6(a))	Without 2ωHV control (Fig. 6(a))
PS grid voltage (V)	**15.47∠–109°**	**15.52∠–109°**
NS grid voltage (V)	**1.38∠–103.2°**	**0.92∠–146°**
ZS grid voltage (V)	**0.76∠–11.52°**	**0.62∠27.34°**
PS grid current (A)	3.16 ∠–115.7°	3.02∠65.55°
NS grid current (A)	1.62∠20.36°	1.16∠179.1°
ZS grid current (A)	1.17∠142.1°	1.16∠–34.4°
PS shunt converter input voltage (V)	**15.21∠–108.6°**	**15.48∠–108°**
NS shunt converter input voltage (V)	**1.83∠–109.9°**	**0.94∠–140°**
ZS shunt converter input voltage (V)	**1.24∠17.9°**	**0.82∠7.14°**
PS shunt converter input current (A)	**1.62∠56.9°**	**1.5∠54.77°**
NS shunt converter input current (A)	**0.69∠–122.6°**	**0.04∠138.4°**
ZS shunt converter input current (A)	0.07∠–119.9°	0.04∠–151°
PS load voltage (V)	**14.83∠–108.1°**	**14.80∠–108°**
NS load voltage (V)	**0.11∠117.5°**	**0.12∠117.1°**
ZS load voltage (V)	**0.36∠154.8°**	**0.45∠136°**
PS load current (A)	1.55∠–107°	1.57∠–108°
NS load current (A)	1.11∠0.59°	1.14∠–1.27°
ZS load current (A)	1.14∠147.5°	1.13∠145.6°

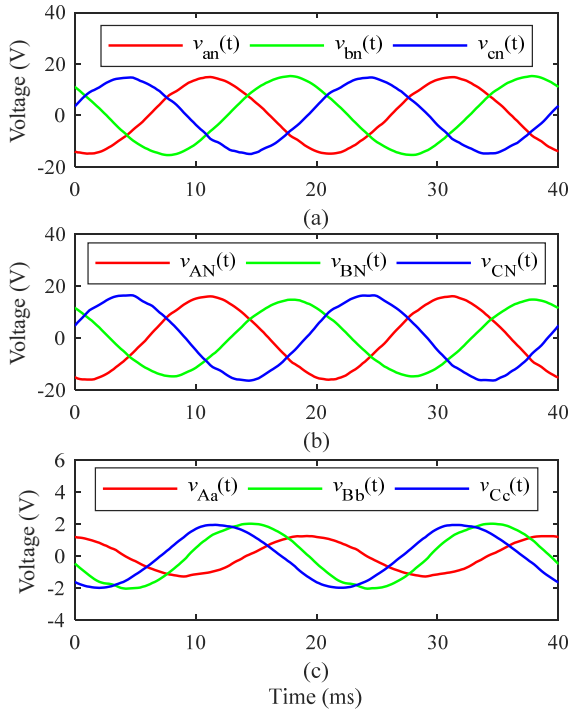

Fig. 20. Experimental results with 2ωHV control: (a) load voltages (v_{an}, v_{bn} and v_{cn}), (b) shunt converter input voltages (v_{AN}, v_{BN} and v_{CN}), and (c) series injection voltages (v_{Aa}, v_{Bb}, and v_{Cc}).

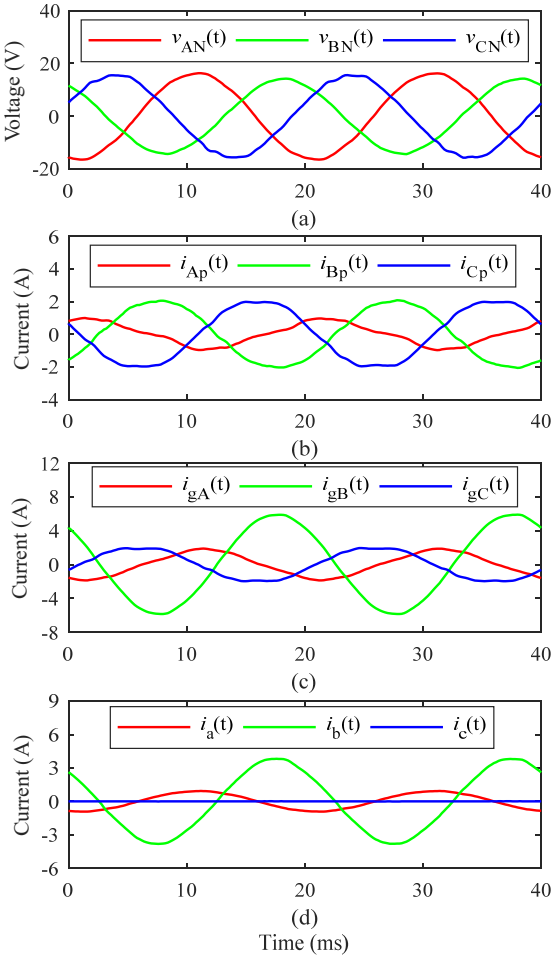

Fig. 21. Experimental results with 2ωHV control: (a) shunt converter input voltages, (v_{AN}, v_{BN}, v_{CN}), (b) shunt converter input currents (i_{Ap}, i_{Bp}, and i_{Cp}), (c) grid currents (i_{gA}, i_{gB}, and i_{gC}), and (d) output load currents (i_a, i_b, and i_c).

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As seen from Table II, the shunt converter increases NS current demand for suppressing the 2ωHV ripple from the dc-link capacitor. At the same time, the PS current demand increases to satisfy the real power requirement to correct the PS voltage drop at load terminal. It is also evident that, without the 2ωHV control system, NS current drawn by the four-leg shunt converter is nearly zero. In addition, in this case, the NS and ZS voltage magnitudes slightly increase and supply current from the grid reduces.

The effectiveness of the proposed sequence based control methods for series and shunt converters of the 4L-UPFC are shown in Figs. 20-23. The experimental results for the 4L-UPFC with 2ωHV control in Fig. 6(a) are shown in Figs. 20 and 21. In this case, the 2ωHV control in Fig. 6(a) is set to the active state. Fig. 20(b) shows that the shunt converter input voltages are quite unbalanced and v_{BN} (green trace) is low. The voltage is purposefully lowered by inserting a small series resistor in the supply. Fig 20(a) shows that the regulated load voltages are well balanced and exactly follow the peak of the reference voltages. The experimental results for the current regulator of the four leg shunt converter are shown in Fig. 21. As seen from Fig. 21(b), the shunt converter currents are slightly unbalanced. The shunt converter draws currents from the grid which are a combination of PS and NS currents to control load voltages and the 2ωHV at the dc-link capacitor simultaneously. The load currents are unbalanced as determined by the unbalanced load.

The experimental results for the 4L-UPFC without 2ωHV control in Fig. 6(a) are shown in Figs. 22 and 23. In this case, series converter ac voltage control system is active, however the 2ωHV control is turned to the inactive state. As series converter ac voltage control system is active, the series converter provides the correction voltage and ac load voltages become balanced as seen from Fig. 22(a) and (b). However, the shunt converter does not draw any NS current component from the grid for 2ωHV suppression as the 4L-UPFC is running without 2ωHV control. As a result, the shunt converter currents are seen to be nearly balanced in Fig. 23(b). Consequently, the input grid currents also reduce as shown in Fig. 23 (c). Fig. 23(d) shows that the load currents remain unchanged as determined by the loads.

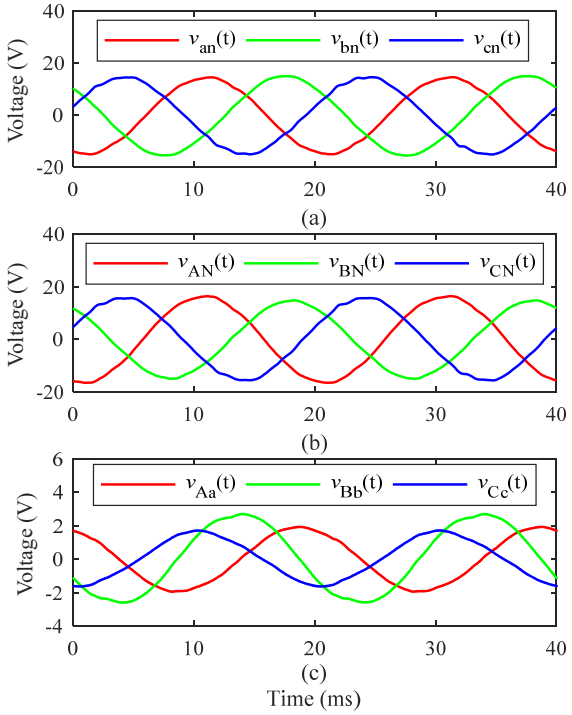

Fig. 22. Experimental results without 2ωHV control: (a) load voltages (v_{an}, v_{bn} and v_{cn}), (b) shunt converter input voltages (v_{AN}, v_{BN} and v_{CN}), and (c) series injection voltages (v_{Aa}, v_{Bb}, and v_{Cc}).

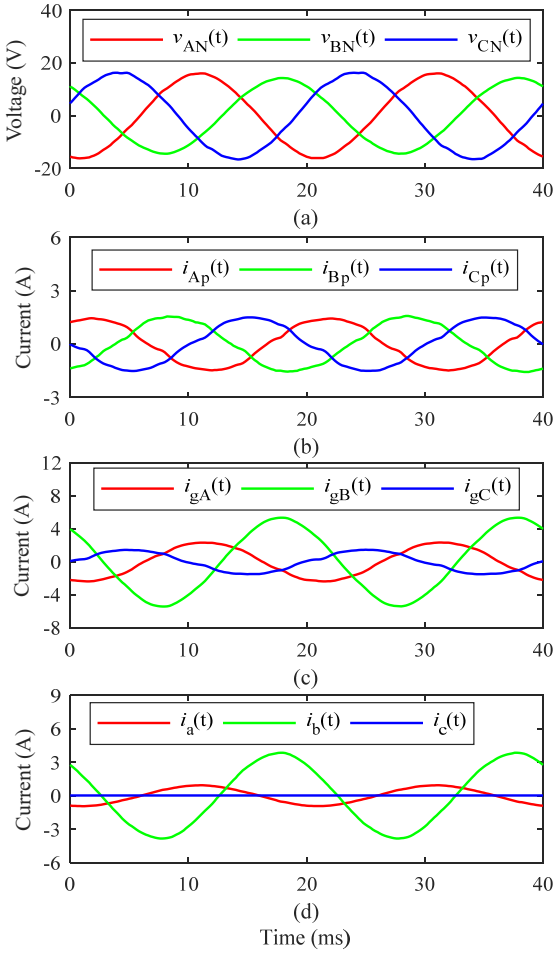

Fig. 23. Experimental results without 2ωHV control: (a) shunt converter input voltages, (v_{AN}, v_{BN}, v_{CN}), (b) shunt converter input currents (i_{Ap}, i_{Bp}, and i_{Cp}), (c) grid currents (i_{gA}, i_{gB}, and i_{gC}), and (d) output load currents (i_a, i_b, and i_c).

The effectiveness of 2ωHV suppression control system in Fig. 6(a) is validated by the experimental results as shown in Fig. 24. When the 2ωHV control system is set to the inactive state, the shunt converter cannot track the 2ωHV fluctuation and the dc-link capacitor therefore has to sustain a 100 Hz ripple. It is seen from the red trace in Fig. 24(a) that, without a 2ωHV control system, the ripple voltage, V_r is sinusoidal and fluctuates at 2ω (100 Hz). After the 2ωHV control system is applied, the 2ωHV fluctuation on the dc-link is significantly removed as seen from the blue trace in Fig. 24(a). This has been further confirmed by the frequency spectrum of the dc-link voltage ripple which is presented in Fig. 24(b) using the 500 - point discrete Fourier transform analysis of the traces in Fig. 24(a). The frequency spectrum shows that the 2ωHV is centered at 100 Hz with a magnitude of 3.28 V peak without the 2ωHV

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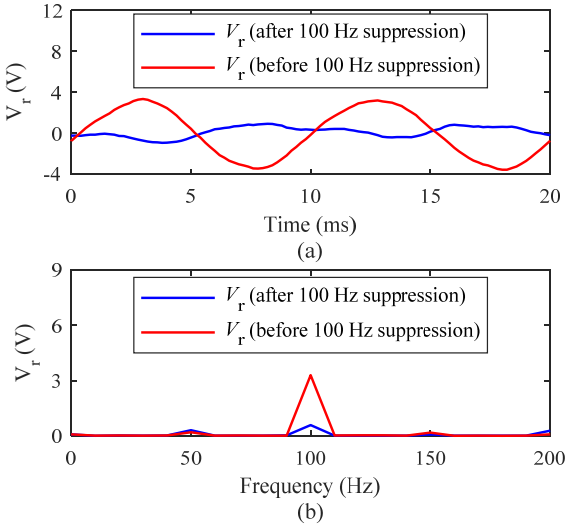

Fig. 24. Experimental results before and after 2ωHV control applied: (a) dc-link ripple voltage, V_r, and (b) frequency spectrum.

control system. However, this reduces to 0.58 V peak after the 2ωHV control system is applied in the 4L-UPFC experimental system. It is seen from Fig. 24(b) that the 2ωHV control system can suppress the ripple voltage by 83%.

IX. Conclusion

In this paper, improved sequence based control strategies are proposed for the series and shunt converters of a 4L-UPFC to regulate the ac load voltages and simultaneously suppress the 2ωHV from the dc-link of the 4L-UPFC. A controlled PS current is used for ac load voltage correction while a controlled NS current is utilized for suppressing the 2ωHV component from the dc-link capacitor of the 4L-UPFC. The simulation and experimental results show that the proposed sequence based control strategies applied to the series and shunt converters of the 4L-UPFC prototype provide precise load voltage regulation while, simultaneously, 2ωHV is suppressed from the dc-link of the UPFC without any additional compensating circuit. A relational framework is established to design an application specific dc-link capacitor size in regard to the operating voltages and currents of the converter. The stability analysis of multiple control loops of the 4L-UPFC with the proposed control scheme is investigated and the results show that the control loops are decoupled, and the overall converter system are stable. It is noticed that the proposed grid current feedback based passive damping method enhances the stability of the overall converter system as demonstrated by the frequency response and step response analysis. The experimental results also show that improved phase current balance can be provided by the shunt converter and extend the lifetime of distribution transformers. The compact 4L-UPFC can be applied as a pole-top installation in LV distribution feeders to allow increased penetration of PV systems and to provide economic and operational benefits.

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