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Design and Implementation of a Single-Phase 15-Level Inverter With Reduced Components for Solar PV Applications

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ABSTRACT A new single-phase 15-level inverter with a reduced number of components for the Solar PV application is proposed in this paper. It is incorporate the proposed inverter with a boost converter to extract energy from the solar PV modules, the proposed inverter aids to generate fifteen stepped output voltage levels with lower THD. The proposed inverter can improve efficiency and reduce losses, cost, and complexity of the overall system. The conventional boost converter will boost the output voltage to a maximum voltage from Solar PV with MPPT(P&O). The proposed inverter is tested experimentally using the dSPACE RTI 1104 controller along with MATLAB/Simulink. A detailed comparison with existing MLIs with the proposed inverter. The work presents experimental results not only to show its efficiency but also to the effectiveness under different circumstances of linear and non-linear loads. The inverter is stable during the non-linear loads and well suits for grid-connected systems.

INDEX TERMS Inverter, MPPT, converter, solar PV, total harmonics distortion (THD).

I. INTRODUCTION

The world has been experiencing an everlasting bloom in both developments and population; there is a huge power demand. The world is also trying to shift towards greener and sustainable energy. Researchers are coming up with fresh ones and complex approaches for using complex methods to tackle both the power demands and the pollution caused by extracting power. However, the extraction of power from a renewable source is not as simple as from conventional sources. DC is the form of energy derived from renewable sources such as solar energy, and our current transmission systems use AC [1]. However, the recent advancements made in power electronic converters along with controllers have made integrating renewable energy sources into a grid. Different control methods, and various topologies of converters, are researched to a great extent in [2]–[9]. In most of the papers cited below it is seen that research is being done extensively to connect three-phase grids using inverters with pulse width modulation and for a low to micro-grid, single-phase inverters with medium power are being preferred [10]–[14]. Microgrids connected to renewable can reduce the demand for power in residential area energy [15]. However, renewable energy sources tend to supply fluctuating power depending on time and several other factors; hence it is essential to optimize getting energy [16]. With solar panels and wind turbines, the sun and wind respectively depend on the energy that can be generated from them [17]. Therefore, the systems are in charge of them should be capable of adjusting themselves to these varying factors. Thus, the output voltage and current solar panel have to be adjusted for different temperatures, times of the day so that the energy generated from the panel is heavily optimized and the system has to be at the maximum power

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point [18]. DC-DC converters are, therefore, used to power the PV panel's variable output voltage [4]. Since there is a strong demand for applications with low and medium power [19]–[22], multilevel (MLIs) inverters are common because they can increase the output voltage without the use of transformers. The cascaded type of multilevel inverter is preferred in microgrids for RES as it is possible to connect individual H bridges. To individually even with other various sources of renewable energy, such for example solar panels, using wind turbines fuel cells that have been stacked and for power distribution purpose the step-up transformers are possible to be eliminated by including the use of DC-DC converters and connections of H bridge outputs through cascading [16]. This paper deals with the development of an inverter to be used for micro-grids powered by renewable energy. There is a constant demand for clean and sustainable energy all over the world as the existing fossil fuel resources are being depleted, and the condition of the environment we live in is getting worse each day. This calls for a major shift towards renewable energy for a better and stable future. As most of our existing systems are built around fossil fuel, it is not possible to just shift to other energy instantly; the process has to be slow. It associates the grid with a photovoltaic system, which could be seamlessly integrated into our existing system. Since the output produced from solar panels is in DC, and the grid distributes current as AC, inverters have to play a huge role in converting the DC to AC. Therefore, the inverter used has a direct influence on the overall performance of this integrated system. Prefer an inverter with low total harmonic distortion and high efficiency. Multilevel inverters are used as they have higher efficiency and (THD) lower total harmonic distortion when compared to the other inverters. However, the number of switches used in the circuit must decrease to minimize losses. As the switches play an essential role in the multilevel inverters, instead of trying to directly decrease the switches, have used here the PWM technique. There are three relevant kinds of multilevel inverters [23], H bridge, Neutral point clamped MLI, and flying capacitor MLI. Cascaded H Bridge MLI. Besides these are formed by connecting in sequence with the H bridge MLI with each other. The H bridge is called so, as the circuit when connected looks like "H". Comprising four switches, using the H bridge for both single and three-phase conversion [24]. Based on the required mechanical or solid-state switches may be used, although mechanical switches are rare nowadays. This system has the least number of switches but is mostly used when there are two or more sources. The H bridge rectifier has the least amount of Total harmonic distortion but is less preferred as the device makes use of two different power sources, which is what is present in almost all real-life scenarios. In flying capacitor multilevel inverter, the diodes are also replaced by capacitors [25]. They have a tree-like structure comprising capacitors, where each capacitor has a different voltage. For the flying capacitor, the number of switches required is given by doubling the level of the MLI and then subtracting two from the result, and for the capacitor, the number of levels

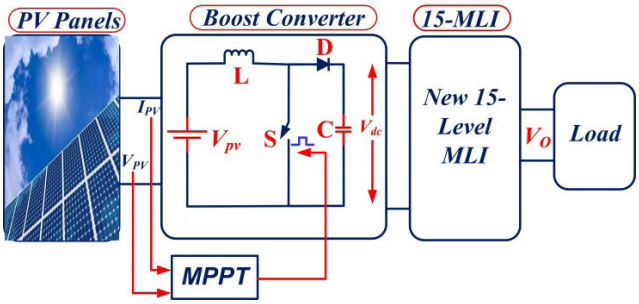

FIGURE 1. Proposed system configuration.

in MLI is doubled, and then one is subtracted from it. The real and reactive power flow is better controlled, during the outage the capacitors present makes way for the inverter to save itself; however, the circuit and design are much more complex, and switching efficiency is low, it is costlier than the other setups. Neutral point clamped inverters have a lot of numbers of switches when compared to H bridge but work ideally better with a single source. The THD levels and efficiency are quite better than H-bridge for a singular source. With the increase in the number of switches, the overall (THD)total harmonic distortion also increases, which is eliminated by bringing in a filter at the end of the circuit. In the Neutral point Clamped Multilevel inverter [26], diodes clipping devices, and use the capacitors as instruments for clamping. The number of switches varies depending on the stage of the converter; the switches are less concerning the levels, and dynamic loads have been tested experimentally and well suits for renewable energy applications [27]–[30]. A new 15-level inverter with a reduced number of components is proposed in this article. Section-II provides paper structure in the following manner; A boost converter with solar PV and MPPT. Section-III presents the proposed multilevel inverter, along with simulation and experimental results. Section-IV describes comparative studies of proposed MLI with existing MLIs. Last, Section V offers a conclusion.

II. CONFIGURATION OF PROPOSED SYSTEMS

Proposed Solar PV Arrays based converter boost converter is shows incorporated inverter in Fig.1. The photovoltaic cells are cascaded or parallel; it requires connected based on whether higher voltage or current. They can withstand the harshest environmental conditions and are built to last for a long time. This design of Solar PV cells is done by simulating the natural conditions of the environment which are then processed to get the Irradiance vs Time graph and the Temperature vs Time graph, both of which have been simulated for ten seconds. It can represent a solar cell as a current source connected to a diode parallel, where the output of the current source is directly proportional to the light that falls on the cell. Thus, the VI characteristics of the cell are characterized by the diode. It cannot use this model for simulating the real, as it lacks other external factors other than sunlight. However, these can be solved by adding complexity

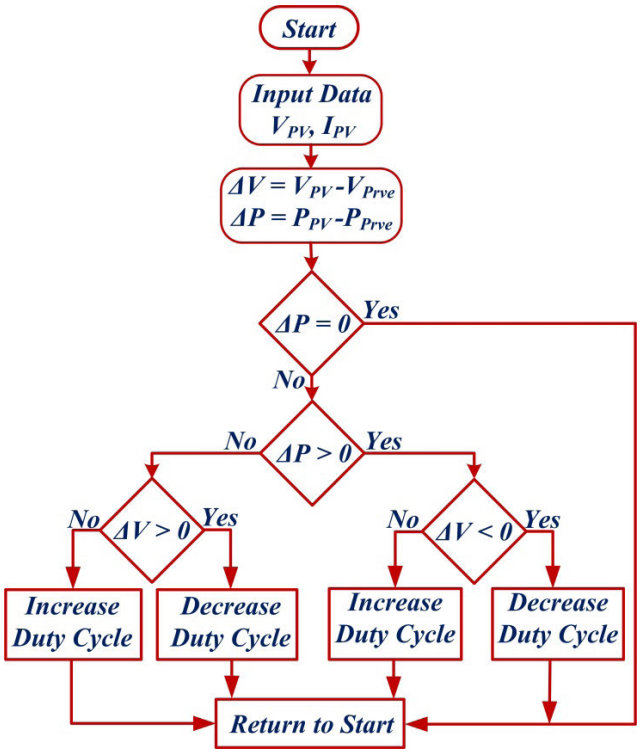

FIGURE 2. MPPT flow chart.

and increasing accuracy. After this, the diodes are connected parallel with two distinct sets of saturation current. Consider in this program temperature dependence of the diode and its saturation current connected with a series of resistance.

Its ability to achieve the best match in the curve determined the diode quality factor, unlike other power-producing facilities where the output can be easily be controlled by reducing the fuel. Renewable sources naturally fluctuate on their own, have several external factors that can cause havoc as we need a steady and regulated power supply—implemented hence algorithms to achieve the optimum output which can be regulated easily and sent to the grid directly. Here the algorithm used is perturbed and observe in the (MPPT)Maximum power point tracking. The maximum power point tracking (MPPT) which enables us to get the optimum range of output is a DC to DC power electronic boost converter and is placed in between the load and the solar cell array in the circuit is shown in Fig.2. This design makes sure that optimum output is produced even though there is variation in temperature, insulation, and load. Although several tracking algorithms have already been verified and used in countless other research, this model was chosen to concern Matlab and the extent of work to be covered in this research. It tracks various peak power points and also compares with genuine configurations of irradiation data and strategies that could be reached using real irradiation data. The Conventional DC to DC converter is important because the voltage produced from renewable sources is very low and very difficult to regulate. Therefore, these converters help the system reach the required level of voltage for sustained practical operations. The capacitor and

TABLE 1. System parameters.

Item	Parameters
VPV	115V
Vo	400V
fs	100kHz
Capacitor	3.2nF
Inductor	94.22Uh
Duty ratio	71.25%
IGBT	CM75DU-12, 600V, 75A
dSPACE RTI Controller	1104

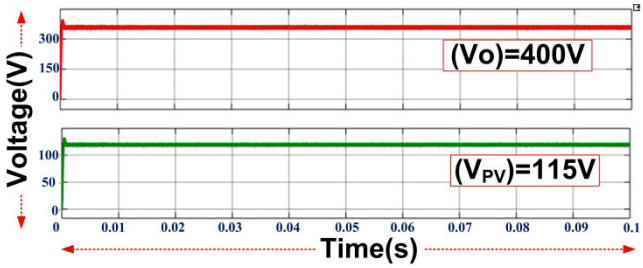

FIGURE 3. Simulation output waveforms of Converter & Solar PV.

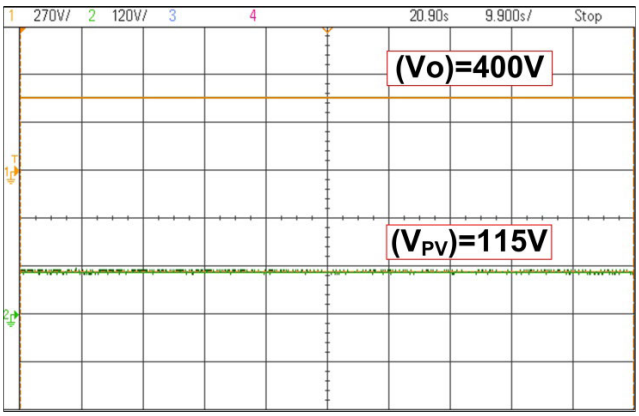

FIGURE 4. Experimental output waveforms of Converter & Solar PV.

inductor of values 3.2nF and 94.22uH are named as C and L, respectively. From the Maximum power point tracker system, it directs the gate pulses to the boost converter after adding additional delay. The voltage and current measurement for the diode is taken by setting up the voltmeter and ammeter. Boost converter up along with a snubber circuit, which contains a resistance of 100Ω, and set the capacitor value to its maximum and is being infinite. This to make the circuit resistive. The C capacitor produces a ripple-free boost voltage of 400V from 115V PV with a duty ratio D=0.7125 after an initial gap of 0.019 seconds. It shows the system parameters in Table 1.

$$V_O = \frac{V_{PV}}{(1 - D)} \tag{1}$$

The PV simulator 5kW & 8A takes the sources for the proposed system. Fig.3 to Fig.4 displays the converter and solar PV simulation and experimental effects. The boost converter can afford greater DC–linking voltage from solar PV. The got DC-link voltage can be fed to the proposed inverter for generating an AC stepped waveform.

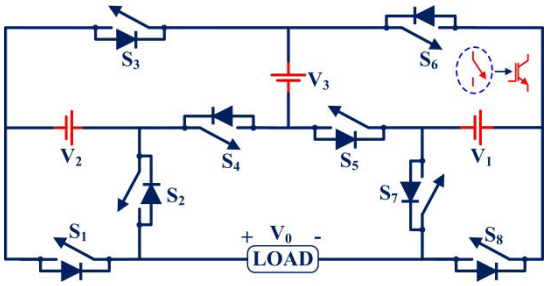

FIGURE 5. Proposed 15-Level topology.

TABLE 2. 15L-MLI switching states.

States	Switches (ON)
1	S2, S3, S5, S7
2	S2, S3, S5, S8
3	S1, S3, S7, S5
4	S1, S3, S5, S8
5	S2, S3, S6, S7
6	S2, S3, S6, S8
7	S1, S3, S6, S7
8	S2, S4, S5, S7
9	S2, S4, S5, S8
10	S1, S4, S5, S7
11	S1, S4, S5, S8
12	S2, S4, S6, S7
13	S2, S4, S6, S8
14	S1, S4, S6, S7
15	S1, S4, S6, S8

III. PROPOSED 15-LEVEL MLI

In Fig.5, a newly developed 15-level inverter is shown. The DC-link voltage of the solar PV based boost converter is fed as a source to the proposed inverter. The proposed inverter comprises eight uni-directional switches and three sources of DC. In the proposed 15-level asymmetrical MLI, the switches are selected based on the strategy of avoiding short circuits in the specified path of current traversal. The initial level is obtained by conducting the switches S2, S3, S5, and S7, forming a closed path precisely without a short circuit. In this mode of operation, the blocking voltage of switches is considered in calculating the total standing voltage. In the second mode of operation, the switches S2, S3, S5, and S8 are in conduction. These are selected for avoiding the short circuit, and even the addition of maximum blocking voltages of each semiconductor switch is lesser in value, which results in less TSV and cost-effectiveness. Similarly, the switch selection patterns up to 15-levels are represented in Table 1. Based on this lookup table, the switches are selected based on the above conditions in which the overall loop of conduction of switches provides an efficient operation of an inverter with less standing voltage across switches.

The inverter is proposed with asymmetrical DC input sources with a 1:2:5 ratio for generating 15-level output voltage levels, and source voltages are taken $V_{dc} = V_1 = 57.15V$, $V_2 = 114.3V$, and $V_3 = 285.75V$ respectively, shown the inverter switching states in Table. 2, and by using the staircase PWM technique, produce gate pulses. The output voltage is the number of $V_2 + V_3$ in mode-1, S_2, S_3, S_5, S_7 switches are ON, and the remaining switches are OFF.

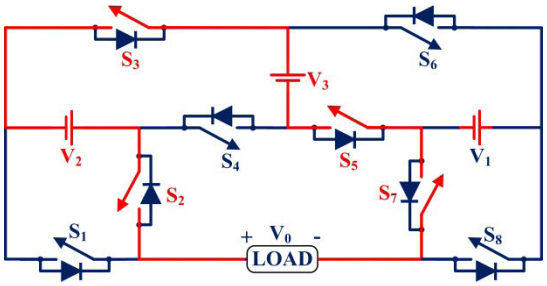

FIGURE 6. State-1 of 15MLI.

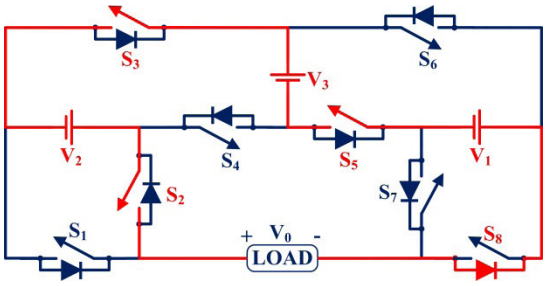

FIGURE 7. State-2 of 15MLI.

In mode-2, the output voltage is $-V_1 + V_2 + V_3$, the S_2, S_3, S_5, S_8 switches are ON, and the remaining switches are OFF. The S_1, S_3, S_7, S_5 switches are ON in mode-3, and the remaining switches are OFF, and the output voltage is the amount of V_3. The output voltage is the number of $-V_1+V_3$ in mode-4, the S_1, S_3, S_5, S_8 switches are ON, and the remaining switches are OFF. The output voltage is the amount of $V_1 + V_2$ in mode-5, the S_2, S_3, S_6, S_7 switches are ON, and the remaining switches are OFF. The output voltage is the amount of V_2 in mode-6, the S_2, S_3, S_6, S_8 switches are ON, and the remaining switches are OFF. The output voltage is the amount of V_1 in mode-7, the S_1, S_3, S_6, S_7 switches are ON, and the remaining switches are OFF. The S_2, S_4, S_5, S_7 switches will ON in mode-8, and the remaining switches are OFF the 0V output voltage. The S2, S_4, S_5, S_8 switches are ON in mode-9, and the remaining switches are OFF, the output voltage is $-V_1$. The S_1, S_4, S_5, S_7 switches are ON in mode-10, and the other switches are OFF, the output voltage is $-V2$. The S_1, S_4, S_5, S_8 switches are ON in mode-11, and the remaining switches are OFF, the output voltage is $-(V_1+V_2)$. In mode-12, the S2, S_4, S_6, S_7 switches will ON and the remaining switches will OFF, the output voltage is the $-(-V_1 + V_3)$. In mode-13, the S_2, S_4, S_6, S_8 switches will ON and the remaining switches will OFF, the output voltage is the $-V_3$. In mode-14, the S_1, S_4, S_6, S_7 switches will ON and the remaining switches will OFF, the output voltage is the $-(-V_1+V_2+V_3)$. In mode-15, the S1, S4, S6, S8 switches will ON and the remaining switches will OFF, the output voltage is the $-(V_2 + V_3)$. Shown the all operational modes as per the conduction of switches and expected waveform in Fig.6 to Fig.21.

A. CIRCUIT PARAMETERS DESIGN

Using the following generalized questions, the suggested inverter circuit parameters, such as the number of levels (N_L),

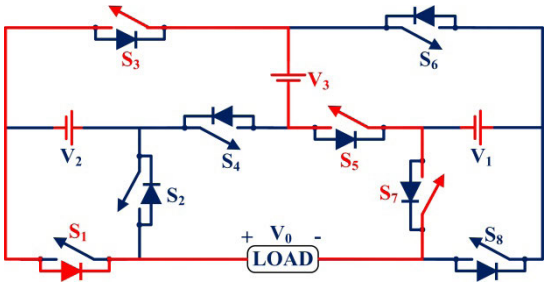

FIGURE 8. State-3 of 15MLI.

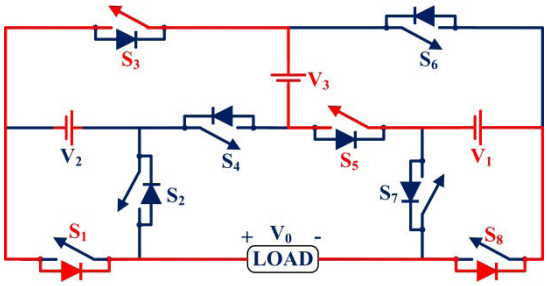

FIGURE 9. State-4 of 15MLI.

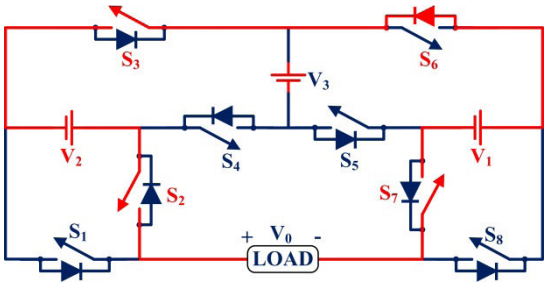

FIGURE 10. State-5 of 15MLI.

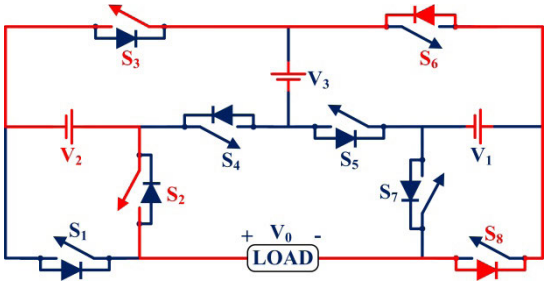

FIGURE 11. State-6 of 15MLI.

number of switches (N_{SW}), number of DC sources (N_{SDC}), and peak output voltage (V_{OP}), can be calculated.

$$N_{SDC} = n \tag{2}$$

$$N_{SW} = (2^{n_{k1}+1}) + (2^{n_{k2}+1}) + \ldots\ldots\ldots + (2^{n_{kj}+1}) \tag{3}$$

$$N_L = (2^{n_{k1}+1} - 1) + (2^{n_{k2}+1} - 1) \ldots + (2^{n_{kj}+1} - 1) \tag{4}$$

$$V_{OP} = \left(\frac{2^{n_{k1}+1} - 2}{2} + \frac{2^{n_{k2}+1} - 2}{2} + \ldots\ldots + \frac{2^{n_{kj}+1} - 2}{2} \right) \times Vdc \tag{5}$$

where n and k for the proposed inverter are the numbers of sources and modules, respectively. The parameters are got by using equations (2), (3), (4), and (5) by taking $n=3$ and

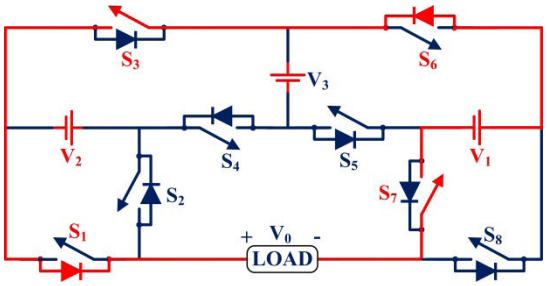

FIGURE 12. State-7 of 15MLI.

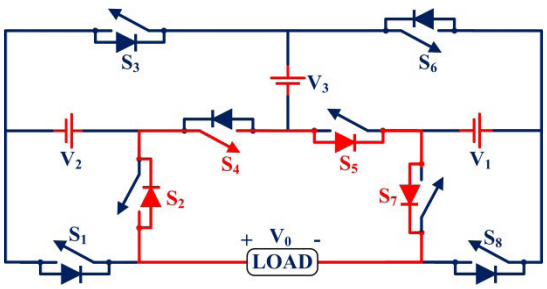

FIGURE 13. State-8 of 15MLI.

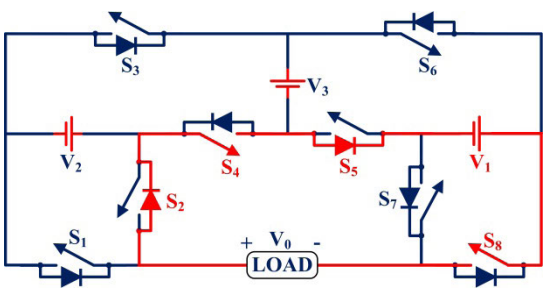

FIGURE 14. State-9 of 15MLI.

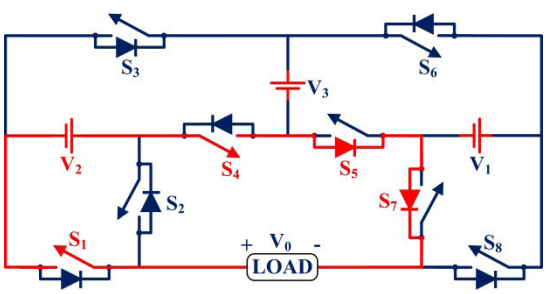

FIGURE 15. State-10 of 15MLI.

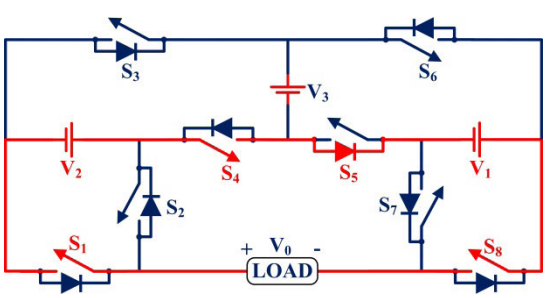

FIGURE 16. State-11 of 15MLI.

$k=1$ and $V_{dc} = V_1 = 57.15V$, respectively. The $N_{SDC} = 3$, $N_{SW} = (2^{3+1}) = 8$, $N_L = (2^{3+1} - 1) = 15$, and

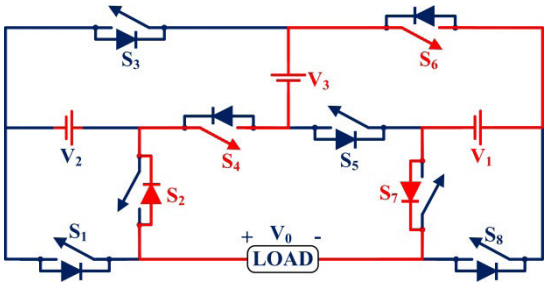

FIGURE 17. State-12 of 15MLI.

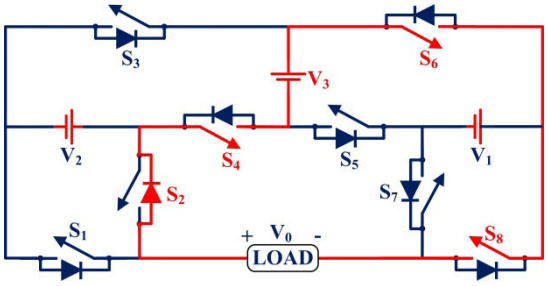

FIGURE 18. State-13 of 15MLI.

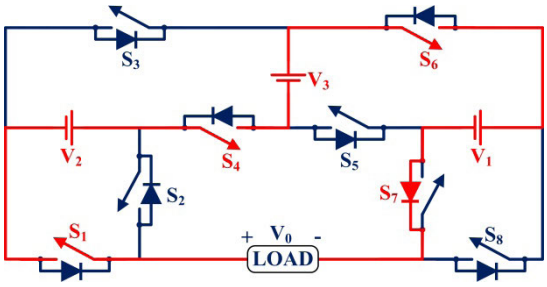

FIGURE 19. State-14 of 15MLI.

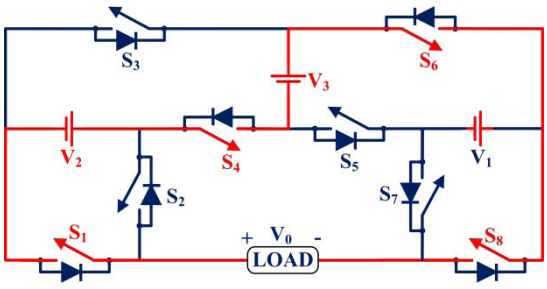

FIGURE 20. State-15 of 15MLI.

$V_{OP} = \left(\frac{2^{3+1}-2}{2}\right) * 57.15 = 400.05V$. Implemented the proposed inverter with two basic modules (k=2) for generating a 29-output voltage level.

B. RESULTS ANALYSIS

The proposed inverter was simulated with MATLAB/Simulink and experimentally verified with the dSPACE RTI11014 Controller, as shown in Fig.34. It shows the simulation output waveforms and THD in Fig.22 to Fig.27. The PV simulator 5kW & 8A as the sources and the high power CM75DU-12H IGBTs are used for the experimental with the range of 600V & 75A, respectively. The dSPACE controller is used to

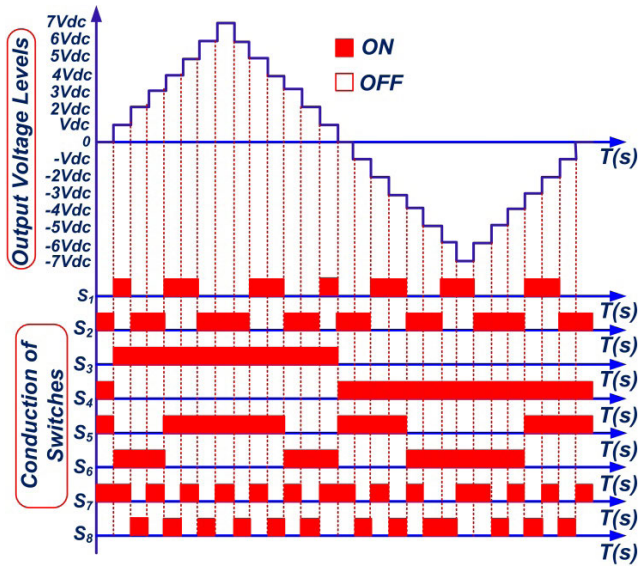

FIGURE 21. The expected waveform of 15MLI.

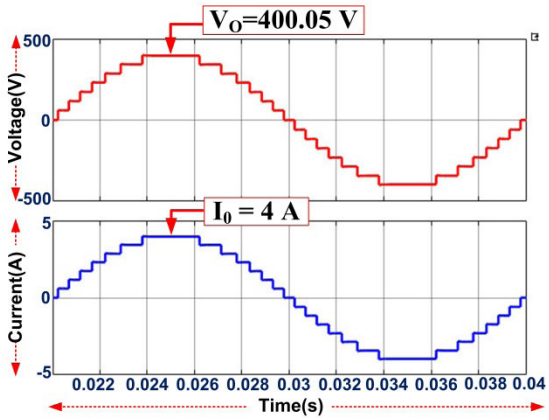

FIGURE 22. The output waveform of 15MLI with one cycle.

produce gate pulses with the TLP250 driver technique of the staircase PWM. For the simulation and experimental, the 100ohm, 175mh, and 0.5HP single-phase with 230V, 373W, and power factor 0.75 respectively were used as loads for the proposed inverter. Source voltages are taken $V_{dc} = V_1 = 57.15V$, $V_2 = 114.3V$, and $V_3 = 285.75V$ to attain maximum peak output voltage Vo=400.05V. The proposed 15-level inverter is tested with linear and non-linear loads for the robustness of the inverter.

The got experimental output power, output voltage and current are Po=782.55W, Vo=400.05V, Io=4A, Vrms=277.5V, & Irms=2.82A correspondingly for the proposed inverter with linear loads, as shown in Fig.28 & Fig.29. It confirms the inverter with motor load(non-linear) to verify the performance and effectiveness with output voltage & current (Vo=400.05V, Io=6.5A) is shown in Fig.30. In the dynamic load, changes are tested and executed with linear to non-linear and vice versa. The proposed inverter produces a stable output during dynamic load changes, and it attained the maximum system peak output voltage at 400V is shown

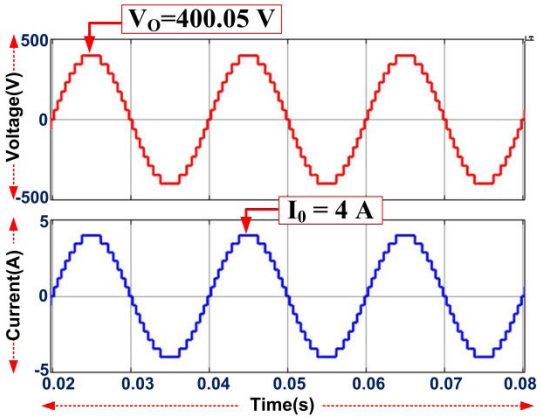

FIGURE 23. The output waveform of 15MLI with two cycles.

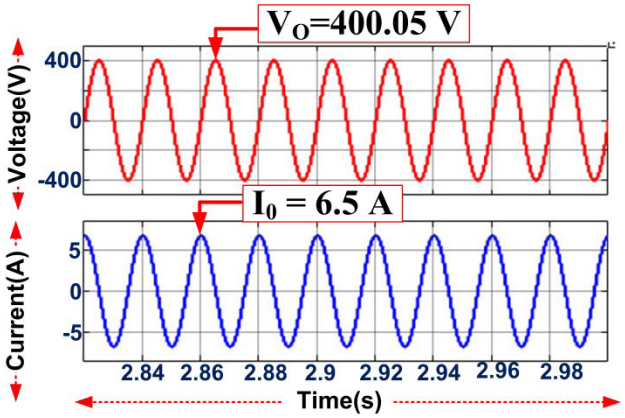

FIGURE 24. The output waveform of 15MLI with L load.

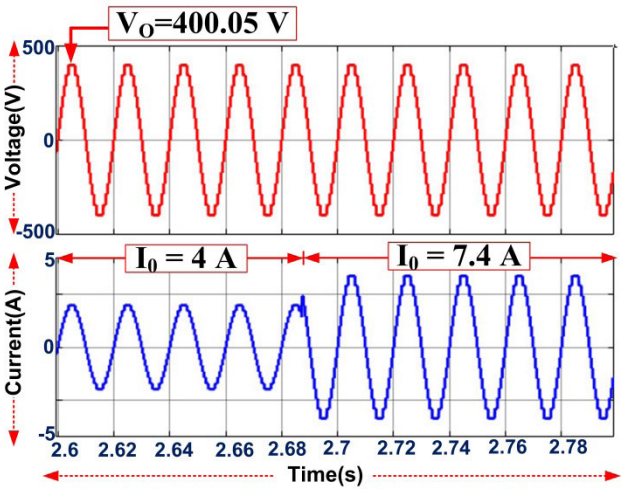

FIGURE 25. The output waveform of 15MLI with R to L load.

in Fig.31 to Fig.32. Fig.33 shows that experimental THD is obtained 4.41% as per IEEE standards and with an efficiency of 95.237%. The proposed inverter can be connected to the grid and FACTS for power quality improvement.

C. LOSS AND EFFICIENCY SETTING

The conduction (P_{CON}) and switching (P_{SWI}) losses are related to the power semiconductor switches in the proposed

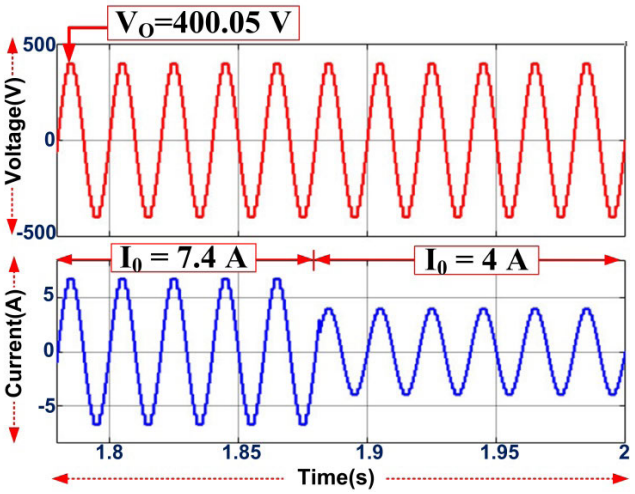

FIGURE 26. The output waveform of 15MLI with L to R load.

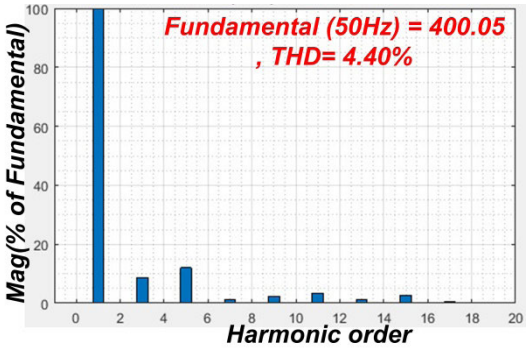

FIGURE 27. 15MLI THD Simulation of 15MLI.

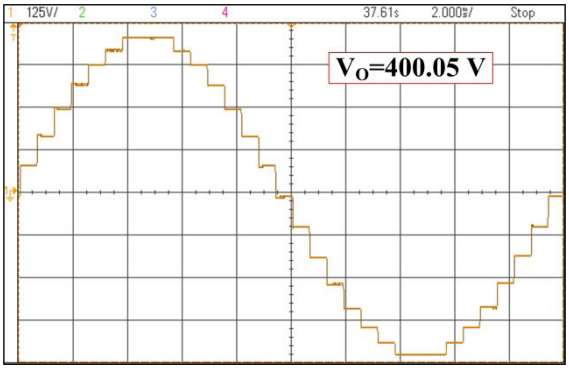

FIGURE 28. 15MLI experimental output waveform.

inverter [28]–[30]. The P_{CON} losses will occur because of current flow into the switch (P_{CON_SW}) and anti-parallel diode (P_{CON_DI}) during the conduction state [28]–[30]. The losses (P_{CON_S} & P_{CON_D}) are estimated as follows [28]–[30];

$$P_{CON_S} = (V_{SW}+R_{SW}i^{\alpha}(t))i(t) \quad (6)$$

$$P_{CON_{DI}} = V_{DI}+R_{DI}i^2(t) \quad (7)$$

Let V_{SW}, R_{SW}, V_{DI}, and R_{DI} are the voltage and resistance of the diode and switch respectively, and α is a constant value of the switch [28]–[30]. Let assume N_{SW}, ON & N_{DI}, ON switch and diodes are in conduction state at the time t

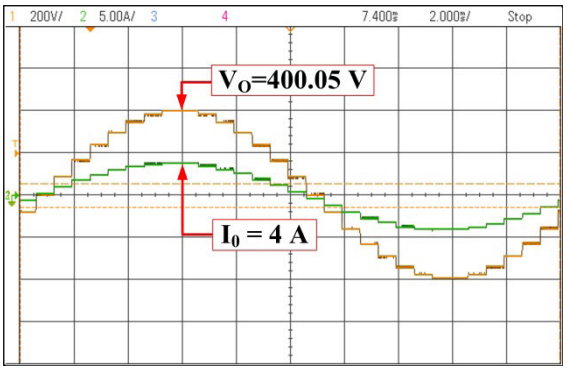

FIGURE 29. 15MLI experimental waveforms with linear load.

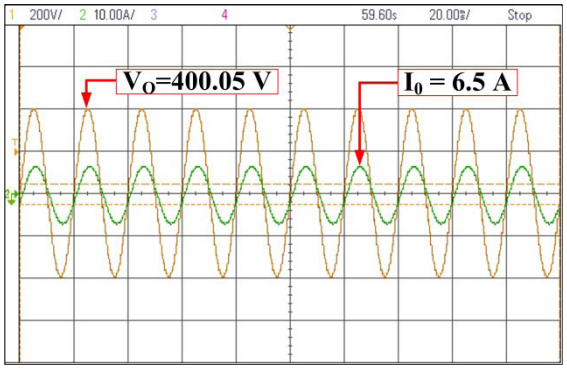

FIGURE 30. 15MLI experimental waveforms with non-linear load (Motor load).

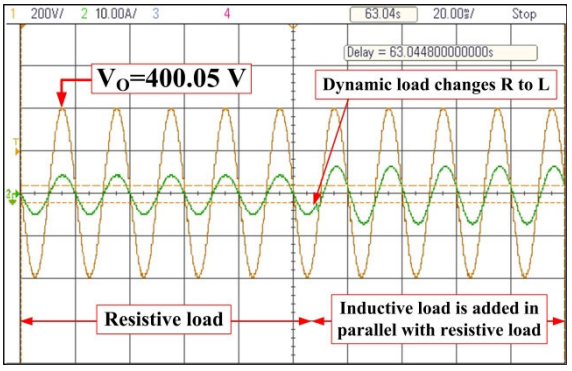

FIGURE 31. 15MLI experimental waveforms with linear to a non-linear load.

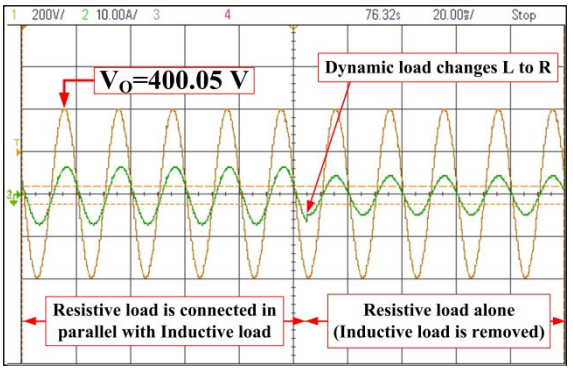

FIGURE 32. 15MLI experimental waveforms with non-linear to a linear load.

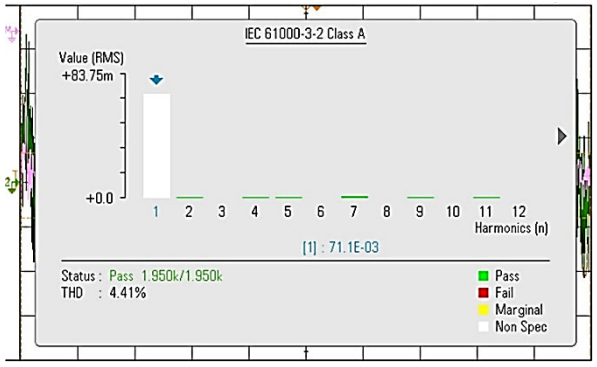

FIGURE 33. Experimental THD of 15MLI.

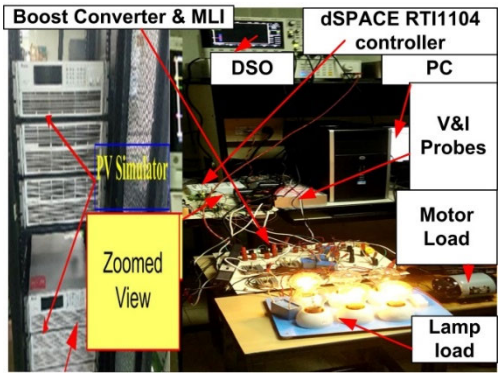

FIGURE 34. Prototype model of 15MLI.

interval [28]–[30]. The P_{CON} average losses can be as follows;

$$P_{CON} = \frac{1}{2\pi}\int_0^{2\pi} [N_{SW}(t)P_{CON,SW}(t)dt] \tag{8}$$

The energy losses (Eny_{off}&Eny_{on}) of the switch (j) are calculated during turn-ON & turn-OFF intervals.

$$Eny_{off,j} = \int_o^{t_{off}} v\,(t)\,i\,(t) = \frac{1}{6}V_{SW,j}I't_{off} \tag{9}$$

$$Eny_{on,j} = \int_o^{t_{on}} v\,(t)\,i\,(t) = \frac{1}{6}V_{SW,j}I't_{on} \tag{10}$$

The switching (P_{SWL}) losses are the sum of energy losses ($Eny_{off,j}$&$Eny_{on,j}$) in the fundamental cycle(j) of the inverter with frequency (f) [28]–[30].

$$P_{SWL} = f\sum_{j=1}^{N_{sw}}\left[\sum_{k=1}^{N_{on,j}} Eny_{on,jk} + \sum_{k=1}^{N_{off,j}} Eny_{off,jk}\right] \tag{11}$$

The total inverter losses(P_{Loss}) is obtained as follows

$$P_{Loss} = P_{CON} + P_{SWL} \tag{12}$$

The inverter efficiency is determined as follows;

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{Loss}} \tag{13}$$

The P_{IN} & P_{OUT} are the input and output powers are obtained from the proposed inverter. By using the above

questions, the losses and efficiency can be obtained. The proposed inverter experimental output power obtained is $P_{OUT} = 782.55W$ with the $V_{rms} = 277.5V$ & $I_{rms} = 2.82A$ respectively. The IGBT CM75DU-12 power switches with $V_{SWI} = 0.6V$, $R_{SWI} = 0.4V$, 100ns, and 250ns turn-on delay and rise time [28]. The turn-off delay and fall time with 200ns and 300ns for eight switches with 29 steps for the completed cycle is considered from the characteristics plot from the IGBT switch data sheet [28]. The $P_{CON} = [0.6 + 0.4\,(2.82)] * 2.82 * 8 = 38.98W$, $Eny_{ON} = 277.5 * 2.82 * [350 * 10^{-9}] * 29 * 8 = 0.0635W$, $Eny_{OFF} = 277.5 * 2.82 * [500 * 10^{-9}] * 29 * 8 = 0.0907W$, $P_{SLW} = Eny_{ON} + Eny_{OFF} = 0.0635 + 0.0907 = 0.1542W$, $P_{Loss} = P_{CON} + P_{SWL} = 38.98 + 0.1542 = 39.1342W$, and $\%\eta = \frac{P_{OUT}}{P_{OUT}+P_{Loss}} = \frac{782.55}{782.55+39.1342} = 95.237\%$ are obtained using equations (8) to 13 respectively [28]. In the proposed 15-level MLI, the crucial power losses are conduction losses and switching losses. Conduction losses of IGBT are because of the on-state value of resistance and voltages of all switches. The internal resistance of the IGBT under simulation and experimental cases are 0.01Ω and 0.4Ω, respectively. Hence for the R-load, the conduction losses P_{con} in simulation can be calculated from equation (6), i.e., $P_{con} = [0.6 + 0.01(2.82)] \times 2.82 \times 8 = 39.96W$, whereas experimentally. $P_{con} = [0.6 + 0.4(2.82)] \times 2.82 \times 8 = 38.98W$. Switching losses, P_{sw} is calculated from equation (11) and found to be 0.1572 in both simulation and experimentally. The total losses are 40.1172W in simulation and 39.1372 in experimental. Efficiency is 95.21% in simulation and 95.32% in experimental. For the L-load, the conduction losses P_{con} in simulation can be calculated from equation (6), i.e., $P_{con} = [0.6 + 0.01(4.596)] \times 4.596 \times 8 = 23.75W$, whereas experimentally, $P_{con} = [0.6 + 0.4(4.596)] \times 4.596 \times 8 = 89.655W$. Switching losses, P_{sw} is calculated from equation (11) and found to be 0.2562 in both simulation and experimental cases. The total losses are 24W in simulation and 89.911 in experimental. Efficiency is 98.18% in simulation and 93.5% in experimental. For the RL-load, the conduction losses P_{con} in simulation can be calculated from equation (6) i.e., $P_{con} = [0.6 + 0.01(7.4)] \times 7.4 \times 8 = 39.9W$, whereas experimentally $P_{con} = [0.6 + 0.4(7.4)] \times 7.4 \times 8 = 210.752W$. Switching losses, P_{sw} is calculated from equation (11) and found to be 0.4126 in both simulation and experimental cases. The total losses are 40.31W in simulation and 211.16 in experimental. Efficiency is 98.11% in simulation and 90.83% in experimental. The losses and efficiency are shown in Table. 3 and graphically Fig. 35 to Fig.37.

The proposed inverter significantly boosts the efficiency of 95.237% and reduces the losses with fewer components. The modulation index is shown in Table 4 and Fig.38.

D. TOTAL STANDING VOLTAGE (TSV)

The total standing voltage (TSV) plays a significant role in the selection of switches in the circuit. It is the sum of all blocking voltages for the total number of semiconductor devices in the topology. The voltage stresses on the bi-directional and uni-directional switches are given $V_{Sbi} = V_i$ and $V_{Suni} = 2V_i$, respectively, where i=1, 2 . . . . . n, and n are complimentary switches count [41]. In the proposed MLI, the voltages are equal for complimentary switches, and all switches are uni-directional. Hence TSV is calculated using the following relation:

$$TSV = 2(V_{S1} + V_{S3} + \ldots\ldots\ldots\ldots V_{S(2n+1)})$$
$$TSV = 2(V_{S1} + V_{S3} + V_{S5} + V_{S7})$$
$$= 2(2V_{dc} + 7V_{dc} + 5V_{dc} + V_{dc}) = 30V_{dc} \quad (14)$$

For the developed 15-level MLI, TSV can be calculated based on the equation (14) and found to be $30V_{dc}$.

TABLE 3. Power and efficiency of proposed 15-level MLI.

Parameters	R load		L load		RL load	
	Simulation	Experimental	Simulation	Experimental	Simulation	Experimental
Vrms (V)	282.84	282.84	282.84	282.84	282.84	282.84
Irms (A)	2.82	2.82	4.59	4.59	5.23	5.23
P_{Con} (W)	39.96	38.98	23.75	89.655	39.9	210.752
P_{SW} (W)	0.1572	0.1572	0.2562	0.2562	0.4126	0.4126
Total losses (W)	40.1172	39.1372	24	89.911	40.31	211.16
Output power (W)	797.6	797.6	1299.93	1299.93	2093	2093
Efficiency(%)	95.21	95.32	98.18	93.5	98.11	90.83

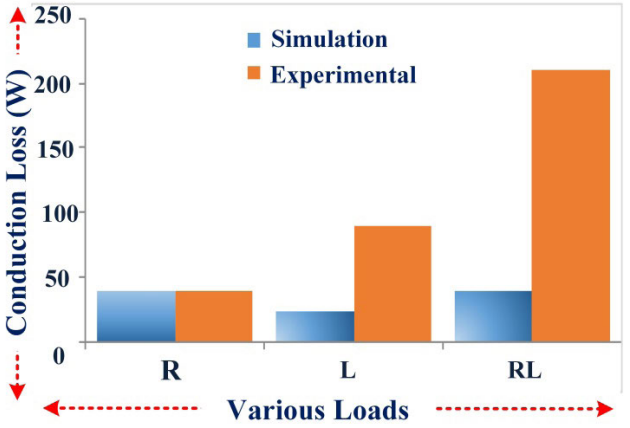

FIGURE 35. Conduction losses of 15MLI.

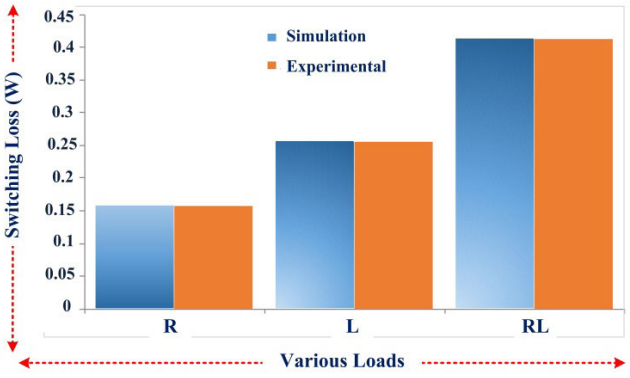

FIGURE 36. Switching losses of 15MLI.

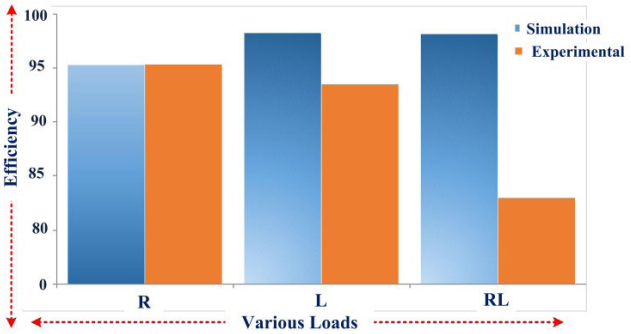

FIGURE 37. Efficiency losses of 15MLI.

TABLE 4. Levels vs Modulation index.

MI (Modulation Index)	L (Number of Levels)
0.14	3
0.29	5
0.43	7
0.57	9
0.71	11
0.86	13
1.00	15

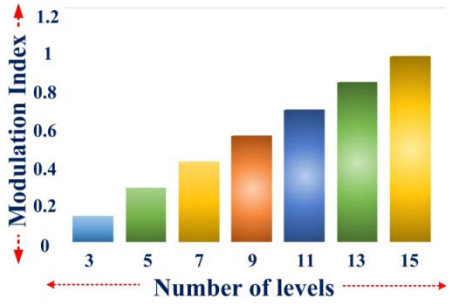

FIGURE 38. Levels vs MI of 15MLI.

E. COST FUNCTION

The cost factor for the proposed 15-level MLI can be calculated using the parameters like several switch counts, source count, total standing voltage, driver circuits count and using the formula shown in equation (15)

$$CF = (N_S + N_{dk} + N_d + N_c + \alpha TSV_{pu}) \times n \quad (15)$$

where CF is the cost factor, N_S is the number of switches, Dk is the gate driver circuit count, N_d is the diodes count, N_c is the number of capacitors. TSV is the maximum standing voltage for the switches in conduction. TSV_{pu} is the total standing voltage per unit, which is given by

$$TSV(pu) = V_{TSV}/V_{omax} \quad (16)$$

where n is the DC sources count in the circuit. α is the weight coefficient which is multiplied with TSVpu. For the proposed asymmetrical 15-level topology, as the diodes and capacitors are not used; hence these can be neglected, and the cost function is calculated using the relation.

$$CF = (S + N_{dk} + \alpha TSV_{pu}) \times n \quad (17)$$

The value of α is to be considered in such a way that one value is greater than one, and the other is less than one.

TABLE 5. Parameters comparison with Same Existing MLIs [27], [30]–[40].

MLIs	N_L	N_{SDC}	N_{SW}	N_D	N_C	TSV/L	THD %	Eff %	C.F/Nlev	
									α=0.5	α=1.5
[31]	15	3	8	-	-	-	5.66	94.1	-	-
[32]	15	7	16	-	-	-	-	-	-	-
[33]	15	1	14	2	4	-	5.77	96.72	-	-
[34]	15	5	10	2	-	-	5.54	90	-	-
[35]	15	3	10	-	-	-	-	-	-	-
[36]	15	3	12	-	-	-	5	-	-	-
[37]	15	3	7	3	-	-	4.74	-	-	-
[30]	15	7	16	-	-	-	5.02	93.8	-	-
[38]	15	5	10	2	-	1.06	3.96	90	1.74	1.89
[39]	15	5	10	-	-	-	7.97	93.7	-	-
[27]	15	3	9	-	-	2.06	5.66	94.1	1.54	1.84
[40]	15	4	10	-	-	4.6	5.50	-	1.89	2.47
Proposed MLI	15	3	8	-	-	2	4.41	95.2	1.4	1.68

In this paper, the value of α is realized as 0.5 (<1), and the other value is 1.5 (>1) for the evaluation of the cost function. The cost-effectiveness of any MLI is calculated with level count (CF/L). This value is to be calculated for both values of α shown in Table 5. The cost function for the various developed MLI is calculated based on the equation (15). For the developed 15-level MLI, the cost function per level count is found to be 1.4 (<1) and 1.68 (>1).

IV. COMPARATIVE ANALYSIS

In a real-world scenario, cost and other factors such as several components (N_L, N_{SDC}, N_{SW}, N_D, N_C, TSV/L, THD, Eff & C.F/Nlev) and reliability of these components are also essential. In comparison with other existing topologies [30], [31], [31]–[40] is shown in Table 5 & Fig.39. It is found out that the number of circuit components is more compared to the proposed MLIs, but because of their better-suited for use regarding the number of sources and lack of difference in terms of harmonic distortion on the lower scale; it is much preferable to use them. In [33], efficiency is high because the inverter was proposed for low-power applications. But circuit components more compared suggested inverter will increase the cost, power losses, and circuit bulkiness. Similarly, in [37] the switches are less but additionally having three switched diodes leads to higher losses, and also THD is high compared to proposed MLI. For demonstrating this 15-level multilevel inverter was also designed, and the results between both were analyzed, the difference in circuit component THD was relatively less than when compared to existing MLIs.

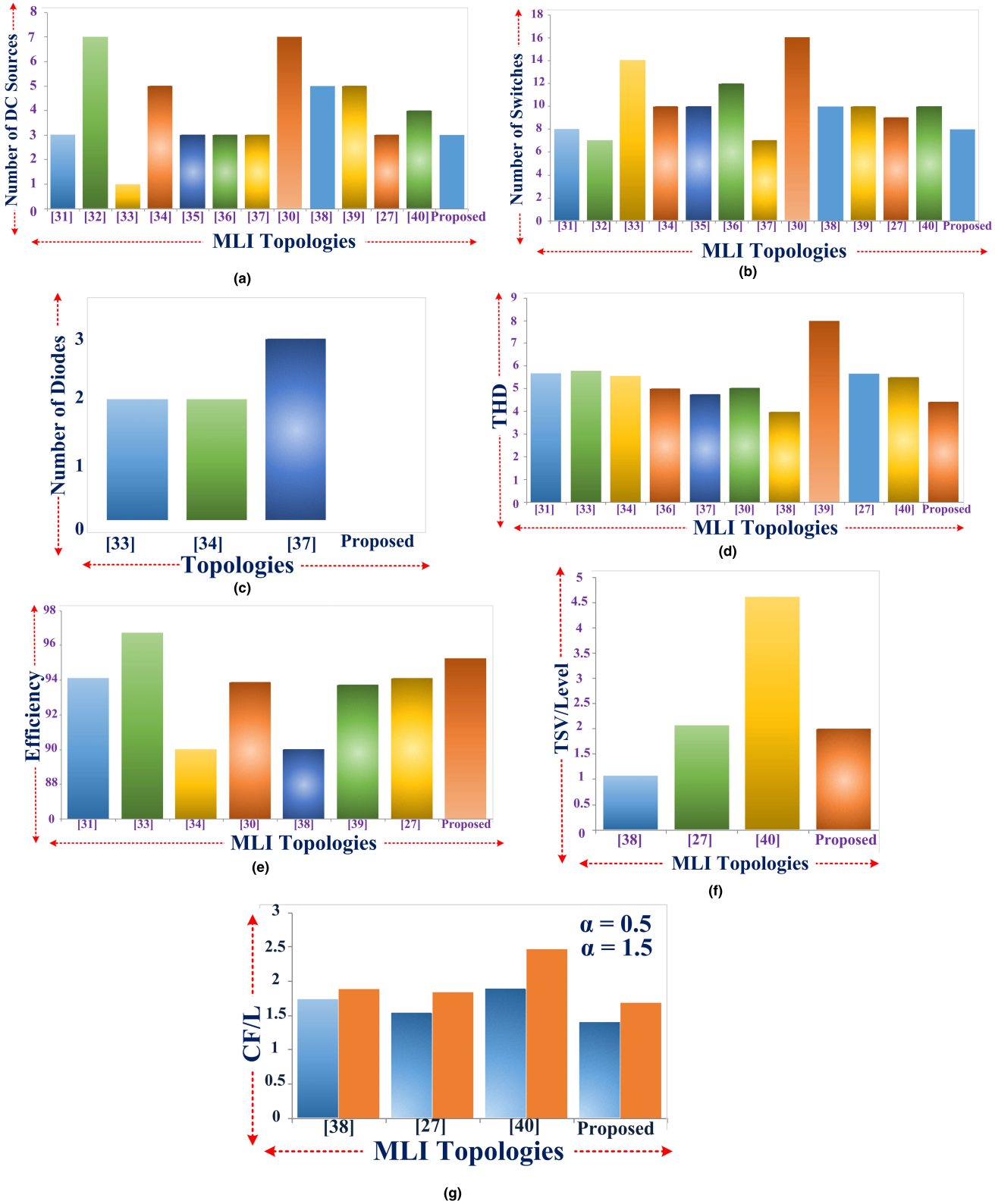

FIGURE 39. Components comparison with Recent MLIs. (a) N_{SDC}, (b) N_{SW}, (c) N_D, (d) THD, (e) Eff, (f) TSV, (g) C.F/Levels.

The efficiency(Eff) of 95.237% was observed to be almost lesser compared to existing MLIs. The proposed inverter several merits, such as the reduction in the losses and reduced circuit components reduced the cost and complexity, and gave a high efficiency of the inverter.

In the proposed 15-level asymmetrical MLI, there are eight switches accordingly gate drive circuits, and three sources with the absence of inductors and capacitors. The blocking voltage across each switch is calculated, and the total standing voltage per level count is calculated and found to be 2, which

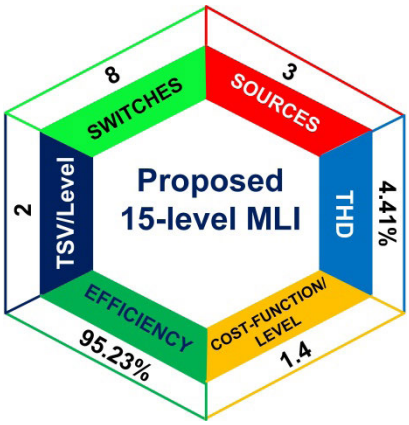

FIGURE 40. Outstanding features of the proposed 15MLI.

is significantly less compared with the various topologies. The total harmonic distortion is found to be 4.41 % which is under the IEEE standards and even found less compared with different topologies of 15-level MLI. The losses exerted in the proposed MLI are less with high efficiency and are compared. The cost function analysis is carried out and the cost function per level count is tabulated and found to be significantly less compared with the various topologies shown in Table 5. The overall structure of the proposed MLI stands best in its design based on the different parametric considerations and is tested with multiple dynamic load disturbances.

In the proposed 15-level asymmetrical MLI, there are eight switches accordingly gate drive circuits, and three sources with the absence of inductors and capacitors. The blocking voltage across each switch is calculated, and the total standing voltage per level count is calculated and found to be 2, which is significantly less compared with the various topologies. The total harmonic distortion is found to be 4.41 % which is under the IEEE standards and even found less compared with different topologies of 15-level MLI. The losses exerted in the proposed MLI are less with high efficiency and are compared. The cost function analysis is carried out and the cost function per level count is tabulated and found to be significantly less compared with the various topologies shown in Table 5. The overall structure of the proposed MLI stands best in its design based on the different parametric considerations and is tested with multiple dynamic load disturbances.

The outstanding features of the proposed 15-level asymmetrical MLI are shown in Fig.40 The unique inverter features are the reduced switch count; there are eight switches accordingly gate drive circuits and three sources with the absence of inductors and capacitors. The blocking voltage across each switch is calculated, and the total standing voltage per level count is calculated and found to be significantly less compared with the various topologies. The total harmonic distortion is under the IEEE standards and even found less compared with different topologies of 15-level MLI. The losses exerted are less with high efficiency. The cost function analysis is carried out, and the cost function per level count is tabulated and found to be significantly less, which prefers the inverter design. The overall structure of the proposed MLI stands best in its design based on the various parameters. The proposed inverter is integrated with a boost converter to enhance high DC-link Voltage for Solar PV applications.

V. CONCLUSION

A new 15-level inverter has been designed with a reduced number of components for solar PV applications was proposed in this work. The conventional boost converter produces a higher DC-link voltage and is fed to the inverter for AC stepped output waveform. The proposed inverter generates higher output voltage levels with a lesser number of circuit components with low THD. The proposed inverter has eight insulated-gate bipolar transistors triggered by using the staircase pulse-width modulation technique, and three DC voltage source was provided with reduced losses, high efficiency, and total harmonic distortion is found to be relatively low compared to existing inverters. Reduced stress and complexity of the inverter compared to existing multilevel inverters. Experimentally tested the inverter with linear, and non-linear loads and well stable during dynamic circumstances and suits for grid-connected and FACTS.

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