A High-Fidelity PHIL-based Platform for Real-Time Simulation and Testing of Power and Energy Systems

Integrated Energy System – IES Lab

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Abstract

Future power and energy systems with increasing integration of emergent technologies, converter-interfaced distributed generation and energy storage units as well as responsive loads, require suitable testbed setups to evaluate their performance, reliability, and stability. Power Hardware-in-the-Loop (PHIL) systems have been considered a testbed which offers a reasonable tradeoff between test fidelity and coverage.

HIL x PHIL

Differently of the Hardware-in-the-Loop (HIL), PHIL deals with real power exchange between the Digital Real Time Simulator (DRTS) and Equipment under Test (EUT) by using a Power Amplifier (PA) normally implemented by a power converter as shown in Fig. 1.

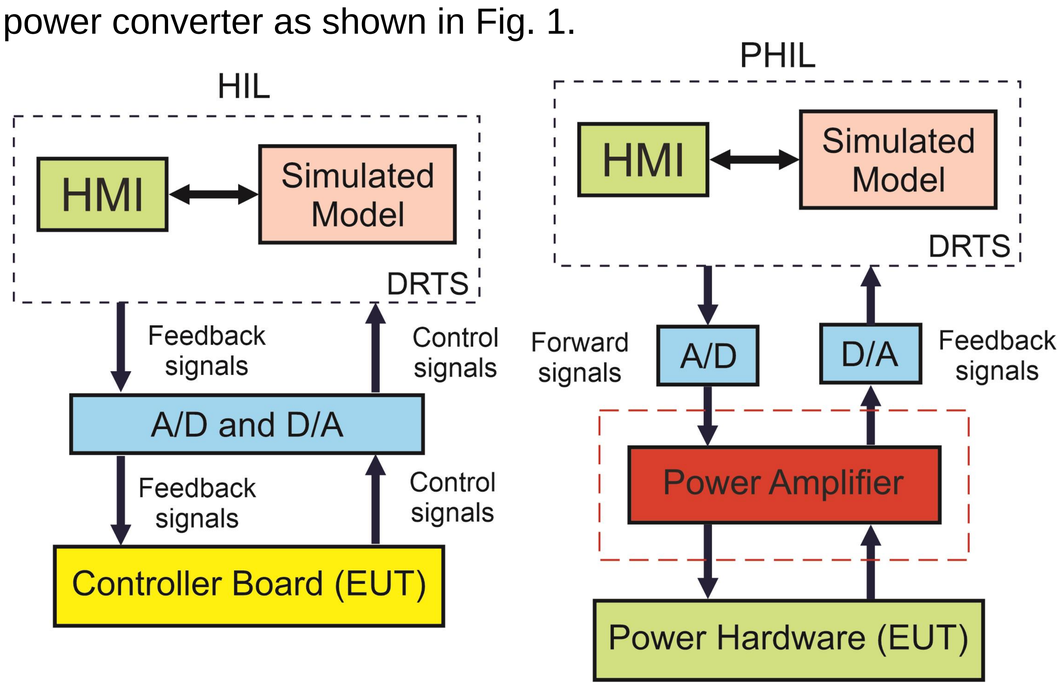

Fig. 1 Main differences between HIL and PHIL

System Description

The IES-Lab's high-fidelity PHIL-based Platform includes the following main components:

- DRTS, OPAL-RT - OP5600.
- Power Grid Emulator and Power Amplifier – CINERGIA.
- EUT.
- Control Fast Prototype System – dSPACE Microlab 1202.
- AC/DC Controlled Load – CINERGIA.

Fig. 2 presents the simplified block diagram of the proposed PHIL.

Main Features

The main features of the PHIL testbed are:

- Flexible DRTS for covering device-level studies (e.g., power converters) to system-level evaluations (e.g., full-scale energy systems)
- Co-simulation of multiple power/energy networks through web interconnection.
- Emulation of several operation scenarios such as faults, asymmetries, harmonic conditions, and frequency variation.
- Interface EUT – DRTS implemented using digital twin systems.
- Interconnection of different load types and energy storage systems (ESS) with different technologies and dynamic behaviors.

Experimental Results

The effectiveness and practicality of the high-fidelity PHIL-based platform was evaluated by using the interconnection of a Grid-Forming Power Converter (GFPC), operating as EUT, with the simulated network in the DRTS. The experiment comprises the following operational scenarios: (A) GFPC self-synchronization (Figs. 3(a)-(b)), (B) power delivering (Fig. 3 (c)-(d)), and (C) steady-state operation (Figs. 3(e)-(f)).

The self-synchronization strategy is implemented by PLL-PO[1] soft-transition approach. Figs. 3 (a)-(b) presents the GFPC output voltages and voltage vector angle during the self-synchronization procedure.

Fig. 3(c)-(d) shows the active and reactive power observed in the EUT and DRTS, respectively. Fig. 3(e)-(f) presents output voltages of the EUT also observed in the DRTS. These experimental results demonstrate the fidelity of the results, which validate the proposed twin system.

[1] Phase Locked Loop (PLL), Power Oscillator (PO)

Digital Real Time Simulator (DRTS)

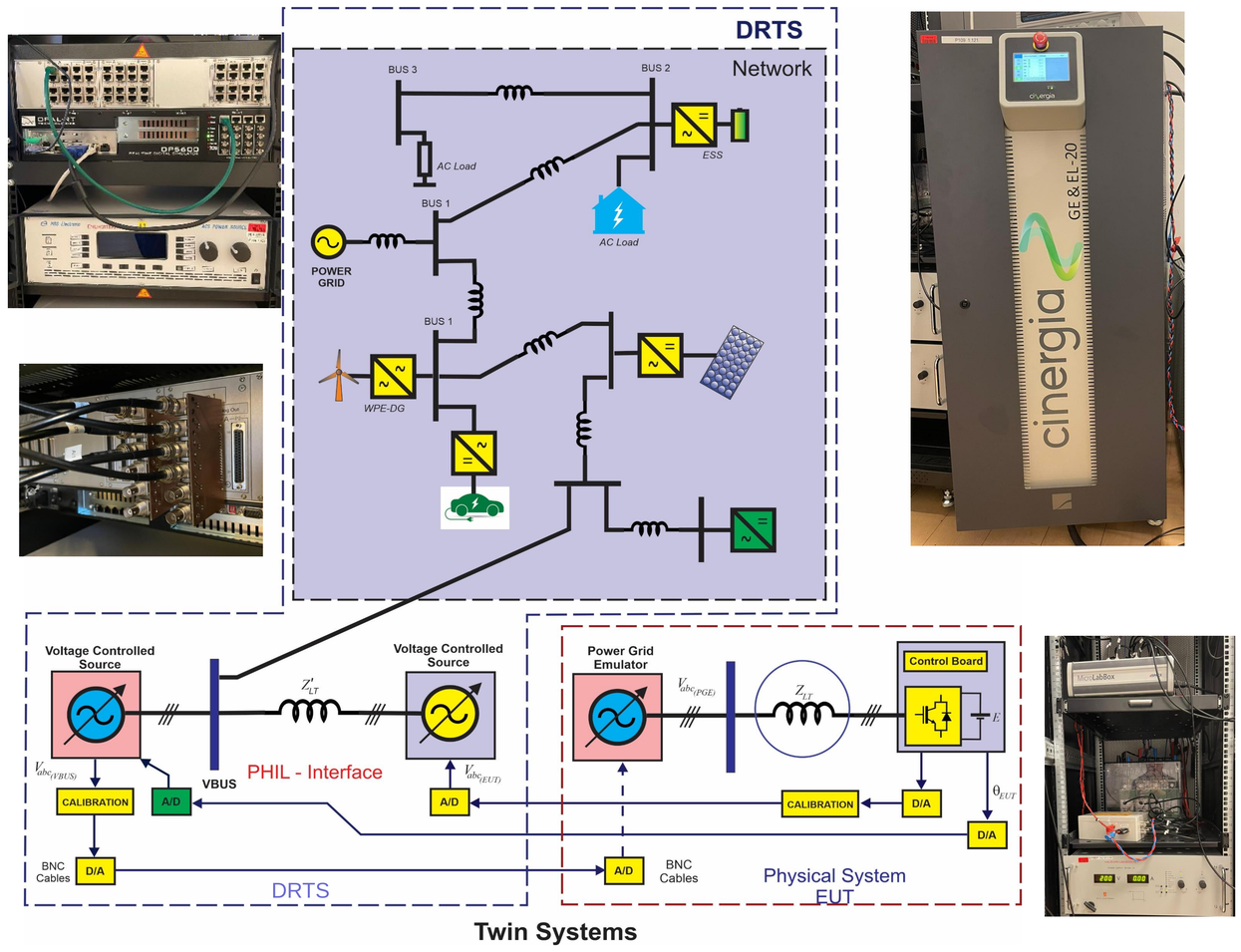

Fig. 2 Block diagram of the PHIL

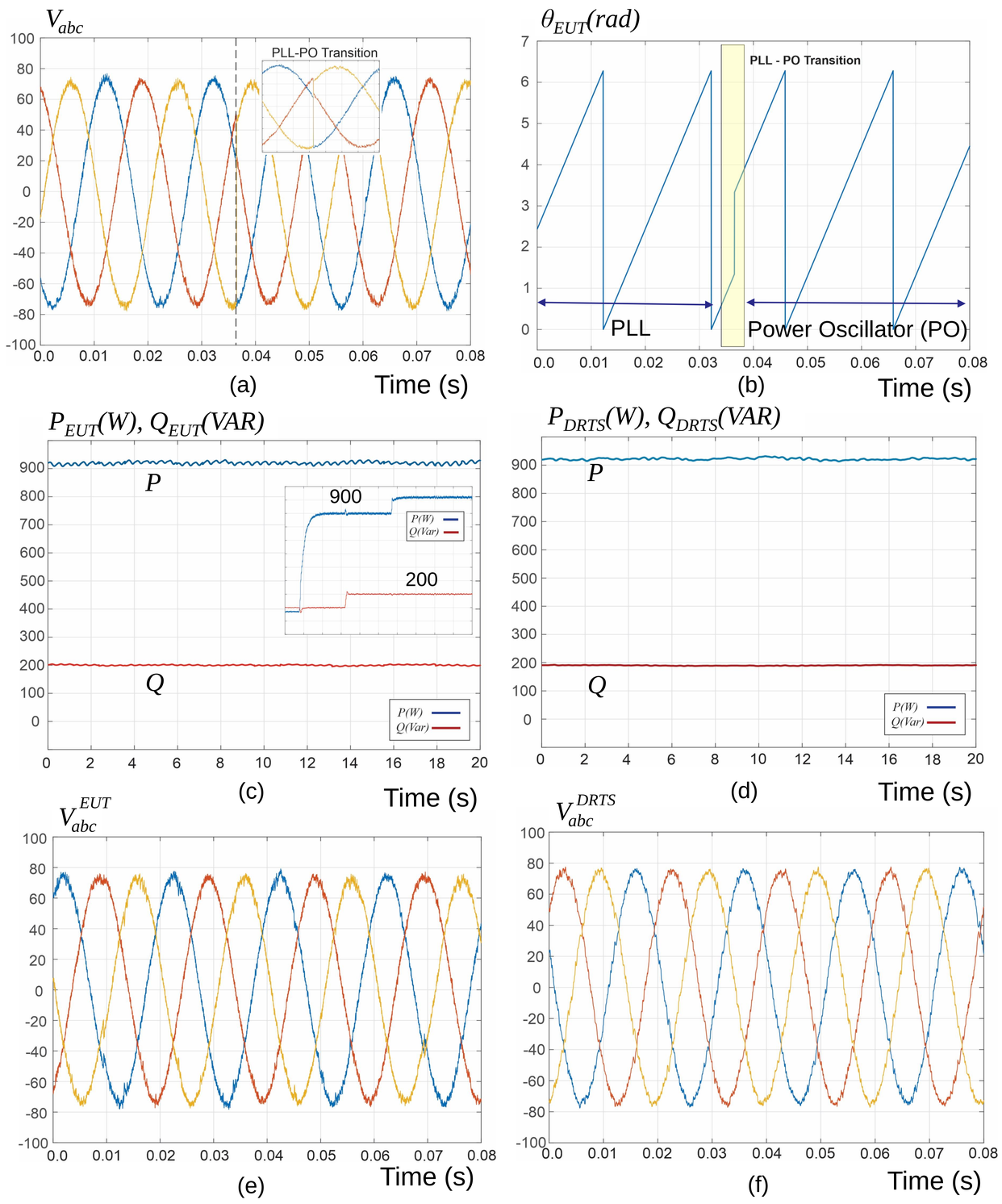

Fig. 3 Experimental results of the PHIL power interface for a Grid Forming converter.