Low-Frequency Oscillation Suppression in Series Resonant Dual-Active-Bridge Converters under Fault Tolerant Operation

Pan, Yiwei; Yang, Yongheng; He, Jinwei; Sangwongwanich, Ariya; Blaabjerg, Frede

Published in:
Proceedings of 2019 IEEE Energy Conversion Congress and Exposition (ECCE)

DOI (link to publication from Publisher):
10.1109/ECCE.2019.8913130

Publication date:
2019

Document Version
Accepted author manuscript, peer reviewed version

Low-Frequency Oscillation Suppression in Series Resonant Dual-Active-Bridge Converters under Fault Tolerant Operation

Yiwei Pan*, Yongheng Yang*, Jinwei He+, Ariya Sangwongwanich*, and Frede Blaabjerg*
* Department of Energy Technology, Aalborg University, Aalborg, Denmark
+ School of Electrical and Information Engineering, Tianjin University, Tianjin, China
E-mails: ypa@et.aau.dk, yoy@et.aau.dk, jinwei.he@tju.edu.cn, ars@et.aau.dk, fbl@et.aau.dk

***Abstract*—When an open-switch fault occurs in the inverter-side of the series resonant dual-active-bridge (SRDAB) converter, the rectified DC voltage will drop by a half. One solution to maintain the continuous power supply of the converter is to regulate the duty-cycle of the rectifier output voltage. Nevertheless, it may excite the resonance between the resonant inductors and the DC capacitors, leading to severe low-frequency oscillations, which appears as the envelope of the high-frequency current. This phenomenon may trigger the over-current protection and make the SRDAB fail to ride through the fault. In this paper, a low-frequency equivalent model is proposed for the SRDAB, enabling the frequency-domain analysis of the conventional single-loop voltage control. It is revealed that the oscillation depends on the duty-cycle and control parameters, and it is not possible to suppress such oscillations by the conventional control method. Thus, a dual-loop fault tolerant control method consisting of an outer voltage control-loop, an inner current envelope control-loop and a non-linear correction unit is proposed in this paper to suppress the oscillation. Experimental tests on a 1-kW SRDAB are performed. The test results have validated the effectiveness of the proposal in terms of oscillation suppression.**

Keywords*—Series resonant converter, Dual-active-bridge (DAB) converter, Fault tolerant control, Oscillation suppression, DC distribution systems.

I. INTRODUCTION

With the growing penetration of multiple renewable energy sources, high-performance DC/DC converters are in a continuous need to enhance the integration and exploitation of DC distribution systems [1]. Among various DC/DC topologies, the series resonant DAB (SRDAB) converter is a promising candidate as an isolated DC/DC interface in DC distribution systems [2]. On the other hand, the reliability for power converters is important to guarantee the stable operation of DC distribution systems [3]-[7], and thus, as one way to enhance reliability, fault tolerant control should be equipped with power converters. Since open-circuit faults do not always trigger the protections immediately, but will deteriorate the performance of converters, possibly leading to secondary problems [4], fault tolerant control methods for open-switch faults have been discussed in the literature [3]-[7]. When an open-switch fault happens in the SRDAB inverter side, the output DC voltage will drop by a half [8], as shown in Fig. 1. To ensure the continuous power supply and conversion, the fault tolerant operation should be enabled once the fault is detected. This can be achieved through topological modifications (adding redundant devices) or advanced control [3], [4].

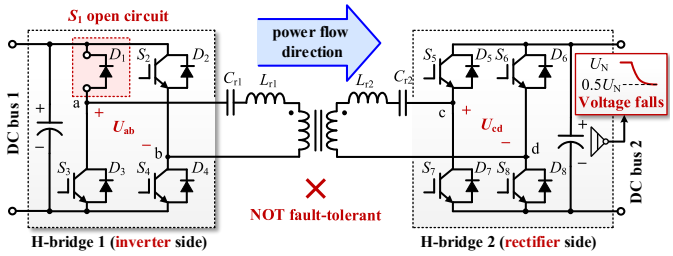

Fig. 1. Schematic of the Series-Resonant Dual-Active Bridge (SRDAB) converter, where an open-circuit fault is exemplified (S_1 is in the open-circuit fault).

Nevertheless, fault tolerant control methods for the SRDAB have been discussed rarely in the literature. For instance, in [9], a fault tolerant topology was introduced, where the rectifier-side is reconfigured to a voltage-doubler rectifier if an open-circuit fault occurs. This method can effectively improve the fault tolerant capability of the SRDAB, but it requires four bidirectional switches and split-capacitors at both DC buses, increasing the overall cost and complexity. To address this issue, a hybrid fault tolerant control method was proposed in [10] without hardware modifications. In this case, the duty-cycle of the rectifier-side H-bridge was regulated through a single-voltage closed-loop control to realize fast voltage control performance. However, the duty-cycle regulation may excite the resonance between the resonant inductors and the DC bus capacitors, resulting in un-damped low-frequency oscillations as the envelope of the high-frequency current. This may subsequently trigger the over-current protection, leading to failures of operation. As a result, it is necessary to explore the suppression techniques for the SRDAB in the fault-tolerant operation.

Considering the above, the oscillation mechanism and its suppression method are addressed in this paper. A dynamic equivalent model under the duty-cycle regulation is introduced, which enables the frequency response analysis of the system under fault tolerant operation. A dual-loop control strategy is accordingly proposed to suppress the low-frequency oscillations. The effectiveness of the proposed method is then

This work was supported by the China Scholarship Council (CSC).

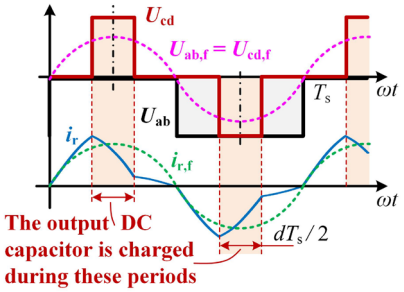

Fig. 2. Voltage and current waveforms of the SRDAB under the duty-cycle regulation, where S_1 is open-circuited.

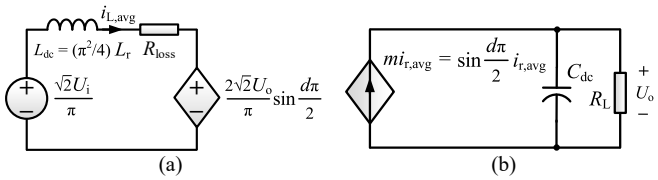

Fig. 3. Proposed equivalent circuit of the SRDAB with duty-cycle regulation: (a) controlled voltage source circuit, and (b) controlled current source circuit.

verified on a 1-kW SRDAB system. Finally, concluding remarks are provided.

II. Dynamic Equivalent Model under Duty-Cycle Regulation

Although many SRDAB models have been developed in the literature [11]-[14], most of them concentrate on the power flow, voltage dynamic and soft-switching performances. Therefore, in order to develop a model that is able to mimic the behavior of the actual system, the steady-state operational waveforms of the SRDAB should be analyzed.

The steady-state voltage and current waveforms of the SRDAB under the duty-cycle regulation are demonstrated in Fig. 2. In this case, S_1 is open-circuited (Fig. 1), and thus, the output voltage the inverter is halved. The duty-cycle of the rectifier is regulated. As a result, the fundamental components of U_{ab} and U_{cd}, denoted as $U_{ab,f}$ and $U_{cd,f}$, are described as

$$U_{ab,f} = \frac{4}{\pi}\left(\frac{1}{2}U_i\right)\sin\omega_s t,\ U_{cd,f} = \frac{4}{\pi}U_o \sin\frac{d\pi}{2}\sin\omega_s t \qquad (1)$$

where U_i and U_o denote the input and output DC voltage, respectively, and ω_s is the switching frequency. To sustain the normal output DC voltage, $U_{ab,f}$ and $U_{cd,f}$ should be identical. Therefore, d equals to 1/3 in the steady state. With the duty-cycle regulation, the entire resonance cannot be maintained, and thus, the high-frequency current i_r becomes discontinuous. The fundamental component of i_r, denoted as $i_{r,f}$, is also depicted in Fig. 2.

Based on the converter features discussed in the above, a DC model is developed as shown in Fig. 3. In this model, the AC sources $U_{ab,f}$ and $U_{cd,f}$ are replaced by two DC voltage sources, whose amplitudes are $\frac{\sqrt{2}U_i}{\pi}$ and $\frac{2\sqrt{2}U_o}{\pi}\sin\frac{d\pi}{2}$, respectively. An inductor L_{dc} is added between the two DC sources, as shown in Fig. 3(a). The stored energy in L_{dc} and the resonant tank should be the same, i.e., $L_{dc} = \frac{\pi^2}{4}L_r$, according to [12]. A series resistor

TABLE I. Simulation Parameters.

Circuit parameters	Value
Nominal DC voltages U_i, U_o	750 V
DC capacitance C_{in}, $C_{out} = C_{dc}$	1000 μF
Transformer ratio N_1:N_2	1:1
Output DC load R_L	40 Ω
Resonant capacitors C_{r1}, C_{r2}	4 μF
Resonant inductors L_{r1}, L_{r2}	27 μH
Switching frequency f_s	4.8 kHz
Magnetic inductance of HF transformer L_m	19.9 mH
Series resistor R_{loss}	0.8 Ω

R_{loss} is also included, which is used to emulate the converter losses of the power semiconductors. The average inductor current of this model, denoted as $i_{L,avg}$, can be used to study the low-frequency behavior of the high-frequency current i_r in the SRDAB. It can be further observed in Fig. 3(b) that a controlled current source circuit is added in the proposed model to study the DC terminal behavior. As shown in Fig. 2, the SRDAB converter charges the rectifier DC capacitor for an interval of dT_s in every switching cycle, with T_s being the switching period. Thus, the controlled DC current is proportional to the average current $i_{L,avg}$, represented by $mi_{L,avg}$, and the proportional coefficient m can be approximated as

$$m = \frac{\frac{2}{dT_s}\int_{\frac{T_s}{4}-\frac{dT_s}{4}}^{\frac{T_s}{4}+\frac{dT_s}{4}} i_{r,f}\,dt}{\frac{2}{dT_s}\int_0^{\frac{T_s}{2}} i_{r,f}\,dt} = \sin\frac{d\pi}{2} \qquad (2)$$

Subsequently, the small-signal state-space model can be obtained as

$$\begin{aligned}\begin{bmatrix}\dot{\hat{i}}_{L,avg}\\ \dot{\hat{u}}_o\end{bmatrix} &= A\hat{x} + B\hat{u}_i + K\hat{d}\\ &= \begin{bmatrix}-\frac{4R_{loss}}{\pi^2 L_r} & -\frac{8\sqrt{2}\sin\frac{D\pi}{2}}{\pi^3 L_r}\\ \frac{\sin\frac{D\pi}{2}}{C_{dc}} & -\frac{1}{R_L C_{dc}}\end{bmatrix}\begin{bmatrix}\hat{i}_{L,avg}\\ \hat{u}_o\end{bmatrix} + \begin{bmatrix}\frac{4\sqrt{2}}{\pi^3 L_r}\\ 0\end{bmatrix}\hat{u}_i\\ &\quad + \frac{\cos\frac{D\pi}{2}}{2\sqrt{2}R_L\sin^2\frac{\pi}{2}D + \pi R_{loss}}\begin{bmatrix}-\frac{8R_L U_i \sin\frac{\pi}{2}D}{\pi^2 L_r}\\ \frac{\sqrt{2}\pi U_i}{2C_{dc}}\end{bmatrix}\hat{d}\end{aligned} \qquad (3)$$

According to (3), the transfer function of $i_{L,avg}(s)$ and $u_o(s)$ in respect to the duty-cycle $d(s)$, denoted as $G_{iLd}(s)$ and $G_{ud}(s)$, can be calculated. To validate the accuracy of the proposed model, the frequency domain response between the proposed model and a circuit simulation model in MATLAB/Simulink are compared in Fig. 4. The Bode plots of $G_{iLd}(s)$ and $G_{ud}(s)$ are shown in solid lines. The frequency-response results in the MATLAB/Simulink are obtained through perturbing the duty-cycle D with a frequency sweeping signal ranging from

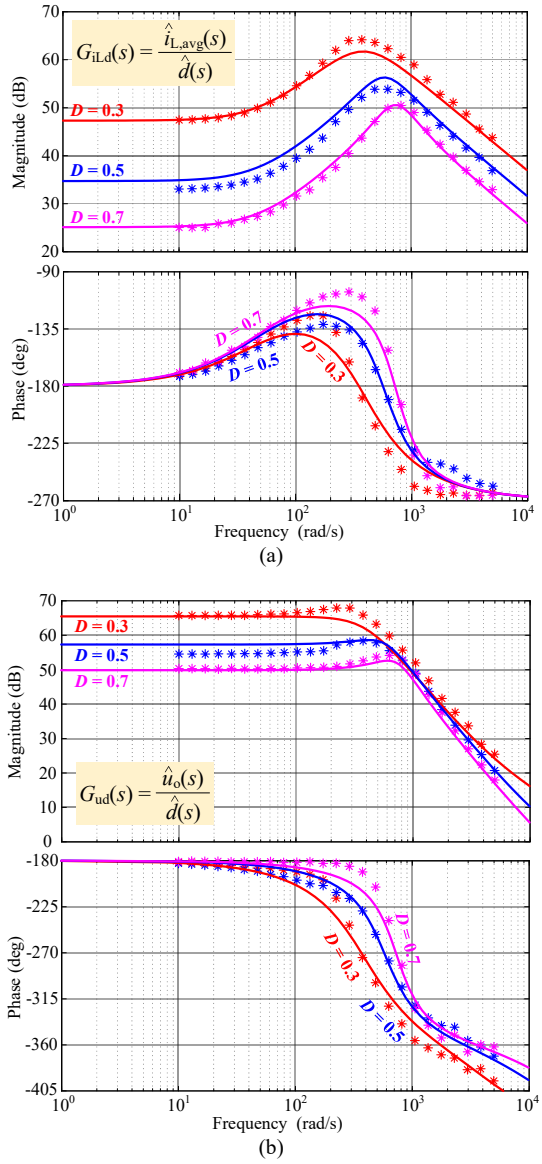

Fig. 4. Frequency responses of the simulation model (*) and the proposed model (solid lines and dash lines) under various steady-state duty-cycles D: (a) Bode plots of $G_{iLd}(s)$ and (b) Bode plots of $G_{ud}(s)$. Here, $\hat{d}(s)$ is the disturbance of the duty-cycle D, $\hat{i}_{L_avg}(s)$ is the disturbance of the current through L_{dc}, and $\hat{u}_o(s)$ is the disturbance of the output voltage.

$10 \sim 5\times10^3$ rad/s, and then the fast Fourier transform (FFT) is applied to the output signals (u_o and the absolute average value of i_r) to obtain the frequency-domain responses, which are shown by " * " in Fig. 4. The simulation parameters are listed in Table I.

As it can be observed in Fig. 4, the proposed model (Fig. 3) and the simulation model exhibit similar characteristics in the frequency range of 10 to 5×10^3 rad/s, which means that the proposed equivalent model shown in Fig. 3 can be used to study the behavior of the SRDAB under fault-tolerant operation in the low frequency domain.

For simplicity, assuming that R_{loss} equals to zero, the transfer functions $G_{iLd}(s)$ and $G_{ud}(s)$ can be obtained through $G_{xd}(s) = (sI - A)^{-1}K$, as

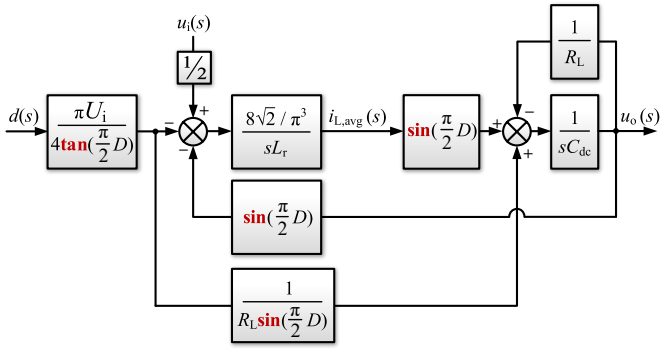

Fig. 5. Block diagram of the proposed equivalent model.

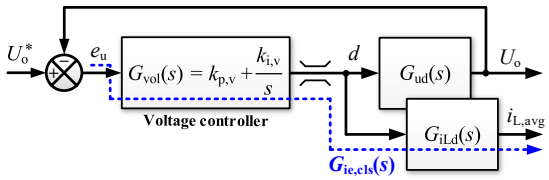

Fig. 6. Control diagram of the conventional single-closed-loop fault tolerant method.

$$\begin{bmatrix} G_{iLd}(s) \\ G_{ud}(s) \end{bmatrix} = \frac{\begin{bmatrix} -\frac{2\sqrt{2}U_i}{\pi^2 L_r \tan\frac{D\pi}{2}}\left(s+\frac{2}{R_L C_{dc}}\right) \\ \frac{U_i\cos\frac{D\pi}{2}}{C_{dc}}\left[\frac{\pi}{4R_L\sin^2\frac{D\pi}{2}}s-\frac{2\sqrt{2}}{\pi^2 L_r}\right] \end{bmatrix}}{s^2+\left(\frac{1}{R_L C_{dc}}\right)s+\frac{8\sqrt{2}\sin^2\frac{D\pi}{2}}{\pi^3 L_r C_{dc}}} \tag{4}$$

Referring to the Bode plots in Fig. 4, Eq. (4) reveals that the system is a second-order system. When compared with the typical second-order system, it is known that:

1) There is a resonant point between the resonant inductor and the DC capacitor, which moves to the high-frequency region with the increase of D.
2) Since $G_{ud}(s)$ has a right-half plane (RHP) zero, the system is a non-minimum-phase system.
3) The system damping ratio decreases with the increase of the duty-cycle D.

With the above analysis, the proposed model can be represented as shown in Fig. 5. Moreover, this system is highly nonlinear, as there are many trigonometric elements in its transfer functions, as shown in Fig. 5. Therefore, when the duty-cycle of the rectifier is regulated, the fault tolerant operation of the SRDAB is a nonlinear, parameter-variable, and a non-minimum-phase second-order system.

III. Characteristics under Conventional Fault Tolerant Method

In the conventional fault tolerant method, a single-loop voltage PI regulator is implemented to control the rectified DC voltage, when the open-circuit fault happens. The control diagram is shown in Fig. 6, where $G_{vol}(s)$ is the transfer function

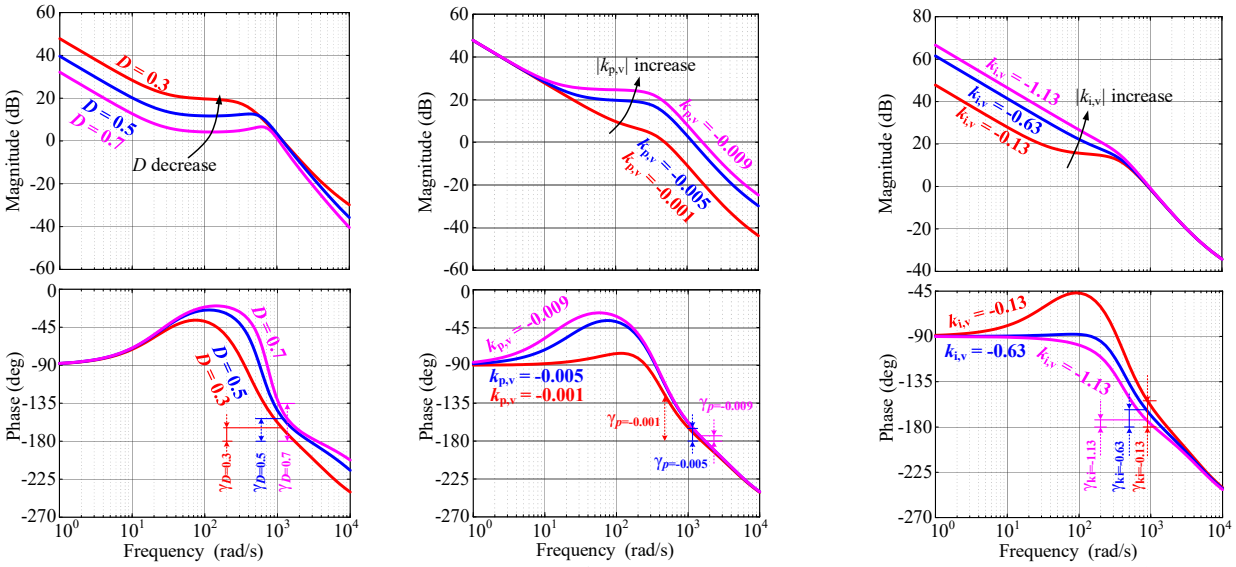

Fig. 7. Frequency responses of the open-loop system: (a) when $k_{p,v} = –0.005$, $k_{i,v} = –0.13$, (b) when $D = 0.3$, $k_{i,v} = –0.13$, and (c) when $D = 0.3$, $k_{p,v} = –0.003$.

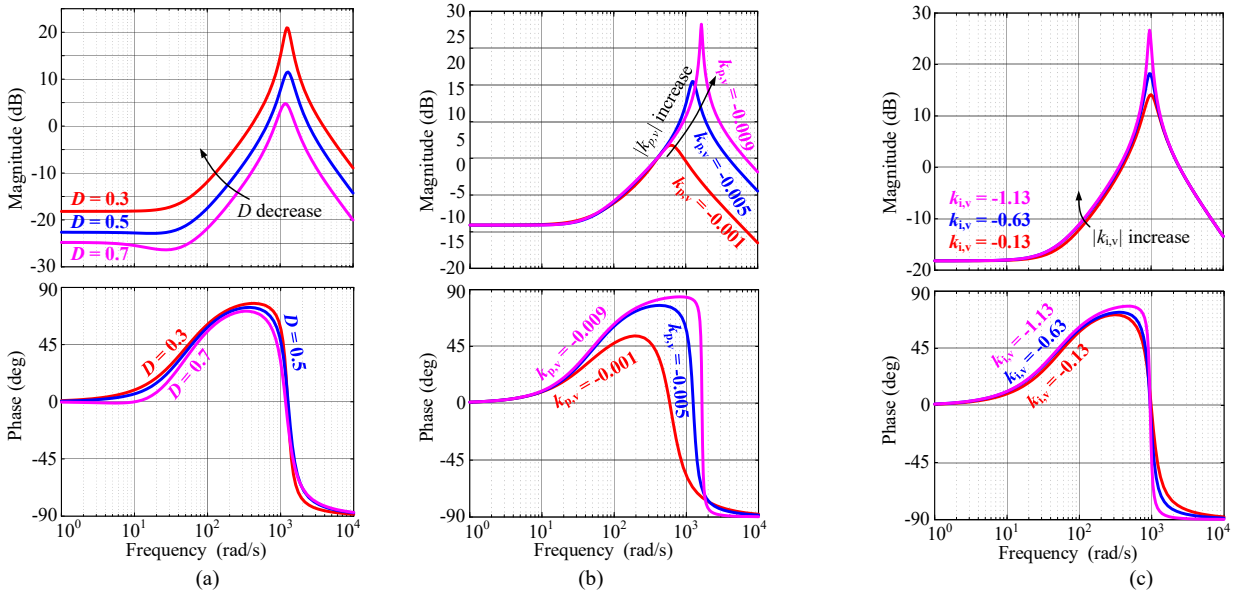

Fig. 8. Frequency responses of the closed-loop system: (a) when $k_{p,v} = –0.005$, $k_{i,v} = –0.13$, (b) when $D = 0.3$, $k_{i,v} = –0.13$, and (c) when $D = 0.3$, $k_{p,v} = –0.003$.

of the proportional integral (PI) voltage regulator with $k_{p,v}$ and $k_{i,v}$ being its proportional and integral gains. Since the increase of d will decrease the output DC voltage, $k_{p,v}$ and $k_{i,v}$ should be negative. The frequency response of the open-loop system $G_{vol}(s)\cdot G_{ud}(s)$ is shown in Fig. 7. As it can be seen in Fig. 7(a), when $k_{p,v} = -0.005$, $k_{i,v} = -0.13$, the cut-off frequency is around 1000 rad/s, and the phase margin γ is larger than 14° with D = 0.3 ~ 0.7, indicating that the system is stable. The increase of D will lower the magnitude of $G_{vol}(s)\cdot G_{ud}(s)$. In contrast, the increase of $|k_{p,v}|$ and $|k_{i,v}|$ leads to higher magnitudes of the open-loop system in the high and low frequency bands, respectively, but with a reduced phase margin of the system. Therefore, the PI parameters should be tuned in consideration of the fault tolerant control performances and stability.

To explore the characteristics of the average inductor current $i_{L,avg}(s)$ with the single-closed-loop control, the frequency responses of $G_{ie,cls}(s) = i_{r,avg}(s) / e_u(s)$, as shown in Fig. 6 (dashed lines), with $e_u(s)$ being the DC voltage error, are given in Fig. 8. It can be clearly observed that $G_{ie,cls}(s)$ has a peak with the frequency being near 1000 rad/s. Moreover, when D decreases or $|k_{p,v}|$ increases, the resonant frequency will increase, as demonstrated in Fig. 8(a) and (b), respectively. In addition, the increase of $|k_{p,v}|$ or $|k_{i,v}|$ will increase and sharpen the peaks of the frequency responses, as shown in Fig. 8(b) and (c). Therefore, it is implied in Fig. 8 that even when the system is stable under the voltage single-closed-loop control, the PI voltage controller is not able to suppress the resonance. In this case, during the transition to fault tolerant operation, the sudden change of e_u will introduce harmonics near the resonant peak. Subsequently, the harmonics are amplified, resulting in large low-frequency oscillations as the envelope of the high-frequency current.

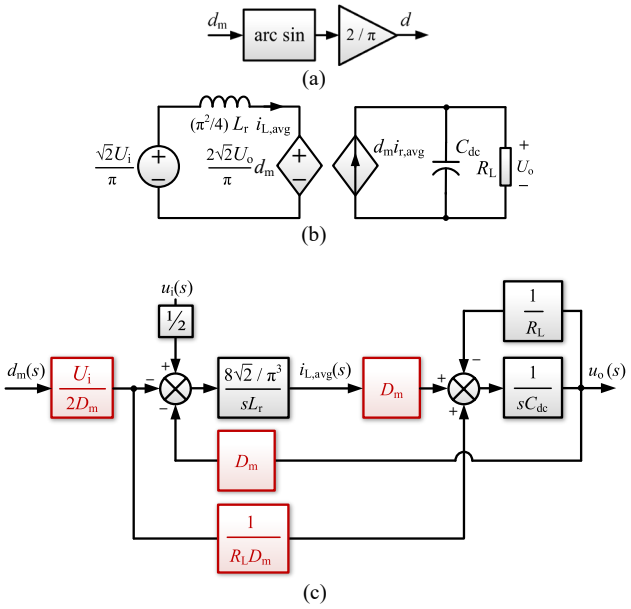

Fig. 9. Dynamic equivalent model after the nonlinearity correction: (a) nonlinearity correction unit, (b) equivalent circuit, and (c) modified block diagram.

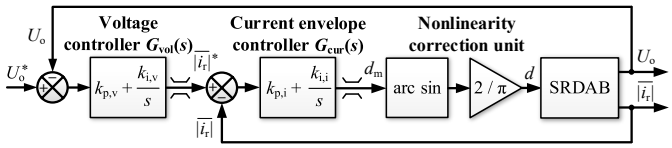

Fig. 10. Control diagram of the proposed dual-loop fault tolerant method.

IV. Proposed Dual-Loop Fault Tolerant Control Method

In order to address the above issues for the conventional voltage single-loop method, a dual-loop fault tolerant control method is proposed in this section. Firstly, since there are many nonlinear elements in the model of the system, as shown in Fig. 5, a nonlinearity correction unit is introduced in the control loop, as shown in Fig. 9(a). By doing so, the trigonometric term $\sin\frac{d\pi}{2}$ in Fig. 3 is corrected as $\sin\frac{\pi}{2}\left(\frac{2}{\pi}\arcsin d_{\mathrm{m}}\right)=d_{\mathrm{m}}$. The corrected equivalent circuit corresponding to the modified duty-cycle d_{m} is shown in Fig. 9(b). The state-space model of the modified system is presented in Fig. 9(c). As shown in Fig. 9(c), the nonlinear correction unit simplifies the model. It becomes clear that the proposed model is very similar to the conventional DC/DC boost converter, indicating that the resonant frequency of the system is also duty-cycle-dependent, and the system is a non-minimum phase system. Since the voltage/current dual-loop control method is widely used in DC/DC boost converters, a cascaded dual-loop fault tolerant method is proposed. More specifically, the outer loop of the proposed method regulates the rectified DC voltage and the inner loop controls the envelope of the high-frequency current. The entire control diagram of the proposed dual-loop method is shown in Fig. 10, where $G_{\mathrm{cur}}(s)$ represents the inner current envelope PI controller, and $k_{\mathrm{p,i}}$ and $k_{\mathrm{i,i}}$ are its proportional and integral gains. In the proposed method, the absolute average value of the inductor current, denoted as $|\bar{i}_{\mathrm{r}}|$, is employed as the control variable of the inner current envelope controller.

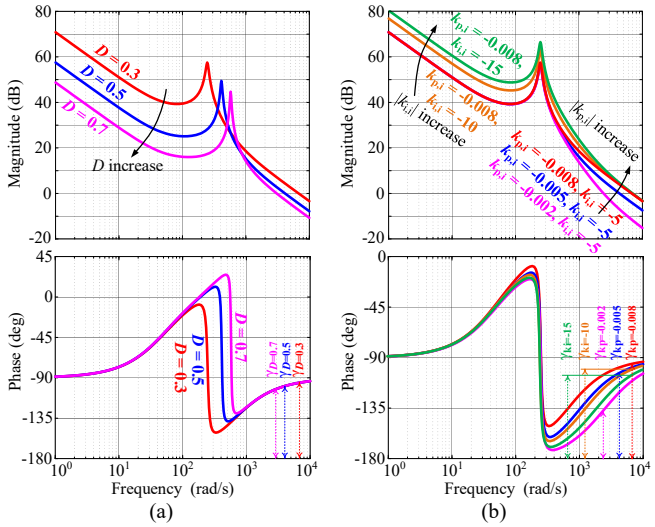

Fig. 11. Frequency responses of the current open-loop system: (a) when $k_{\mathrm{p,i}}$ = –0.008, $k_{\mathrm{i,i}}$ = –5, and (b) when D = 0.3, with varying $k_{\mathrm{p,v}}$ and $k_{\mathrm{i,v}}$.

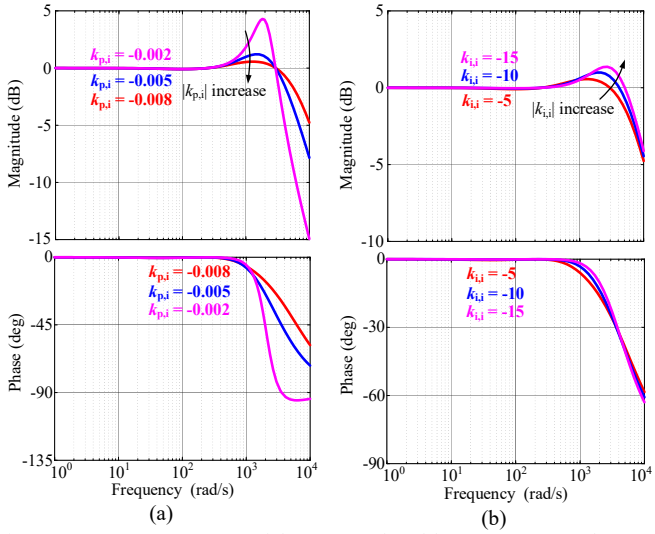

Fig. 12. Frequency responses of the current closed-loop system: (a) when D = 0.3, $k_{\mathrm{i,i}}$ = –5, and (b) when D = 0.3, $k_{\mathrm{p,i}}$ = –0.008.

To tune the parameters of the current controller, the open-loop Bode plots of the inner current loop can be used, as shown in Fig. 11. As it can be seen in Fig. 11(a), when $k_{\mathrm{p,i}} = -0.008$, $k_{\mathrm{i,i}} = -5$, the cutoff frequencies of the inner loop system is placed between 3k ~ 7k rad/s, thus the current control bandwidth is relatively high. The phase margin is 78° when D = 0.7, which is sufficient to ensure the control stability. The increase of $|k_{\mathrm{p,i}}|$ will lead to higher bandwidth and higher phase margin of the inner current loop, as shown in Fig. 11(b), but it will also introduce high-frequency noises as the cut-off frequency moves closer to the converter switching frequency. On the other hand, the increase of $|k_{\mathrm{i,i}}|$ will raise the amplitude-frequency curve in the low-frequency region, bringing a better steady-state performance, but at the same time, it decreases the phase margin of the current loop.

To demonstrate the oscillation suppression performance of the inner current loop, the closed-loop Bode plots of the inner

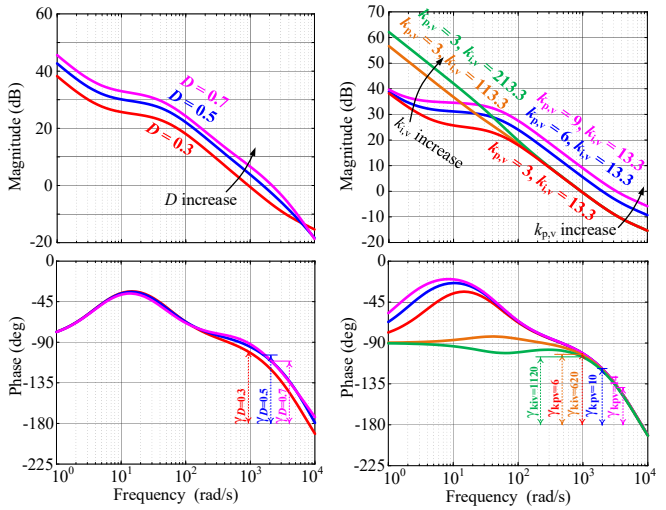

Fig. 13. Frequency responses of the voltage open-loop current closed-loop system: (a) when $k_{p,v} = 3$, $k_{i,v} = 13.3$, $k_{p,i} = -0.008$, $k_{i,i} = -5$, and (b) when $D = 0.3$, $k_{p,i} = –0.008$, $k_{i,i} = -5$.

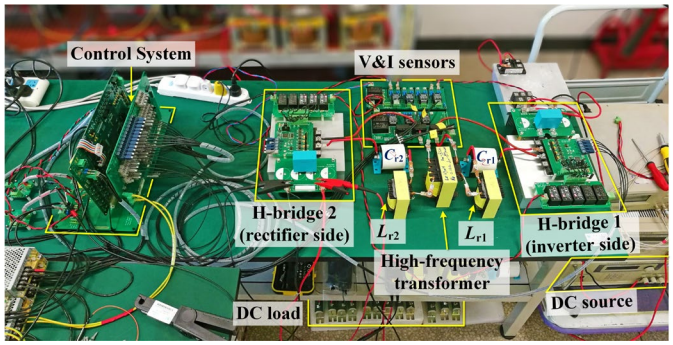

Fig. 14. Photo of the experimental prototype.

current loop are given in Fig. 12 when $D = 0.3$. As shown in Fig. 12, when $k_{i,i} = –5$, with the increase of $|k_{p,i}|$, the resonant peak can be effectively suppressed. On the other hand, when $k_{p,i} = –0.008$, the increase of $|k_{i,i}|$ will slightly increase the resonant peaks of the current closed-loop system, while pushing the peaks to the higher frequency region. With the help of the current open-loop and closed-loop Bode plots (Figs. 11 and 12), parameters of the current loop can be properly tuned.

To tune the parameters of the voltage outer-loop controller, frequency responses of the voltage open-loop and current closed-loop systems are shown in Fig. 13. As can be seen in Fig. 13(a), when $k_{p,v} = 3$, $k_{i,v} = 13.3$, $k_{p,i} = -0.008$, $k_{i,i} = -5$, the cut-off frequencies of the voltage loop is set around 1k rad/s, with the phase margin larger than 68° under different static duty-cycles. The increase of the proportional and integral gains, $k_{p,v}$ and $k_{i,v}$, will enhance the dynamic and steady-state voltage control performances, respectively, but the phase margin will be reduced, as shown in Fig. 13(b). Compared to the voltage single-loop control where either phase margin and control bandwidth should be compromised, the proposed dual-loop method can keep high control bandwidth while ensuring high phase margin. Therefore, with the proposed method, fast fault tolerant dynamics, high stability and suppression of the low-frequency oscillation can be achieved simultaneously.

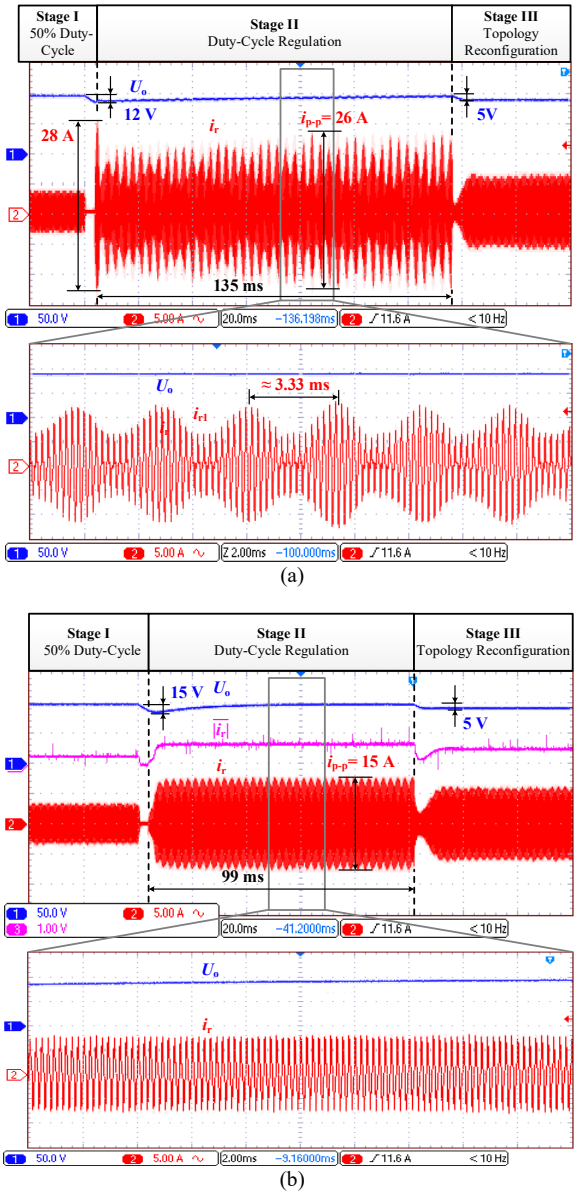

Fig. 15. Performance (experimental tests) of the SRDAB with the two fault tolerant methods (U_o [50 V/div]: the output DC voltage; i_r [5 A/div]: the high frequency current of the H-bridge 1; $|\overline{i_r}|$ [20 A/div]: the extracted current envelope from the analog circuit; time – top [20 ms/div], time – bottom [2 ms/div]): (a) the conventional voltage-single-loop method and (b) the proposed dual-loop method.

V. Experimental Results

To validate the effectiveness of the proposed dual-loop fault tolerant control method, experimental tests were performed on a downscaled 1-kW SRDAB prototype. The parameters of the experimental setup are shown in Table I.

Firstly, the conventional voltage single-closed-loop fault tolerant method was tested. The experimental results are shown in Fig. 15(a), where $k_{p,v} = – 0.009$ and $k_{i,v} = – 0.13$. At the beginning of the test, the output DC voltage was 96 V. Then, one switch in the inverter-side H-bridge (see Fig. 1) was in open-circuit fault. In this case, the output DC voltage is maintained at its output value with a short transient period, and a maximum

voltage drop of 12 V is observed in Fig. 15(a). When the open circuit fault was identified within 135 ms after the fault tolerant control, H-bridge 2 was reconfigured to be a half bridge and operates in the open-loop mode. However, as it is observed in Fig. 15(a), during the duty-cycle regulation period (fault tolerant operation), there are large oscillations with the frequency being about 300 Hz as the envelope of the high-frequency current. This oscillation frequency is very close to the resonant frequency of the Bode plot in Fig. 8(b), when $k_{p,v} = -0.009$ and $D = 0.3$, where the resonant frequency is around 1650 rad/s (≈ 262.6 Hz). The peak-to-peak value of the oscillations is measured as 26 A, which is 3.7 times larger than the nominal current. Moreover, during the transition to fault tolerant operation, e.g., at the beginning of the fault tolerant control, the peak-to-peak value reaches 28A, which is four times larger than the nominal current. This may trigger the system overcurrent protection, and it is demonstrated that the conventional method cannot suppress the oscillations.

The proposed dual-loop control method is then applied to the SRDAB system. The corresponding experimental results are shown in Fig. 15(b). In this case, the control parameters are $k_{p,v} = 3$, $k_{i,v} = 13.3$, $k_{p,i} = -0.008$ and $k_{i,i} = -5$. The same test procedure in respect with that for the conventional method was applied. As it is shown in Fig. 15(b), the high-frequency current envelope becomes flat and stable. That is, there are no low-frequency oscillations in the current. The peak-to-peak current is reduced to 15 A, being 2.1 times larger than the nominal current. The largest voltage drop is 15 V and the transient time for the duty-cycle regulation is 99 ms, which is slightly larger and shorter than the conventional method, respectively. It can be explained that the saw-toothed edge in the waveform of the high-frequency current is caused by the poor resolution of the oscilloscope. The zoomed-in waveform and the current envelope $|\bar{i}_r|$ measured from the analog circuit illustrate that there are no oscillations. Therefore, the proposed dual-loop control method can effectively suppress the low-frequency oscillation induced by the resonant inductors and the DC capacitors under fault tolerant operation, as analyzed in the previous sections.

VI. Conclusions

This paper analyzed the low-frequency oscillation issue as the envelope of the high-frequency current during the fault tolerant operation of the SRDAB. A detailed small signal model was presented to characterize the resonance, which reveals that the oscillation between the resonant inductors and the output DC capacitors cannot be suppressed by the conventional fault tolerant control method. Then, a dual-loop fault tolerant control method was proposed in this paper. In this control method, the outer loop regulates the DC voltage and the inner loop controls the envelope of the high-frequency current, leading to the suppression of the oscillations. Experimental results have demonstrated the effectiveness of the proposed method, where the low frequency oscillation can be suppressed compared to the conventional duty-cycle regulation method.

References

[1] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1311–1331, Jul. 2017.

[2] J. E. Huber and J. W. Kolar, "Solid-state transformers: on the origins and evolution of key concepts," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19-28, Sept. 2016.

[3] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron*., vol. 29, no. 12, pp. 6319-6331, Dec. 2014.

[4] U. Choi, F. Blaabjerg, and K. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron*., vol. 30, no. 5, pp. 2517-2533, May 2015.

[5] F. Wu, J. Zhao, Y. Liu, D. Zhou, and H. Luo, "Primary source inductive energy analysis based real-time multiple open-circuit fault diagnosis in two-level three-phase PWM boost rectifier," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3411-3423, Apr. 2018.

[6] J. Chen, C. Zhang, A. Chen, and X. Xing, "Fault-tolerant control strategies for T-type three-level inverters considering neutral-point voltage oscillations," *IEEE Trans. Ind. Electron*., vol. 66, no. 4, pp. 2837-2846, Apr. 2019.

[7] E. Ribeiro, A. J. M. Cardoso, and C. Boccaletti, "Fault-tolerant strategy for a photovoltaic DC-DC converter," *IEEE Trans. Power Electron*., vol. 28, no. 6, pp. 3008-3018, Jun. 2013.

[8] L. Costa, G. Buticchi, and M. Liserre, "Bidirectional series-resonant DC-DC converter with fault-tolerance capability for smart transformer," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.

[9] L. F. Costa, G. Buticchi, and M. Liserre, "A family of series-resonant DC–DC converter with fault-tolerance capability," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 335-344, Jan./Feb. 2018.

[10] Y. Pan, C. Zhang, L. Du, A. Chen, and J. He, "Control method of hybrid fault tolerant for series resonant dual-active-bridge interfacing converters in DC distribution systems," *Automation of Electric Power Systems* (in Chinese), vol. 42, no. 20, pp. 130-137, Oct. 2018.

[11] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle DCM series resonant converters," *IEEE Trans. Power Electron*., vol. 33, no. 1, pp. 4-7, Jan. 2018.

[12] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," in *Proc. IEEE Energy Conversion Congr. Expo. (ECCE)*, Montreal, QC, 2015, pp. 5021-5029.

[13] F. M. Ibanez, J. M. Echeverria, J. Vadillo, and L. Fontan, "A step-up bidirectional series resonant DC/DC converter using a continuous current mode," *IEEE Trans. Power Electron*., vol. 30, no. 3, pp. 1393-1402, Mar. 2015.

[14] F. Ibanez, J. M. Echeverria, J. Vadillo, and L. Fontan, "Frequency response analysis for bidirectional series resonant DC/DC converter in discontinuous mode," *IET Power Electron*., vol. 7, no. 9, pp. 2374-2386, Sept. 2014.