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Wang, Rui; Jørgensen, Asger Bjørn; Zhao, Hongbo; Munk-Nielsen, Stig

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Short-circuit Characteristic of Single Gate Driven SiC MOSFET Stack and Its Improvement with Strong Anti-short Circuit Fault Capabilities

Rui Wang, *Student Member, IEEE*, Asger Bjørn Jørgensen, Hongbo Zhao, Stig Munk-Nielsen, *Member, IEEE*

***Abstract*- The single gate driven series connected power device stack possesses the advantages of high compactness and low cost. However, research of its short circuit (SC) characteristic remains uncovered. This paper fills this gap and points out that, with the single gate driver it has the potential of over-current limitation. Further, based on it, an improved single gate driven SiC MOSFET stack with strong anti-short circuit fault capabilities is proposed. By adding auxiliary circuits to adjust the driving process of the single gate driver, the SiC MOSFET stack can be automatically turned off in both SC conditions of Fault Under Load (FUL) and Hard Switch Fault (HSF), while the normal working principle of the stack is not influenced. Neither active control nor overcurrent detection is required, which is the biggest merit of the proposed topology. Its design and analysis are presented in detail, followed by the validation by conducting simulations and experiments.**

Keywords—Short circuit fault; SiC MOSFET stack; single gate driver

I. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) as an emerging wide-bandgap semiconductor device has the potential to gain a dominant position in power electronics applications thanks to its superior characteristics. However, for medium/high voltage applications using of SiC MOSFETs is still limited due to the voltage blocking capability of a single device. In the pursuit of reducing complexity compared with the multi-level topologies [1], series connecting multiple SiC MOSFETs as a stack is a meaningful approach to overcome the obstacle. To make the SiC MOSFET stack operate reliably as expected, firstly, the voltage sharing characteristic and voltage balancing control of the stack are crucial, therefore much research has concentrated on this topic [2 - 4]. Secondly, the short circuit (SC) fault characteristic and protection of the stack are crucial as well.

For a single SiC MOSFET, the corresponding protections of its SC faults, including fault under load (FUL) and hard switch fault (HSF), have been investigated extensively. In [5], the SC faults are detected by comparing the on-state voltage drop in the desaturation region of SiC MOSFET, and the driving signal is actively pulled low for protection. Similar desaturation strategies are widely used in industries, but the specific blanking time requires delicate design and influences the timeliness of protective actions. In [6], the fault current is directly measured by a tunnel magnetoresistance which is integrated into a SiC MOSFET module, as the criterion for protection. Also, using Rogowski switch-current sensor in the power loop could achieve the same purpose [7], but the expensive cost is a common drawback. Comparatively, a better alternative is detecting the voltage across the parasitic inductance between Kelvin source and power source, so as to estimate the change rate of drain current, and an additional processing circuit is required to identify the SC fault. To achieve this goal, in [8, 9], the resistive-capacitive (RC) and resistive-capacitive-diode (RCD) integrator circuits are respectively applied to filter the voltage for comparing it with a threshold voltage; in [10], the gate-source voltage is additionally evaluated to help distinguish between the normal state and the SC state.

Nevertheless, applying the above SC protection schemes into a SiC MOSFET stack is debatable since the voltage unbalancing in the SC fault occurrence should be considered. As depicted in Fig. 1(a), *n* series connected SiC MOSFETs are

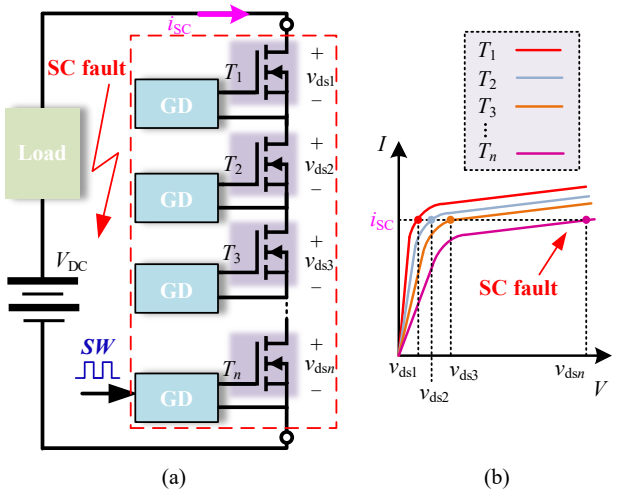

Fig. 1. (a) Conventional SiC MOSFET stack with seperated gate drivers. (b) *I-V* characteristics of *n* SiC MOSFETs.

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Rui Wang, Asger Bjørn Jørgensen, Hongbo Zhao and Stig Munk-Nielsen are with the Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark (e-mail: rwa@et.aau.dk; abj@et.aau.dk; hzh@et.aau.dk; smn@et.aau.dk)

configured to clarify the potential issues. If the SC fault of load side occurs, the drastically increasing SC current will flow through the SiC MOSFETs. However, due to the inconsistency of their I-V characteristics, as presented in Fig. 1(b), the SiC MOSFET with a lower I-V characteristic curve will withstand a higher voltage in the stack, resulting in its corresponding SC current tolerable time becoming less [11]. Therefore, even if the SC protection is delicately designed for a single SiC MOSFET application, it may be not suitable anymore for a SiC MOSFET stack application since a faster response may be required, which further makes the SC protection design of SiC MOSFET stack challenging.

Consequently, in consideration of the SC fault occurrence, achieving the maximum SC current tolerable time is a goal in the design of SiC MOSFET stack, that is, making the voltage and current trajectories of the SiC MOSFETs in the stack as identical as possible. Although active gate drivers and active voltage/current balancing circuits could adjust the trajectories by dynamically changing the gate loop parameters, most of them are designed for normal switching process [12 - 16], while not suitable for SC conditions. Instead, adopting passive clamping mode circuits is the effective way. In [17], a clamping mode snubber is equipped in parallel with each device in a series stack. When the voltage reaches the clamping value in the SC duration, a portion of the SC current flows into the snubber capacitor, and the voltage gets limited. Besides this, a resistor is placed at the intersection of power loop and gate loop, as a feedback to reduce the SC current difference of devices. However, a large snubber capacitor is required if the voltage increment of the snubber capacitor is expected to be low. In order to solve this issue, in [18], the SC current mismatch of adjacent two devices is controlled to have a minimum value, so as to reduce the value of the snubber capacitor. However, its influence on the normal working process of the stack should still be considered.

Compared with the above conventionally configured stack that has separated gate drivers, a single gate driven stack is an attractive way to series-connect devices, as it possesses the advantages of high compactness and low cost [19 – 26]. Nevertheless, the existing single gate driven stacks can still not handle the SC fault. Although the SC characteristic and protection of conventional stack have already been analyzed as mentioned, there are limited research and design regarding the characteristic and protection in the SC fault occurrence of the single gate driven stack.

Therefore, in this paper, the SC characteristic of single gate driven SiC MOSFET stack is analyzed in detail, which is completely different from that of a conventional one. It is pointed out that, the single gate driven SiC MOSFET stack has the potential of overcurrent limiting, which is a quite intriguing feature worthy of attention. Further, based on the analysis, it is proposed to add an auxiliary circuit to achieve an improved single gate driven SiC MOSFET stack, which possesses strong anti-short circuit fault capabilities. Its main features and advantages are:

- By adding auxiliary circuits to adjust the driving process of the single gate driver, the SiC MOSFET stack can be automatically turned off in both SC conditions of FUL and HSF, while the normal working principle of the SiC MOSFET stack is not influenced.
- During the whole anti-short circuit fault process, neither the overcurrent detection circuits nor active control circuits are required, which simplifies the design significantly.

In Section II, the SC characteristic of single gate driven stack is analyzed and its overcurrent limiting potential is pointed out, then a principle to utilize the anti-SC potential is concluded. Based on that, in Section III, the stack is improved to possess strong anti-short circuit fault capabilities, and a simplified model is established to estimate the process. In Section IV, the simulation and experimental results are shown to validate the design. Finally, in Section V, the conclusion is given.

II. Short-circuit Characteristic of Single Gate Driven SiC MOSFET Stack and Overcurrent Limiting Potential

Fig. 2(a) shows the general configuration of single gate driven SiC MOSFET stack with n SiC MOSFETs T_i (i =1 ~ n) in series, which is based on a buck chopper circuit with load inductor L, resistor R_L and diode D_L. T_n is equipped with a standard Gate Driver (GD), while others are equipped with individual Passive Driving Units (PDUs). Although PDUs could be connected in more possible ways than the one shown in Fig. 2(a), their basic working principles are the same [22].

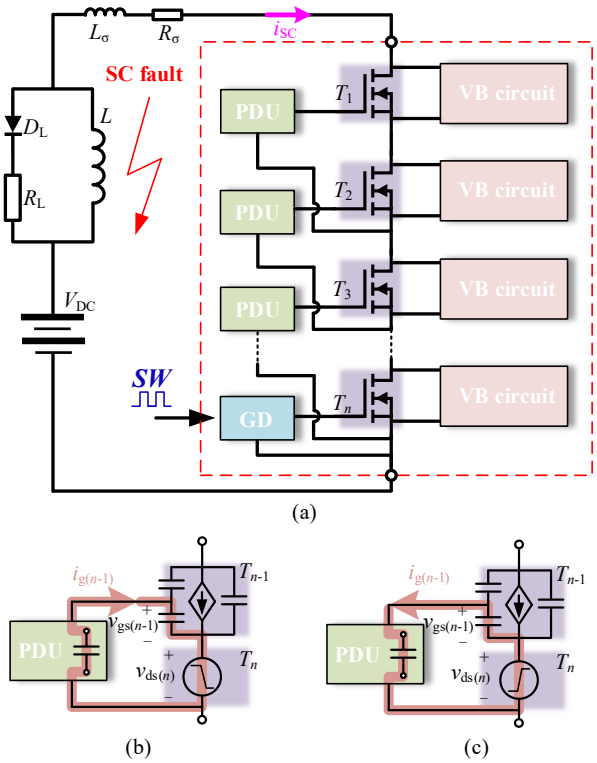

Fig. 2. (a) General configuration of single gate driven SiC MOSFET stack. Gate charging/discharging states during (b) turn-on and (c) turn-off.

In addition, using an auxiliary isolated power supply to construct PDU is one option if it can provide enough driving power and isolation voltage [23]. However, as more devices are connected in series, more separated auxiliary power supplies are required, resulting in a higher cost. Instead, using coupling capacitor is a cheaper option, and it also makes the single gate driver feature a simple and compact structure.

During the normal turn-on process of the stack, only T_n is controlled to turn on by one external switching signal *SW*. Then the falling of drain-source voltage $v_{ds(n)}$ of T_n could be regarded as a negative exciting source for turn-on of T_{n-1}, as presented in Fig. 2(b). A current $i_{g(n-1)}$ will flow into the gate of T_{n-1}, resulting in the rising of its gate-source voltage $v_{gs(n-1)}$. In this manner, T_{n-1} will be turned on as well, followed by $T_{n-2}\ldots T_1$. The consequence is similar during the normal turn-off process of the stack, as the rising of $v_{ds(n)}$ is regarded as a positive exciting source for turn-off of T_{n-1} shown in Fig. 2(c). However, the sequence of driving all devices also leads to voltage unbalancing among T_i (i =1 ~ n). Therefore, in addition to the gate side parts depicted in Fig. 2(a), Voltage Balancing (VB) circuits must be delicately designed if a balanced voltage sharing is expected, which is also a constraint on increasing the count of n. For this reason, a lot of research has been done for the voltage balancing design with single gate driver [19 – 25], but they are only targeted on the normal turn-on and turn-off processes of the stack, which leaves the analysis in the SC fault occurrence uncovered.

TABLE I
Simulation parameters of the single gate driven SiC MOSFET stack

Name	Parameter
T_i (i=1~ 4)	C2M1000170D (1700V/5A)
D_{ai}, D_{bi} (i=1~ 4)	PTZ20B (20V), TDZ6_2B (6.2V)
R_{gi}, R_{si} (i=1~ 4)	25Ω, 500kΩ
R_{g0}, C_{ai} (i=0~ 3)	25Ω, 47pF
RCD[2] circuit	50kΩ, 56nF, C5D05170H (1700V/5A)

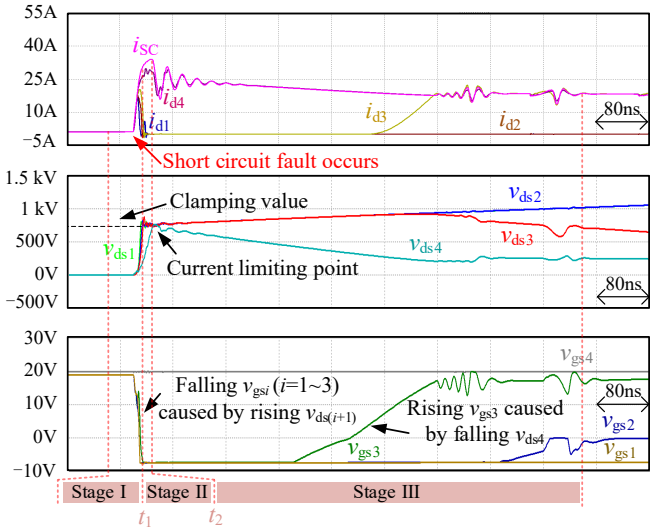

Fig. 3. Simulated waveforms of single gate driven stack when the FUL occurs

Consequently, in this section, the SC characteristic of the single gate driven stack will be analyzed to fill the gap. Further, it is pointed out that, although not able to handle the SC fault with the general configuration, the stack has a potential of over-current limiting capability when the SC fault occurs, which provides the basis for the following improvement in the next Section III.

To facilitate the analysis, based on the preserved single gate driven SiC MOSFET stack (n = 4) with corresponding clamping VB circuits in [24] (also shown as the stack without the improved part in the next Section III) and the key parameters described in Table I, the LTspice simulation waveforms are presented to reveal the mechanism in the SC occurrence of single gate driven stack, as shown in Fig. 3 when FUL occurs under a bus voltage V_{DC} of 3 kV. Three working stages could be divided as follows.

Stage I: Originally the stack operates normally, and the current i_{SC} flowing through it is kept low. Suddenly, the SC fault of load L occurs, and i_{SC} increases drastically, which will result in a rapid rising of the drain-source voltage v_{dsi} (i = 1~ 4) of T_i as T_i enters its saturation region, and the relationship could be expressed as [27 - 29]:

$$i_{SC} = f(v_{gsi}, v_{dsi}, T_j) = f_1(v_{gsi}) \cdot f_2(T_j) \cdot \frac{p(v_{gsi}) \cdot v_{dsi}}{1 + q(v_{gsi}) \cdot v_{dsi}} \quad (1)$$

where $f_1(v_{gsi})$ represents parameter of the transfer characteristic, $p(v_{gsi})$ and $q(v_{gsi})$ are parameters of the output characteristic, $f_2(T_j)$ represents the influence of junction temperature T_j.

During this process, T_i could also be regarded as a positive exciting source as depicted in Fig. 2(c). Therefore, similar to the turn-off process of the stack, the rising of $v_{ds(i+1)}$ will cause the falling of v_{gsi} (i = 1~ 3), which brings about a consequence: T_1, T_2 and T_3 will be turned off automatically and immediately after FUL occurs. Therefore, T_1, T_2 and T_3 will go back into the cut-off region while only T_4 will remain in the saturation region to limit i_{SC}.

Stage II: Since T_i (i = 1~ 3) is in its cut-off region, after v_{dsi} (i = 1~ 3) reaches the clamping value $V_{DC}/4$ of parallel clamping VB circuit, i_{SC} flows through the clamping circuit while the current i_{di} (i = 1~ 3) flowing through T_i drops to zero, and the moment is marked as t_1. Consequently, this feature of single gate driven stack makes T_i (i = 1~ 3) withstand a small SC duration (less than 20 ns in this simulated case), which is completely different from the conventional separated gate driven stack. Owing to the existence of additional clamping circuit, despite the turn-off inconsistency by using single gate driver, dynamic voltage unbalancing of v_{dsi} (i = 1~ 3) is avoided in the FUL occurrence. Afterwards, turned-off T_i (i = 1~ 3) and the capacitor C_{clamp} in clamping VB circuit are connected in parallel since the diodes are conducting, as shown in Fig. 4.

Hence, v_{dsi} (i = 1~ 3) becomes equal to the voltage across C_{clamp}. Due to the large value of C_{clamp}, v_{dsi} (i = 1~ 3) will get limited and continue to rise slowly at a rate of i_{SC}/C_{clamp}, and thus the following relationships are established:

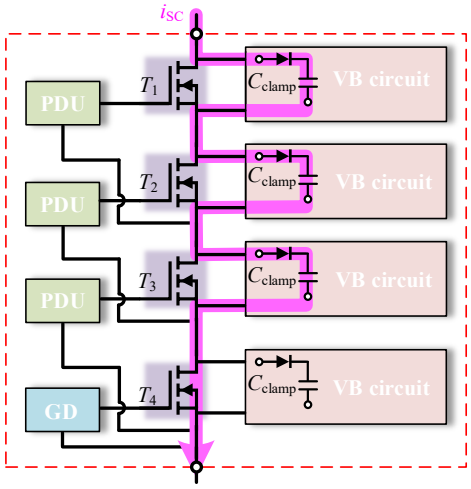

Fig. 4. SC fault current path after T_i (i = 1~ 3) is automatically turned off

$$\begin{cases} \dfrac{V_{DC}}{4}+\int_{t_1}^{t}\dfrac{i_{SC}}{C_{clamp}}dt=v_{dsi}, \quad i=1\sim 3 \\ v_{ds1}+v_{ds2}+v_{ds3}+v_{ds4}+L_\sigma\dfrac{i_{SC}}{dt}+R_\sigma i_{SC}=V_{DC} \end{cases} \tag{2}$$

where L_σ and R_σ are the parasitic inductance and resistance of the power loop, respectively.

Since T_4 is still in the saturation region, as i_{SC} continues to increase, v_{ds4} gets increased as well according to (1). Besides this, according to (2), v_{dsi} (i = 1~ 3) also gets increased, which contributes to the decreasing of di_{SC}/dt. As di_{SC}/dt gradually decreases to zero, i_{SC} will reach its maximum value at the end of Stage II, and the moment is marked as t_2, which corresponds to the arrival of the current limiting point.

Combining (1) and (2), the parameters representing the characteristic of device and the parameters regarding of the power loop (that is, L_σ, R_σ, C_{clamp} and V_{DC}) could have an influence on the current limiting point. Qualitatively, a higher V_{DC} and a larger C_{clamp} will induce a longer duration of this stage (t_2-t_1) and a higher i_{SC}. To specify this influence, the stack together with the improved part will be modeled in the next Section III.

Stage III: i_{SC} starts to decrease in this stage. Despite that T_4 is still turned on, T_1, T_2 and T_3 tend to withstand the total bus voltage finally since T_1, T_2, T_3 and T_4 are in a series stack. Hence, ideally, the SC current will be gradually decreased to zero and the stack will be turned off automatically, which means the single gate driven SiC MOSFET has the current limiting potential.

However, as i_{SC} is decreasing, v_{ds4} is falling as well since T_4 is in the saturation region. It will cause v_{gs3} to rise again as the state in Fig. 2(b), which means T_3 will be turned on again. Therefore, i_{d3} starts to increase as the current flowing through the parallel clamping VB circuit of T_3 is commutated to T_3. After that, the rising of v_{gs2} is followed. This unstable state will induce severe oscillation of v_{dsi} (i = 1~ 4), and finally cause a single device in the stack to withstand an extremely high voltage beyond its voltage rating, which is unacceptable for reliable operation.

Based on the above analysis, it is concluded that, the single gate driven stack has the overcurrent limiting potential as it limits the SC current in Stage I and II, but it would be destroyed afterwards because of the severe oscillation. Consequently, an assumption can be made in this paper: if v_{gsi} (i = 1~ 3) is kept negative during the overcurrent limiting process after the SC fault occurs, the overcurrent limiting potential of the stack could be utilized and would be quite meaningful.

Consequently, for purpose of achieving this goal, the principle is concluded as: the capacitor in PDU for T_i (i = 1~ 3) should sustain enough energy storage under the normal turn-off condition for the next normal turn-on of T_i; while it should sustain only a little or even no energy storage under the SC fault condition, so that it will not induce the turn-on of T_3 during the overcurrent limiting process. In this manner, a single gate driven stack with intrinsic anti-short circuit capabilities could be designed.

III. Improved Single Gate Driven SiC MOSFET Stack with Strong Anti-short Circuit Capabilities

According to the above principle, in this section, an improved single gate driven SiC MOSFET stack is further proposed, and it is shown in Fig. 5. Only one standard GD is required; PDU in this stack consists of coupling capacitor C_{ai} (i =1~ 4), gate resistor R_{gi}, static voltage balancing resistor R_{si} and Zener diodes D_{ai}, D_{bi}; RCD^2 circuit and additional $R_{g0}C_{a0}$ branch are for voltage balancing. In the previous work [24], along with detailed parameters design, it has been validated that this single gate driven stack topology performs a much lower total loss compared with conventional separated gate driven stack with RCD snubbers. In this paper, to make it

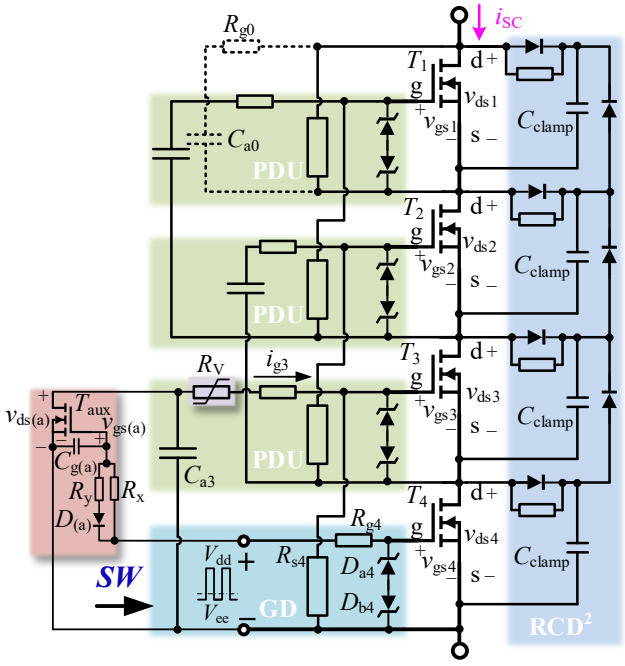

Fig. 5. The proposed improved single gate driven SiC MOSFET stack

possess strong anti-short circuit capability, a varistor R_V is added in the gate loop of T_3, and an auxiliary low-power MOSFET T_{aux} is added in parallel with C_{a3}. The improved part works synergistically to provide a low impedance loop for C_{a3} when the SC fault occurs, and C_{a3} will not sustain energy storage. In the meantime, it does not influence the normal switching of the stack. Next, its working principle under normal condition, the FUL condition and the HSF condition are respectively illustrated.

A. Working principle under the normal condition

When the turn-on signal arrives, the turn-on of T_{aux} should lag Δt_1 compared to T_4, so that C_{a3} will provide enough driving power for T_3 as normal, as shown in Fig. 6. As an option, by placing additional gate capacitor $C_{g(a)}$ and gate turn-on resistor R_x, Δt_1 could be directly provided and adjusted as:

$$\Delta t_1 = R_x(C_{g(a)} + C_{iss(a)})\ln\frac{V_{ee}-V_{dd}}{V_{th(a)}-V_{dd}} - R_{g4}C_{iss(4)}\ln\frac{V_{ee}-V_{dd}}{V_{th(4)}-V_{dd}} \quad (3)$$

where $C_{iss(a)}$ ($C_{iss(4)}$) and $V_{th(a)}$ ($V_{th(4)}$) are respectively the input capacitance and threshold voltage of T_{aux} (T_4).

In this manner, the stack will be turned on normally as analyzed in Section II, and i_{SC} flowing through the stack is increased to load current I_L. It is noticed that, after v_{ds4} falls to zero and v_{gs3} reaches V_{dd}, the gate-source voltage $v_{gs(aux)}$ of T_{aux} starts to reach $V_{th(a)}$ and T_{aux} enters the saturation region. Due to the existence of R_V, whose maximum continuous voltage is chosen to be greater than V_{dd}, the gate discharging loop of T_3 is not formed during the normal on state. Hence, v_{gs3} remains nearly unchanged, which is necessary for the normal operation of the stack under normal conditions.

When the turn-off signal arrives, the turn-off of T_{aux} should lead Δt_2 compared to T_4, so that the energy storage of C_{a3} will not be influenced. Similarly, in this case Δt_2 is adjusted by setting the values of $C_{g(a)}$ and gate turn-off resistor R_y since the turn-on and turn-off gate loops are separated by a diode $D_{(a)}$. Therefore, since the low impedance loop for C_{a3} is switched off in advance, the voltage of C_{a3} will rise as normal and enough driving energy is sustained for the next turn-on of T_3.

In brief, under the normal condition, the improved single gate driven stack works the same as the non-improved stack. And only in the SC fault occurrence, the improved part plays its role in showing the anti-short circuit fault capabilities as follows.

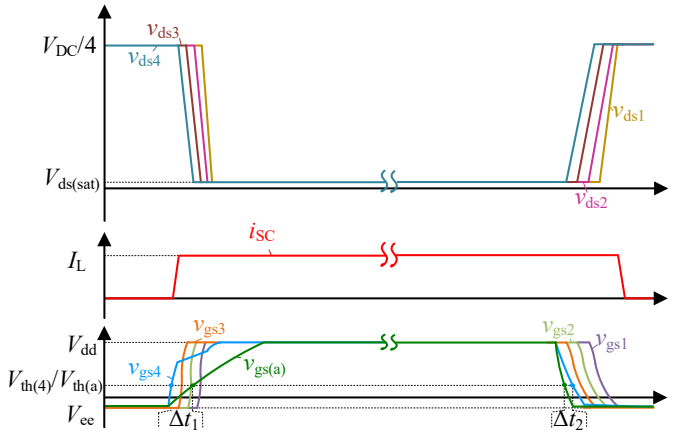

Fig. 6. Normal switching waveforms

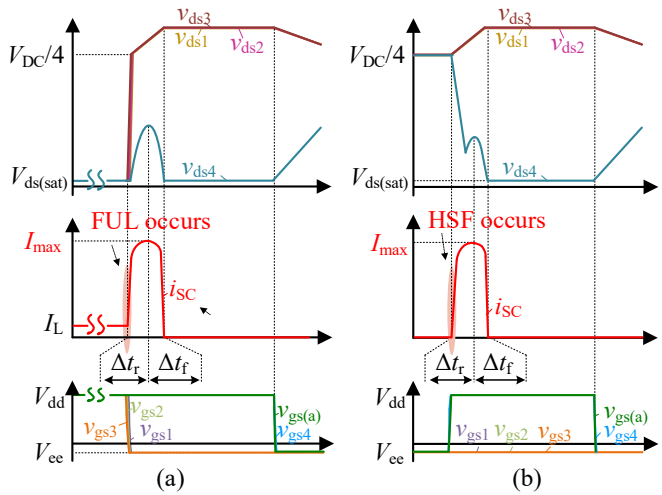

Fig. 7. Switching waveforms under the (a) FUL and (b) HSF occurence

B. Working principle under the FUL condition

As shown in Fig. 7(a), the stack is originally operating in the normal on-state and i_{SC} is equal to I_L. Suddenly, the SC fault occurs, and i_{SC} rises rapidly, accompanied by the rising of v_{dsi} (i=1~ 4) as T_i enters the saturation region. Same as analyzed in Section II, the rising of v_{dsi} (i=2~ 4) causes a gate discharging loop of T_i (i=1~ 3), v_{gsi} (i=1~ 3) falls to V_{ee}, which behaves as the normal turn-off process. Meanwhile, v_{gs4} and $v_{gs(a)}$ remain V_{dd} since the switching signal is in a logic "high" state, i.e. SW = "1". Therefore, only T_4 and T_{aux} are kept turned on while T_1, T_2 and T_3 are turned off immediately, which indicates the automatic turn-off of the stack. After a time interval of Δt_r, i_{SC} increases to the maximum value I_{max}, and then decreases to zero after another time interval of Δt_f.

Most importantly, since T_{aux} provides a low impedance loop for C_{a3} as the FUL occurs, no energy storage is sustained in C_{a3}. In fact, T_{aux} and R_V provide an additional branch for the current flowing of a portion of i_{SC}, and the gate charging loop of T_3 will not be formed during the v_{ds4} falling process. Therefore, v_{gs3} is kept negative. Finally, v_{dsi} (i=1~3) is equal to $V_{DC}/3$ while v_{ds4} is zero. Moreover, i_{SC} is zero as well, which illustrates that the proposed stack has a strong anti-FUL capability. When SW is changed to "0", v_{gs4} and $v_{gs(a)}$ become negative, and thus v_{ds4} rises while v_{dsi} falls gradually. In the end, all of them are back to $V_{DC}/4$.

C. Working principle under the HSF condition

As shown in Fig. 7(b), the SC fault occurs when SW is changed from "0" to "1", as it results in a rapid rising of i_{SC}. Due to this situation, v_{ds4} will fall much slower than the normal turn-on process. When $v_{gs(a)}$ reaches $V_{th(a)}$, T_{aux} is turned on and the energy stored in C_{a3} will be released through it. Therefore, the gate charging loop of T_3 is also not formed as

v_{ds4} is decreasing, and v_{gs3} remains negative. Since T_3 is not turned on, T_1 and T_2 will not be turned on either. Therefore, the stack is automatically turned off, and v_{gsi} (i =1~ 3) remains negative while v_{gs4} and $v_{gs(a)}$ remain V_{dd}. It should be noticed that, due to the existence of parasitic parameters L_σ and R_σ of the power loop, v_{ds4} will fall drastically in the beginning, and it could cause the instant turn-on of T_3 before $v_{gs(a)}$ reaches $V_{th(a)}$. Once T_{aux} is turned on and a portion of i_{SC} flows through it from the gate side of T_3, T_3 will be turned off immediately. Since this process is extremely short, it is named as "fake switching process" in this paper, and that is the reason for v_{ds4} not decreasing to zero smoothly as depicted in Fig. 7(b).

Similar to the FUL condition, i_{SC} increases to I_{max} after Δt_r. In the meantime of i_{SC} decreasing to zero after Δt_f, v_{dsi} (i=1~3) is equal to $V_{DC}/3$ while v_{ds4} is zero, which indicates that the proposed stack has a strong anti-HSF capability as well.

D. Simplified model of the anti-short circuit fault process

In summary, after improving the design of the single gate driven SiC MOSFET stack, its overcurrent limiting potential is analyzed and exploited, adding strong anti-short circuit fault capabilities without neither active control nor overcurrent detection design.

After analyzing the working principle, it is concluded that T_i (i=1~ 3) will be turned off immediately after the SC fault occurs, while T_4 will tolerate the high SC current for a certain time duration and might suffer from break-down. Therefore, the potential hazard during the anti-short circuit fault process of the stack lies in T_4, and it is important to estimate I_{max}, Δt_r and Δt_f to ensure the reliable operation of the SiC MOSFET stack. In this paper, an equivalent circuit model is established to illustrate and estimate the anti-short circuit fault process. To reduce the complexity of model, two simplifications are made: (1) for the FUL occurrence, the rapid increasing process of v_{dsi} (i=1~ 3) is neglected; (2) for the HSF occurrence, the instant "fake switching process" is neglected.

As shown in Fig. 8, this model consists of an exciting voltage source V_m, an inductor L_m, a resistor R_m, a capacitor C_m and a current source i_{eq}. V_m is equal to $V_{DC}/4$ as representing the voltage excitation across T_4 of the real circuit. L_m and R_m are respectively the loop inductance and resistance. C_m is equal to $C_{clamp}/3$ since the clamping capacitors C_{clamp} of T_i (i =1~3) are connected in series during this process. i_{eq} represents the behavior of T_4 (also including parts in parallel with it) in the saturation region, which is expressed as:

$$i_{eq} = f(v_{eq}, T_j) = f_2(T_j) \cdot \frac{a \cdot v_{eq}}{1 + b \cdot v_{eq}} \tag{4}$$

where v_{eq} the voltage across this current source. Compared to (1), i_{eq} is only related to v_{eq} and T_j since the gate voltage remains equal to V_{dd} during the whole anti-short circuit process, and thus parameters a and b can be obtained by fitting the I-V characteristic curve.

Additionally, in the modelling of anti-short circuit process, the influence of junction temperature, that is, $f_2(T_j)$ must be included due to the thermal effect of the high SC current. For accuracy, Cauer and Foster RC networks are two commonly adopted junction-to-case thermal models [30, 31]. To reduce the complexity, only one thermal Resistor-Capacitor (R_tC_t) unit is applied in this case as shown in Fig. 9. Based on the above, the following relationships exist in this equivalent model:

$$\begin{cases} C_t \cdot dT_j / dt + (T_j - T_c) / R_t = i_t = i_{eq} v_{eq} \\ v_{eq} + v_{Cm} + v_{Lm} + i_{eq} \cdot R_m = V_m \\ v_{Lm} = L_m \cdot di_{eq} / dt \\ i_{eq} = C_m \cdot dv_{Cm} / dt \end{cases} \tag{5}$$

where v_{Lm} (v_{Cm}) is the voltage across L_m (C_m), a current source i_t represents the induced power loss during the anti-short circuit fault process and a voltage source T_c represents the case temperature.

In (4) and (5), the relationship $f_2(T_j)$ and other unknown parameters could be obtained by fitting experimental data as illustrated in the next Section IV. Consequently, i_{eq} could be solved to estimate i_{SC}, and thus, I_{max}, Δt_r and Δt_f could be estimated as well, which provides the guideline of this design. In the next section, in addition to the validation of the anti-short circuit fault capabilities of the improved stack, the solved i_{eq} and estimated parameters are also compared with the experimental results to verify the effectiveness.

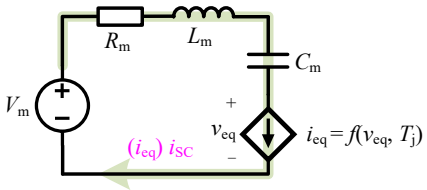

Fig. 8. Simplied model of the anti-short circuit fault process

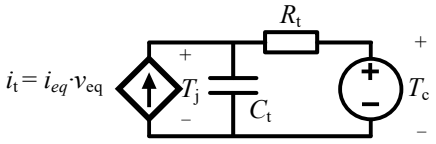

Fig. 9. Junction-to-case thermal model

IV. Simulation and Experimental Validation

Based on the main circuit diagram indicated in Fig. 2(a), as in a pulsed power application, the improved single gate driven SiC MOSFET stack is configured as a high voltage switch, and the combined unit of L, R_L and D_L is considered as a load. Afterwards, a corresponding experimental setup is established to evaluate the improved SiC MOSFET stack, as shown in Fig. 10. The key experimental parameters are consistent with the simulation parameters as listed in Table I. In addition to those, parameters of the improved part in the proposed stack are designed with the theoretical calculation and the aid of simulation, which are listed in Table II.

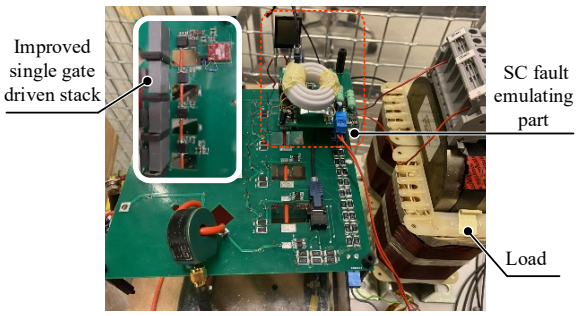

Fig. 10. Photograph of the experimental setup

TABLE II
Parameters of the improved part in the proposed stack

Name	Parameter
T_{aux}	STD2N105K5
R_V	2*AVRH10C270150NA8
R_x, R_y, $C_{g(a)}$	100Ω, 3.3Ω, 1nF
$D_{(a)}$	1N4148W

Besides this, for emulating the SC faults, a controlled high voltage Insulated Gate Bipolar Transistor (HV IGBT, IXEL40N400) is connected in parallel with L (30 mH). The switch signal with the designed timing is sent out by the DSP controller, and then HV IGBT is turned on and off at specific moments to emulate both HSF and FUL conditions. For measurement, Pearson probe (Model 2877) is applied to measure the SC current i_{SC} for ensuring the accuracy, and the differential probe (HVD3605A) is applied to measure the voltages.

A. Normal working process in the pulsed power application

In this pulsed power application, multiple switching pulses are expected to deliver the energy from the V_{DC} side to the load side. During the normal working process, the switching performance of the proposed stack under V_{DC} = 3 kV is shown in Fig. 11. It is seen that the stack is turned on and off normally under a frequency of 5 kHz and a duty cycle of 2%, as the voltage across the stack is defined as v_{stack}, that is, v_{stack}= v_{ds1}+v_{ds2}+v_{ds3}+v_{ds4}. By enlarging one switching cycle as depicted in the bottom of Fig. 10, it is observed that the turn-on *dv/dt* is 60 kV/μs and the turn-off *dv/dt* is 6 kV/μs, approximately. Moreover, the good voltage balancing of v_{dsi} (i = 1 ~4) is guaranteed by the passive RCD[2] circuit, which validates the good performance of the stack.

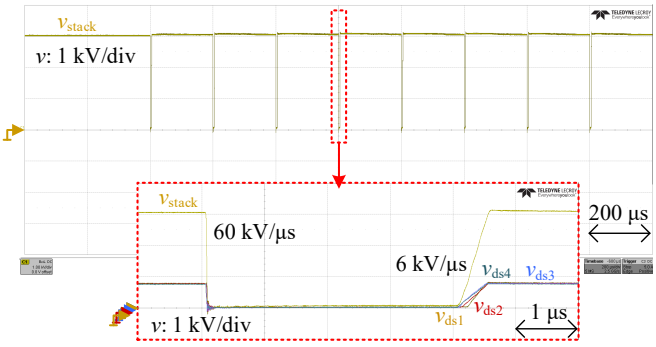

Fig. 11. Nomal working process of the proposed stack in the pulsed power application

B. Validation of anti-short circuit fault capabilities

In order to further validate the anti-short circuit fault capabilities of the stack, a reference under the normal condition of V_{DC} = 3 kV is set firstly, and v_{dsi} (i=1~4) and i_{SC} of SiC MOSFET stack during one switching cycle are given in Fig. 12. It is seen that, as *SW* is changed from "0" to "1", the stack is turned on and i_{SC} increases from zero gradually with current overshoot. After 20 μs, the signal is changed back from "1" to "0", then the stack is turned off and i_{SC} drops to zero. It is noticed that, since the parasitic capacitance exists in parallel with the load, a large "positive overshoot" of i_{SC} is induced by a relatively large *dv/dt* during the turn-on process. Also, a small "negative overshoot" of i_{SC} is induced by a relatively small *dv/dt* during the turn-off process. During this switching process, the voltage balancing of four SiC MOSFETs is good, which means the normal working the single gate driven SiC MOSFET stack is not influenced by the improved design. In the meantime, due to the improved part, the voltage v_{Ca3} across C_{3a} is subsequent to v_{ds4} while it is a little bit lower than v_{ds4}, which is determined by the clamping voltage of R_V.

Afterwards, using the same *SW* signal and no other protection circuit provided, v_{dsi} (i = 1~ 4) and i_{SC} under the FUL and HSF conditions are respectively given in Fig. 13 and Fig. 14. From Fig. 13, it is seen that i_{SC} increases slowly from zero as "1" is received, where a larger current overshoot could be observed compared with that under the normal condition due to the additional connection of HV IGBT for emulating SC fault condition. Then, the SC fault occurs after 10 μs (HV IGBT is turned on in this moment to emulate FUL), and suddenly i_{SC} increases rapidly. Consistent with the analysis, T_4 is in the saturation region as v_{gs4} remains at the high level, while T_3 is turned off as v_{gs3} falls to the low level,

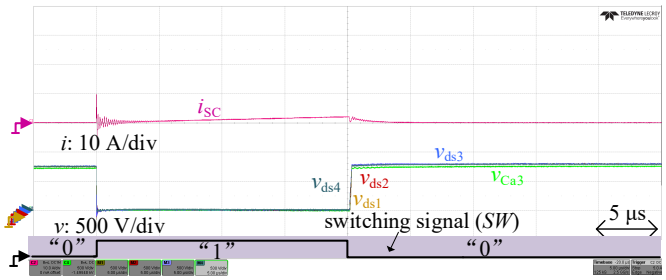

Fig. 12. Performance under the normal condition

consequently followed by T_2 and T_1. Owing to R_V and T_{aux}, C_{3a} can not sustain enough energy since v_{Ca3} is subsequent to v_{ds4}. Therefore, as i_{SC} rises to 34 A after 220 ns, i_{SC} is limited and then falls to zero after 450 ns. It means the stack is automatically turned off, which verifies the anti-FUL capability of the improved stack. From Fig. 14, it is found that the SC fault occurs in advance (HV IGBT is turned on in advance to emulate HSF) and i_{SC} rises rapidly from zero when *SW* is "1". After 120 ns, i_{SC} reaches 37 A and gets limited. Then, i_{SC} falls to zero after 480 ns, which further verifies the anti-HSF capability.

In both cases, T_1, T_2 and T_3 equally withstand the total bus voltage as v_{dsi} (i =1 ~3) = 1 kV after FUL or HSF occurs, and the good voltage balancing is observed. When *SW* is back to "0", v_{dsi} (i =1 ~3) is gradually back to normal, and finally T_1, T_2, T_3 and T_4 equally withstand the total bus voltage as v_{dsi} (i =1 ~4) is back to 750 V.

It is noticed that, the experiments have been conducted under V_{DC} is 1.0 kV, …3.0 kV, and good voltage balancing and anti-short circuit fault performances are obtained in all the cases, which verifies the robustness of the improved stack. Based on the above results, a comparison is made to discuss the advantage of the proposed stack: the separated gate drivers [2 - 4] have the advantage of having flexible gate control (i.e. useful for active balancing strategies), but it comes at the cost of low compactness and high cost, moreover it does not perform well under SC conditions without additional detection and active triggering circuitry. The existing single gate driven stacks [19 - 26], have proved high compactness and low cost, but careful design must be provided to avoid potential gate voltage oscillation [20]. It has been identified in this paper, although the single gate driven stack already shows some overcurrent limiting potential in the SC fault occurrence, it will continuously trigger several short circuits until failure as simulations show, which means it can still not handle the SC fault. Hence, in this paper, by using an auxiliary circuit to clamp the driven switch in its off-state following a SC event, the single gate driven stack gets improved with strong anti-SC fault capabilities.

Next, i_{SC} in all the experimental cases are recorded to make a comparison with the estimated results, so as to verify the simplified model.

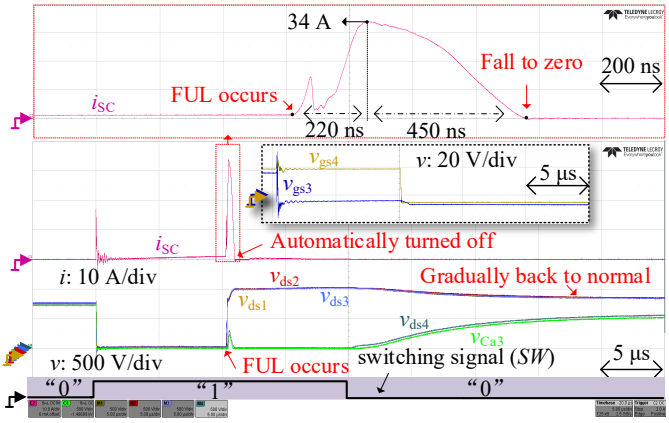

Fig. 13. Performance under the the FUL condition

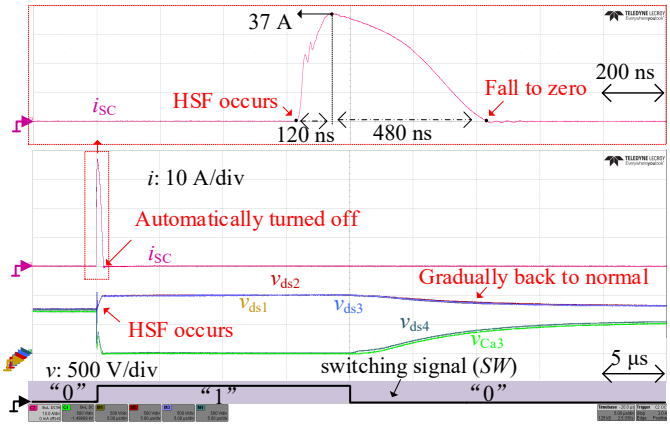

Fig. 14. Performance under the HSF condition

C. Verification of the simplified model

(1) Parameter identification of the simplified model

In order to identify the parameters of (4) and (5) in Section

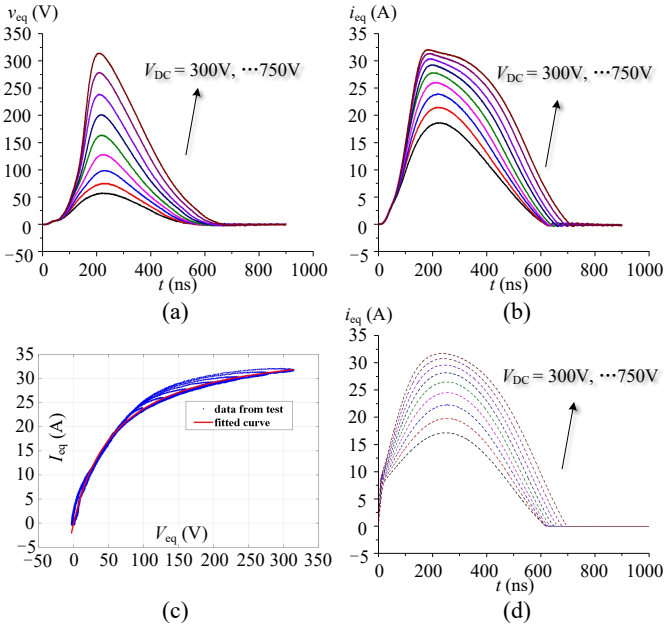

Fig. 15. (a) Measured v_{eq} (b) Measured i_{eq} (c) Fitting of I-V characteristic (d) Solved i_{eq} using derived model

TABLE III
Derived parameters of the simplified model

Parameters	L_m	R_m	C_m	a	b
values	3e-7	2	1.87e-8	0.6339	0.01671
Parameters	R_t	C_t	$f_2(T_j)$		k
values	10	9e-4	1-{k}×$exp(T_c$-$T_j)$		0.75

III, the following experiment is designed to obtain the data for fitting purpose: based on Fig. 5, T_i (i =1 ~ 3) is controlled to be constant off by short-circuiting the gate and source terminals, while T_4 and T_{aux} are constant on by making v_{gs4} and $v_{gs(a)}$ equal to V_{dd}. Therefore, under lower voltage cases, the transient behavior when it is connected to a DC voltage source V_{DC} can be captured by an oscilloscope, and the test data of v_{ds4} and i_{SC} are used to approximate v_{eq} and i_{eq} in Fig. 8.

In this manner, v_{eq} and i_{eq} under different voltage cases (V_{DC} = 300V, …750V) are obtained, as shown in Fig. 15(a) and Fig. 15(b), respectively. It is found that i_{eq} and v_{eq} get increased as V_{DC} increases, while the relationship between i_{eq} and v_{eq} is not linear. By importing those data to a fitting program, the relationship between v_{eq} and i_{eq} can be obtained, that is, the I-V characteristic curve can be drawn, as shown in Fig. 15(c). It is seen that, in addition to data points along the fitted curve, other data points are higher than the curve, which corresponds to the I-V characteristic influenced by the increased junction temperature T_j. Afterwards, other parameters are determined by fitting the current curves in Fig. 15(b), which are listed in Table III. Finally, the simplified model is derived, and the solved current curves are presented in Fig. 15(d). Based on the above, the solved current i_{eq} is used to estimate SC current i_{SC} of experiments under the SC fault occurrence as follows.

(2) Estimation under the FUL occurrence

Under the FUL occurrence of the improved single gate driven stack, the comparison results between the experiment and the model are shown in Fig. 16(a). It is seen that their initial stages are different since the simplified model neglects the rapid increasing process of v_{dsi} (i =1 ~ 3) in the anti-FUL process. To compensate this influence, the thermal parameter k in Table III is fine-tuned to be 0.65, and 80 ns delay is reserved.

Instead of making the solved i_{SC} in good agreement with the real i_{SC}, the aim of this established model is to estimate I_{max}, Δt_r and Δt_f, and it will be enough to evaluate the reliable operation of the proposed stack. Therefore, based on the data in Fig. 16(a), the measurement and estimation of Δt_r, Δt_f, Δt_r+Δt_f under different V_{DC} cases are shown in Fig. 16(b), and the corresponding results of I_{max} are shown in Fig. 16(c). Although there is a certain deviation between the estimated values and measured values of Δt_r and Δt_f, the deviation of Δt_r+Δt_f is controlled within 50 ns, and the deviation of I_{max} is within 2A. Hence, it is concluded that the simplified model well estimates the anti-FUL process of the proposed improved stack.

(3) Estimation under the HSF occurrence

Under the HSF occurrence, with the consistent parameters of model as in Table III, the comparison results between the experiment and the model are shown in Fig. 17(a). Also, the estimated and measured curves differ to some extent due to the simplification of this model, but their trends are in line with each other. Similarly, based on the data in Fig. 17(a), the measurement and estimation of Δt_r, Δt_f, Δt_r+Δt_f, I_{max} are given

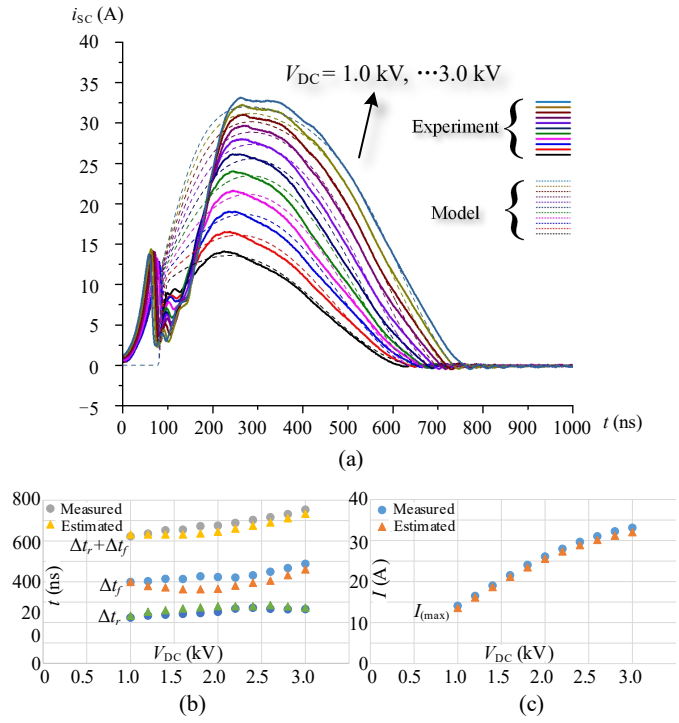

Fig. 16. (a) i_{SC} (b) Δt_r, Δt_f, Δt_r+Δt_f (c) I_{max} comparisons between experiment and simplified model under the FUL condition

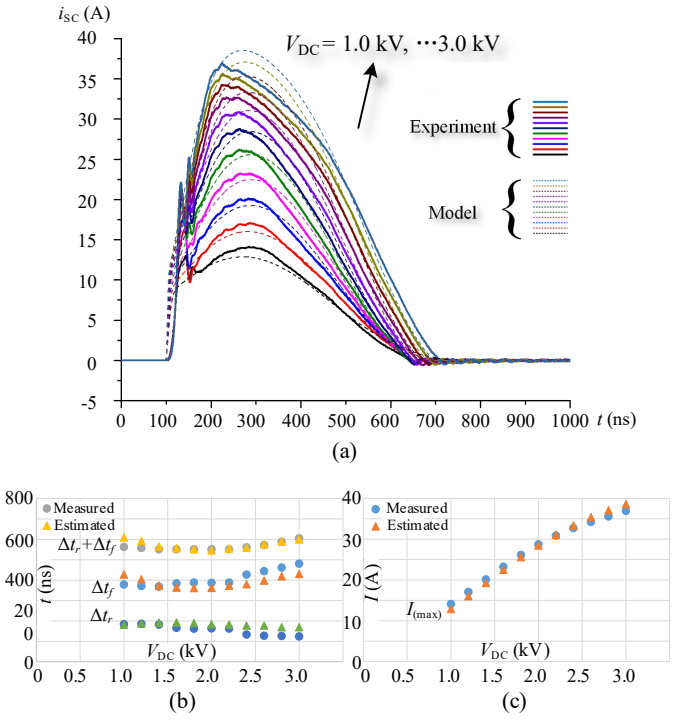

Fig. 17. (a) i_{SC} (b) Δt_r, Δt_f, Δt_r+Δt_f (c) I_{max} comparisons between experiment and simplified model under the HSF condition

in Fig. 17(b) and Fig. 17(c). It is found that, the deviation of $\Delta t_r+\Delta t_f$ is within 40 ns, and the deviation of I_{max} is within 2A, which proves the simplified model well estimates the anti-HSF process as well.

V. Conclusion

At last, this paper is summarized as follows. (1) the short circuit characteristic of the single gate driven SiC MOSFET stack is analyzed to fill the gap, and its overcurrent limiting potential is firstly pointed out; (2) based on the derived principle, the potential gets utilized with the proposed improved design, adding strong anti-short circuit fault capabilities. Neither active control nor overcurrent detection is required, as the stack can be automatically turned off when SC faults (both FUL and HSF conditions) occur; (3) Further, a simplified model is established to estimate the anti-short circuit process of the improved stack, so that the design guideline is derived; (4) finally, simulations and experiments have validated the design and proved its strong anti-short circuit fault capabilities.

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Rui Wang (S'18) received the B.S. degree in Electrical Engineering and Automation from Hunan University, Changsha, China, in 2017. He received the M.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2020. He is currently pursuing the Ph.D. degree in Aalborg University, Aalborg, Denmark.
His research interests include wide band-gap power semiconductor devices, their active gate drivers, series-connection technology and converter design.

Asger Bjørn Jørgensen received the M.Sc. and Ph.D. degrees in energy engineering from Aalborg University, Denmark, in 2016 and 2019, respectively.
He is currently working as an Assistant Professor at the Department of Energy Technology, Aalborg University. His research interests include power module packaging, wide bandgap power semiconductors and multi-physics finite element analysis within power electronic applications.

Hongbo Zhao (S'16, M'21) received the Ph.D. degree in Power Electronics from Aalborg University, Denmark in 2021. Currently, he is a Postdoc Researcher with Aalborg University, Aalborg, Denmark.

His research interests include high-frequency modeling and analysis of high-power magnetics and filters, as well as medium-voltage converters enabled by wide band-gap power devices.

Stig Munk-Nielsen (S'92–M'97) received the M.Sc. and Ph.D. degrees from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.
He is currently a Professor at the Department of Energy Technology, Aalborg University. His research interests include LV and MV Si, SiC and GaN converters, packaging of power electronic devices, electrical monitoring apparatus for IGBTs, failure modes and device test systems. In the last ten years, he has been involved or has managed 10 research projects.
Published 242 international power electronic papers being co-author or author.