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Reliability of DC-link Capacitors in Three-Level NPC Inverters under different PWM Methods

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***Abstract*—Pulse-width modulation (PWM) method plays an important role to ensure high efficiency and reliability of the three-level neutral-point-clamped (NPC) inverter. However, a comparison of the PWM methods in previous research has only considered power loss and reliability of power devices, while other reliability-critical components such as dc-link capacitors are not taken into account in the analysis. In this paper, the impact of PWM methods on the reliability of the dc-link capacitors in three-level NPC inverters is investigated by considering the capacitor power loss and their thermal stress. The evaluation results indicate that the PWM method which aims at minimizing the switching loss may introduce a significant power loss in the dc-link capacitors due to high amplitude of the low-frequency neutral-point (NP) voltage fluctuation. In that case, the thermal stress of the dc-link capacitors can be significantly increased, especially when the discontinuous modulation scheme is applied, affecting the reliability of the dc-link capacitors.**

***Index Terms*—Reliability, capacitors, power loss, pulse-width modulation (PWM), three-level inverter.**

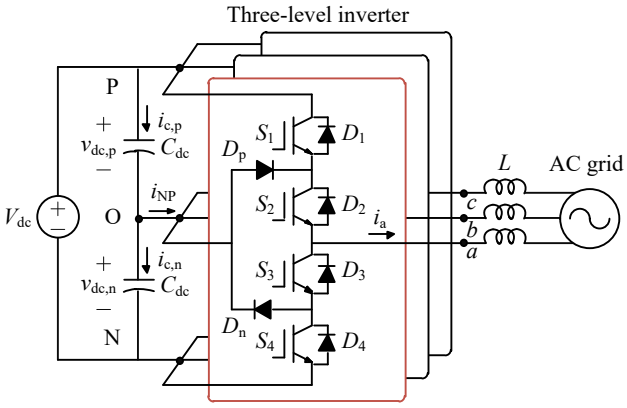

Fig. 1. System configuration of a grid-connected three-level neutral-point-clamped inverters, where P is the positive dc-link connecting point, O is the neutral point, and N is the negative dc-link connecting point.

I. Introduction

The three-level neutral-point-clamped (NPC) inverters have been widely applied in several applications including grid-integration such as wind and solar energy systems. Key performance metrics of the three-level NPC inverter like power quality, efficiency, and reliability are strongly affected by the used PWM methods. The three-level inverter topology shown in Fig. 1 offers more possible switching combinations compared to a two-level inverter to generate a certain (average) output voltage thanks to its redundant switching states. This gives a possibility to improve the inverter performance by applying a suitable PWM method, which was driving great research efforts in developing the PWM methods for three-level NPC inverters in the past [1]–[3].

To ensure high efficiency, several PWM methods for the three-level inverter aim at minimizing the number of switching transitions within one switching cycle, and thereby reduces the switching losses in the power devices. These PWM methods are generally realized by using the nearest-three-vector (NTV) approach [4]–[6], where the three voltage vectors around the reference voltage are used for generating the desired output voltage. In general, the PWM methods based on the NTV approach can effectively reduce the switching loss, especially when a discontinuous PWM scheme is used [7]. However, they usually have a limited impact on the NP voltage balancing (unless additional compensation methods are implemented).

The balancing of the NP voltage is an inherent drawback of the NPC topology, which can affect the performance of the inverter if not properly being controlled. Thus, another group of PWM methods developed for three-level inverters aim at minimizing the fluctuation of the NP voltage over the switching cycle. This is usually achieved by utilizing redundant voltage vectors to assist the NP voltage balancing mechanism such as the nearest-three-virtual-vector (NTV^2) PWM method [8], [9]. By using the NTV^2 PWM method, the fluctuation in the NP voltage can be eliminated within one switching cycle. However, the use of extra redundant voltage vectors results in an increased number of switching transitions and thus the switching loss, which is the trade-off of using this PWM approach.

In previous work, a comparison among different PWM methods for the three-level NPC inverter focusing solely on the power losses in the power devices (which thereby affects the efficiency) and the power quality of the output voltage/current (and thus affects the filter size) [10]–[13]. The NP voltage fluctuation issue was mainly considered from the safety aspect related to overvoltage of the power devices, which is crucial for an application with low-frequency AC output voltage such as motor drives. However, the variation in the NP voltage of the PWM method also contributes to the ripple current and thus the power losses in the dc-link capacitors [14]–[17]. This will certainly affect the lifetime and reliability

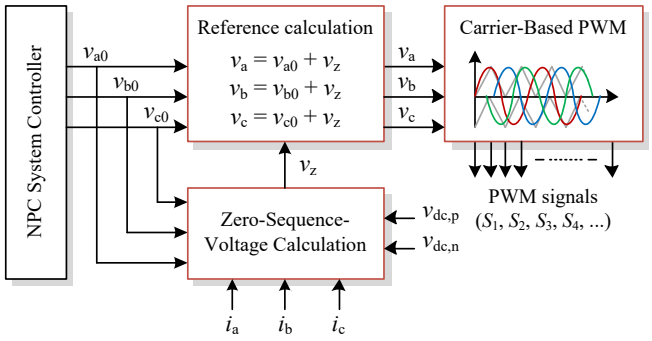

Fig. 2. Control diagram of carrier-based pulse-width modulation method with the injection of zero-sequence voltage for three-level NPC inverters.

of the dc-link capacitors, which needs to be considered in order to ensure the overall trade-off between efficiency, power quality, and reliability of the entire system. This issue has not been addressed in the previous studies when comparing the performance of different PWM strategies for three-level NPC inverters.

To address this issue, the evaluation of the PWM methods for the three-level NPC inverter is carried out in this paper. A comparison is done by considering the impact of PWM methods on the power losses, the thermal stress, and the reliability of dc-link capacitors. The rest of this paper is organized as follows: the overall control and NP balancing issue of grid-connected three-level inverter is described in Section II. Then, the reliability analysis of the dc-link capacitors which includes power loss, thermal stress, and lifetime modeling are provided in Section III. In Section IV, the operating principle and implementation of the selected PWM methods are demonstrated, while their impact on the reliability of dc-link capacitors is carried out in Section V. Finally, concluding remarks are given in Section VI.

II. Three-Level Neutral-Point-Clamped Inverters

The overall control structure of the three-level NPC inverter is shown in Fig. 2. Generally, the PWM methods of the three-level NPC inverter can be implemented either with the space vector modulation (SVM) or the carrier-based (CB) PWM approaches [18]. In this section, the CB-PWM control of the three-level NPC inverter and its impact on the NP voltage variation will be discussed.

A. Carrier-Based Pulse-Width Modulation

The overall goal of the PWM technique is to generate the output voltage according to the reference three-phase voltage v_{a0}, v_{b0}, and v_{c0} as

$$\begin{aligned} v_{a0} &= V_m \cos(\omega t) \\ v_{b0} &= V_m \cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_{c0} &= V_m \cos\left(\omega t - \frac{4\pi}{3}\right) \end{aligned}$$

where V_m is the amplitude of the three-phase sinusoidal reference voltage and ω is the angular frequency.

For the CB-PWM technique, the addition of zero-sequence voltage v_z to all the three-phase reference voltage provides a degree of freedom to effectively utilize different vector combinations. Thus, the reference voltages after the zero-voltage injection (v_a, v_b, and v_c) can be obtained as

$$\begin{aligned} v_a &= v_{a0} + v_z \\ v_b &= v_{b0} + v_z \\ v_c &= v_{c0} + v_z \end{aligned}$$

and various PWM methods can be realized by utilizing different methods for identifying the zero-sequence voltage v_z, which will be elaborated in Section IV.

B. Neutral-Point Voltage Balancing

When one of the phases is connected to the NP (e.g., when S_2 and S_3 are turned on), there will be a current flowing into (or from) the NP i_{NP}, as it is shown in Fig. 1, causing the NP potential to fluctuate. The average NP current over one PWM switching cycle $i_{NP,avg}$ can be calculated as [19]

$$\begin{aligned} i_{NP,avg} &= -|v_a| \cdot i_a - |v_b| \cdot i_b - |v_c| \cdot i_c \\ &= -(s(v_a) \cdot v_{a0} i_a + s(v_b) \cdot v_{b0} i_b + s(v_c) \cdot v_{c0} i_c) \\ &\quad -v_z(s(v_a) \cdot i_a + s(v_b) \cdot i_b + s(v_c) \cdot i_c) \end{aligned} \quad (1)$$

where $s(v_x)$ indicates the sign function, which has a value of either 1 or -1 for positive and negative value of v_x, respectively.

During the steady-state operation, half of the average NP current $i_{NP,avg}$ will flow into each of the dc-link capacitors C_{dc} following

$$i_{c,p} = -i_{c,n} = \frac{i_{NP,avg}}{2}$$

where $i_{c,p}$ and $i_{c,n}$ are the ripple current of the upper and lower dc-link capacitors, respectively. This ripple current will contribute to the power loss in the dc-link capacitor and also result in the voltage variation of

$$\Delta v_{dc,p} = -\Delta v_{dc,n} = -\frac{1}{C_{dc}} \frac{i_{NP,avg}}{2} T_s \quad (2)$$

where $\Delta v_{dc,p}$ and $\Delta v_{dc,n}$ are the variations in the upper and lower dc-link voltage over the switching period T_s.

It can be seen from (2) that there will be variation in the upper and lower dc-link voltage (i.e., $\Delta v_{dc,p}$ and $\Delta v_{dc,n}$), if the average NP current $i_{NP,avg}$ is not controlled to be zero within one switching period T_s.

III. Reliability of DC-Link Capacitors

During operation, the ripple current in the electrolytic capacitor will generate power loss and increase the core temperature of the capacitors (e.g., hotspot temperature). This will consequently accelerate the degradation and wear-out of the capacitor overtime. To evaluate the impact of PWM methods on the efficiency and reliability of the three-level inverter, the modeling of power loss and thermal stress of the dc-link capacitors is necessary as it is illustrated in Fig. 3.

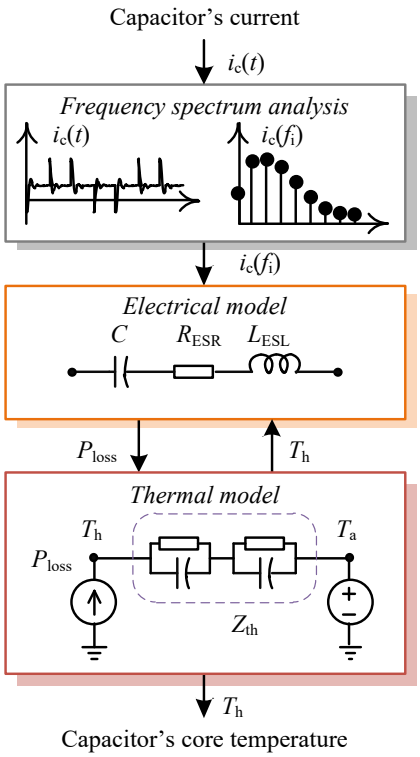

Fig. 3. Power loss and thermal stress analysis of dc-link capacitors.

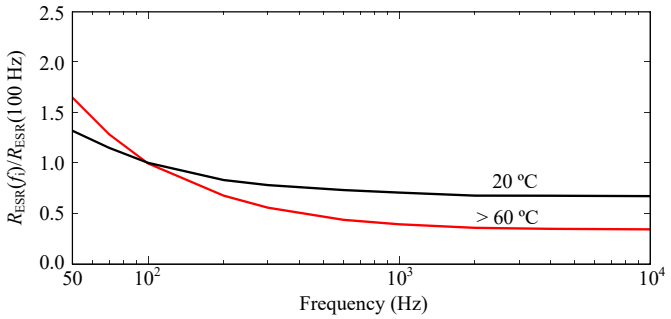

Fig. 4. Frequency-dependent characteristic of equivalent series resistance (ESR) $R_{ESR}(f_i)$ for different temperature in capacitors, where $R_{ESR}(100\ Hz)$ is the ESR at f_i = 100 Hz [20].

A. Power Loss Modeling

Power loss in the dc-link capacitor P_{loss} can in general be calculated from the ripple current (RMS) in the capacitor i_c and the equivalent series resistance R_{ESR} following:

$$P_{loss} = \sum_{i=1}^{n} i_c^2(f_i) \cdot R_{ESR}(f_i) \tag{3}$$

where $i_c(f_i)$ and $R_{ESR}(f_i)$ being the ripple current and equivalent series resistance at the frequency f_i, respectively, while n is the number of frequency components.

The frequency-dependent equivalent series resistance $R_{ESR}(f_i)$ parameters of the dc-link capacitors used in this paper are shown in Fig. 4, where $R_{ESR}(100\ Hz)$ = 0.23 Ω.

B. Thermal Stress Modeling

The thermal model of the dc-link electrolytic capacitor is shown in Fig. 3, where it can be seen that the power loss in the capacitor will cause the core temperature T_h to rise following

$$T_h = R_{th,dc} \cdot P_{loss} + T_a \tag{4}$$

where T_a is the ambient temperature and $R_{th,dc}$ = 7.93 K/W is the capacitor thermal impedance [20].

C. Lifetime Modeling

The increase in the core temperature of the electrolytic capacitors generally has a negative impact on their lifetime. For the electrolytic capacitors, the lifetime model is given as in the following [21], [22]:

$$L_f = L_0 \times 2^{(\frac{T_0 - T_h}{10})} \tag{5}$$

where L_f is the time-to-failure under the thermal stress level of T_h, while L_0 = 3000 hours is the nominal lifetime when the capacitor operates at the core temperature T_0 = 105 °C.

In many cases, the lifetime of the electrolytic capacitor will approximately reduce to half when the core temperature T_h is increased by 10 °C from the nominal value T_0. Thus, the lifetime and reliability of the dc-link capacitors are very sensitive to the power losses and thus thermal stress, e.g., induced by different PWM methods.

IV. Pulse-Width Modulation Methods for Three-Level NPC Inverters

As discussed earlier, the differences among the PWM methods are mainly related to the injection of the zero-sequence-voltage v_z. In the following, the selected PWM methods, which are widely used in researches and industries, and their implementation of zero-sequence-voltage injection method will be discussed.

A. Nearest-Three-Vector Continuous PWM (NTV-CPWM)

The NTV PWM approach can be implemented with a continuous modulation scheme by utilizing two redundant voltage vectors in each area of the sector. This is effectively equivalent to the SVM when using four vectors where the number of switching transitions within one switching cycle is six [4]–[6]. The implementation of the NTV continuous PWM method with the carrier-based PWM approach can be realized by using the zero-sequence-voltage v_z as it is given in the following [4]:

$$v_z = \frac{V_{dc}}{4} - \frac{\max(v_a', v_b', v_c') + \min(v_a', v_b', v_c')}{2} \tag{6}$$

where

$$v_x' = v_x \bmod \left(\frac{V_{dc}}{2}\right), \quad (x = a, b, c) \tag{7}$$

An example of the NTV-CPWM method with CB-PWM implementation is shown in Fig. 5. Generally, this method provides lower THD in the output voltage than the other PWM strategies, resulting in a good trade-off between switching loss

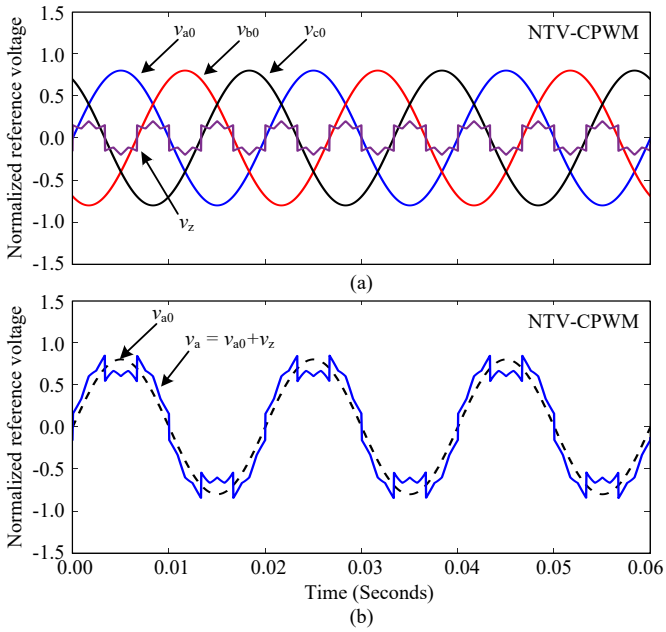

Fig. 5. Nearest-three-vector continuous PWM method: (a) original reference voltages and zero-sequence voltage and (b) modified reference voltages.

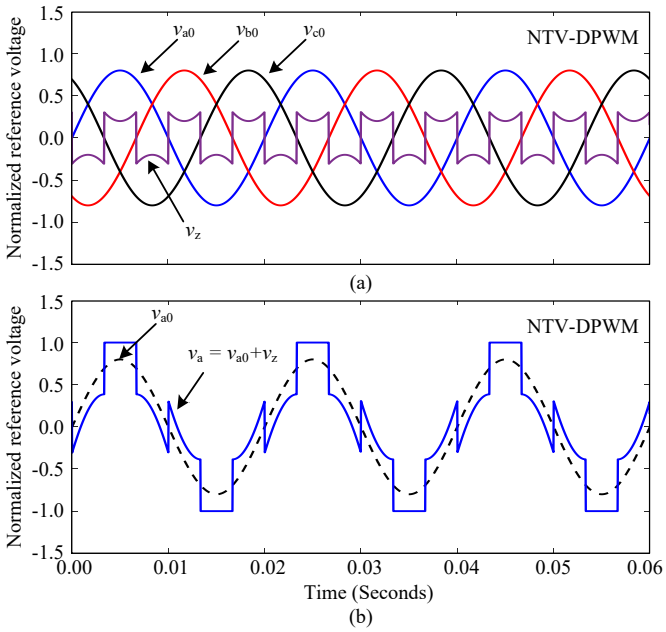

Fig. 6. Nearest-three-vector discontinuous PWM method: (a) original reference voltages and zero-sequence voltage and (b) modified reference voltages.

and power quality. However, a low-frequency oscillation in the NP voltage exists when using the NTV-CPWM method, which may increase the power loss in the dc-link capacitors.

B. Nearest-Three-Vector Discontinuous PWM (NTV-DPWM)

The NTV PWM method can also be implemented with a discontinuous PWM scheme. In this case, only three voltage vectors are used within one switching cycle, and one of the phase voltages is clamped either at positive or negative dc-bus. Since one of the output phases is clamped for 60 electrical degrees, the switching loss can be reduced compared to the NTV-CPWM method [7]. In order to implement the NTV-DPWM method with CB-PWM approach, the zero-sequence-voltage v_z can be determined as given in the following:

$$v_z = \mathrm{s}(\max(v_a, v_b, v_c)) \cdot \frac{V_{dc}}{2} - \max(v_a, v_b, v_c) \quad (8)$$

which is in fact similar to the zero-sequence-voltage used in DPWM strategy for two-level inverters. An example of the reference voltage and the zero-sequence-voltage when using the NTV-DPWM method is shown in Fig. 6.

While clamping the phase voltage can effectively reduce the switching loss, the power quality of the output waveform is also decreased (e.g., resulting in a higher THD), which is a typical trade-off for discontinuous modulation schemes. Moreover, the use of the NTV-DPWM method usually results in a relatively high amplitude of low-frequency oscillations in the NP voltage, inducing a higher power loss in the dc-link capacitor compared to the other PWM strategies due to a high ripple current in the dc-link capacitors.

C. Zero-Sequence-Voltage Injection with NP Voltage Feedback (ZVI-PWM)

The zero-sequence-voltage v_z can also be analytically calculated based on its relationship with the NP current $i_{NP,avg}$ as derived in (1) [19]. In principle, any arbitrary NP current $i_{NP,ref}$ can be controlled by using the zero-sequence-voltage v_z calculated by

$$v_z = \frac{-i_{NP,ref} - (\mathrm{s}(v_a) \cdot v_{a0} i_a + \mathrm{s}(v_b) \cdot v_{b0} i_b + \mathrm{s}(v_c) \cdot v_{c0} i_c)}{\mathrm{s}(v_a) \cdot i_a + \mathrm{s}(v_b) \cdot i_b + \mathrm{s}(v_c) \cdot i_c} \quad (9)$$

and the reference NP current for compensating the dc-link voltage unbalance can be determined following

$$i_{NP,ref} = -C_{dc} \frac{(v_{dc,p} - v_{dc,n})}{T_s} \quad (10)$$

One fundamental challenge with this method is that the information of the zero-sequence-voltage v_z is required in order to determine the sign of the reference voltage, i.e., $\mathrm{s}(v_x) = \mathrm{s}(v_{x0} + v_z)$. However, the sign of the reference voltage $\mathrm{s}(v_x)$ is actually unknown before the zero-sequence-voltage is determined. This can cause an error in the calculation if the sign of the reference voltage changes after the injection of zero-sequence-voltage, i.e., $\mathrm{s}(v_{x0}) \neq \mathrm{s}(v_{x0} + v_z)$. A solution to this problem was proposed in [23], where it is necessary to verify if the estimated zero-sequence-voltage can be used without affecting the signs of the reference voltages. Otherwise, the zero-sequence-voltage needs to be re-calculated.

When using the ZVI-PWM method, the switching sequences are not predefined like those in the NTV PWM approaches, since the zero-sequence-voltage is strongly dependent on the load current and the dc-link voltage unbalance. An example

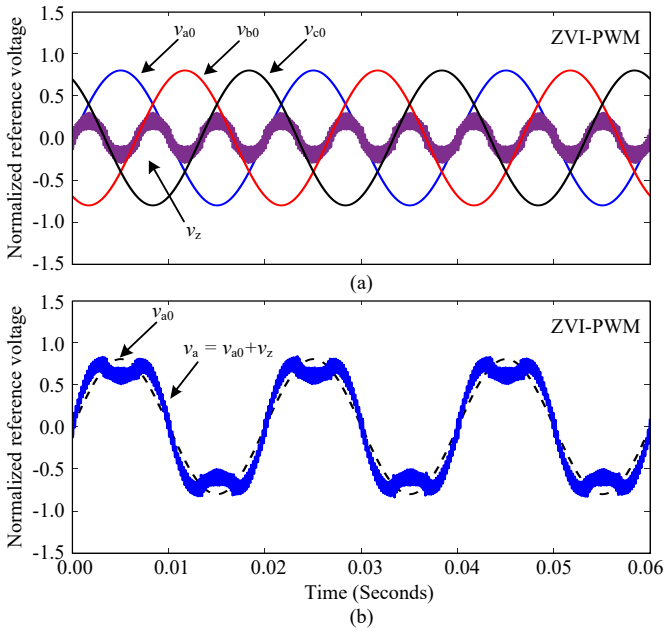

Fig. 7. Zero-sequence-voltage injection with NP voltage feedback PWM method: (a) original reference voltages and zero-sequence voltage and (b) modified reference voltages.

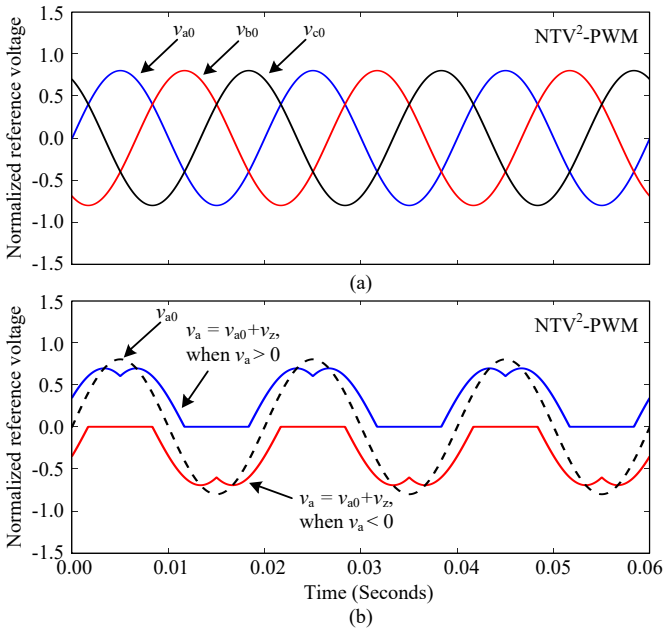

Fig. 8. Nearest-three-virtual-vector PWM method: (a) original reference voltages and zero-sequence voltage and (b) modified reference voltages.

of the reference voltages and the zero-sequence-voltage when using the ZVI-PWM method is shown in Fig. 7. This method utilizes four voltage vectors with six switching transitions over one switching cycle similar to the NTV-CPWM method. However, the low-frequency variation in the NP voltage can be minimized under a certain operating range (e.g., modulation index and power factor) with the ZVI-PWM method [23].

D. Nearest-Three-Virtual-Vector PWM (NTV^2-PWM)

To address the shortcoming of the previous methods, the nearest-three-virtual-vector PWM method which is capable of fully eliminating the NP voltage variation over the full range of operation (e.g., modulation index and power factor) was proposed in [8], [9]. The concept of virtual vectors is realized by utilizing a combination of redundant vectors whose impact on the NP current are complementary. By doing so, the use of each virtual vector in the NTV^2 PWM method essentially result in a zero averaged NP current.

The implementation of the NTV^2 PWM method can be realized with the CB-PWM approach by decomposing each phase reference voltage v_{x} into the reference for the upper v_{xp} and lower v_{xn} carrier as given in the following

$$\begin{cases} v_{\mathrm{xp}} = \frac{v_{\mathrm{x}} - \min(v_{\mathrm{a0}}, v_{\mathrm{b0}}, v_{\mathrm{c0}})}{2}, \\ v_{\mathrm{xn}} = \frac{v_{\mathrm{x}} - \max(v_{\mathrm{a0}}, v_{\mathrm{b0}}, v_{\mathrm{c0}})}{2} \end{cases} \tag{11}$$

where $v_{\mathrm{xp}} > 0$, $v_{\mathrm{xn}} \leq 0$, and $(x = a, b, c)$, as it is illustrated in Fig. 8.

When using the NTV^2 PWM method, the average NP current $i_{\mathrm{NP,avg}}$ is forced to be zero in every switching cycle. On one hand, this ensures that no low-frequency variation in the NP voltage exists. As a consequence, the ripple current and thereby the power loss in the dc-link capacitors are minimized. On the other hand, the number of switching transitions is increased considerably, resulting in an increased switching losses, which is a trade-off when using this PWM method.

TABLE I
PARAMETERS OF THE THREE-LEVEL NPC INVERTER.

Rated output power	69 kW
AC output current (rated)	70 A (RMS)
AC grid voltage	230 V
DC-link voltage	700 V
DC-link capacitance	C_{dc} = 4.1 mF
Filter inductance	L = 0.7 mH
Maximum switching frequency	$f_{\mathrm{sw}} < 20$ kHz
Nominal output frequency	f_g = 50 Hz
Power factor	pf = 1
IGBT power module part number	SKiiP 28MLI07E3V1
DC-link capacitor part number	B43547

V. IMPACT OF PWM STRATEGIES ON RELIABILITY OF DC-LINK CAPACITORS

In this section, the impact of different PWM methods on the power loss and thermal stress of the dc-link capacitors in the three-level inverter will be analyzed.

A. System Parameters

The system parameters of the three-level inverter are based on the evaluation inverter specified in [24], where the key parameters are provided in Table I. The selection of the switching frequency f_{sw} plays an important role in both the

TABLE II
SWITCHING FREQUENCY OF DIFFERENT PWM STRATEGIES.

PWM strategy	Switching frequency f_{sw}	THD of the output current
NTV-CPWM	3150 Hz	4.5 % at I_a = 70 A
NTV-DPWM	5600 Hz	4.5 % at I_a = 70 A
ZVI-PWM	3100 Hz	4.5 % at I_a = 70 A
NTV^2-PWM	7050 Hz	4.5 % at I_a = 70 A

power loss and the power quality performances of the PWM method. In order to ensure a fair comparison among different PWM methods, the switching frequency of the inverter f_{sw} for each PWM method is selected to achieve the same THD level of the output current when operating at the rated output current condition, i.e., THD = 4.5 % at I_a = 70 A (RMS), following Table II. By doing so, all the PWM strategies will have the same power quality and thus the output filter size, while their difference in the power loss in the dc-link capacitors can be compared. Similar approach has also been used in previous research when comparing the power loss in the power devices of the three-level inverter [11].

B. Neutral-Point Voltage Variation

The output current of the three-level inverter i_a when operating at the rated output current and unity power factor (i.e., I_a = 70 A RMS and pf = 1) is shown in Fig. 9, while a comparison of NP voltage variation between different PWM methods is demonstrated by simulation in Fig. 10. In this case, the operating condition of the three-level NPC inverter is kept similar for all the PWM methods (e.g., output power, dc-link voltage, output current THD). It can be observed from the results in Fig. 10(a) and Fig. 10(b) that both NTV-CPWM and NTV-DPWM methods introduce a certain low-frequency oscillation in the voltage across the dc-link capacitors. The amplitude of the NP voltage oscillation is more severe with the NTV-DPWM method. In contrast, both ZVI-PWM and NTV^2-PWM methods can suppress the NP voltage oscillation during operation, where it can be seen that the ripple in the dc-link voltage in Fig. 10(c) and Fig. 10(d) are minimized.

C. Power Loss and Thermal Stress of DC-link Capacitors

A comparison of power loss in the dc-link capacitors among different PWM methods is shown in Fig 11(a), where it can be observed that using the NTV-DPWM method results in a significant power loss in the capacitors. This is due to the high ripple voltage in the dc-link capacitors shown in Fig. 10(b). In that case, the power loss in the dc-link capacitor of the NTV-DPWM method is almost twice as high as the case when the NTV^2-PWM method is applied. It is interesting to see that both the NTV-CPWM and the ZVI-PWM methods result in similar power loss in the dc-link capacitors although the ripple in the dc-link voltage of the ZVI-PWM method is significantly lower. This is mainly due to the fact that the frequency spectrum of the dc-link capacitor current for both PWM methods are quite similar, as their switching frequency

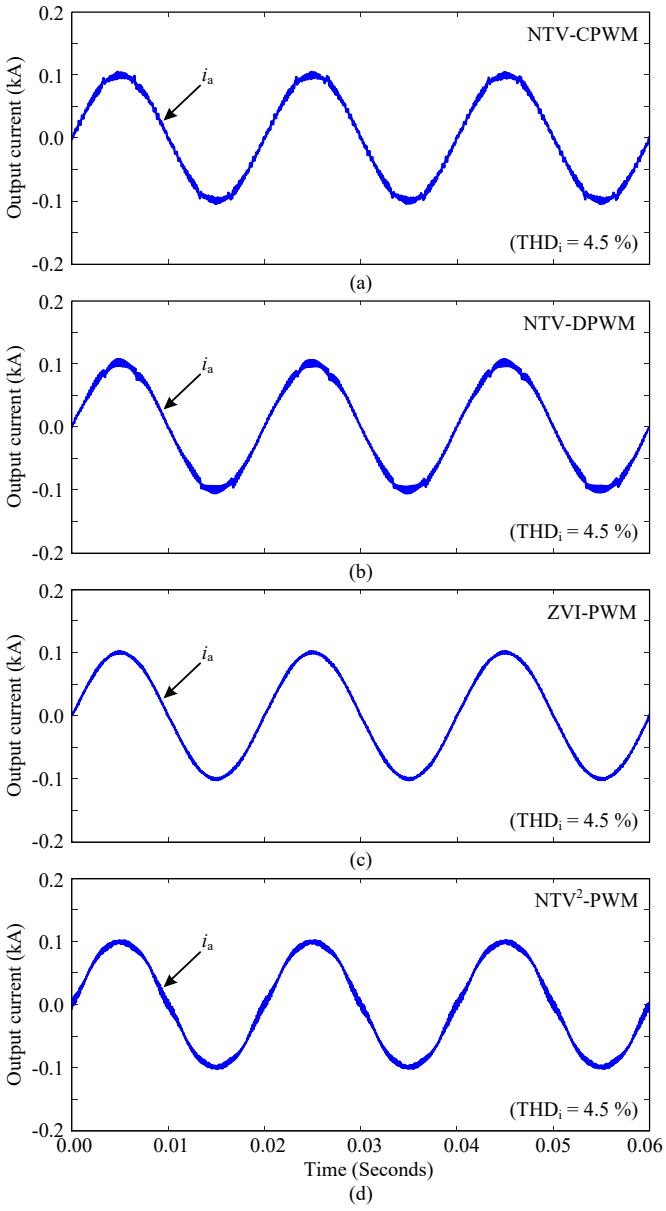

Fig. 9. The output current of the three-level inverter (i.e., i_a) when using: (a) NTV-CPWM, (b) NTV-DPWM, (c) ZVI-PWM, and (d) NTV^2-PWM methods (at I_a = 70 A RMS, V_{dc} = 700 V, V_{ac} = 230 V).

f_{sw} is almost equal. The only difference in the dc-link capacitor current spectrum between the two methods are the low-frequency components, which only exists in the case when the NTV-CPWM method is applied. However, their amplitude are significantly lower than the frequency components close to the switching frequency and their multiples. Therefore, the total power loss in the dc-link capacitors of these two PWM methods are quite similar.

When applying the power loss to the thermal model with the ambient temperature of T_a = 40 °C, the core temperature of the capacitor can be estimated as shown in Fig. 11(b). The difference in the thermal stress of the dc-link capacitors

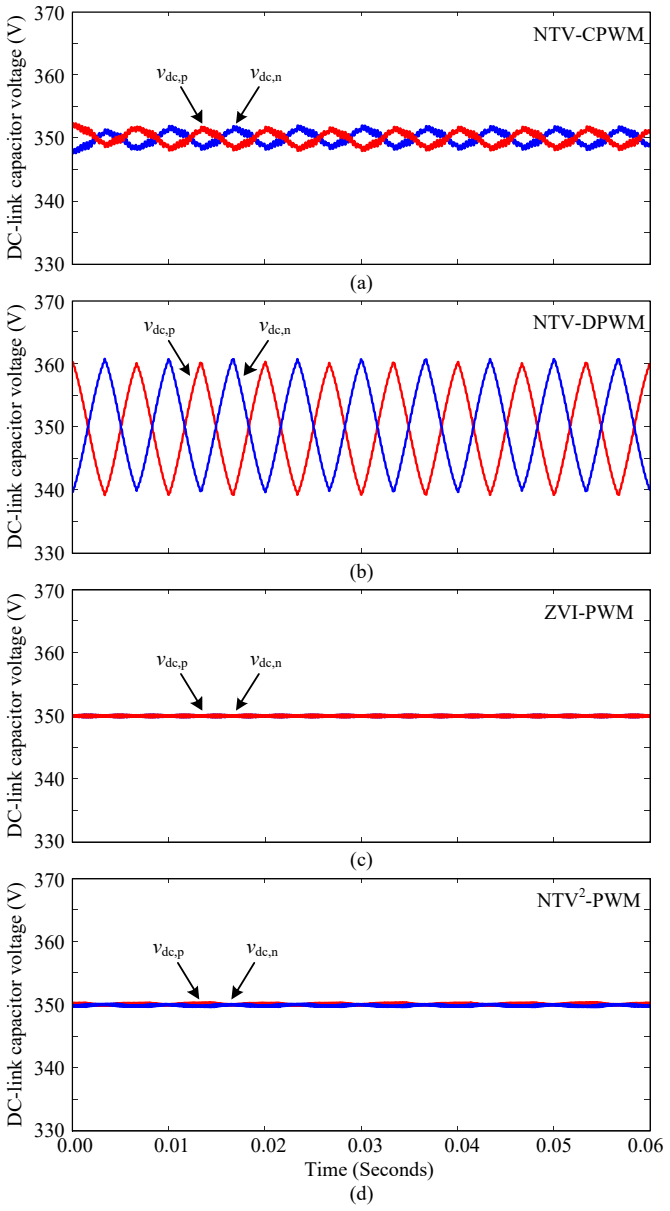

Fig. 10. The voltage across the dc-link capacitors (i.e., $v_{dc,p}$ and $v_{dc,n}$) when using: (a) NTV-CPWM, (b) NTV-DPWM, (c) ZVI-PWM, and (d) NTV^2-PWM methods (at I_a = 70 A RMS, V_{dc} = 700 V, V_{ac} = 230 V).

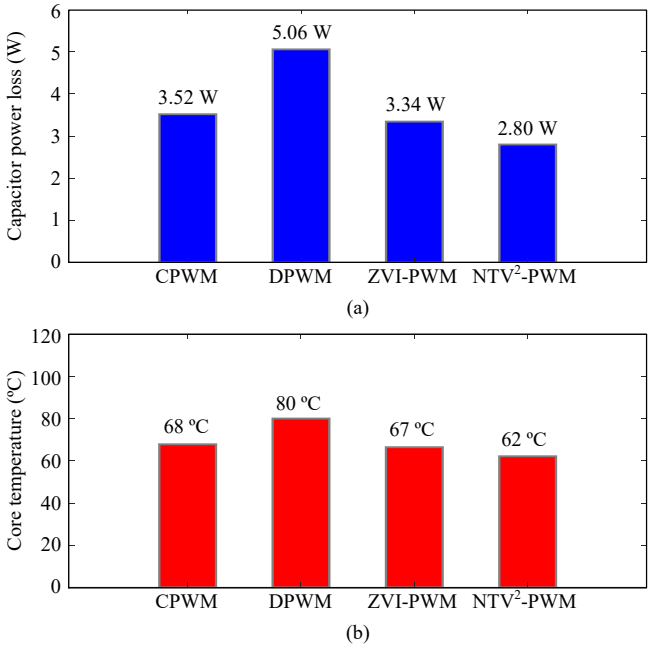

Fig. 11. Reliability performance metrics of dc-link capacitor when using different PWM methods: (a) power loss and (b) core temperature (at I_a = 70 A RMS, V_{dc} = 700 V, V_{ac} = 230 V, T_a = 40 °C).

TABLE III
LIFETIME ESTIMATION OF DC-LINK CAPACITORS.

PWM strategy	Core temperature T_h	Estimated lifetime L_f
NTV-CPWM	67.89 °C	120,000 hours
NTV-DPWM	80.09 °C	30,000 hours
ZVI-PWM	66.50 °C	141,000 hours
NTV^2-PWM	62.19 °C	233,000 hours

follows the same trend as that in the power loss analysis. In this case, there is 18 °C difference in the capacitor's core temperature when using the NTV-DPWM and the NTV^2-PWM methods, which will significantly affect the capacitors' lifetime. In contrast, only 4-5 °C difference in the core temperature can be observed when the NTV-CPWM or ZVI-PWM methods are used compared to the core temperature of the capacitor when the NTV^2-PWM method is applied.

D. Lifetime of DC-link Capacitors

The lifetime of the dc-link capacitors is calculated by applying the thermal stress conditions in Fig. 11(b) to the lifetime model in (5), where the obtained results are summarized in Table III. Notably, the estimated lifetime is based on an assumption of constant loading condition for the inverter according to Fig. 9, in order to simplify the analysis. In practical application, the mission profile of the inverter (e.g., dynamic loading condition) should be applied to more accurately estimate the lifetime of the components [25]. Thus, the results in Table III is only used for a comparative analysis of the dc-link capacitors' lifetime under different PWM methods.

According to the lifetime estimation results, it can be seen that the capacitor lifetime reduces significantly when the NTV-DPWM method is applied. The relatively high core temperature condition results in the shortest lifetime of the capacitors with only 30,000 operating hours. In the case of the NTV-CPWM and the ZVI-PWM methods, the lifetime is increased by more than a factor of 4 due to the lower core temperature condition. Nevertheless, the NTV^2-PWM method is the best solution to ensure a long lifetime for the capacitors, where the estimated lifetime is almost 8 times higher than the case with the NTV-DPWM method.

VI. Conclusion

In this paper, the impact of PWM methods on the reliability of dc-link capacitors in three-level NPC inverters is evaluated. The evaluation is carried out by considering the most commonly used PWM methods. The reliability performances are compared in terms of power loss, thermal stress, and lifetime of the dc-link capacitors. The simulation results have demonstrated that the nearest-three-vector PWM method with discontinuous modulation technique introduces a significant power loss in the dc-link capacitors due to the high amplitude of low-frequency ripple in the dc-link capacitor voltage. In that case, the core temperature of the capacitor can be much higher than the case when using the other PWM methods, and thus reducing the capacitors lifetime under long-term operation. On the other hand, the power loss and thermal stress of the dc-link capacitors are minimized when using the NTV^2-PWM method. Therefore, the reliability of the dc-link capacitors also need to be considered during the selection of the PWM methods in addition to the other performance metrics such as power quality and switching loss, in order to ensure the overall system efficiency and reliability.

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