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Impedance Analysis of Single-Phase PFC Converter in the Frequency Range of 0-150 kHz

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Abstract- This paper investigates the influence of power converter impedance for below 150 kHz frequency range from power quality and EMI performance perspectives. Moreover, feasible solutions to maintain the performance of the power converter are analyzed. For this purpose, the analytical closed loop impedance model of a single-phase PFC converter is derived. Then, a suitable experimental impedance measurement approach and hardware requirement is proposed and the derived closed loop impedance model is validated experimentally at different operating conditions and control bandwidth. The investigations are performed based on different control, filter configurations and operating conditions.

I. INTRODUCTION

Over the years, many studies have been devoted to EMI (Electromagnetic Interference) analysis and modeling of power electronic converters. So far, all the prior-art investigations are dedicated to frequency ranges above 150 kHz as this range is well covered with multitude standards. However, there are no general emission standards for below 150 kHz frequency range (i.e., low frequency EMI). Recently, the number of reported disturbances caused by this emission range is growing. This is due to the extensive penetration of the power electronic converters and Mains Communication Systems (MCS) owing to their technological advancement and significant market price reduction, which has increased the harmonic emission interferences within this frequency range [1]-[7]. Currently, Working Group (WG) 8 and joint working group (JWG) 6 of the IEC Technical Committee 77A (TC77A) is specifically charged with developing consensus compatibility and emission levels in the 2 kHz–150 kHz frequency range.

One of the important issues in this low frequency EMI range, besides the power converter generated emission from pulse width modulation (PWM), is the converter impedance behavior which can cause interaction with new filtering requirement, grid side impedance and even shunt/attenuate the communication signals sent over the power lines [3]. Therefore, there is a need to analyze and study the converter impedance behavior within the 0-150 kHz frequency range. Notably, for below 150 kHz frequency range, the converter impedance behavior is not only dominated by the passive and parasitic components but it is in combination with the power converter closed loop impedance behavior as well. This further highlights the necessity of studying the converter impedance characteristic within this frequency range as it requires

synergy between control and EMI design point of views.

This paper investigates the influence of power converter impedance for below 150 kHz frequency range and the effect of the controller parameters and compensation methods. It is shown that depending on the selected control structure, bandwidth and power level the converter impedance behavior changes which may introduce adverse effect by shunting emissions/signal within 2-150 kHz frequency range. For this purpose, a single-phase boost power factor correction (PFC) converter is selected.

II. CURRENT CONTROL LOOP STABILITY

A PFC converter schematic along with the closed loop control block diagram are shown in Fig. 1. The current control loop stability is not a new topic and has been discussed in literature. In order to emphasize on the importance of sampling frequency on stability and impedance of the converter, the control loop transfer functions are developed. Following Fig. 1(b), one can derive the current closed loop transfer function as below:

$$G_{cli}(s) = \frac{G_{opi}(s)}{1 + G_{ci}(s)G_{id}(s)} \quad (1)$$

Here G_{ci} and G_{opi} represents the current controller and open loop transfer functions respectively. The effect of the G_{LPF} (here $G_{LPF} = 1$) and input voltage feedforward ($k = 0$) are neglected here as their effect will be discussed in the next section.

By including the controller and finding the G_{id} transfer function, G_{cli} can be expanded through (2) – (4).

$$G_{ci}(s) = k_{pi} + \frac{k_{ii}}{s} \quad (2)$$

$$G_{id}(s) = \frac{2U_{dc}(1 + 0.5R_{load}C_{dc}s)}{R_{load}(1 - D)^2 + Ls + R_{load}LC_{dc}s^2} \approx \frac{U_{dc}}{Ls} \quad (3)$$

$$G_{cli}(s) = \frac{\frac{k_{pi}U_{dc}}{Ls} + \frac{k_{ii}U_{dc}}{Ls^2}}{1 + \frac{k_{pi}U_{dc}}{Ls} + \frac{k_{ii}U_{dc}}{Ls^2}} \quad (4)$$

Although the control system is not a true low-pass second order system due to the presence of the open loop zero, the parameters ζ and ω_n as defined in the second order system open loop transfer function (i.e., G_k) shown below can be used to estimate the response of the control system.

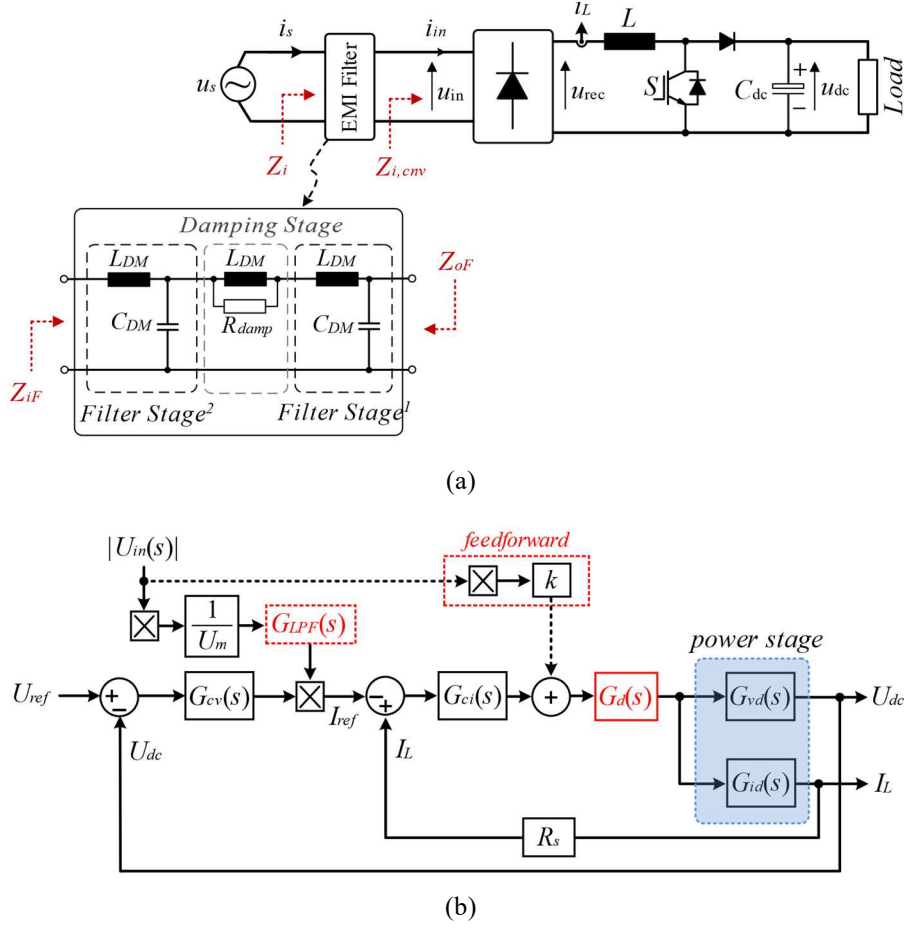


Fig. 1. Block diagram of a single-phase PFC converter: (a) circuit schematic, (b) closed loop control system.

$$G_k(s) = \frac{b}{s^2 + 2\xi\omega_n s + \omega_n^2} = \frac{\frac{b}{s^2}}{1 + \frac{2\xi\omega_n}{s} + \frac{\omega_n^2}{s^2}} \quad (5)$$

By comparing (4) and (5) the current loop control parameters can be found as:

$$k_{pi} = \frac{2\xi\omega_n L}{U_{dc}}, k_{ii} = \frac{\omega_n^2 L}{U_{dc}} \quad (6)$$

The controller bandwidth (BW) can be calculated as:

$$\left| \frac{2\omega_n s + \omega_n^2}{s^2} \right| = 1 \xrightarrow{s=j\omega_{BW}} \omega_{BW} = 2.0582\omega_n = k_{BW}\omega_n \quad (7)$$

By substituting ω_n from (7) into (6) and assuming $\xi = 1$, the PI (proportional-integral) parameters can be calculated based on the controller bandwidth:

$$k_{pi} = \frac{2\omega_{BW} L}{k_{BW} U_{dc}}, k_{ii} = \frac{\omega_{BW}^2 L}{k_{BW}^2 U_{dc}} \quad (8)$$

As it is illustrated in Fig. 1(b), in order to analysis the controller stability, the PWM and calculation delay (i.e., $G_d(s)$) need to be included. Therefore, by including $G_d(s)$ and considering (1) and (5), $G_{opi,new}(s)$ can be defined as:

$$G_{opi,new}(s) = \frac{G_{opi}(s)}{s^2} \frac{e^{-sT_d}}{G_d(s)} \quad (9)$$

In order to satisfy the stability criterion, the phase angle of the open-loop gain $G_{opi,new}(s)$ at the crossover frequency (i.e., $\omega_{BW} = 2\pi f_c$) must be smaller than $-\pi$.

$$G_{opi,new}(j\omega_{BW}) = \left(\frac{-2j}{k_{BW}} - \frac{1}{k_{BW}^2} \right) e^{-j\omega_{BW}T_d} \quad (10)$$

Following (10) the controller bandwidth can be calculated based on the desired phase margin ϕ_{PM} :

$$\angle G_{opi,new}(s)|_{f_c} = (-0.5759\pi - \omega_{BW}T_d) = -\pi + \phi_{PM} \quad (11)$$

Conventionally, the sampling time and the switching frequency are set together in the controller. Following [8] the total delay caused by the triangular PWM and calculation time under single update mode can be considered as $T_d = 1.5 T_s$, where T_s is the sampling time.

It is common to consider 45° phase margin for the inner current control loop to ensure suitable stability margin:

$$-0.5759\pi - \omega_{BW} \frac{3\pi}{\omega_s} = -\pi + \frac{\phi_{PM}}{4} \rightarrow \omega_{BW} = 0.058\omega_s \quad (12)$$

$T_d = 1.5T_s$

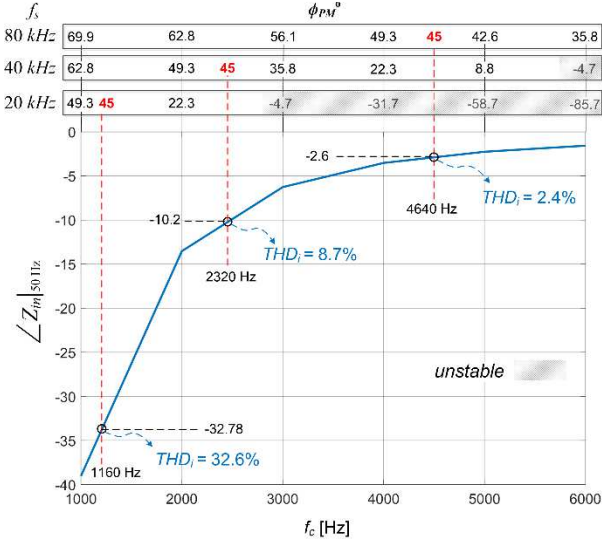


Fig. 2. PFC converter THDi and impedance phase performance versus the control bandwidth at $P_o = 1$ kW following Table I parameters.

If double update sampling is selected $T_d = 0.75T_s$ the bandwidth is extended by a factor of 2 comparing to (12):

$$-0.5759\pi - \omega_{BW} \frac{1.5\pi}{\omega_s} = -\pi + \frac{\pi}{4} \rightarrow \omega_{BW} = 0.1161\omega_s \quad (13)$$

$T_d = 0.75T_s$

Equations (12) and (13) clearly shows the effect of the switching frequency on the controller bandwidth.

To investigate the effect of the controller bandwidth on the performance of the single-switch boost PFC converter the total harmonic current distortion (THDi) and converter impedance at 50 Hz are examined under continuous conduction mode (CCM) operation as shown in Fig. 2. As it can be seen at low sampling frequency which the controller corner frequency (f_c) is limited to about 1 kHz the THDi is quite high and the converter impedance at 50 Hz is away resistive behavior. Increasing the sampling frequency significantly improve the THDi and resistive behavior while achieving acceptable phase margin.

Since the switching/sampling frequency is always limited and considering the adverse effect of low bandwidth current controller on the converter power factor and impedance other approaches need to be utilized to obtain good performance while keeping the bandwidth of the controller within an acceptable phase margin.

III. CLOSED LOOP INPUT IMPEDANCE MODELING

To understand the effect of the system parameters on the power converter impedance and later investigate their influence in the frequency range below 150 kHz the impedance model of the PFC converter needs to be derived analytically.

A. Large Signal Modeling

In [9] the closed input impedance model of a PFC converter is developed based on using large signal modeling approach. However, the effect of the sampling delay was not considered. Fig. 3 illustrates the equivalent

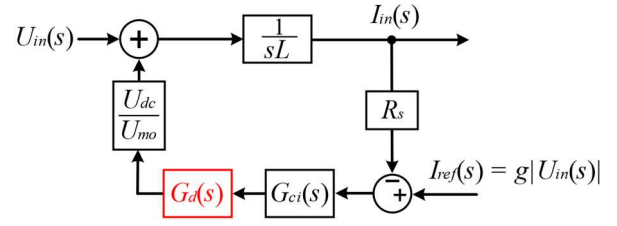


Fig. 3. Block diagram of boost single-phase PFC converter representing high-frequency dynamics including sampling delay effect.

block diagram of boost single-phase PFC converter dynamics. Here, comparing to [9] the effect of sampling delay is included. Therefore, according to Fig. 1(a), following the modeling strategy introduced in [9], the input closed loop impedance of the converter can be determined as (14).

$$Z_{i,cnv} = \frac{U_{in}}{I_{in}} = \frac{sL + \frac{R_s}{U_{mo}}(U_{dc}G_{ci}G_d)}{1 + \frac{1}{U_{mo}}(gU_{dc}G_{ci}G_d)} \quad (14)$$

Here, U_{mo} is the peak amplitude of the modulation signal (typically 1), R_s is the current sensor gain and g is a constant defined as $g = P_{in}/U_{in}^2$ where P_{in} is the input power and U_{in} is the input voltage RMS value.

B. PFC Performance Enhancement

In order to enhance the zero-crossing distortion of PFC converter two compensation approaches are introduced [9], [10]. Both methods are based on phase lead compensation in order to achieve zero phase angle in the converter input impedance at low frequency range. The first approach as illustrated in Fig. 1(b) utilizes low pass filter (LPF). Applying LPF [9], (14) can be updated as below:

$$Z_{i,cnv} = \frac{U_{in}}{I_{in}} = \frac{sL + \frac{R_s}{U_{mo}}(U_{dc}G_{ci}G_d)}{1 + \frac{1}{U_{mo}}(gU_{dc}G_{ci}G_dG_{LPF})} \quad (15)$$

$$G_{LPF}(s) = \frac{1}{1 + \frac{2s}{\omega_{LPF}}} \quad (16)$$

In the second approach the compensation is based on input voltage feedforward [10]. Applying the input voltage feedforward following Fig. 1(b) the input closed loop admittance can be calculated as below:

$$Y_{i,cnv}(s) = \frac{gG_{opi,new}}{1 + G_{opi,new}} + \frac{1/sL}{1 + G_{opi,new}} - \frac{k\left(\frac{U_{dc}}{sL}\right)G_d}{1 + G_{opi,new}} \quad (17)$$

$Y_0(s)$ $Y_1(s)$ $Y_2(s)$

By selecting $k = 1/U_{dc}$, $Y_1(s)$ effect would be ideally cancelled out resulting in a resistive behavior, however this effect is valid until G_d effect is negligible.

Finally, the effect of EMI filter impedance need to be included into the developed $Z_{i,cnv}$ models following Middle

Brook extra element theorem [12] following Fig.1(a) as:

$$Z_i(s) = Z_{iF\infty} \frac{1 + \frac{Z_{oFo}}{Z_{i,cnv}}}{1 + \frac{Z_{oF\infty}}{Z_{i,cnv}}} \quad (18)$$

- $Z_{i,cnv}$: Power converter closed loop input impedance
- $Z_{iF\infty}$: EMI filter input impedance with output port open
- $Z_{oF\infty}$: EMI filter output impedance with input port open
- Z_{oFo} : EMI filter output impedance with input port shorted

IV. IMPEDANCE ANALYSIS

In order to understand the effect of compensation methods, Table I shows the parameters of the system. Regarding the EMI filter, $L_{DM} = 180 \mu\text{H}$, $C_{DM} = 1.4 \mu\text{F}$ and $R_d = 11 \Omega$ are selected. Fig. 4 illustrates the closed loop input impedance model of PFC converter based on (14), (15) and (17) analytical models. As it can be seen the compensation methods are quite effective (see Fig. 4) in improving the low frequency phase response making it close to resistive behavior while a limited bandwidth is utilized. However, there is a big difference in the impedance response below 9 kHz. This shows that depending on the employed control strategy the converter impedance may shunt emission/signal in this frequency range. Above 9 kHz which is beyond the control bandwidth it is the boost inductor L and EMI filter which are dominating the impedance behavior.

TABLE I PARAMETERS OF THE SYSTEM

Symbol	Meaning	Value
U_s	Grid phase voltage	230 Vrms
f_g	Grid frequency	50 Hz
L	Boost inductor	1.9 mH
C_{dc}	DC link capacitor	500 μF
U_{dc}	Output voltage	400 V _{dc}

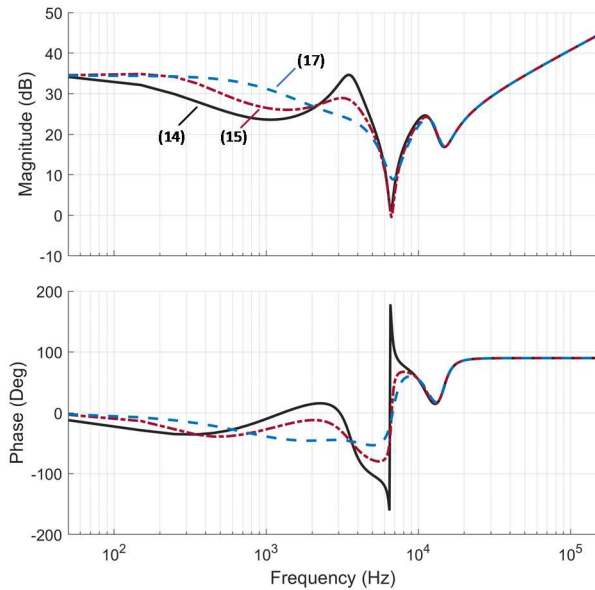


Fig. 4. Effect of phase lead compensation on closed input impedance of PFC converter at 1 kW with $f_s = 40 \text{ kHz}$, with single update sampling and $f_c = 2320 \text{ Hz}$.

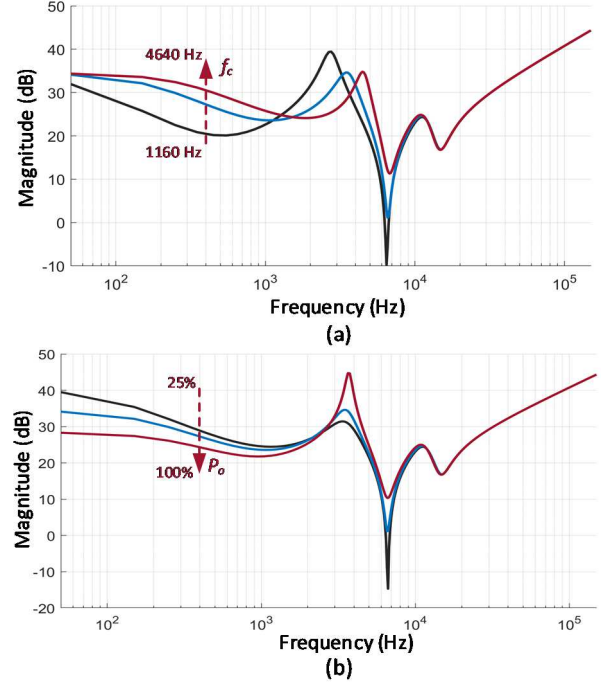


Fig. 5. Input impedance behavior at $f_s = 40 \text{ kHz}$ w/o compensation: (a) f_c variation ($P_o = 1 \text{ kW}$), (b) output power variation ($P_o 100\% = 2 \text{ kW}$, $f_c = 2320 \text{ Hz}$).

Fig. 5 shows the influence of control bandwidth and variation of the output power level on the input impedance. Here the magnitudes are intentionally shown in dB in order to better understand the damping effect of the converter impedance. As it can be seen up to 10 dB difference is achievable based on the selected control parameters and the loading conditions. The changes of the output power affect the input impedance since according to Fig. 3 the reference current is dependent on the input phase voltage.

V. EXPERIMENT

In order to validate the developed analytical models, the closed loop impedance of the power converter need to be measured experimentally. Fig. 6 shows the hardware setup employed for perturbation. Here a voltage injection method is selected using an injection transformer in series with the source voltage. For the perturbation signal a multi-tone signal is selected [11], [13] with 46 frequency points (i.e., $N_{tones} = 46$) covering up to 150 kHz frequency range. The multi-tone signal is analytically described with the following expression:

$$S_{multi-tone}(t) = \sqrt{\frac{2}{N_{tones}}} \sum_{k=1}^{N_{tones}} \sin(\omega_k t + \theta_k) \quad (19)$$

$$\omega_k = 2\pi k f_b \quad \theta_k = \frac{\pi(k-1)^2}{N_{tones}}$$

Notably, in order to prevent from possible interactions with the PFC controller the base frequency f_b is selected as 53 Hz. Fig. 7 shows the time domain and spectrum of the injected multi-tone signal.

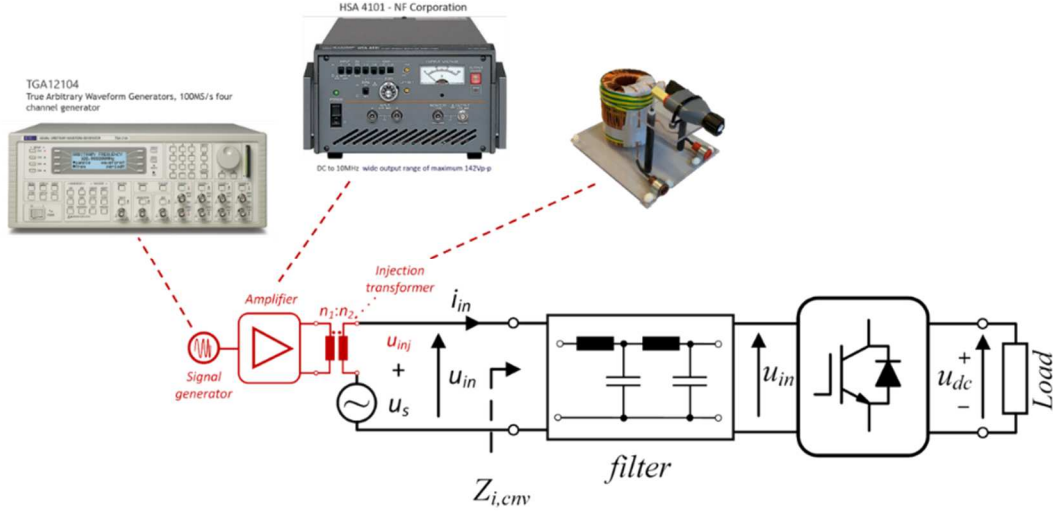


Fig. 6. Perturbation hardware setup for input impedance measurement of power converter.

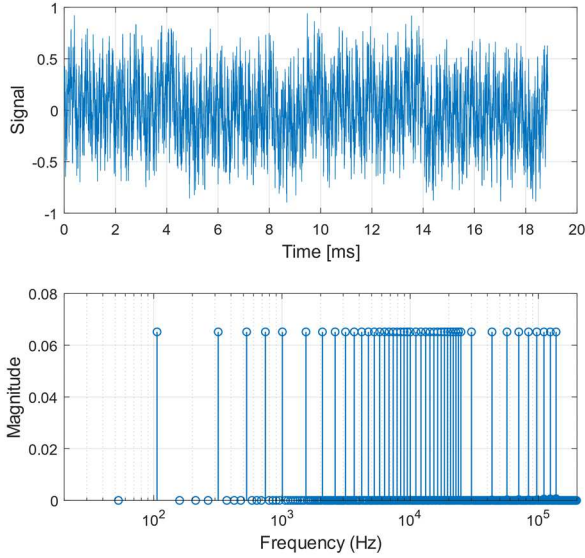


Fig. 7. Injected multi-tone signal with 46 frequency points.

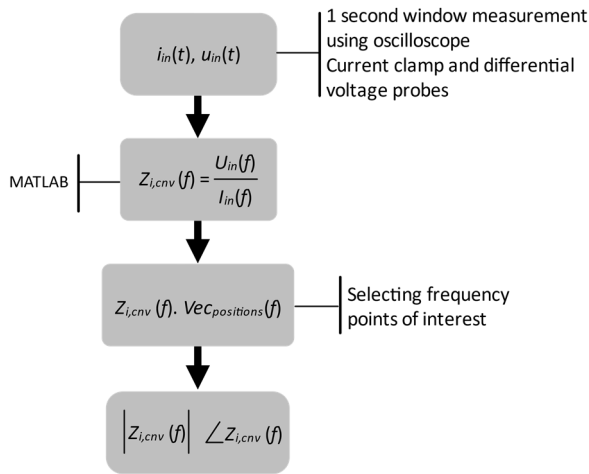


Fig. 8. Flow chart of impedance calculation using time-domain waveform measurements and MATLAB FFT function.

As it can be seen from Fig. 7, more frequency points are injected at higher frequencies in order to better capture the existing resonances in the input impedance.

Fig. 8 illustrates a flow-chart diagram on how the input current and voltages are captured using an oscilloscope and the obtained input impedance in the frequency domain using MATLAB FFT function.

In order to validate the developed closed impedance model, the input impedance of the PFC converter was first measured without any EMI filter. As it is shown in Fig. 9 the obtained experimental measurement has an excellent agreement with the analytical model in (15). As it is expected beyond the bandwidth of the controller the boost inductor L dominates the impedance behavior as the impedance increases and its phase reaches to $+90$ degrees.

To investigate the accuracy of the model a film capacitor $C_{DM} = 1.4 \mu\text{F}$ was placed in front of the PFC converter. Fig. 10 presents the obtained experimental results versus the analytical model in (15) which the C_{DM} impedance is included into the model.

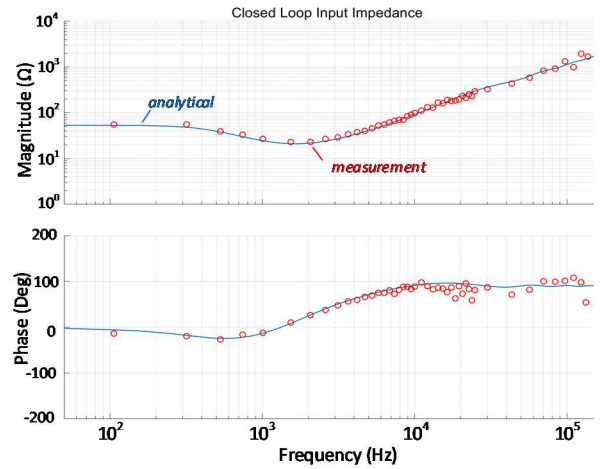


Fig. 9. Obtained experimental results versus analytical model of the PFC converter input impedance following Table I parameters at 1 kW with LPF@ 500 Hz and $f_s = 20$ kHz, $k_{pi} = 0.06$, $k_{ii} = 600$ (BW = 2.5 kHz) without EMI filter.

As it can be seen from Fig. 10, after the resonance frequency the capacitor C_{DM} dominates the impedance behavior as the impedance starts dropping and the phase goes to -90 degrees.

To further validate the accuracy of the developed analytical model in (15), two more experimental measurements including the EMI filter were conducted. Fig. 11 shows the obtained comparative results when the EMI filter as shown in Fig. 1(a) is placed in front of the PFC converter. As explained in (18), applying Middle Brook theorem the effect of the EMI filter is included into the impedance model. As it can be seen, due to the filtering effect of EMI filter the obtained experimental results frequency points matches the analytical model perfectly comparing with the two previous case studies. Here the EMI filter inductance dominates the impedance behavior at higher frequencies.

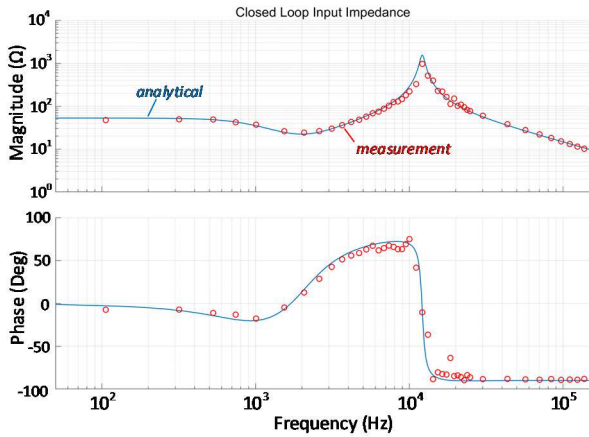


Fig. 10. Obtained experimental results versus analytical model of the PFC converter input impedance following Table I parameters at 1 kW with LPF@ 500 Hz and $f_s = 20$ kHz, $k_{pi} = 0.06$, $k_{ii} = 600$ (BW = 2.5 kHz) with only C_{DM} filter.

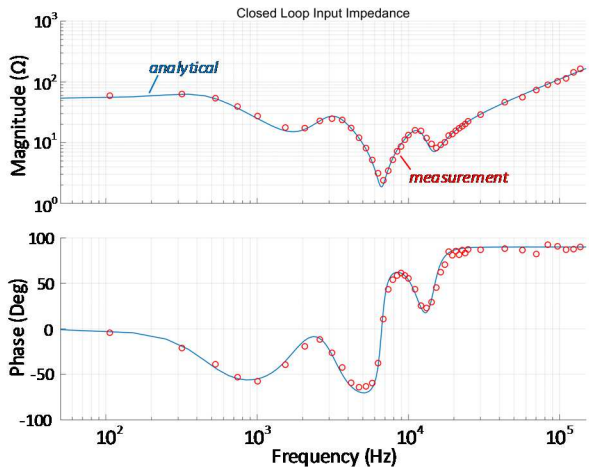


Fig. 11. Obtained experimental results versus analytical model of the PFC converter input impedance following Table I parameters at 1 kW with LPF@ 500 Hz and $f_s = 20$ kHz, $k_{pi} = 0.06$, $k_{ii} = 600$ (BW = 2.5 kHz) with EMI filter.

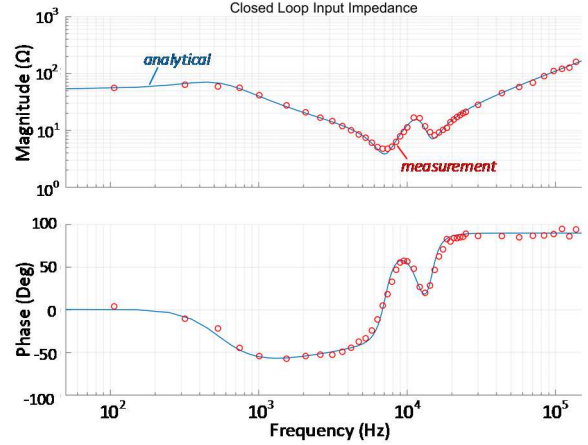


Fig. 12. Obtained experimental results versus analytical model of the PFC converter input impedance following Table I parameters at 1 kW with LPF@ 500 Hz and $f_s = 20$ kHz, $k_{pi} = 0.1275$, $k_{ii} = 903$ (BW = 4.6 kHz) with EMI filter.

Finally, to validate the control parameters effect, the PI parameters have changed by increasing the controller bandwidth. As it is shown in Fig. 12, the analytical model accurately reflects the impedance behavior of the experimental setup.

VI. CONCLUSION

This paper revisited the effect of current controller on the PFC converter input impedance response. Analytical models of the PFC converter input closed loop impedance are developed including the digital control delay, low-pass filter and phase lead compensation. The investigations are focused on below 150 kHz frequency range as considering the new coming standards it is important to understand how the impedance of the power converter can be reshaped in order to avoid its adverse effect on the emission/signals within this frequency range. Furthermore, an experimental measurement setup was developed to validate the input impedance model of the PFC converter. The proposed approach can be applied to any power converter which facilitate to evaluate the power converter impedance behavior.

For future study, the impedance behavior of other common topologies such as three-phase PWM rectifier and voltage source inverter need to be investigated. Furthermore, studying the common mode impedance of the converter besides its differential model impedance would help to get better insight to the converter impedance behavior and its effect of the power converter EMI performance.

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