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Quantitative Feedback Design Based Robust PID Control of Voltage Mode Controlled DC-DC Boost Converter

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***Abstract*—This work addresses the problem of instability occurring in the voltage control mode of a non-minimum phase (NMP) DC-DC boost converter. To solve this instability issue in the presence of uncertainties and the external disturbances, quantitative feedback theory (QFT) is adapted to systematically design a robust proportional integral derivative (PID) controller, which is realized using only sensed output voltage as feedback. The advantages of the proposed PID design using the QFT are: (i) it eliminates the burden of tedious and ad-hoc tuning of PID gains using the conventional PID design approaches, (ii) current measurement is not required, (iii) disturbance dynamics (input voltage and load current variations) are included in the design stage itself, which further enhances the disturbance rejection performance of the output voltage, and (iv) it allows direct design for the non-minimum phase boost converter despite the bandwidth limitations. Extensive simulations and experiments are carried out to validate the efficacy of the proposed PID controller in the presence of the external disturbances and compared its superiority over a conventional PID controller.**

***Index Terms*—DC-DC converter, Disturbance dynamics, PID, Quantitative feedback theory, Voltage regulation.**

I. Introduction

The growing applications of DC-DC boost converters in continuous conduction mode (CCM) have become prevalent in automotive, battery charging applications and so on, whose performance highly depends on the deployed control scheme [1]. The main objective is to always provide constant output voltage across the load despite input voltage and load variations. However, the control strategies for these converters are not robust against model uncertainties as well as the external disturbances. Thus, the closed-loop operation requires a robust control, which not only rejects the disturbance but also handles variations in the system parameters satisfactorily.

Current mode control (CMC) exhibit current loop instability for a duty ratio > 50% regardless of the DC-DC converter [2]. In voltage mode control (VMC), there is no duty ratio restriction. However, VMC operation provides a sluggish dynamic response for boost converters due to the presence of a right half plane (RHP) zero, thereby restricting the closed-loop bandwidth [2]. Hence, operating the non-minimum phase (NMP) boost converter close to the performance limits set by RHP zero is a challenging control task under VMC operation.

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Among the robust control schemes [3-6, 25-27], sliding mode control (SMC) achieves the desired load voltage regulation at the extra cost of current and voltage sensors [3, 4, 5]. The usage of many sensors increases the overall cost and may also affect the reliability owing to fault in any of the additional sensors. Further, the presence of chattering phenomena in SMC prevents it from being used in commercial applications [4]. [6] implemented a model based internal model control (IMC) on NMP boost converter under VMC operation. However, this strategy significantly increases the computational complexity. This serves as a motivation to design a computationally simple robust controller using only the measured output voltage as a feedback, avoiding the usage of many sensors as in SMC [3, 4,5], hybrid control [7], switching control [8] and in feed-forward control [9].

In the literature studies, several control schemes for dc-dc converters have been proposed but a simplified and systematic robust design are yet to be addressed. The PID controllers are employed to control the output voltage of dc-dc converters [6, 14, 15]. PID tuning is a cumbersome task, particularly in the presence of changes in input voltage, load current and parameter variations in the filtering components (L, C). In [15], PID tuning for a NMP boost converter is based on the phase margin obtained from an additional phase sensitive device. The tuning of conventional PID does not deal with a RHP zero and lacks the systematic design to control the output voltage. The PID design without RHP zero for a NMP boost converter exhibits overdamped/sluggish output voltage response [14]. The direct synthesis method based PID design incorporates RHP zero improves the output voltage [16]. Moreover, the conventional PID is non-robust for NMP boost converter using only single output voltage sensor.

The disturbance rejection capability of DC-DC converters can be improved by considering the disturbance dynamics in the controller design stage itself [6]. In the proposed work, a renowned robust control method known as the quantitative feedback theory (QFT) is employed [10-13]. The research works carried out in [10-13] consider the converter model of both minimum phase behavior and NMP boost converter [13]. These studies design the controller using the equivalent minimum phase system obtained with an all-pass filter. Most importantly, these works are entirely simulation studies carried under no real-world plant-model mismatch conditions. Further, it does not account dynamic disturbance models [2, 6] in their design process, which fails to improve the performance. The QFT method incorporates the disturbance models into PID design in a systematic manner (no ad-hoc tuning required). Such a design utilizing the disturbance dynamics in VMC operation is a challenging robust control problem. The effectiveness of proposed robust controller is validated extensively in simulations and verified under experimental conditions. It has been established that the

designed robust PID controller works satisfactorily in the simulation and requires only one voltage sensor for conducting experiments. This constitutes the technical contribution of the paper.

II. QFT Design Procedure for Disturbance Rejection Problem

QFT is renowned for its suitability of implementation in the practical systems [12, 17]. The idea is to design a controller using the loop-shaping technique [18, 19], which reduces the controller gain at high frequency. The specifications are transformed into the so-called "QFT bounds," which is converting the closed loop specification into open loop bounds for subsequent controller design. The QFT bound captures the system uncertainty, which keeps the restriction on the controller design. Then, the loop shaping is carried out in such a way that it satisfies the QFT bounds. To generate the QFT bounds, there exist couple of algorithms based on quadratic inequalities for different specifications (disturbance rejection, set point tracking [17]).The uncertain linear time-invariant (LTI) plant is given by $G(s) \in \{\mathcal{P}(s,\lambda): \lambda \in \boldsymbol{\lambda}\}$, where $\lambda \in R^l$ is a vector of plant parameters whose values vary over a parameter box $\boldsymbol{\lambda}$ given by $\lambda = \{\lambda \in R^l: \lambda_i \in \left[\underline{\lambda_i}, \overline{\lambda_i}\right], \underline{\lambda_i} \leq \overline{\lambda_i}, i = 1., \ldots, l\}$. The open-loop transmission function is defined as $L(s, \lambda) = C(s)G(s, \lambda)$. The objective is to synthesize the controller $C(s)$ such that the following specifications are satisfied

1. Robust stability margin:

$$\left|\frac{C(j\omega)G(j\omega)}{1 + C(j\omega)G(j\omega)}\right| \leq \omega_s \quad (1)$$

2. Robust output disturbance rejection:

$$\left|\frac{1}{1 + C(j\omega)G(j\omega)}\right| \leq \omega_d(\omega) \quad (2)$$

In the above specifications (1-2), ω_s is the stability margin specification (M-circle magnitude corresponding to a desired gain and phase margin), and ω_d is the output disturbance rejection specification. There are two ways to handle NMP system in QFT loop-shaping method [17]. First approach is by performing the loop-shaping design directly on the actual NMP system. Another way is to perform the loop-shaping on the minimum phase part of the actual system by shifting the minimum phase bound with the phase angle of the all-pass factor. In this work, the loop-shaping is carried out directly on the actual NMP system with the disturbance dynamics. This makes the proposed method different from the other methods in [12, 13] which does not account the disturbances in the design stage. With the addition of the disturbance dynamic models, the designed controller is more robust with respect to the disturbances than the design without it [12, 13].

The output disturbance rejection specification (2) with disturbance dynamics (β) becomes as follows:

$$\left|\frac{\beta(j\omega)}{1 + C(j\omega)G(j\omega)}\right| \leq \omega_d(\omega) \quad (3)$$

III. Application for NMP DC-DC Boost Converter

This section deals with the application of QFT design procedure outlined in section II to design a robust PID controller for a boost converter. The circuit diagram of a power stage boost circuit is shown in Fig. 1. The CCM operated DC-DC boost converter parameters are: L = 3.1 mH, R_L = 0.3 Ω, and C =1930 μF, R_c=0.08 Ω. The nominal load resistance is R_n= 90 Ω. Switching frequency is 25 kHz. The input voltage, V_i = 10 V and the output voltage, V_o = 15 V. From [2, 6], the plant model is given as:

$$G_n(s) = \frac{V_o}{1-D}\frac{(1 + CR_C s)\left[R^2(1-D)^2 - (R + R_C)(R_{eq} + Ls)\right]}{\text{den}(s)} \quad (4)$$

where, $\text{den}(s) = R(1-D)[R(1-D) + R_C(1 + C(R + R_C)s] + (R + R_C)(R_{eq} + Ls)(1 + C(R + R_C)s)$

The uncertain transfer function of the boost converter system becomes as,

$$G(s) = \frac{k(a_1 s + 1)(a_2 s + 1)}{(b_1 s^2 + b_2 s + 1)} \quad (5)$$

The nominal parameters of transfer function are, $k = 22.0617$, $a_1 = 1.5440 \times 10^{-4}$, $a_2 = -7.8287 \times 10^{-5}$, $b2 = 1.8847 \times 10^{-3}$, $b1 = 1.3345 \times 10^{-5}$, With an uncertainty of about 10% [20-23], $k \in [19.85, 24.27]$, $a_1 \in [1.3896, 1.6984] \times 10^{-4}$, $a_2 \in [-7.04583, -8.61157] \times 10^{-5}$, $b_1 \in [1.20105, 1.46795] \times 10^{-5}$, $b_2 \in [1.67, 2.073] \times 10^{-3}$.The converter system exhibits a resonant behavior around 274 rad/s.

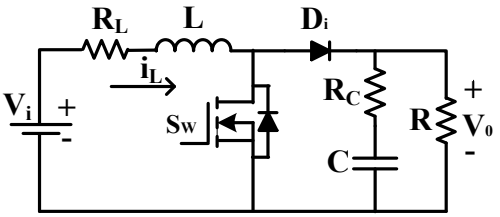

Fig. 1. Circuit diagram of a power stage dc-dc boost converter.

Design Specifications:

A. Robust Disturbance Rejection Problem:

(i). Audio susceptibility disturbance rejection problem: The dynamics of variations in the input voltage w.r.t the output voltage around the neighborhood of the operating point is given by the following transfer function (refer Fig.2):

$$D_a(s) = \frac{v_0(s)}{v_i(s)} = \frac{1.4857(0.0001544s + 1)}{(1.3345 \times 10^{-5}s^2 + 0.0018847s + 1)} \quad (6)$$

The specification for this disturbance rejection problem is (for unit step input, $|V_o| < 0.2$ V for time > 20ms):

$$\left|\frac{D_a(j\omega)}{1 + L(j\omega)}\right| \leq \omega_d(\omega) = \left|\frac{s}{s + 75}\right|_{s=j\omega} \quad (7)$$

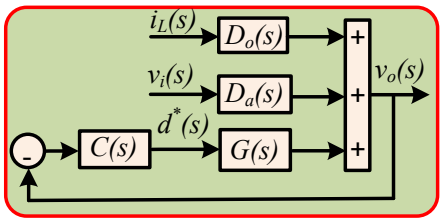

Fig. 2 Feedback control for disturbance rejection problem of Boost converter.

The disturbance rejection specification chosen as the controller should reject the unit step disturbance within 20ms and keep the output voltage variation below 0.2 V. This time domain specification is captured by the tolerance (ω_d). Basically, the closed loop response should reject the effect of the disturbances once it is applied and settle down to its

desired position. So, the tolerance transfer function must have zero at the origin along with the one or more poles such that as time tends to infinity (i.e. Laplace operator $s \rightarrow 0$), the tolerance approaches zero, i.e., $\omega_d(s) = \lim_{s\to 0} \frac{s}{s+a}$.

By selecting just one parameter, the pole in the eq (7), different performance levels of disturbance rejection can be achieved. Further guidelines/practical tips for selecting the output disturbance rejection specification are given in the reference [22, 24].

(ii). Output impedance disturbance rejection problem: The linear perturbations of load current w.r.t the output voltage around the neighborhood of the operating point is

$$D_o(s) = \frac{v_0(s)}{-i_L(s)} = \frac{-0.8567(0.0001544s+1)(0.0080639s+1)}{(1.3345\times 10^{-5}s^2 + 0.0018847s + 1)} \quad (8)$$

Specification for this disturbance rejection is same as in (7).

B. ROBUST STABILITY MARGIN: ω_s=1.2 (Gain margin ≥ 5 dB, Phase margin (PM) ≥ 60^o).

The chosen design frequency set is

$\boldsymbol{\Omega} = 2\pi$ [1,2.5,7.5,10,20,30,50,100,200,274,350, 500,1000,2000,5000,12500] Hz

Note that the frequency set contains the frequencies upto half the switching frequency i.e., 12.5 kHz. The objective of loop-shaping is by adding the poles/zeros (real and/or complex) elements to the nominal plant such that it satisfies the QFT bounds at each frequency. Here, satisfying the bounds means the nominal L should lie on (or) above the open bounds at low frequency and lie outside the closed stability margin bounds at high frequency in order to satisfy the specification constraint. Figure 3 shows the nominal loop-shaping plot for the chosen converter and the designed feedback controller is

$$C(s) = \frac{6.14\,(\frac{s}{117.9}+1)(\frac{s}{150}+1)}{s(\frac{s}{2000}+1)} \quad (9)$$

Hereafter, the designed controller C is denoted as PID_{QFT}.

IV. SIMULATION STUDIES

This section evaluates the performance of the designed PID controllers to control the output voltage of a boost converter. The uncompensated NMP boost converter transfer function given by (4) exhibits a PM of 12^0 at a gain cross over frequency of 1.33 krad/s. For the NMP system, the achievable bandwidth is restricted by the position of RHP zero [2]. To have a fair comparison, a recently used PID controller from [6] is chosen as reference to obtain a PM of about 60^0 and a loop gain crossover frequency of 600 rad/s. In general, such a frequency domain designed PID has been considered for comparisons as delineated in [6, 17]. Following [2, 6, 16], the conventional PID parameters are given as:

$$K_p = 78.4\times 10^{-3}, K_i = 3.34, K_d = 0.245\times 10^{-3} \text{ and } T_f = 0.811\times 10^{-3} \quad (10)$$

K_p,K_i, K_d, T_f denotes the proportional, integral, derivative gains and derivative filter time constant, respectively.

In linear simulation, a step change in the input source voltage is considered to analyze the performance of robust PID controller. The boost converter is operated in steady state with the output voltage V_0=15 V. Here, a step change in the input voltage from 10 V to 7 V is given at t=20 ms. As sown in Fig. 4(b), the proposed robust PID controller reacts quickly in the form of providing slightly large plant input (d*) than the conventional PID controller during the transient time period to the external variation in the input voltage. Due to the quick corrective action with the proposed robust PID controller, the output voltage reaches back quickly to the nominal operating point (V_0=15 V) in comparison to the conventional PID with smaller undershoot, as shown in Fig. 4(a).

For simulation, the complete dynamics of DC-DC boost converter is realized using the SIMSCAPE POWER SYSTEMS toolbox of MATLAB/Simulink. A step change in the input voltage is considered in down direction (10 V to 7 V). During the transient (Fig. 5), the proposed robust PID controller input (d*) provides a quick corrective action than the conventional PID and thereby achieving significant improvements such as fast settling time and reduced over/undershoot, respectively.

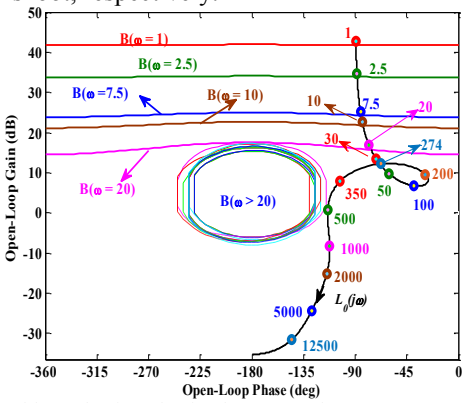

Fig. 3 Nominal loop shaping plot for the DC-DC boost converter.

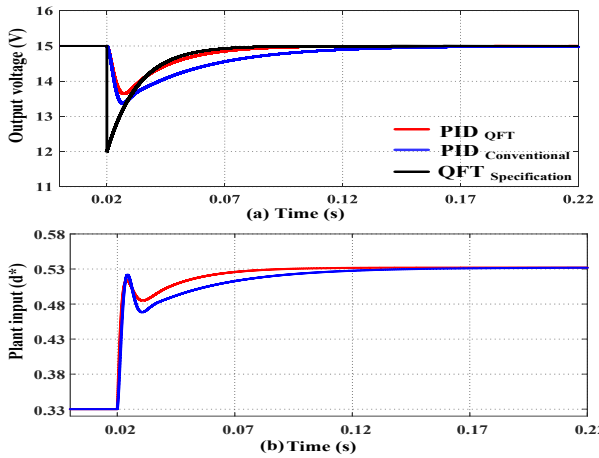

Fig. 4 Regulatory behaviour in linear simulations for a change in input source voltage from 10 V to 7 V: (a) Output voltage, and (b) Plant input (d*).

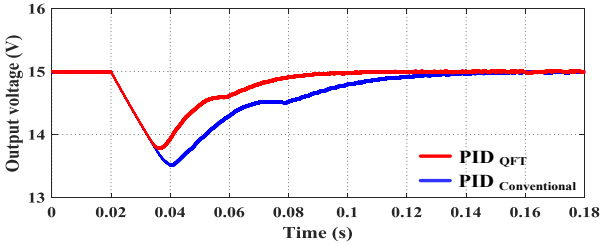

Fig. 5 Comparison of output voltage responses in non-linear simulations for a step change in input source voltage from 10 V to 7 V.

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In the nonlinear simulations, the parameters for both the robust PID and conventional PID controllers are held identical as in linear simulations. The salient feature is that the closed-loop responses obtained here are similar to linear simulations. Hence for both linear and nonlinear simulations, it is observed that if the PID controller is designed by incorporating the disturbance models into the QFT design procedure, then such PID controller provides a quick corrective plant input to reject the effect of the external disturbances and provides robustness.

V. Experimental Verification

To validate the designed PID controller using QFT approach and the observations obtained from the simulations studies, a laboratory prototype of boost converter is built. The experimental setup is shown in Fig. 6. To expedite the experimental verification, dSPACE controller board was used. The prototype converter consists of a controllable MOSFET switch IRF 640, MUR 860 diode and TLP 250 gate driver circuit. To test the feasibility of designed P-I-D controllers on hardware experimental setup, the P-I-D parameters are kept as in the simulations (refer Section IV).

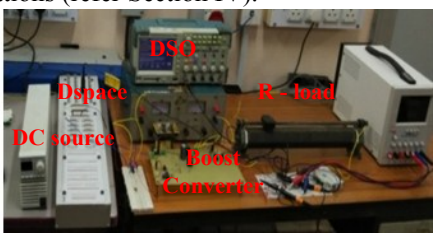

Fig. 6. Laboratory prototype of experimental setup.

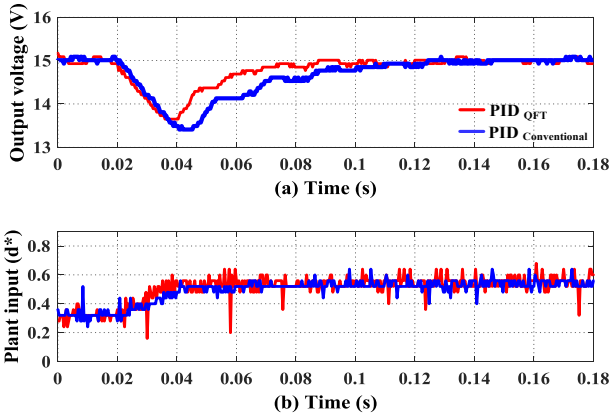

Fig. 7. Regulatory responses for input voltage variation from 10 V→ 7 V at nominal load: (a) Output voltage (b) Plant input.

Scenarios (a-b): A step change in the input voltage from 10 V to 7 V and 10 V to 13 V are given at a nominal load current of 0.166 A. The proposed robust PID controller is able to bring the output voltage quickly to the reference voltage compared to the conventional PID controller as shown in Fig. 7 and 8 with plant inputs (duty ratio).

Scenario (c): For this case, it can be observed from Fig. 9that the conventional PID controller exhibits more deviation and takes long time to reach the steady-state in comparison to the proposed PID. Thereby, the response due to the proposed PID controller shows a significant improvement in the settling time with minimal deviation. The plant inputs for these scenarios are shown in Figs 9(b).

Scenarios (d-e): For a set-point of 18 V and 11 V, a step change in the input voltage is given from 10 V to 7 V and the corresponding closed-loop responses are shown in Fig. 10 and 11. It can be seen that, in both the scenarios, the output voltage reaches quickly with the proposed PID design as compared to the conventional PID. For instance, as shown in Fig. 11(a), the proposed PID reacts quickly with less deviation from the voltage reference i.e. peak deviation of 1.5 V as opposed to 2V in conventional PID and fast settling time of around 0.13 s against 0.18 s in existing PID.

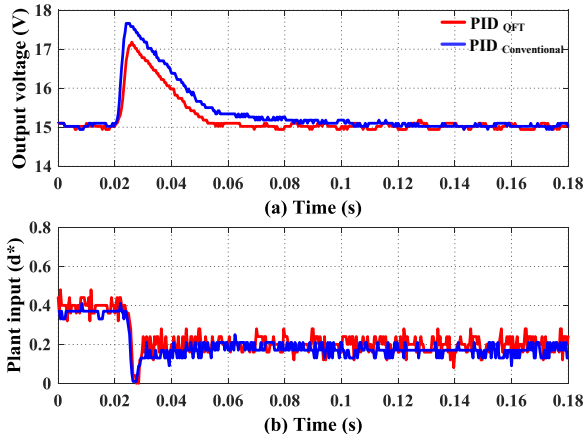

Fig. 8. Regulatory responses for input voltage variation from 10 V→ 13 V at nominal load: (a) Output voltage (b) Plant input.

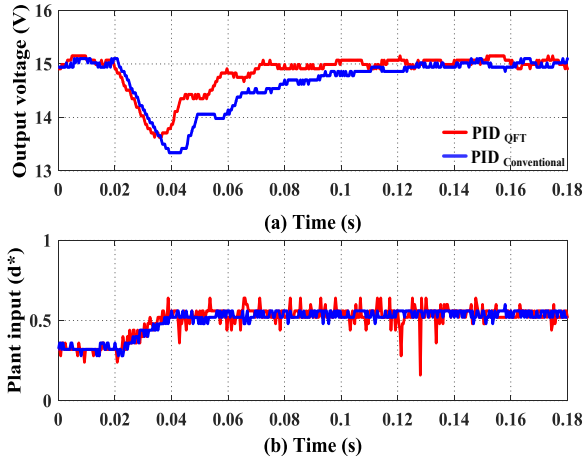

Fig. 9. Regulatory responses for input voltage variation from 10 V→ 7 V at a load current of 0.2A: (a) Output voltage (b) Plant input.

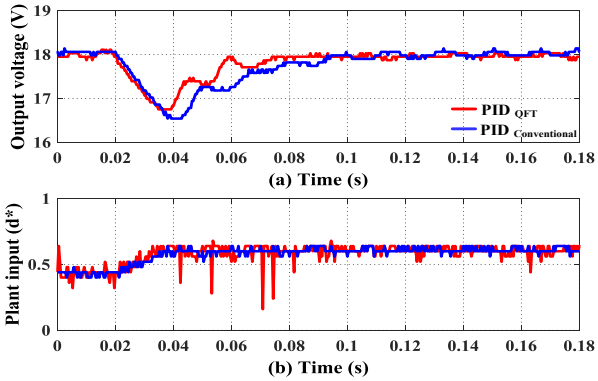

Fig. 10. Regulatory responses for a for input voltage variation from 10 V→ 7 V at a set-point of 18 V: (a) Output voltage (b) Plant input.

VI. CONCLUSIONS

In this work, a computationally simple robust PID controller is designed using QFT to control the output voltage of a NMPDC-DC boost converter under voltage mode control. The controller design for the disturbance rejection is formulated by including the disturbance dynamics of boost type dc-dc converter in the design stage itself. The proposed robust PID controller exhibits improvement in the output voltage response in the presence of uncertainty and external disturbances. The simulation results clearly show that the proposed robust PID controller performs better than the conventional PID controller for various disturbances. Further, the experimental results validate that the closed-loop responses guarantee significant improvement for all the disturbances. As a future scope of work, this work will be extended to deal with the tracking and start-up control problem using only a single voltage sensor.

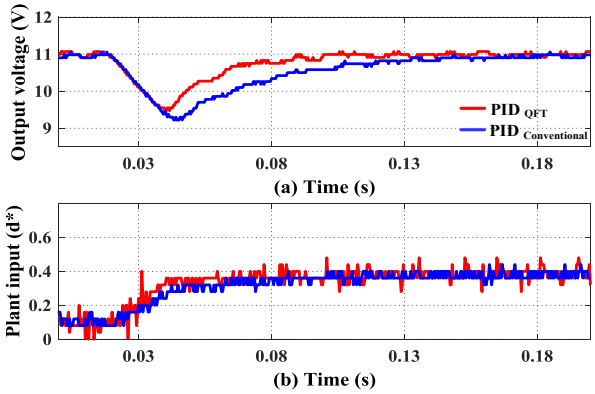

Fig. 11 Regulatory responses for a for input voltage variation from 10 V→ 7 V at a set-point of 11 V: (a) Output voltage (b) Plant input.

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