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Six-Switch Step-up Common-Grounded Five-Level Inverter with Switched-Capacitor Cell for Transformerless Grid-Tied PV Applications

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***Abstract*— Photovoltaic (PV) string inverters with transformerless grid-connected architecture are the most commonly used solar converters owing to their appliance-friendly and cost-effective benefits. A novel circuit configuration for these converters is presented in this study, which seeks to address the shortcomings of most of the conventional topologies such as the problem of leakage current, voltage ratio transformations, and power quality. The proposed structure is based on the series-parallel switching conversion of the switched-capacitor (SC) cell and is comprised of only six unidirectional power switches with a common-grounded (CG) feature. Through the use of the SC cell and the CG connection of active and passive used elements, not only is the number of output voltage level enhanced by up to five but also a two times voltage boosting feature with a single stage operation as well as elimination of the leakage current is acquired. Herein, to inject a tightly controlled current into the grid, a peak current controller approach has been used which can handle both the active and reactive power supports modes. Theoretical analysis, design guidelines, comparative study, and some experimental results are also given to corroborate the feasibility and accurate performance of the proposed topology.**

***Index Terms*— Transformerless inverter, Common ground type, Switched Capacitor module and Grid connected converters**

I. Introduction

For at least the last decade, the transformerless grid-connected photovoltaic (PV) string inverters have been viewed as the most efficient and popular solar inverters. These inverters are supplied by a group of series PV panels (strings) and they can be directly tied to the grid providing high efficiency, low cost and high power density [1-2]. To meet different grid codes and safety standards, various converter and control techniques have been widely rehearsed in both academia and industry [1]-[3].

An efficient structure of a transformerless grid-tied PV inverter should address the leakage current problem caused by the variable common-mode voltage, voltage ratio concern e. g. a compromise between the number of PV main strings and the grid voltage amplitude, and also the power quality issues [3]. The leakage current problem can be removed through the bipolar pulse width modulation (PWM) technique; however, the quality of the injected grid current waveform will be low since the number of the inverter's output voltage levels is only two and therefore the switching/ripple losses are prone to be high [4]. The performance of a PV-based grid-connected system from the leakage current concern can be also improved through enhanced version of the unipolar PWM-based full-bridge (FB) inverter structure. The most important topologies of this category are the conventional four-switch FB-based inverter with a series additional power switch (H5) [5], Highly Efficient Reliable Inverter Concept (HERIC) [6], Optimized H5 (OH5) [7], and different families of H6 structures (six-switch-based topologies) [8-10]. In all the above mentioned topologies, in addition to the higher value of the conduction losses caused by the higher number of ON state power switches, the value of leakage current is also intensified during the reactive power support mode, whereas the HERIC inverter is not theoretically able to pass the reverse current flowing path and handle the reactive power support mode [3].

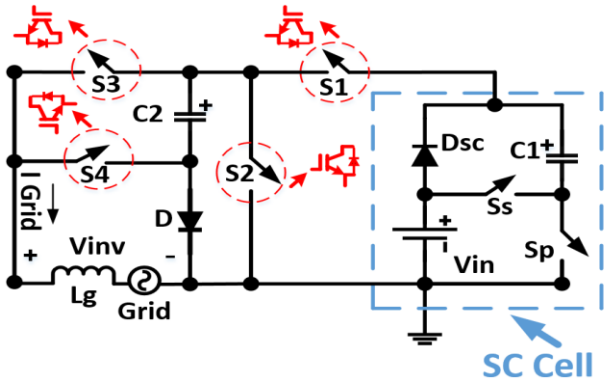

Fig. 1. Circuit schematic of the proposed five-level CG-based transformerless inverter.

The mid-point clamping topologies represent another alternative for mitigating the leakage current problem as well as increasing the quality of the injected current through enhancing the number of output voltage levels. Active neutral point clamp (ANPC) [11-12], T-type [13] and the hybrid flying-capacitor (FC)-based inverters [14] are the most important inverter structures within this category. Like the previous conventional structures, the lack of voltage boosting ability to meet the peak of the grid voltage is the biggest drawback of these topologies; hence an additional dc-dc power processing stage is required for a low voltage PV string. Common-grounded (CG) or doubly-grounded structures are also valuable since the negative terminal of the PV panel is directly tied to the null of the grid and therefore both the dc

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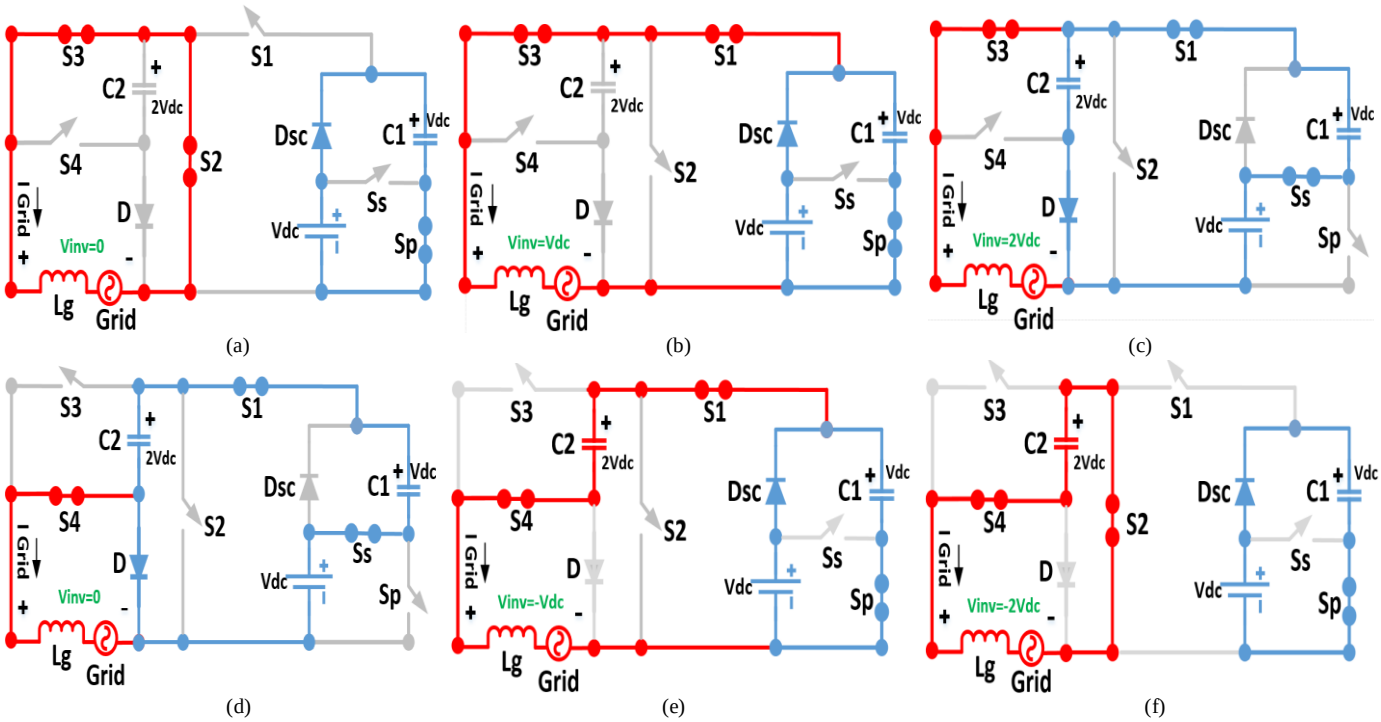

Fig. 2. The current flowing paths of the proposed inverter at (a) the zero-level of the output voltage in the positive half-cycle (b) the first positive level of the output voltage (c) the top positive level of the output voltage (d) the zero-level of the output voltage in the negative half-cycle of (e) the first negative level of the output voltage (f) the top negative level of the output voltage.

and ac sides are clamped to a grounded potential. Regarding this concept, the common mode voltage of the inverter is kept constant and the leakage current concern is removed [3]. Furthermore, the bipolar PWM version of the CG-based inverters has been reported by [15] and [16]. Herein, to provide a unipolar PWM three-level (3L) output voltage, a virtual dc bus is required to provide a path for converting the dc voltage to the ac side during the negative half-cycle of power injection. Kraschny inverter [17], Siwakoti-H inverter [18], the inverters presented in [19] and [20], and the charged-pumped-based inverter [21] are some of the key examples in this category. Here also, the top level of the output voltage is equal to the main-dc link value, so such inverters reflect again a voltage buck feature. A buck-boost version of the CG-based 3L inverter has also been proposed in [22] in which a flying inductor is utilized rather than the capacitor in the virtual dc link. Such a buck-boost feature is yielded through the means of a number of passive and active elements which can in turn affect the overall losses and weighted efficiency.

To increase the power quality and decrease the size of output filters, a few types of multilevel-based CG inverters have been recently put forward. A five-level (5L) CG-based inverter was presented in [23] and a mix of the CG concept with the FC technique is reported in [24]. Both of these structures possess a voltage buck feature and need another dc-dc stage to deal with the low-scaled PV strings.

The aim of this paper is to present a new type of 5L-CG-based transformerless inverter, which can improve the performance of the grid-connected systems by its inherent boosting feature and its unipolar PWM scheme. The proposed topology is constructed on the basis of the switched-capacitor (SC) cell and is able to generate at least five output voltage levels by the contribution of only six unidirectional power switches. Using the series-parallel switching conversion of the SC cell, a double voltage boosting feature can be achieved within a single stage operation. Therefore, a much lower value of the input voltage can be utilized to meet the peak of the grid's voltage. Herein, the concept of the virtual dc link is applied through an extra capacitor located in the outer loop of the SC cell. So, the charging/discharging operation of the capacitors is self-controlled. In addition, a simple peak current controller (PCC) strategy with an appropriate dynamic response is employed to modulate the gate of the involved switches. Through the proposed PCC strategy, a tightly controlled current is also obtained which is able to support both the active and reactive powers of the grid. The rest of this paper is organized as follows: (a) The working principle of the proposed inverter is explained in section II; (b) The PCC operation of the proposed grid-tied system is described in section II; (c) Design guidelines, voltage/current stresses and the conduction losses analysis are given in section IV; (d) A complete comparative study with other existing topologies is presented in section V; and finally the built prototype results are shown in section VI to verify the feasibility and accurate performance of the proposed system.

II. Proposed 5L-CG-based Inverter

The overall configuration of the proposed 5L-CG-based transformerless grid-connected inverter is depicted in Fig. 1. An SC circuit working on the basis of series-parallel switching conversion is used which includes one dc power supply, one power diode, one capacitor and two high frequency series-parallel power switches (S_s and S_p). This SC cell is connected

to four other power switches and another capacitor/power diode to tie to the grid with a simple L-type filter. Regarding Fig. 1, the direction realization of S_s and S_p is also the same as S_4 and S_2, respectively. Considering the high frequency SC cell integrated into the proposed topology, the voltage boosting feature is doubled and five output voltage levels are achieved. Here, the capacitor C_2 acts as a virtual dc link which is similar to what has been used in the conventional approaches [18],[20]. Regarding this circuit architecture, the negative terminal of the input source is directly connected to the null of the grid, which makes a CG feature for the proposed topology. The current flowing paths of different output voltage levels are also illustrated in Fig. 2(a)-(f). Herein, it is assumed that the polarity of the inverter's output voltage and its injected current is the same. Also, the red and blue lines represent the grid-current and the capacitors' charging current flowing paths, respectively. Below, the depicted current flowing paths of the proposed 5L-CG-based inverter during the generation of five distinct output voltage levels are described in detail. Throughout the circuit description, it is assumed that the V_{dc} is the fixed voltage value of the input source.

a) The current flowing path of the zero-level of the output voltage during the positive half-cycle

In relation to Fig. 2(a), to make the zero-level of the proposed inverter's output voltage during the positive half cycle, three power switches named as S_p, S_2 and S_3 must be ON. So, regarding the paralleled ON state switch in the SC cell (S_p), the capacitor C_1 is charged to the input dc voltage value (V_{dc}) through the forward-biased SC cell's diode (D_{SC}) in every direction of the grid current, while C_2 is disconnected from the grid.

b) The current flowing path of the first positive level of the inverter's output voltage

Following this, the first positive level of the output voltage ($+V_{dc}$) can be made just by turning the state of two power switches (S_1 and S_2) in compare to the described zero level of the output voltage in the positive half cycle. As shown in Fig. 2(b), the power switch S_p must be again ON to keep on the charging operation of C_1, while V_{dc} can be transferred to the inverter's output through the turned ON switches S_1 and S_3. Here, C_2 is again excluded from the grid current flowing path since its upcoming charged voltage makes the integrated power diode D reverse-biased.

c) The current flowing path of the top positive level of the inverter's output voltage

In order to create the top positive level of the output voltage ($+2V_{dc}$), Fig. 2(c) should be considered. In this case, the series power switch of the SC cell (S_s) must be ON; so C_1 is discharged (or charged) if the injected grid's current polarity is to be positive (or negative). Therefore through the ON state contribution of S_1 and S_3, the sum of the input voltage value and the charged voltage across the C_1 is converted to the output and the voltage level of $2V_{dc}$ is thereby created. Here, since the clamped voltage across the power diode D is positive; it operates in the forward-biased condition. Thus, depending on the injected grid's current polarity, the C_2 can be charged to the output voltage of the SC cell ($2V_{dc}$).

d) The current flowing path of the zero-level of the output voltage during the negative half-cycle

Regarding Fig. 2(d) and during the operation of the proposed inverter in the negative half-cycle, the zero level of the output voltage can again be generated with a different current flowing path. Here, through the ON state power switch S_s in the SC cell, the output voltage of the SC cell will be equal to $2V_{dc}$. So, depending on the grid current direction, the C_1 can be charged or discharged. Having taken the charged voltage of C_2 ($2V_{dc}$) and considering the aim of S_1, the power diode D is in the state of being forward-biased again; so, the zero level of the inverter's output voltage can be generated once again through the contribution of D and S_4, while in respect of the grid current direction, C_2 can be charged (or discharged) to $2V_{dc}$.

e) The current flowing path of the first negative level of the inverter's output voltage

Having taken Fig. 2(e) into account, the first negative level of the output voltage ($-V_{dc}$) can be built by the contribution of C_2 and the input dc voltage source value. Considering the charged voltage value of C_2 in the previous stages ($2V_{dc}$), the power diode D will be in reverse bias; so by the aim of S_p, the output voltage of the SC cell will be equal to V_{dc}. Therefore, through the turned ON switches S_1 and S_4, the voltage level of $-V_{dc}$ will be converted to the output, while irrespective of the grid current direction, C_1 will be charged to V_{dc} once again.

f) The current flowing path of the top negative level of the inverter's output voltage

Finally, to make the top negative level of the proposed inverter's output voltage ($-2V_{dc}$), Fig. 2 (f) must be taken into account. As is clear from the depicted current flowing path, although C_1 can be charged to V_{dc} in every instance of the grid's current polarity through the ON state power switch S_p, the SC cell will be disconnected from the grid by the turned OFF power switch S_1. So, in this case, the output power is directly supplied by the sole contribution of C_2 alongside the aim of the ON state power switches S_2 and S_4.

From the above descriptions, it is clear that the charging/discharging operation of the C_2 in the whole operation in the negative half cycle depends on the grid

current direction. It can also be concluded that through the series-parallel switching conversion of the switches, both the capacitors are self-balanced on V_{dc} and $2V_{dc}$ at the end of one full cycle of the grid-frequency.

As is also evident, the maximum value of the inverter's output voltage is $2V_{dc}$ which reflects the double-voltage boosting feature of the proposed topology. Accordingly, to meet the peak voltage value of the grid, a much lower value of the input voltage (at least 160 V for a 311 V-based maximum voltage of the grid) is required. Also, considering the states of the switches, it is apparent that two of the four involved switches (S_3 and S_4) are only ON in the positive and negative half-cycle of the grid's frequency, respectively. So, they are switched on the basis of the grid's frequency while the other four involved switches are working through a high switching frequency modulation.

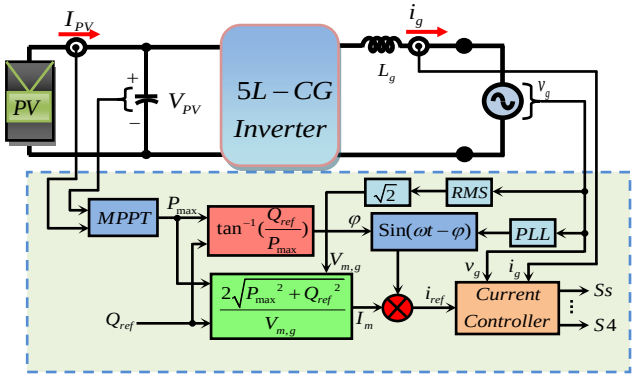

Fig. 3. The overall block diagram of the controlled system.

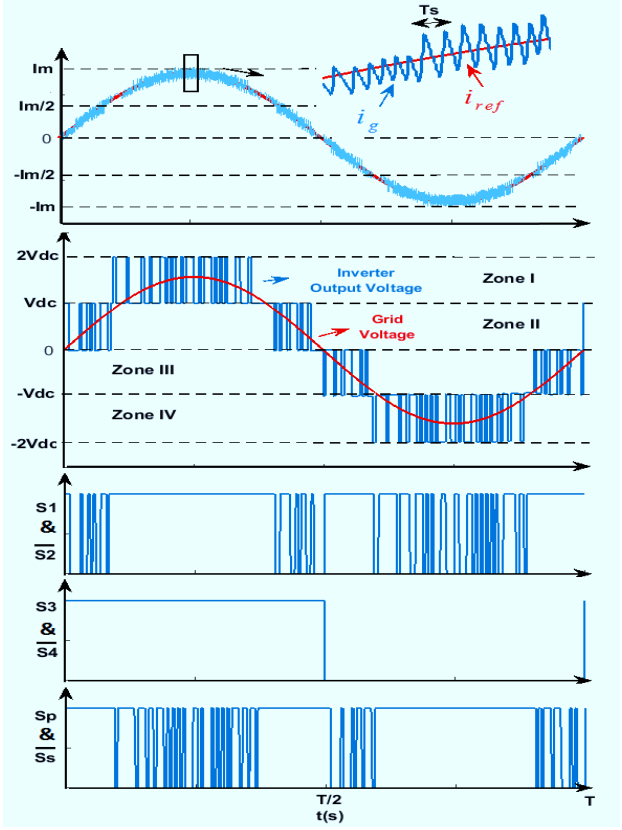

Fig. 4. A typical operation of the proposed PCC technique and the corresponding output voltage with gate switching pulses waveforms.

Table I. Switching States and PCC Description of the Proposed Five-Level CG-Based Inverter

Zone No	PCC Description	ON State Switches	Inverter Output Voltage
I	$i_g \le i_{ref}$	S_3 , S_1 , S_s	$2V_{dc}$
	$i_g \ge i_{ref}$	S_3 , S_1 , S_p	V_{dc}
II	$i_g \le i_{ref}$	S_3 , S_1 , S_p	V_{dc}
	$i_g \ge i_{ref}$	S_2 , S_3 , S_p	0
III	$i_g \le i_{ref}$	S_4 , S_1 , S_s	0
	$i_g \ge i_{ref}$	S_4 , S_1 , S_p	$-V_{dc}$
IV	$i_g \le i_{ref}$	S_4 , S_1 , S_p	$-V_{dc}$
	$i_g \ge i_{ref}$	S_4 , S_2 , S_p	$-2V_{dc}$

III. Implementation of the Proposed PCC

A PCC-based technique is used in this study in order to trigger the gate of power switches and also regulate both the active and reactive injected powers of the grid. Generally, the main objective of the transformerless grid-connected inverters is to inject a tightly controlled current into the grid. Among the various control and modulation strategies, the current controller techniques have been more popular than the voltage-oriented control (VOC) schemes since they possess a very fast and robust performance with almost zero steady state errors under various dynamic conditions of the local grid [25]. Here, the proposed PCC strategy is a derived version of the conventional hysteresis current controller (HCC) techniques, which can properly track the reference waveform of a controlled system without any extra bands and just by comparing the instantaneous value of the grid's current (i_g) with the reference one (i_{ref}). So, the overall complexity and computational burden of a controlled system for a multilevel-based grid-tied inverter can be reduced through the proposed PCC technique. In this case, the single inductor of the inverter's filter (L_g) plays an important role since it can provide the sufficient phase difference between the inverter's output voltage and the grid's voltage to inject power into the grid. The overall block diagram of the proposed controlled system is illustrated in Fig. 3. Here, it is supposed to have a PV panel with a maximum power point tracker (MPPT) block at the input side of the proposed inverter. As can be seen from Fig. 3, the peak value of the reference current (I_m) for the proposed PCC technique can be obtained through the MPPT block. This value depends on the maximum captured power from the PV panel as $P_{\max}$ and the supposed reactive power which is intended to be injected into the grid (Q_{ref}). Also, a phase-locked loop (PLL) block is needed, which can provide the synchronous phase of the grid voltage for the current reference waveform.

To properly address the operating principle of the proposed PCC technique, a measured value of the grid or inductor's current is also required as can be realized by Fig. 3. The proposed PCC technique is on the basis of a sampling time (T_S), which can reflect the maximum switching frequency (

$1/2T_S$) of the high frequency switches (S_s, S_p, S_1 and S_2). The PCC block in the proposed controlled system demands two other input data. The first one is related to the i_g ; so by comparing the desired reference and measured currents within the sampling frequency, the instant slope and value of the inductor's or grid's current are identified.

To generate all the five output voltage levels at the inverter's output, a definition of the working zones depending on the instant location of the grid's voltage ($V_g(t)$) with respect to the input voltage (V_{dc}) is also needed as the second input data of the proposed PCC. Such working zones are defined as: $V_{dc} \le V_g(t) \le 2V_{dc}$ for zone I, $0 \le V_g(t) \le V_{dc}$ for zone II, $-V_{dc} \le V_g(t) \le 0$ for zone III, and $-2V_{dc} \le V_g(t) \le -V_{dc}$ for zone IV. Regarding the instant slope of the measured grid or inductor's current and considering the defined working zones, the switching pulses of the proposed five-level CG-based inverter are obtained.

Considering a low value of the sampling time as a role example, the operation of the proposed PCC technique which serves to provide five-output voltage level for the proposed topology within four defined zones is illustrated in Fig. 4.

Herein, the typical waveforms of the inverter's injected current (i_g), desired reference current (i_{ref}), inverter's output voltage, the grid voltage, and the gate pulses of the involved power switches are depicted.

To further clear the modulation process of the switches, Table I can also be taken into account. From this Table and Fig 4, it is revealed that once the instant value of i_g exceeds the reference current in each working zone, the slope of the grid's current will have an upward trend. So, the PCC generates the lower output voltage level of each working zone ($V_{inv,low}$) to meet the volt-second balanced principle of the filter's inductor. Also, whenever this value is less than the reference, the upper output voltage level of each working zone($V_{inv,up}$) will be made.

Considering the two-time boost factor of the proposed five-level CG-based inverter and assuming the fixed dc link voltage is V_{dc} after the MPPT operation, the average value of the inverter's output voltage in each working zone can be expressed as (1):

$$(V_{inv,up})d_1(t) + (V_{inv,low})d_2(t) = 2d(t)V_{dc} \quad (1)$$

Where, $d(t)$ is the switching duty cycle and can be written as (2).

$$d(t) = D_m Sin(\omega t) \quad (2)$$

Here, D_m is the corresponding modulation index related to the maximum amplitude of the grid's voltage and the fixed value of the dc link voltage. Also, $d_1(t)$ and $d_2(t)$ are respectively denoted as the normalized dwell time of the upper and lower inverter's output voltage level in each working zone. Here, ω is the angular term at the grid frequency. For the sake of simplicity, such values are normalized by T_S. Therefore, the following equation can be written for them:

Table. II. Definition of the Involved Switches' Duty Cycle

Respective Switch	Zone I	Zone II	Zone III	Zone IV
S_1	1	$2d(t)$	1	$2d(t)+2$
S_2	0	$-2d(t)+1$	0	$-2d(t)-1$
S_3	1	1	0	0
S_4	0	0	1	1
S_s	$2d(t)-1$	0	$2d(t)+1$	0
S_p	$-2d(t)+2$	1	$-2d(t)$	1

$$d_1(t) + d_2(t) = 1 \quad (3)$$

Since, four different working zones have been defined, if we consider (1) and (3), the values of $d_1(t)$ and $d_2(t)$ in each are different and can be taken from (4) to (7):

$$\begin{cases} d_1(t) = 2d(t) - 1 \\ d_2(t) = 2 - 2d(t) \end{cases} \xrightarrow{for} Zone\ I \quad (4)$$

$$\begin{cases} d_1(t) = 2d(t) \\ d_2(t) = 1 - 2d(t) \end{cases} \xrightarrow{for} Zone\ II \quad (5)$$

$$\begin{cases} d_1(t) = 1 + 2d(t) \\ d_2(t) = -2d(t) \end{cases} \xrightarrow{for} Zone\ III \quad (6)$$

$$\begin{cases} d_1(t) = 2 + 2d(t) \\ d_2(t) = -2d(t) - 1 \end{cases} \xrightarrow{for} Zone\ IV \quad (7)$$

Therefore, regarding the switching states of the proposed topology as given in Table I and considering the above-mentioned relations, the corresponding duty cycle of six involved power switches in each of the working zones are summarized based on Table II.

IV. Losses, Design Guidelines and Voltage/Current Stresses Analysis

The aim of this section is to give some descriptions about the conduction losses of the involved power switches as well as the design guidelines of the passive involved components and the voltage/current stresses of the switches. In this case, the switching loss analysis of the switches is similar to other research studies and can be found in the literature [21-22].

A. Conduction Losses

As for the first step, the proposed inverter's output voltage waveform emphasizing on the described dwell times, the current stresses of the involved switches, the passing current of capacitors and a typical waveform of the injected grid's current within a cycle of the grid's frequency (T) are shown in Fig. 5. As it is clear, the time intervals of $[t_1 - 0]$ and $\left[\frac{T}{2} - t_2\right]$ belong to the second working zone, while $\left[t_3 - \frac{T}{2}\right]$ and $[T - t_4]$ represent the third working zone. Also, the first and fourth working zones' time intervals are respectively indicated as $[t_2 - t_1]$ and $[t_4 - t_3]$. Considering the transition time between the first and second working zone, the instant value of t_1 is equal to (8). So, the other values of t_2, t_3 and t_4 can be obtained in respect to t_1.

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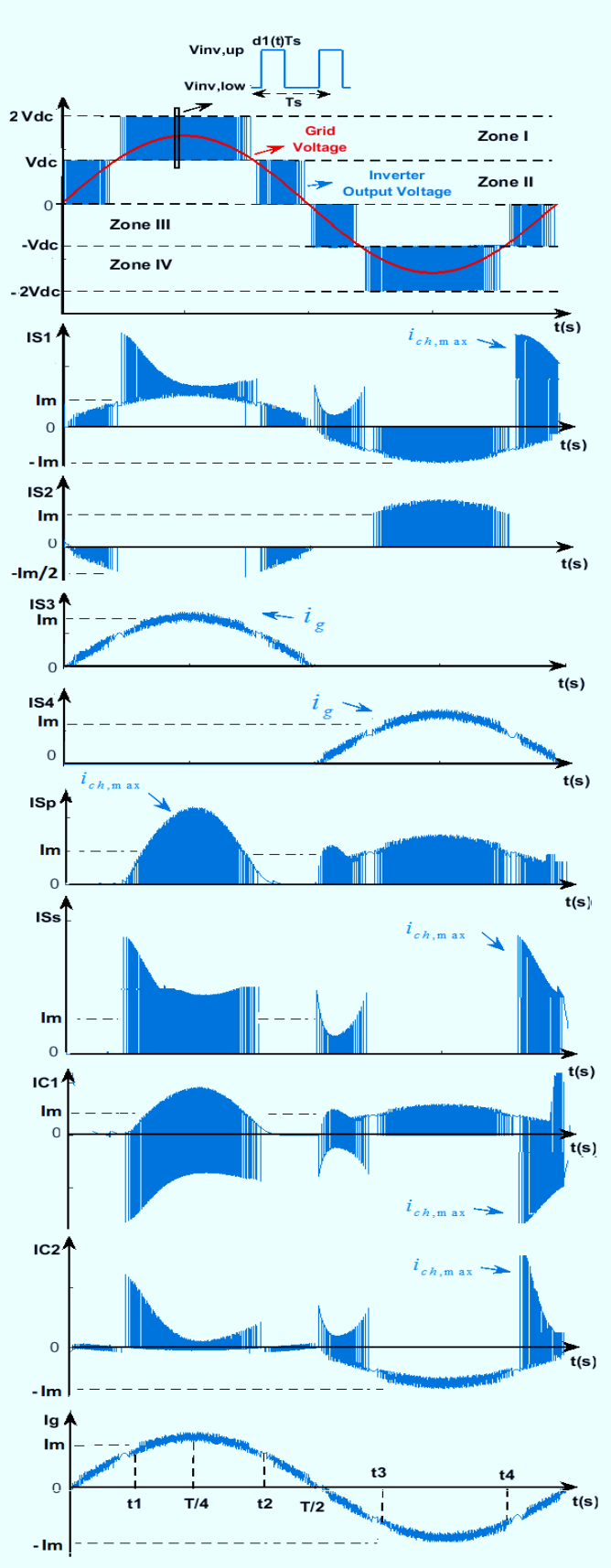

Fig. 5. A typical current stress waveform of the involved power switches and capacitors along with the step-wise inverter's output voltage and the injected grid current.

$$D_m \sin(\omega t_1) = 0.5 \rightarrow t_1 = \frac{1}{\omega} \times \sin^{-1}(\frac{0.5}{D_m}) \quad (8)$$

Contemporary, the conduction loss of each of the involved power switches over a full cycle of the grid's frequency is obtained as (9):

$$P_{C-Si} = \frac{1}{T}\int_0^T \left|V_{on} d_{Si} i_g(t)\right| dt \quad i = 1,2,...,6 \quad (9)$$

where, d_{Si} is the duty cycle of each switch and can be found from Table II. Also, V_{on} is the ON state voltage drop across each power switch and the injected grid current's function can be supposed to be:

$$i_g(t) = I_m \sin(\omega t) \quad (10)$$

Therefore, regarding Fig. 5 and Table II , the conduction loss of a typical power switch such as S_1 can be taken by (11).

$$P_{C-S1} = \frac{V_{on} I_m}{T} \begin{pmatrix} 2\times \int_0^{t_1} \left|(\sin(\omega t)\right| dt + \int_{t_1}^{t_2} \left|(2d(t))\sin(\omega t)\right| dt \\ + 2\times \int_{T/2}^{t_3} \left|(\sin(\omega t)\right| dt + \int_{t_3}^{t_4} \left|(2d(t)+2)\sin(\omega t)\right| dt \end{pmatrix} \quad (11)$$

Using (2) into (11), the obtained value of the conduction loss of S_1 will be about $V_{on} I_m / 2\pi$ and the corresponding conduction loss values of other involved power switches can also be in a similar way. Herein, two power switches named S_1 and S_s are put into the charging path of C_2 during the zero-negative and the top positive output voltage level generation as can be realized by Fig.2 (d) and (c). Also, the power switch S_p is affected by the charging current of C_1 during the negative output voltage levels, the first positive and the zero positive output voltage level generations. These process of the charging currents may cause some extra power losses in the involved power switches.

Regarding such observations, S_1 and S_s experience the highest value of the current stresses ($I_{ch,\max}$) caused by the charging current of C_2. Here, although S_3 and S_4 are involved into the charging path of C_2 during the top positive level and zero-negative output voltage level generation, respectively, they are being switched under the grid's frequency as earlier mentioned. Accordingly, just the shape of the injected grid current during the positive and negative half-cycle can be seen from the point of view of their current stresses, as shown in Fig. 5. Having taken such observations, to calculate the average value of the extra power losses (P_{C-Ext}) caused by C_2 , we can write:

$$P_{C-Ext} = \frac{V_{on}}{T}\int_0^T \left|i_{Ch,C2}(t)\right| dt = \frac{V_{on} Q_{ext}}{T} \quad (12)$$

Where, Q_{ext} is the charge taken away from C_2 over a full cycle of the grid's frequency. Regarding the passing current waveform of C_2 in the third and fourth working zone shown in Fig. 5, Q_{ext} can be expressed as:

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$$Q_{ext} = \int_{t_3}^{t_4} \left| i_g(t) \right| dt + 2 \times \int_{\frac{T}{2}}^{t_3} \left| d_2(t) i_g(t) \right| dt \quad (13)$$

Where, $d_2(t)$ is the normalized dwell time of the third working zone calculated by (6). So, (13) can be rewritten as:

$$Q_{ext} = I_m \left(\int_{\frac{T}{2}+t_1}^{T-t_1} \left| \sin(\omega t) \right| dt + 4D_m \int_{\frac{T}{2}}^{\frac{T}{2}+t_1} \left| \sin^2(\omega t) \right| dt \right) \quad (14)$$

Regarding (8), (12) and (14), P_{C-Ext} is obtained as (15):

$$P_{C-Ext} = \frac{V_{on} I_m}{2\pi} \left(2D_m \sin^{-1}\left(\frac{0.5}{D_m}\right) + \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (15)$$

Therefore, the overall conduction loss of a typical power switch like S_1 can be expressed as (16). A similar framework can also be adopted for the extra charge of C_1 and in consequence for the extra conduction loss of S_p.

$$P_{C-T,S1} = \frac{V_{on} I_m}{2\pi} \left(1 + 2D_m \sin^{-1}\left(\frac{0.5}{D_m}\right) + \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (16)$$

B. Design Guidelines of the Passive Elements

B.1. Inductor Determination

In order to find the required value of the inductor interfacing between the proposed inverter and the grid, the inductor's current relation over a sampling time period should be derived as follows:

$$i_g(t) = \int_0^{d_1 T_S} V_L(t) dt + i_g(0) \quad (17)$$

Where, $i_g(0)$ is the initial stored current of the inductor, and $V_L(t)$ is the voltage across it which has to be obtained during the dwell time which generates the upper level of the inverter's output voltage. So, considering the instantaneous current ripple of the inductor ($\Delta i_g(t)$), the following equation can be written:

$$\Delta i_{g,\max}(t) = \frac{(V_{inv,up} - V_g(t)) d_1(t)}{2 f_{sw,\min} L_g} \quad (18)$$

Since switching frequency is variable on the basis of the proposed PCC, so the worst case must be considered to reflect the maximum value of $\Delta i_g(t)$. Here, the $f_{sw,\min}$ is defined as the minimum switching frequency of the proposed PCC strategy. Since the maximum value of the current ripple ($\Delta i_{g,\max}$) is taking place at the peak value of the grid's voltage ($V_{m,g}$), so regarding (18) and the equation of the dwell time of $d_1(t)$ in zone I provided by (4), the minimum required value of L_g for the proposed topology can be expressed as:

$$L_{g,\min} = \frac{8 D_m V_{dc} (2V_{dc} - V_{m,g}) + {V_{m,g}}^2}{16 D_m f_{sw,\min} V_{m,g} \Delta i_{g,\max}} \quad (19)$$

B.2. Capacitance Determination

To determine a correct value for the capacitance of the involved capacitors, the function of the grid's current in respect of the inverter's output power (P_{out}) injecting to the grid at the unity power factor can be derived as follows:

$$i_g(t) = \frac{P_{out}}{V_{dc} D_m} \sin(\omega t) \quad (20)$$

From the operating principle of the proposed five-level CG-based topology, it is evident that the capacitor C_2 plays an essential role in injecting the inverter's power to the grid since it should be in the injected grid's current flowing path for the negative half cycle of the grid's frequency (zone III and IV). Regarding the current flow path of the SC cell capacitor (C_1) during the positive half-cycle of the grid (Fig. 2(b) and Fig. 2 (c)), it is revealed that C_1 will be directly put in the injected grid's current flowing path once the inverter is working in Zone I (the top positive output voltage level). So, having considered Zone I and IV as the longest discharged cycle (LDC) of C_1 and C_2, respectively and taking ΔV_{C1} and ΔV_{C2} as their voltage ripple during the time interval of $[t_2 - t_1]$ and $[t_4 - t_3]$ shown in Fig. 5, the following relations can be expressed:

$$\frac{1}{C_1} \int_{t_1}^{t_2} i_{C1}(t) = \Delta V_{C1} \quad (21)$$

$$\frac{1}{C_2} \int_{t_3}^{t_4} i_{C2}(t) = \Delta V_{C2} \quad (22)$$

Where, $i_{C1}(t)$ and $i_{C2}(t)$ are denoted as the passing current through the C_1 and C_2 during the operation in Zone I and IV, respectively. Regarding Table II and (4), such functions can be referred to the grid's current as (23) and (24):

$$i_{C1}(t) = d_1(t) i_g(t) = (2d(t) - 1) i_g(t) \xrightarrow{for} Zone\ I \quad (23)$$

$$i_{C2}(t) = i_g(t) \xrightarrow{for} Zone\ IV \quad (24)$$

Therefore, considering (21)-(24), the required capacitance of the capacitors can be obtained as follows:

$$C_1 = \frac{P_{out}}{V_{dc} \Delta V_{C1}} \left(\frac{2T}{3} + \frac{0.5T}{D_m \pi} \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (25)$$

$$C_2 = \frac{P_{out}}{V_{dc} \Delta V_{C2}} \left(\frac{2T}{3} + \frac{T}{D_m \pi} \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (26)$$

From (25) and (26), it is revealed that owing to the series-parallel switching conversion of the SC cell's capacitor (C_1) and a chopped value of the grid current passing through C_1 described by (23), it possesses a much smaller capacitance than C_2.

C. Voltage and Current Stress Analysis

C.1. Voltage Stress of Switches

In order to calculate the voltage stress of the integrated switches of the proposed five-level CG-based inverter, their maximum value of the peak inverse voltage (PIV) is of importance. From the current flowing path analysis depicted in Fig. 2(a)-(f), it can be seen that the integrated high frequency power switches of the SC cell (S_S and S_P) alongside the power

Table III. VA Rating and Type of Switching Frequency of the Involved Power Switches in the Proposed Five-Level CG-Based Inverter

Power Switches	S_S	S_p	S_1	S_2	S_3	S_4
VA Stress	$3V_{dc}I_m$	$3V_{dc}I_m$	$3V_{dc}I_m$	$2V_{dc}I_m$	$2V_{dc}I_m$	$2V_{dc}I_m$
Switching Frequency	High	High	High	High	Low	Low

switch S_1 bear V_{dc} at their OFF state condition, whereas each of other three remaining power switches (including S_2 as a high frequency switch besides S_3 and S_4 as the two mentioned low frequency switches) tolerate $2V_{dc}$ as the maximum PIV. So, the following relations can be expressed for the PIV of the switches:

$$V_{Ss,\max} = V_{Sp,\max} = V_{S1,\max} = V_{dc} \quad (27)$$

$$V_{S2,\max} = V_{S3,\max} = V_{S4,\max} = 2V_{dc} \quad (28)$$

Therefore, the total standing voltage (TSV) of the proposed topology will be equal to $9V_{dc}$ (4.5 in the per unit scale) which offers a very acceptable range for a boost type five-level inverter.

C.2. Current Stress of Switches

So as to calculate the maximum current stress of the involved switches, the maximum value of the charging current of the capacitors should be identified. Considering all the involved resistance of the charging flow path including the Equivalent Series Resistor (ESR) of the C_1 and C_2 ($R_{\Sigma,C1}$ and $R_{\Sigma,C2}$), the maximum value of the charging current of the capacitors can be expressed as (29):

$$i_{Ch,\max,Ci} = \frac{\Delta V_{Ci,\max}}{R_{\Sigma,Ci}} \qquad i = 1,2 \quad (29)$$

Herein, the maximum charging current of C_1 directly affects the current stress of S_p since it will be in the charging path of C_1 during the operation in Zone I. Also, as earlier mentioned, excluding two low frequency power switches (S_3 and S_4), the current stress of the switches S_1 and S_S are affected by $i_{Ch,\max,C2}$ when they are being involved in the charging path of C_2 during the top-positive and the zero-negative output voltage level generation (See Fig. 2(c) and (d)).

Now, having taken Fig. 5 into account along with (29), the maximum current stresses of the switches can be taken as follows:

$$I_{Ss,\max} = I_{S1,\max} = i_{Ch,\max,C2} + I_m \quad (30)$$

$$I_{Sp,\max} = i_{Ch,\max,C1} + I_m \quad (31)$$

$$I_{S2,\max} = I_{S3,\max} = I_{S4,\max} = I_m \quad (32)$$

Here, in order to reflect a quantitative metric as for the above-mentioned current/voltage stresses of the switches and in turn the overall losses, a product value of Volt/Ampere (VA) rating for each of the power switches can be considered. Regarding a 1kW ac power injected to a standard grid (50 Hz/311 V) and considering the two times voltage boosting property of the proposed inverter, the minimum required value of the input voltage (V_{dc}) can be set at 160 V. So, the maximum value of the modulation index (D_m) will be equal to 0.97. Taking into account such parameters and considering five percent as the maximum allowable voltage ripple across the involved capacitors, the maximum current stresses of the capacitors will be about twice the maximum value of the injected current. Therefore, concerning (27)-(32), the VA rating of the involved power switches alongside their switching frequency can be summarized in Table III, where the power switches are divided into two groups with the low and high value of the switching frequency and $3V_{dc}I_m$ / $2V_{dc}I_m$ as the VA stress.

V. COMPARATIVE STUDY

In order to compare the circuit architecture of the proposed five-level CG-based inverter with some other recently-introduced transformerless grid-connected inverters, a comparative study is presented in this section. As shown in Table IV, the comparative items include the number of required passive and active elements, the maximum number of ON-state power switches at each instant, the required value of the input voltage utilization, which can reflect the boosting feature of each structure, the maximum number of inverter's output voltage level, the value of the leakage current, the reactive power support ability and finally the overall reported efficiency at the rated power. Here, in the overall component count column, the input capacitor and the pre-assumed filter of each structure have also been considered. Also, on the basis of the standard IEEE grid's code, the root mean square (RMS) value of the leakage current has been considered low when it is less than 120 mA, whereas it is assumed to be very low when a value is below 10 mA.

From Table IV, it is clear that all the discussed structures except the proposed topology and the ones presented in [16] and [22] possess only a buck-type feature, so more PV strings should be there in a series in to regulate the maximum peak value of the grid's voltage. Considering a standard local grid with the peak voltage value of 311 V, we only need to use a 160 V dc voltage value for the proposed topology, whereas for the conventional types of PV inverters, the minimum required value of the dc link voltage is twice that. So, when the same PV string is available, another boost-based dc-dc stage is required to elevate the range of the input voltage and then more active and passive elements are required. This double stage energy conversion system can also affect the overall efficiency since the efficiency of each stage should be multiplied with each other in order to get the overall efficiency of a PV-based converter.

Zero value of the leakage current through the proposed CG architecture in every stage of the operation (active/reactive power supports modes) alongside the generation of up to five output voltage levels represent the superior nature of the proposed topology over the conventional H5, HERIC, OH5 and H6 structures. Such features can readily improve the quality of the injected current and the overall loss of the system through almost the same number of switching devices. It is also notable that through a reasonable switching frequency, a very low value of the first order L type filter can be utilized as for the proposed topology, whereas to achieve

Table IV. A Comparative Summary Between the Proposed Topology and Different Transformerless Grid-Connected Structures

Type of Converter		No. of Components				Max No. of ON-Switches	Required Value of V_{in} /Boosting Feature	No. of Levels	Leakage Current	Reactive Power Support	Reported Rated Efficiency
		S	D	C	L						
H5 [5]		5	-	2	2	3	V_{dc} /NO	3	Low	Yes	98.5%@0.5kW
HERIC [6]		6	2	2	2	2	V_{dc} /NO	3	Low	NO	97% @1kW
OH5 [7]		6	-	2	2	3	V_{dc} /NO	3	Low	Yes	97.2@1kW
H6 [8-10]		6	2	2	2	3	V_{dc} /NO	3	Low	Yes	97.4%@1kW
[11]		6	2	2	2	4	V_{dc} /NO	5	Very Low	NO	97.5%@2kW
[12]		6	2	2	1	2	$2V_{dc}$ /NO	5	Very Low	Yes	NA@1kW
[16]		4	-	3	3	2	$0.5V_{dc}$ /Yes	2	Zero	Yes	97.7%@300W
[18]	**Type I&II**	4	1	3	1	2	V_{dc} /NO	3	Zero	Yes	99.1%@800W
	Type III	4	-	3	1	2	V_{dc} /NO	3	Zero	Yes	96%@800W
[19]		5	-	2	2	3	V_{dc} /NO	3	Zero	Yes	95.5%@500W
[20]		5	2	2	2	3	V_{dc} /NO	3	Very Low	NO	97%@1kW
[21]		4	2	4	2	2	V_{dc} /NO	3	Zero	Yes	95.2%@500W
[22]		5	-	2	2	2	$0.5V_{dc}$ /Yes	3	Zero	Yes	92.5%@200W
[23]		6	-	3	1	3	V_{dc} /NO	5	Zero	Yes	97%@1kW
[24]		6	1	3	1	3	V_{dc} /NO	5	Zero	Yes	95.8%@1.2kW
Proposed		6	2	3	1	3	$0.5V_{dc}$ /Yes	`5	Zero	Yes	98.1%@600W

the same quality of the injected current in the conventional PV-based inverters, either higher order filters (LC or LCL) have to be employed or the rate of switching frequency should be increased. Obviously, such a procedure can again increase the losses and power density, while in the case of higher order LC or LCL filters, some resonant problems can be associated with the control platform of the conventional structures [21]. Apart from the above-mentioned advantages of the proposed topology over the conventional ones, it is also worth noting that the overall per unit scaled TSV of the proposed topology is only 4.5 (as previously mentioned), whereas the value for the others is five. So, in the case of the same local grid with 311 V as the peak, all the power switches of the conventional H5, HERIC or H6 inverters should bear all the used PV string voltage value, while half of the total number of power switches of the proposed topology should tolerate this maximum PIV and the remaining ones should withstand a half value of the maximum PIV. As a result, such reduction in the value of PIV/TSV can lead to a lower overall manufacturing cost of the proposed 5L-CG-based transformerless inverter in comparison to others.

By contrast, alongside the proposed topology, only four other structures mentioned as [11], [12],[23], and [24] are able to generate five-level of the output voltage. Herein, although the number of required components in these structures are the same with the proposed one, none of them offers any boosting feature. Since two of the six involved power switches operate under the grid's frequency and due to the fact that half the number of total power switches should tolerate the highest PIV, the overall rated efficiency of the proposed structure is also acceptable in contrast to others. Here, [11] and [12] use the midpoint clamping technique to reduce the leakage current, while the proposed topology and the presented structures in [21] and [22] have employed a CG-based circuit architecture that can guarantee almost zero leakage current injection. It is also worth noting that the suggested topologies in [23] and [24] demand a pre-charged circuit procedure with extra voltage sensors for assurance of the capacitors balancing issue, while such a concern is alleviated by using the series-parallel switching conversion of the SC cell in the proposed topology.

TABLE V. Prototype Parameters

Element	Type	Description
Power Switches	47N60C	650V/47A
Gate Driver	TLP 250	IC
Power Diode	MUR1560	600V/15A
Current Transducer	LA55P	Hall Effect
Microcontroller	Beagle Bone Black	ARM
Local Grid's Frequency	50 Hz	-
Sampling Frequency/Maximum Switching Frequency	40 kHz/ 20 kHz	-
C1 & C2	MKT	$0.47mF$ & $1mF$
Magnetizing Inductor	Ferrite Core	$2mH$

VI. EXPERIMENTAL VERIFICATIONS

In this section, some experimental results obtained through a laboratory built prototype are given to reconfirm the feasibility and correctness of the proposed 5L-CG-based inverter topology. Herein, a PV simulator with the fixed dc link voltage of 180 V is used as the input dc source. Here, the peak voltage of the local grid is 310 V and the passive elements' values are chosen based on the presented design guidelines of

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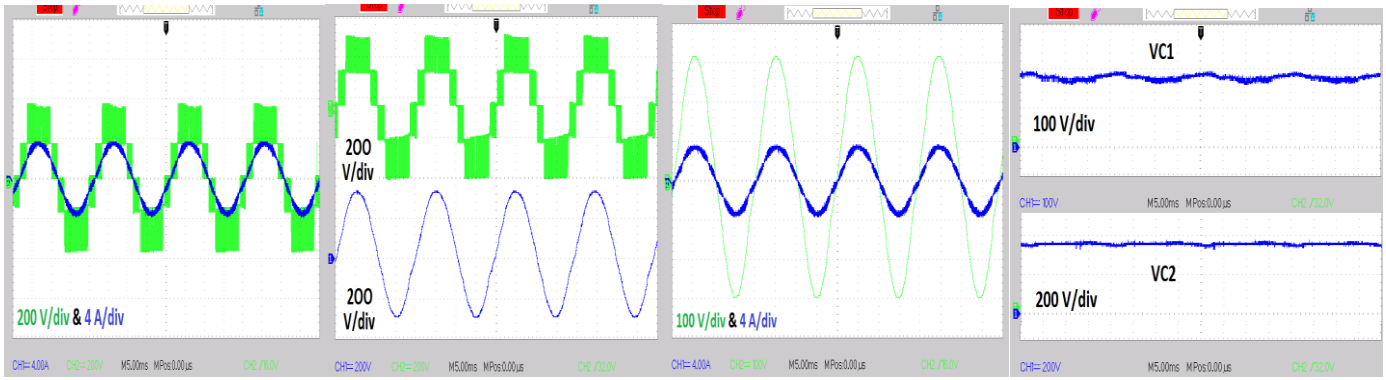
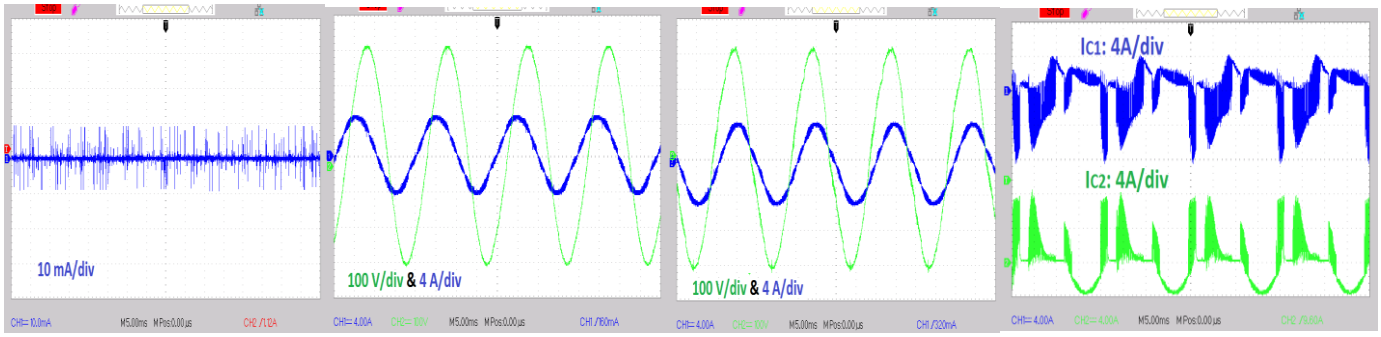


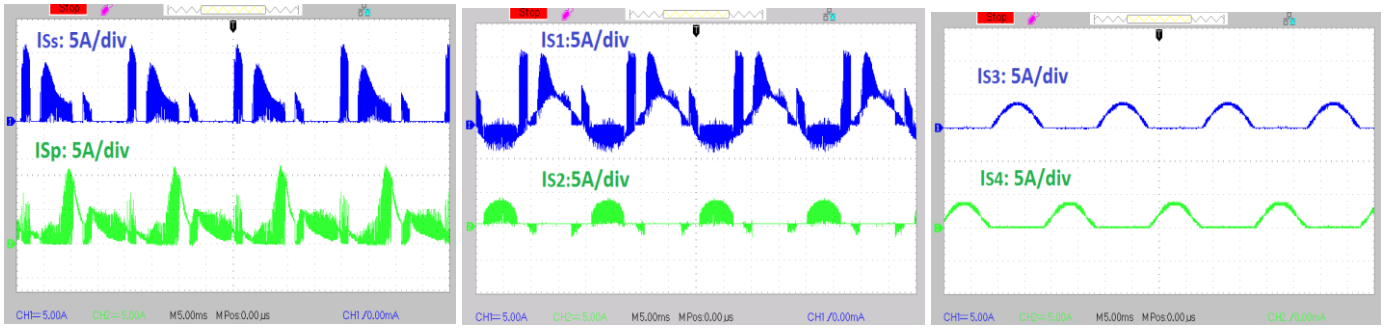
(a) (b) (c) (d)

Fig. 6. (a) Inverter's output voltage (green trace) (200 V/div) and the injected grid's current (blue trace) (4 A/div) (b) Inverter's output voltage (green trace) (200 V/div) and the local's grid voltage (blue trace) (200 V/div) (c) Injected grid's current (blue trace) (4 A/div) and local grid's voltage (green trace) (100 V/div) (d) the voltage across C_1 (100 V/div) and the voltage across C_2 (200 V/div).



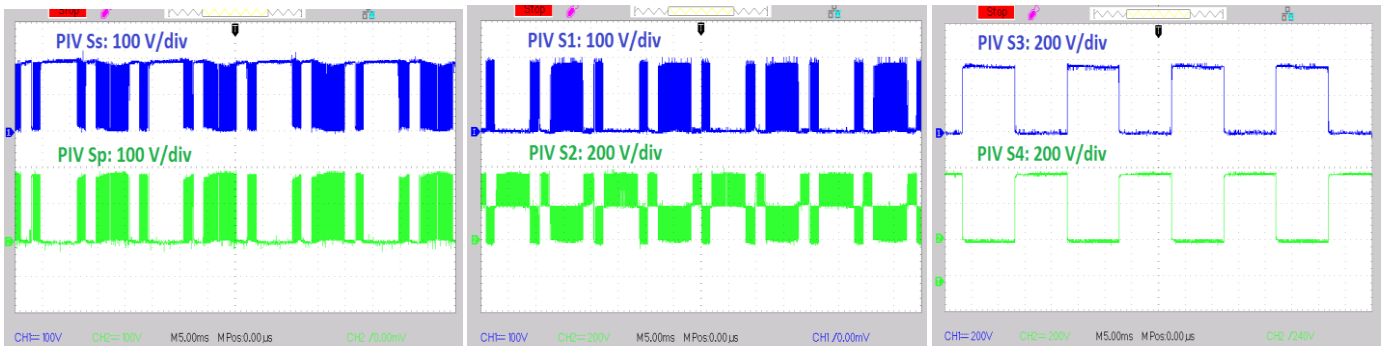
(a) (b) (c) (d)

Fig. 7. Experimental results of the (a) measured value of the leakage current [10 mA/div] (b) the grid's voltage (green trace) [100 V/div] and injected current [4 A/div] (blue trace) at leading power factor (c) the grid's voltage (green trace) [100 V/div] and injected current [4 A/div] (blue trace) at lagging power factor (d) the measured passing current through C_1 [4 A/div] (blue trace) and C_2 [4 A/div] (green trace).



(a) (b) (c)

Fig. 8. Experimental results [5 A/div] of the measured passing current through (a) S_S (blue trace) and S_p (green trace) (b) S_1 (blue trace) and S_2 (green trace) (c) S_3 (blue trace) and S_4 (green trace).



(a) (b) (c)

Fig. 9. Experimental results of the PIVs across (a) S_S [100 V/div] (blue trace) and S_p [100 V/div] (green trace) (b) S_1 [100 V/div] (blue trace) and S_2 [200 V/div] (green trace) (c) S_3 [200 V/div] (blue trace) and S_4 [200 V/div] (green trace).

section IV. Table V also indicates the prototype parameters of the experimental study. To avoid any computational burden, a hardware-based PLL technique is also used to obtain the synchronous phase value of the reference current in the proposed PCC strategy. Regarding these noted notions, the obtained results are presented by the following subsections:

A. *The overall performance evaluation of the proposed 5L-CG-based Inverter*

Considering the proposed 5L-CG-based inverter topology and the discussed operating principle of the proposed PCC, a peak value of 3.8 A as for the reference current has been considered for this case study. The corresponding five-level inverter's output voltage with the injected grid's current waveform and the local grid's voltage with such five-level inverter's output voltage waveforms can be observed in Fig. 6(a) and (b), respectively. As can be seen, the maximum value of the inverter's output voltage and the injected current are 360 V and 3.8 A, respectively, which can reflect the boosting feature of the proposed system with about 590 W output power. To show the correct value of the injected active power, the grid's voltage and the injected in phase current waveforms have been shown in Fig. 6 (c). Herein, since the inverter has been directly connected to a non-stiff local grid, the sinusoidal shape of the local grid's voltage is a little affected by harmonics. From these results, it is clear that the proposed topology with its PCC-based strategy could properly generate all the supposed output voltage levels with appropriate quality of the injected current. Herein, to verify the balanced voltage waveform of the involved capacitors, the voltage across the C_1 and C_2 is captured and they can be seen by Fig. 6 (d). As shown from this result, they could be balanced at 180 V and 360 V, respectively.

To better emphasize the appropriate circuit feasibility of the proposed topology in the transformerless grid-connected condition, the measured waveform of the leakage current is also taken and can be seen in Fig. 7(a). Since the voltage across the virtual capacitor generated by the negative terminal of the PV simulator is short-circuited, so the measured waveform of the leakage current is obtained by the contribution of such virtual capacitor in the positive terminal of the PV simulator. It is clear that the proposed topology could properly cancel out the effects of leakage current trouble. In following, to show the feasibility of the proposed topology in the reactive power support mode, a lead and lag phase shift has been applied in the reference current waveform of the proposed controlled system. The overall experimental results of the local grid's voltage besides the injected grid current with leading and lagging power factor can also be observed in Fig. 7 (b) and (c), respectively.

The passing current waveforms of the capacitors within four fundamental cycles have also been captured to show their overall performance under the 3.8 A peak value of the grid current injection. As it can be seen by Fig. 7 (d), the results are quite compatible with the theory presented in Fig. 5, while the maximum value of the charging current for the capacitors is more than double value of the peak of the injected current. Herein, to better confirm the current/voltage stress analysis of the switches, Fig. 8(a)-(c) and 9(a)-(c) can be considered.

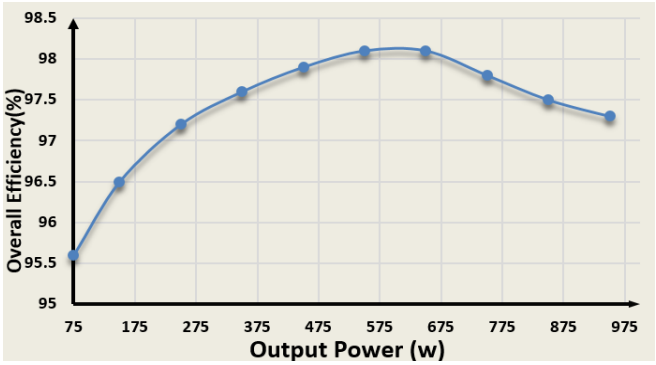
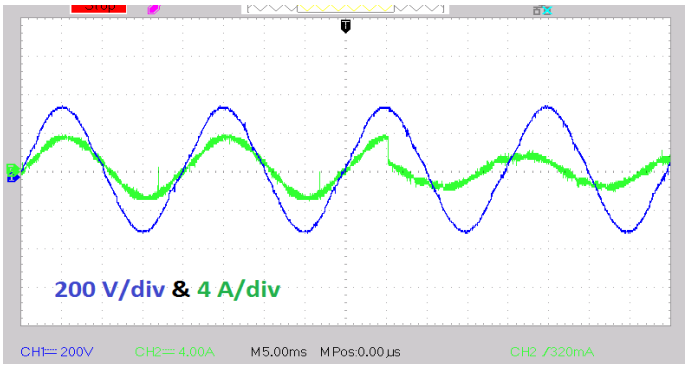
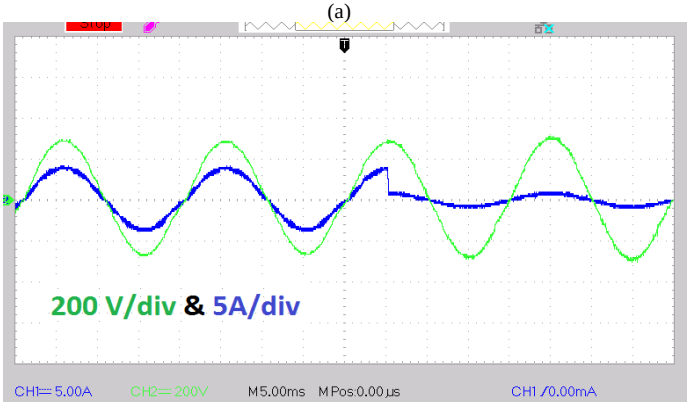


Fig. 10. The variations of overall efficiency versus output power.



(a)



(b)

Fig. 11. The experimental dynamic response waveforms of the local grid and the injected grid current (a) from full active to full reactive power support mode (b) from 100% of the rated power to 10% of rated power.

From these results, it is clear that a group of three power switches (S_1, S_s and S_p) that are involved into the charging path of the capacitors can tolerate the maximum current stress with the peak value of about 12 A (three times more than the peak of injected grid current), while such maximum current stress for the remaining switches is 3.8 A. From the measured PIV waveforms of the switches shown in Fig. 9 (a)-(c), it can also be reconfirmed that the PIV of those switches that are the maximum current stress holders is 180 V, while two low frequency power switches (S_3 and S_4) with minimum current stress possess the highest PIV that is equal to 360 V.

Regarding the above-mentioned current/voltage stress, the measured value of the overall efficiency behavior over a wide range of output power can also be seen in Fig. 10. Herein, since the design guidelines of the passive elements is the same

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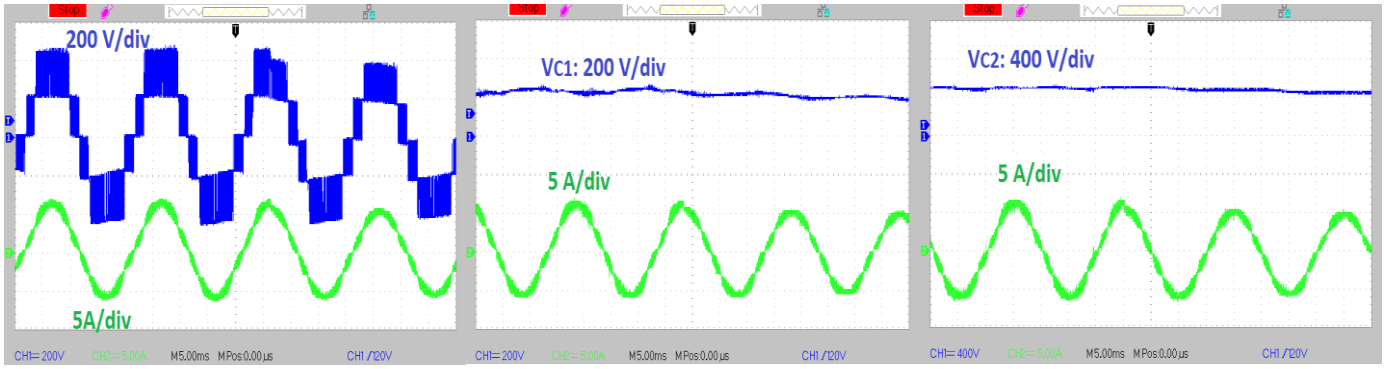
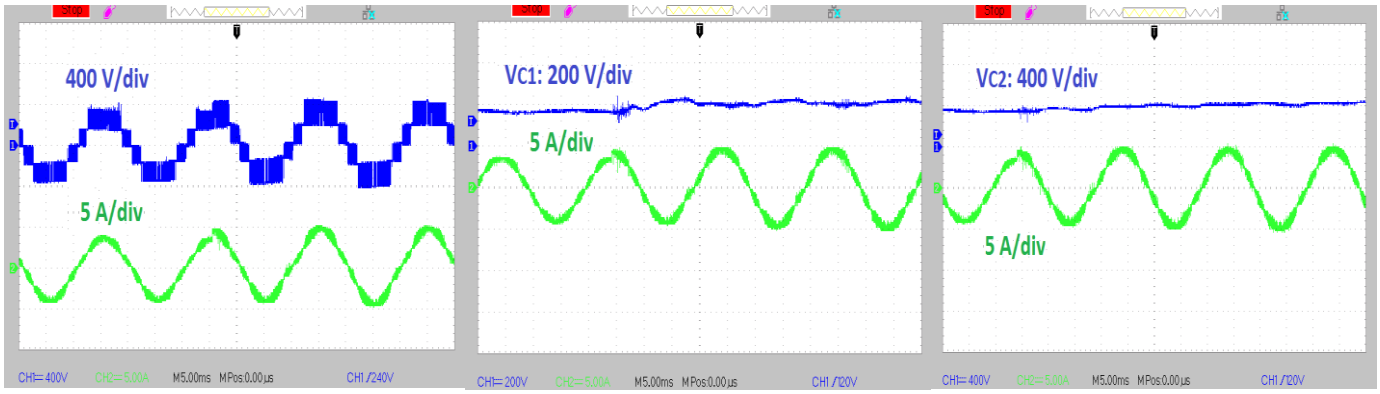


(a) (b) (c)

Fig. 12. The experimental dynamic response waveforms once the input voltage is changed from 230 V to 200 V (downward trend) (a) the inverter's output voltage (blue trace) [400 V/div] and the grid's current (green trace) [5 A/div] (b) the voltage across C_1 [200V/div] with the grid's current[5 A/div] (c) the voltage across C_2 [400 V/div] with the grid's current [5 A/div].



(a) (b) (c)

Fig. 13. The experimental dynamic response waveforms once the input voltage is changed from 180V to 200 V (upward trend) (a) the inverter's output voltage (blue trace) [400 V/div] and the grid's current (green trace) [5 A/div] (b) the voltage across C_1 [200 V/div] with the grid's current [5 A/div] (c) the voltage across C_2 [400 V/div] with the grid's current [5 A/div].

as for the 600 W output power, it can be seen that the overall efficiency hits the peak around this rated power value.

B. *The performance evaluation of the proposed 5L-CG-based Inverter under the Dynamic Condition*

In order to evaluate the correct and precise performance of the presented PCC applied to the proposed topology under the dynamic condition, some specific experimental results are shown in this subsection. Here, since the investigation of the MPPT principle integrated in the control system is beyond the scope of this paper; so the dynamic performance of the proposed PCC is checked by applying some variations in the amplitude of the reference current and in the input dc voltage of the PV simulator.

As for the first dynamic test, the phase and amplitude of the reference current of the proposed PCC are changed from the full active power support mode to the full reactive power support condition. The robustness of the injected grid's current waveform and the local grid's voltage under this condition can be readily seen in Fig. 11(a), while the inverter is injecting about 600 W active power to the grid before applying the changes into the reference current. After this, it injects about 300 VAR reactive power to the grid. Considering 600 W as the rated power of the experimental setup, the fast and correct performance of the proposed PCC can further be clarified from Fig. 11 (b), where the amplitude of the reference current is suddenly changed from about 4 A (100% of the rated power) to 0.4 A (10% of the rated power). In all of the mentioned cases, the injected grid current THD is less than 2%.

As for the next dynamic test, the performance of the proposed system under the variable input voltage condition and the higher rate of injected grid current is checked. Herein, at the first, the input voltage value of the PV simulator is kept fixed on 230 V and then it is suddenly changed to 200 V. As is obvious from Fig. 12 (a), all the expected levels with the high quality of the injected grid current waveform, which is more than 5 A at the peak in this case, can be properly generated. Here, the voltage across both the capacitors can be fixed at their desired level (230 V and 200 V for C_1 and 460 V and 400 V for C_2) and this can be respectively confirmed by Fig. 12 (b) and (c). In following, the input voltage is intentionally changed to offer an upward trend (from 180 V to 200 V). Again the same robust performance of the proposed system can be declared through Fig. 13(a)-(c), where both the capacitors are balanced at the expected voltage level (180 V and 200 V for C_1 and 360 V and 400V for C_2). Here also the peak of injected current is more than 5 A which implies up to

1kW injected active power. It is notable that in both the downward and upward trends of the input voltage changes, the operating point of the PV simulator is supposed to be changed since its output power depends on the input voltage and the input current value. So, whenever the input voltage of the PV simulator is to be changed, the input power follows its trend.

VII. Conclusion

A new five-level transformerless grid-connected inverter has been presented in this study. The proposed topology is able to remove the leakage current concern with a CG-based architecture. Also, with the reasonable number of active and passive involved elements, it offers a two times voltage boosting feature that makes it suitable for PV string applications. A PCC-based strategy has also been employed in this study to regulate the value of the injected current. The details of such a controlled system besides some analysis as for the conduction losses, the design guidelines and the switches voltage/current stresses have been discussed to further explore the performance of the proposed topology. Finally, a comprehensive comparative study alongside the experimental results has been presented to confirm the superiority and accurate operation of the proposed system.

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