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Extendable Switched-Capacitor Multilevel Inverter with Reduced Number of Components and Self-Balancing Capacitors

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***Abstract*—Multilevel inverters (MLIs) with self-balanced switched-capacitors (SC) have received wide recognition for increasing the reliability and efficiency of renewable energy and high-frequency power distribution systems. This paper presents a new SC MLI structure using a reduced number of components. The proposed dual-source SC MLI can be extended in various ways to increase the voltage levels at the output. The SCs are self-balanced by using a suitable charging-discharging pattern and thereby, voltage boosting is achieved. The operational analysis and features of the proposed 25-level MLI are delineated in detail. Comparative analysis with state-of-art MLIs in terms of the number of components, voltage stress, and cost factor demonstrate the merit of the proposed extendable SC MLIs. Extensive simulation of the proposed MLI structure is performed on the MATLAB/Simulink environment using both the low and high switching frequency control schemes. Furthermore, simulation results are validated experimentally by developing a prototype of the proposed MLI under load variations, frequency change condition, and variation in the modulation index.**

***Index Terms*—Extendable multilevel inverter, reduced components, pulse-width modulation (PWM), self-voltage balancing, switched-capacitor (SC), voltage boosting**

I. Introduction

MULTILEVEL inverters (MLIs) have received much attention in varieties of medium-high range of power conversion systems [1]–[3]. This is due to the abilities of the MLI such as significant harmonic reduction, voltage stress reduction, high quality and high-efficiency output [4]. In photovoltaic (PV) power conversion systems, STATCOM, electric vehicles, etc., conventional MLIs have successfully replaced the two/three-level inverters [5]–[8]. The conventional MLIs such as cascaded H-bridge MLI (CMLI), flying capacitor clamped (FMLI) and neutral point clamped (NMLI) are actively used in varieties of applications. The conventional CMLI dominates over the other two types due to the features such as high modularity, smooth fault handling capability, and high reliability. However, the CMLI needs several isolated dc sources to synthesize the staircase output. On the other hand, the FMLI and NMLI require complex voltage balancing circuits, large size capacitors, and several additional passive components [4], [9], [10]. Therefore, the research interest is growing to develop MLIs using reduced isolated sources, fewer semiconductor switches, having low voltage stress and high efficiency. Multiple solutions have been proposed recently to achieve this target [4].

In view of different applications, many alternative topologies are developed in recent years by reconfiguring conventional CMLI. These MLIs are basically of three types, *i.e.*, switched-dc source (SS) type, switched-diode (SD) type and switched-capacitor (SC) type. These MLIs utilize the concept of asymmetrical sources to synthesize higher voltage levels at the output. However, the symmetrical MLIs have simple control and reduced stress on the switches. In [11], [12], generalized SS MLIs are introduced. The MLI in [11] uses a back-end H-bridge for altering the polarity, whereas it is avoided in [12] and thus reduces the voltage stress significantly. The latter topology is a suitable alternative to the CMLI, which consists of only unidirectional switches that can operate both in symmetrical and asymmetrical mode. To reduce the source count, the CMLI topology is reconfigured in [7], [13], by connecting a level doubling circuit to it. A self-balanced capacitor is used to enhance the voltage level to almost twice and thus, the dc source count is reduced appreciably. By using this technique, SD MLI topology has been disclosed recently in [14] for PV application. The extendable SD MLI structure presented in [15] is suitable for standalone PV systems. These structures reduce the switch/drivers count considerably and possess more straightforward control as diodes are used instead of the switches. However, due to the use of diodes, these MLIs are suitable for high power factor loads.

A novel approach is suggested in [16] to reduce the dc source count. This structure uses capacitors and thereby reduces the number of isolated dc sources effectively and can operate in symmetrical as well as in asymmetrical mode. The magnitude of the dc sources can be suitably selected to create multiple voltage steps at the output. The prior-discussed SS and SD MLIs can't boost the voltage magnitude. On the contrary, the SC MLI reduces the number of dc sources in addition to the switch count and can boost the voltage magnitude without using large-sized transformers and inductors. A generalized SC MLI structure introduced in [17] can synthesize higher voltage level by making the dc sources magnitude highly asymmetrical. The basic building block of this MLI consists of a single dc source, two switches along with a capacitor. The SC can be charged using one switch and another switch is used to discharge it. By using the series-parallel charging-discharging technique, the capacitors are self-regulated at the desired voltage and voltage boosting is thereby achieved [18], [19]. The SC MLI structure proposed in [20], [21] features higher step-up of the voltage but uses

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multiple sources when extended to increase the voltage levels at the output. A modified H-bridge is used in the circuit and thus, the voltage stress is very low. Using only two dc sources, SC MLI structure disclosed in [22] produces 13-level and has the possibility of cascaded extension for enhancing the voltage level.

Further reduced components SC MLI topologies are developed recently, considering the boosting factor, load handling ability, and voltage stress. The single-dc SC MLIs proposed in [18], [23], [24] uses a back-end H-bridge for generating the negative levels at the output. High voltage boosting is achieved in [18], [23], but at the cost of a large number of switches. Due to the presence of series-diodes in the conducting path, the topology [23] is inadequate for operating with high inductive loading. The capacitor current spikes are effectively reduced using the SC MLI provided in [24]. However, this topology is inefficient to boost the voltage magnitude. Without using the conventional H-bridge, new single dc SC MLIs employing self-balanced capacitors have emerged. The MLIs in [25] and [26] with 1.5 times boosting ability produces 13-level and 7-level at the output, respectively. The former topology features single-phase extendibility, whereas the latter has the flexibility to extend in three-phase as well. SC MLIs disclosed in [27], [28] contains multiple dc sources when extended to create higher voltage levels. These MLIs can operate in both symmetrical and asymmetrical modes. Single dc 9-level SC MLIs proposed in [29], [30] has quadrupled boosting ability, whereas [31] can boost the voltage magnitude to two-time. The voltage stress reduction is notably achieved, scarifying the switch count.

With the motivation from the above discussion, this paper presents an SC MLI with the ability to extend for producing higher voltage levels. All the capacitors employed in the circuit are self-balanced without using any additional voltage balancing circuit. Next section introduces the proposed dual-source SC (DSC) MLI topology and analyzes the self-balancing ability along with the design considerations. Section III discloses the various possible extensions of the proposed DSC MLI. A comparison concerning different performance parameters is carried out in Section IV to verify the topological advancement. The PWM control technique for the proposed MLI is briefly examined in Section V. To verify the operability of the proposed MLI, simulation and experimental verification are incorporated in Section VI and VII, respectively.

II. Proposed MLI Description

The schematic of the proposed 25-level DSC MLI is shown in Fig. 1(a), which requires only two dc sources with a magnitude of V and $0.5V$ for producing a multilevel output. One of the key applications of the developed MLI is in PV systems [32]. PV panels in such system can be used in (2 X 2) and (1 X 1) arrangement to maintain the dc-link voltages in 2:1 ratio [14], [33]. Additional dc-dc converters can be avoided as the proposed circuit features inherent boosting ability. Two capacitors (C_1 & C_2) are wisely placed to step-up the voltage magnitude as well as to enhance output voltage levels using less number of components. Further, one bi-directional blocking bi-directional conducting switch and eleven unidirectional blocking bi-directional conducting switches are customized to develop the DSC MLI. The switches S_1 & S_2 are utilized to switch among the voltage sources $0.5V$ & V to appear at the output and the sum of the two input sources can be obtained through the switch S_3. The switch S_2 allows the back flow of current in case the load is inductive. Switches S_4 and S_5 can be turned ON for paralleling the capacitor (C_1) with the input sources. Thus, C_1 has the flexibility to be self-charged to the sum of the dc sources magnitude. The switch S_6 is alternatively turned ON with S_4 to make C_1 in series with the input sources. Similarly, S_{5a} and S_{6a} are alternatively turned on to involve the load side capacitor (C_2) in the level generation and to by-pass it, respectively. The switches S_{1a} and S_{2a} operate in the positive half cycle, whereas during the negative half cycle generation switches S_{3a} and S_{4a} are kept on. The detailed switching scheme of the DSC MLI in producing a 25-level output is presented in Table I.

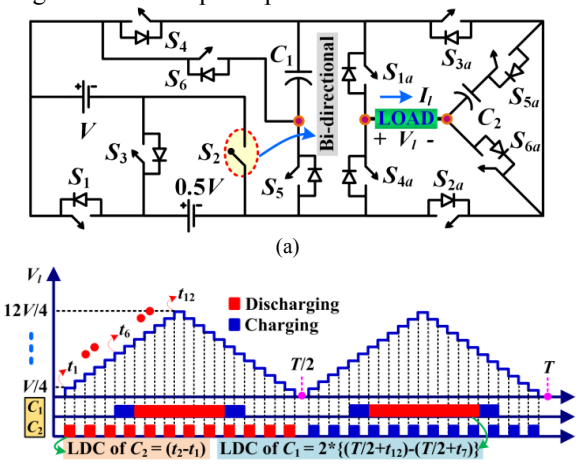

Fig.1. Proposed DSC MLI (a) Proposed 25-level MLI schematic, (b) output voltage waveform pattern

TABLE I

Switching scheme of the 25-level DSC MLI

ON devices for Positive half-cycle	Voltage steps	ON devices for Negative half-cycle
$S_{2a}-S_{4a}-S_{6a}$	0	$S_{1a}-S_{3a}-S_{6a}$
$S_{5a}-S_{3a}-S_{1a}$	$\pm V/4$	$S_1-S_4-S_{3a}-S_{5a}-S_{4a}$
$S_1-S_4-S_{1a}-S_{6a}-S_{2a}$	$\pm 2V/4$	$S_1-S_4-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_4-S_{1a}-S_{5a}-S_{2a}$	$\pm 3V/4$	$S_2-S_4-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_4-S_{1a}-S_{6a}-S_{2a}$	$\pm 4V/4$	$S_2-S_4-S_{3a}-S_{6a}-S_{4a}$
$S_2-S_4-S_{1a}-S_{5a}-S_{2a}$	$\pm 5V/4$	$S_3-S_4-S_5-S_{3a}-S_{5a}-S_{4a}$
$S_3-S_4-S_5-S_{1a}-S_{6a}-S_{2a}$	$\pm 6V/4$	$S_3-S_4-S_5-S_{3a}-S_{6a}-S_{4a}$
$S_3-S_4-S_5-S_{1a}-S_{5a}-S_{2a}$	$\pm 7V/4$	$S_1-S_6-S_{3a}-S_{5a}-S_{4a}$
$S_1-S_6-S_{1a}-S_{6a}-S_{2a}$	$\pm 8V/4$	$S_1-S_6-S_{3a}-S_{6a}-S_{4a}$
$S_1-S_6-S_{1a}-S_{5a}-S_{2a}$	$\pm 9V/4$	$S_2-S_6-S_{3a}-S_{5a}-S_{4a}$
$S_2-S_6-S_{1a}-S_{6a}-S_{2a}$	$\pm 10V/4$	$S_2-S_6-S_{3a}-S_{6a}-S_{4a}$
$S_2-S_6-S_{1a}-S_{5a}-S_{2a}$	$\pm 11V/4$	$S_3-S_6-S_{3a}-S_{5a}-S_{4a}$
$S_3-S_6-S_{1a}-S_{6a}-S_{2a}$	$\pm 12V/4$	$S_3-S_6-S_{3a}-S_{6a}-S_{4a}$

A. Self-regulating ability of the capacitors

Employed capacitors are naturally regulated at the desired voltage level, which thereby reduces the control complexity of the proposed MLI. The capacitor C_1 is self-regulated at the sum of the-input source magnitudes with the series-parallel charging-discharging mechanism [17], [23], [30], [34]. As discussed earlier, S_3 switch adds the two input sources and this

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combination paralleled with the capacitor C_1 through S_4 & S_5 for charging it to $1.5V$. The charging and discharging duration of both the capacitors is illustrated in Fig. 1(b), from which it is evident that, C_2 discharges in the positive half cycle and is charged in the same pattern for the negative half cycle. This in turn, maintains the voltage across the capacitor C_2 at half of the magnitude of the low input source. This is due to the self-balancing level doubling principle [14].

The self-regulatory nature of C_2 can also be mathematically proved considering an appropriate output voltage step. Fig. 2(a) shows the equivalent circuit of the DSC MLI during the synthesis of $\pm\ 11V/4$ voltage step across the load and the current flowing through the capacitor C_2 (I_{c2}). The mean value of the I_{c2} facing net impedance of z is expressed in (1-2) and the total charge (Q_{c2}) stored in C_2 over a fundamental period (T) is given in (3).

$$I_{c2}(+) = \frac{V+V_{c1}-V_l+V_{c2}}{Z} \quad (1)$$

$$I_{c2}(-) = \frac{1.5V+V_{c1}-V_{c2}+(-V_l)}{Z} \quad (2)$$

$$Q_{c2} = [I_{c2}(+) - I_{c2}(-)]T = \left[\frac{-0.5V+2V_{c2}}{z}\right]T \quad (3)$$

where V_{c1}, V_{c2}, and V_l are the voltage across C_1, C_2, and load, respectively.

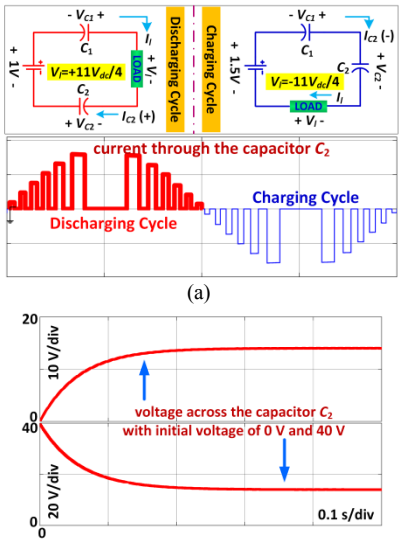

Fig.2. Self-regulating mechanism of C_2 (a) Equivalent circuit of DSC MLI during $V_l = 11V/4$, (b) Self-regulation of C_2 with different initial voltages

The total charge stored or drained by a capacitor in steady-state is zero. Therefore, simplifying (3) gives $V_{c2} = V/4$. Thus, C_2 naturally attains the required voltage ($V/4$) without any external voltage balancing control. Fig. 2(b) delineates the self-tracking of V_{c2} to the desired value (15 V) considering $V =$ 60 V and with a different initial voltage across C_1.

B. *Design consideration of the capacitors*

Fig. 1(b) implies that the charging time of the capacitors is less than the total output voltage duration, which ascertains the quick restoration of charge after the discharge of capacitors. The optimum capacitance value can be determined taking into account the Largest discharging Cycle (LDC) of the capacitor, fundamental frequency, and loading type. LDC is the time interval during which the maximum charge is drained from the capacitor as indicated in Fig. 1(b). The expression for the net charge (Q) stored or drained by any capacitor is given in (4), which gives the capacitance value (C) in (5), where ρ is the percentage ripple in voltage corresponding to the capacitor voltage (V_c). By taking $V =$ 60 V, resistive-inductive loading, and 50 Hz as nominal frequency, the impact of change in phase angle (ϕ) over the selection of capacitance is shown in Fig. 3 for different ρ values. This figure implies that the capacitance can be chosen optimally, considering low ρ value.

$$Q = \int_0^{LDC} I_l(t).dt \quad (4)$$

$$C = \frac{Q}{\rho V_c} \quad (5)$$

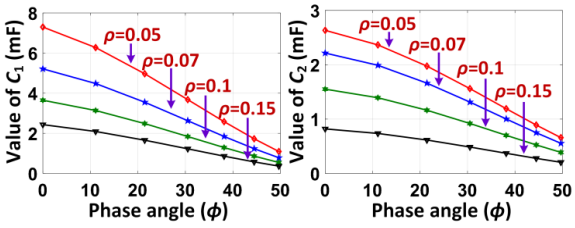

Fig.3. Design analysis of the capacitor (a) value of C_1 versus phase angle, (b) value of C_2 versus phase angle

III. Extension of the Proposed MLI

The proposed DSC MLI features extendibility to synthesize a higher number of voltage levels utilizing a reduced number of components in the following ways.

A. *Switched capacitor extension* (PE1)

Additional SC modules can be integrated with the proposed DSC MLI structure to create more steps in the output voltage waveform. As illustrated in Fig. 4(a), SC modules in the PE1 comprises of two semi-conductor switches, one diode, and one capacitor. Capacitors are symmetrically charged to the higher input source magnitude (V) through the common charging switch S_5 and are discharged through the switch $S_{(n+1)c}$; where n is the number of SC modules. The essential advantage of the PE1 extension is that there is no requirement of an additional charging switch for each of the SCs. The switch S_{nc} is used to by-pass the corresponding SC and the discrete diode D_{nc} is employed to block the reverse current through the charging switch. Number of switches (N_{sw}), number of drivers (N_{driv}), number of discrete diodes (N_{dd}), and number of capacitors (N_c) used to devise the PE1 in terms of the number of SC modules is expressed in (6-10) along with the total switch stress (TSS) in (11). TSS is the summation of voltage stress of individual switches that decides the voltage rating of the MLI. Voltage gain (ratio of output voltage to the input voltage magnitude) and number of output voltage levels (N_l) that can be obtained using PE1 are given in (12) and (13), respectively.

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$$N_{sw} = 2n + 13 \quad (6)$$

$$N_{driv} = 2n + 12 \quad (7)$$

$$N_{dd} = n + 1 \quad (8)$$

$$N_c = n + 2 \quad (9)$$

$$N_{dc} = 2 \quad (10)$$

$$TSS = \frac{18n+41}{2} \quad (11)$$

$$Gain = n + 2 \quad (12)$$

$$N_l = 12n + 25 \quad (13)$$

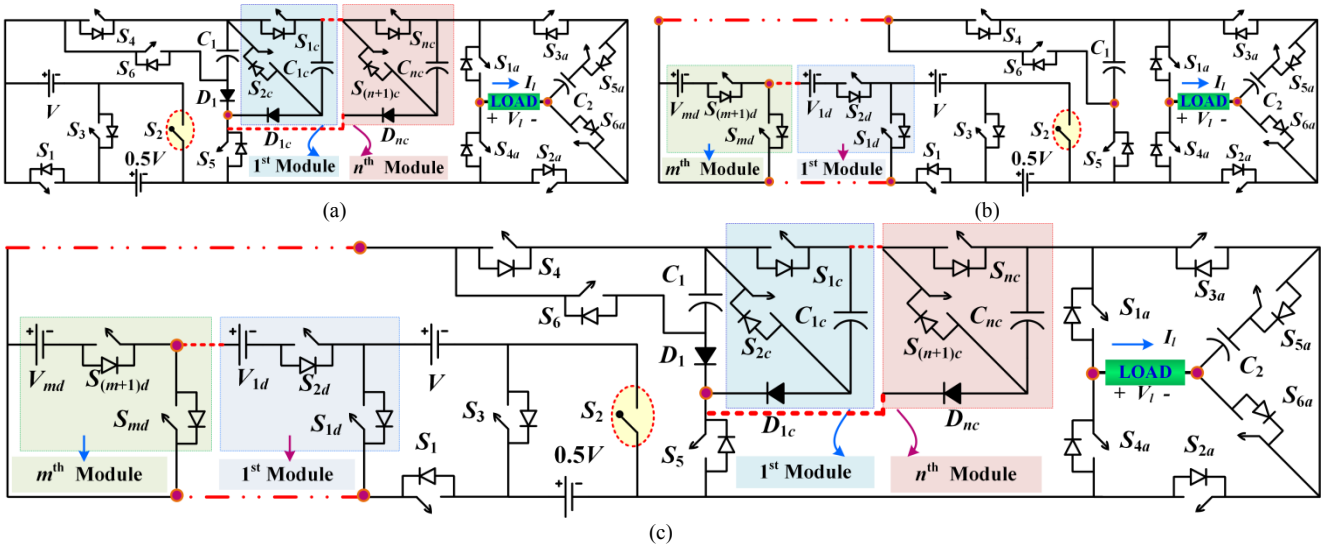

Fig.4. (a) Switched capacitor extension of the proposed DSC MLI (PE1), (b) switched dc source extension of the proposed DSC MLI (PE2), (c) switched capacitor and dc source extension of the proposed DSC MLI (PE3)

B. *Switched dc source extension* (PE2)

The generalized structure of the PE2 is shown in Fig. 4(b), where switched source (SS) modules are used to extend the proposed DSC MLI. The SS modules are the combination of two switches and one dc source. The dc source magnitude of these modules is symmetrically chosen, which is equal to the higher input source magnitude of the DSC MLI. The dc source V_{md} of m^{th} SS module is by-passed through the switch S_{md} and appears at the output when $S_{(m+1)d}$ switch is turned ON. The capacitor C_1 works in a similar principle as discussed in the earlier section. However, it is charged to the sum of input sources magnitude when all the dc sources are available to appear at the output. The required number of components in terms of the number of SS modules (m) is expressed in (14-18) along with the performance parameters of PE2 in (19-21).

$$N_{sw} = 2m + 13 \quad (14)$$

$$N_{driv} = 2m + 12 \quad (15)$$

$$N_{dd} = 0 \quad (16)$$

$$N_c = 2 \quad (17)$$

$$N_{dc} = m + 2 \quad (18)$$

$$TSS = \frac{26m+41}{2} \quad (19)$$

$$Gain = 2 \quad (20)$$

$$N_l = 16m + 25 \quad (21)$$

C. *Switched capacitor and dc source extension* (PE3)

The proposed MLI can also be extended by connecting both SC and SS modules to synthesize higher voltage levels. This combination is termed as PE3, which is shown in Fig 4(c). Individual module operation of PE3 is the same as disclosed for the PE1 and PE2 structures. All the capacitors used in the SC modules are equally charged to the sum of all the dc sources through the common charging switch S_5. The number of components involved in the PE3 structure is given in (22-26). The performance parameters TSS, gain, and N_l are expressed in (27-29).

$$N_{sw} = 2(m + n) + 13 \quad (22)$$

$$N_{driv} = 2(m + n + 6) \quad (23)$$

$$N_{dd} = n + 1 \quad (24)$$

$$N_c = n + 2 \quad (25)$$

$$N_{dc} = m + 2 \quad (26)$$

$$TSS = \frac{12mn+26m+18n+41}{2} \quad (27)$$

$$Gain = n + 2 \quad (28)$$

$$N_l = 8mn + 16m + 12n + 25 \quad (29)$$

IV. Comparative Analysis

A variety of MLI structures are developed in the recent past focusing on SC technique that enables boosting and self-balancing of the MLI. Moreover, TSS and component count in the MLIs are the key design constraints that need to be minimized. In this context, the excellence of the proposed topology is validated over the variety of MLIs presented in T1 [23], T2 [18], T3 [28], T4 [24], T5 [20], T6 [22], T7 [27], T8 [17], T9 [29], and T10 [16]. The comparisons are carried out with respect to N_l.

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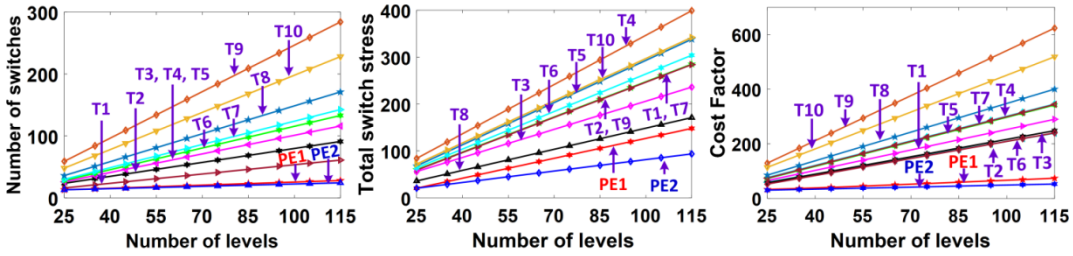
It is evident from Fig. 5(a) that the switch count of the T1 and T2 are lower than other MLIs, but it is still higher than the proposed MLIs PE1 & PE2. Fig. 5(b) demonstrates the TSS of all the MLIs against number of output voltage levels. TSS is calculated with an assumption that current rating of all the switches is same as the peak load current. The proposed PE1 and PE2 withstand the lowest TSS, which implies the applicability of the proposed topology in high voltage.



(a) (b) (c)

Fig.5. Comparison between the MLI topologies (a) N_{sw} against N_l,, (b) TSS against N_l, and (c) CF against N_l

TABLE II

COMPARISON OF THE 25-LEVEL SC MLIS

Parameters	[16]	[17]	[18]	[20]	[22]	[23]	[27]	[28]	[29]	Proposed DSC MLI
N_{sw}	48	36	37	26	28	16	30	26	59	13
N_{driv}	48	36	37	26	22	16	30	20	59	12
N_{dd}	0	6	0	10	0	22	6	3	0	0
N_c	12	6	11	10	4	11	6	6	11	2
N_{dc}	6	6	1	2	4	1	6	3	1	2
CF	114	86.5	85.56	72.94	56.67	65.42	74.5	57.33	129.41	30.42
ILA	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
Gain	1	2	12	6	2	12	2	2	12	2
TSS (x V_{dc})	72	60	81	68	64	60	60	56	59	20.5

In addition, design consideration of the proposed MLI structure is verified by comparing the MLIs in terms of the cost factor (CF) as given in (30). All the components involved in the MLI structure are included in calculating the CF. Per unit TSS per gain is also considered for a fair comparison among the SC-based MLI topologies. It is apparent from Fig. 5(c) that CF of PE1 and PE2 is the lowest among all the MLIs.

$$\mathrm{CF} = N_{sw} + N_{driv} + N_{dd} + N_c + \left(\alpha * \mathrm{TSS_{pu}}/\mathrm{Gain}\right) \qquad (30)$$

where α is the factor which is generally considered to decide importance between the number of components and TSS. α is chosen less than or greater than 1 based on the importance given either to the number of components or TSS, respectively. In this work, α is taken as 1 to keep a balance between both the parameters. A comparison of the 25-level SC MLIs is further carried out in Table II. The series-connected diodes in T1 block the negative current flow, which therefore lacks in inductive loading ability (ILA). Except T10, all other topologies including the proposed MLI have the boosting ability. Therefore, the proposed DSC MLI is a suitable alternative to synthesize high-quality output using less number of components.

V. CONTROL TECHNIQUES

To validate the operability, both the well-established fundamental frequency and high switching frequency control schemes are developed. In this regard, nearest level control (NLC) fundamental frequency control technique and sinusoidal pulse width modulation (SPWM) high-frequency control scheme are employed. NLC reduces the computational complexity on the controller for synthesizing higher voltage steps [22], [35]. Fig. 6 shows the block diagram of both the control schemes with the pulse logic for the DSC MLI.

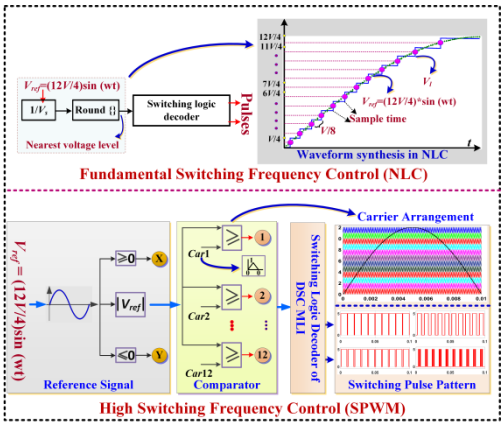


Fig.6. Block diagram of PWM control techniques for the DSC MLI

In NLC method, a sampled waveform is produced with the comparison of reference sinusoidal waveform and the desired staircase output waveform. Afterward, the controller rounds the sampled waveform to the nearest level based on the switching logic, as given in Table I. This process is again duplicated for each sampling instance. For the SPWM control technique [14], twelve carriers are disposed in the same phase with a finite offset value. This combination of carriers is compared with a sinusoidal reference signal in the comparator module. The pulse decoder circuit then generates the desired switching pulses with the appropriate switching logic.

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VI. SIMULATION ANALYSIS

Simulation analysis of the proposed 25-level DSC MLI is carried out in MATLAB/SIMULINK platform. Different dynamic tests are conducted to verify the feasibility of the DSC MLI by using the control techniques discussed in Section V. Considering the design analysis of capacitors shown in Fig. 3, the value of C_1 and C_2 are chosen as 4700 µF and 2200 µF, respectively assuming 5-7 % of voltage ripple, 50 Hz nominal frequency, unity power factor (PF) load, and 60 V as higher input source magnitude (V). All the parameters of the DSC MLI are listed in Table III.

TABLE III

SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Value
Input voltages	60 V (V), 30 V (0.5 V)
C_1, C_2	4700 µF, 2200 µF
R-load, RL-load, R_1L_1-load	80 Ω, 80 Ω - 250 mH, 80 Ω - 500 mH
Non-linear load	60 Ω -50 mH
f_o	50 Hz
f_{sw}	50 Hz (NLC) and 5 kHz (SPWM)

The working performance of the DSC MLI employing NLC control under different dynamic conditions is depicted in Fig. 7(a). It can be observed that loading is suddenly switched to inductive (RL-load) at 0.14 s from resistive loading (R-load). The smooth transition of voltage waveform verifies the satisfactory operation and control of the DSC MLI. The load current (I_l) waveform is identical to the load voltage (V_l) waveform shape during resistive loading; however, it attains the sinusoidal pattern for inductive loading. Further, the proposed MLI allows the reverse flow of current, which leads to the suitable operation at the time of low PF loading (R_1L_1-load) at 0.18 s. Further, for testing under non-linear loading condition, a diode bridge rectifier is fed from the MLI at 0.21 s, which therefore draws the non-linear current without affecting the output voltage. The reliable operation of the MLI is also tested under a dynamic change in output frequency (f_o) from 50 Hz to 100 Hz at 0.26 s. During this condition, the increase in frequency makes the proportional change in the inductive reactance and therefore, the output current magnitude decreases. In all the above test cases, capacitor voltages (V_{c1} and V_{c2}) are also depicted in Fig. 7. It is worth noting that, the ripple in the V_{c1} and V_{c2} reduces as the phase angle increases and is very less for high output frequency operation.

Fig. 7(b) shows the workability of the proposed MLI with SPWM control. Almost similar test conditions as shown in Fig. 7(a) are considered in this case. Carrier frequency is taken as 5 kHz with a nominal output frequency of 50 Hz. By changing the reference signal magnitude, modulation index (M_i) is changed at 0.14 s. During low M_i value (≈0.4), MLI works at a reduced voltage level, but the desired voltage levels are obtained at high M_i value. The switching frequency (f_{sw}) is reduced to half (2.5 kHz) at 0.26 s, thus the output voltage as well as the capacitor voltage ripples changes accordingly. Fig. 7(c) shows the harmonic spectra of load voltage and current under 80 Ω - 250 mH loading using the NLC scheme. Similar results are shown in Fig. 7(d) using the SPWM control technique. The resulted total harmonic distortion (THD) well-satisfies the IEEE-519 standard. Due to the high-switching operation, the current THD is significantly low using the SPWM control scheme as compared to the NLC scheme.

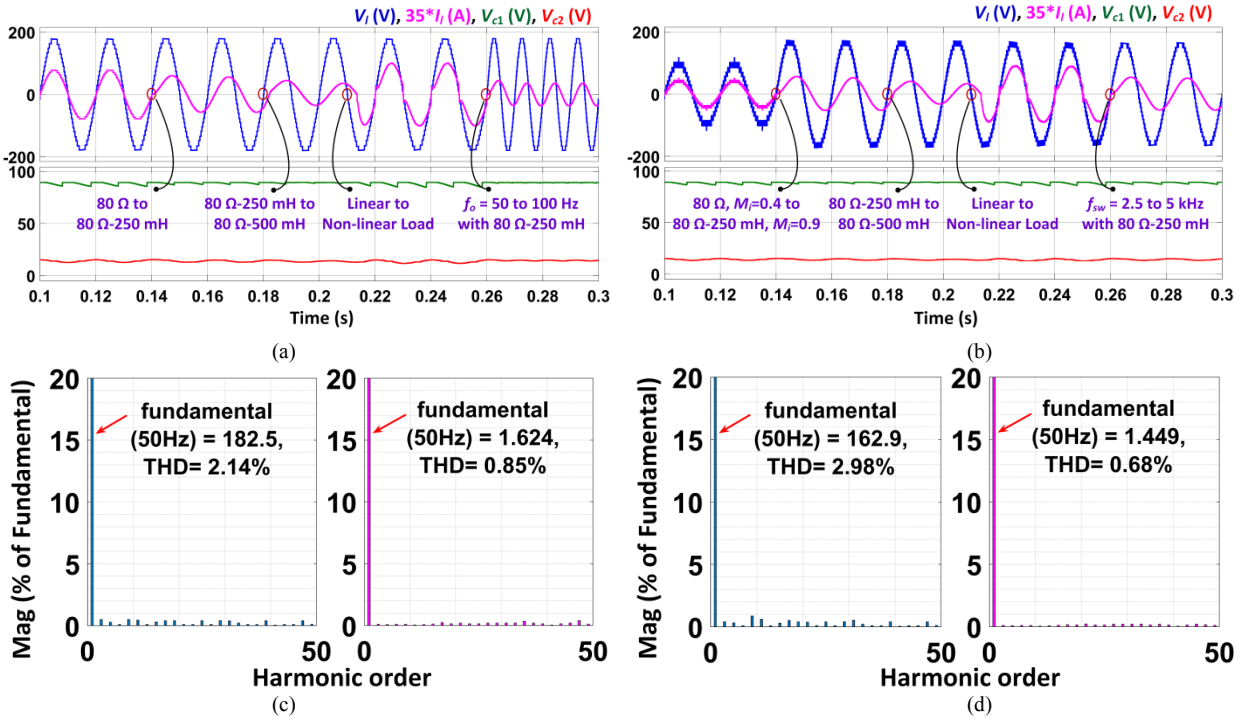

Fig.7. Dynamic simulation results under (a) NLC, (b) SPWM control technique, V_l and I_l harmonics under RL-load, (c) using NLC, (d) using SPWM control

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VII. Experimental Results

Theoretical and simulation findings are further validated experimentally with a developed small-scale laboratory prototype of the DSC MLI shown in Fig. 8. The 12N60A4D IGBT switches are utilized to device the 25-level DSC MLI. All the experimental parameters are considered as per Table III. A TMS320F28335 DSP controller is used for generating the real-time switching pulses, which are again amplified by TLP250 gate drivers. All the waveforms are captured using a YOKOGAWA ScopeCoder.

Fig. 9 shows the experimental results obtained using the NLC control scheme. The load voltage and load current waveforms along with the capacitor voltages are shown in Fig. 9(a) under *R*-load. The capacitor voltages are maintained at the desired value irrespective of the loading without using any external voltage balancing controller. The capacitor voltage ripples are certainly decreased with an increase in phase angle in Fig. 9(b) as the load is suddenly changed from *R* to *RL*-load without distortions in the load voltage. Fig. 9(c) implies the non-linear load handling ability of the proposed MLI. Except I_l, the shape and magnitude of V_l, V_{c1}, and V_{c2} remains unaffected. Similar test as done in simulation is performed to verify the practicality of the MLI with a change in frequency. Results are shown in Fig. 9(d) & (e) as the frequency changes from 100 Hz to nominal frequency 50 Hz under pure resistive loading and inductive loading, respectively. The magnitude of the I_l remains same under *R*-load, but it changes with *RL*-load because of the proportional change in inductive reactance. Voltage stress across different switches (S_1, S_2, S_3, S_4, S_5, S_6, S_{1a}, and S_{6a}) is depicted in Fig. 9(f) and the capacitor voltage ripples along with the currents are shown in Fig. 9(g). The load voltage and current harmonic spectra obtained under the *RL*-load in Fig. 9(h) and (i), respectively, closely match with the simulation results.

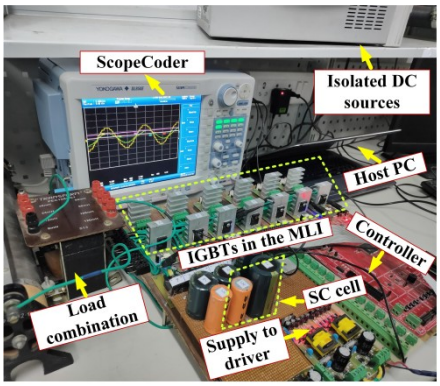

Fig.8. Experimental test setup developed in laboratory

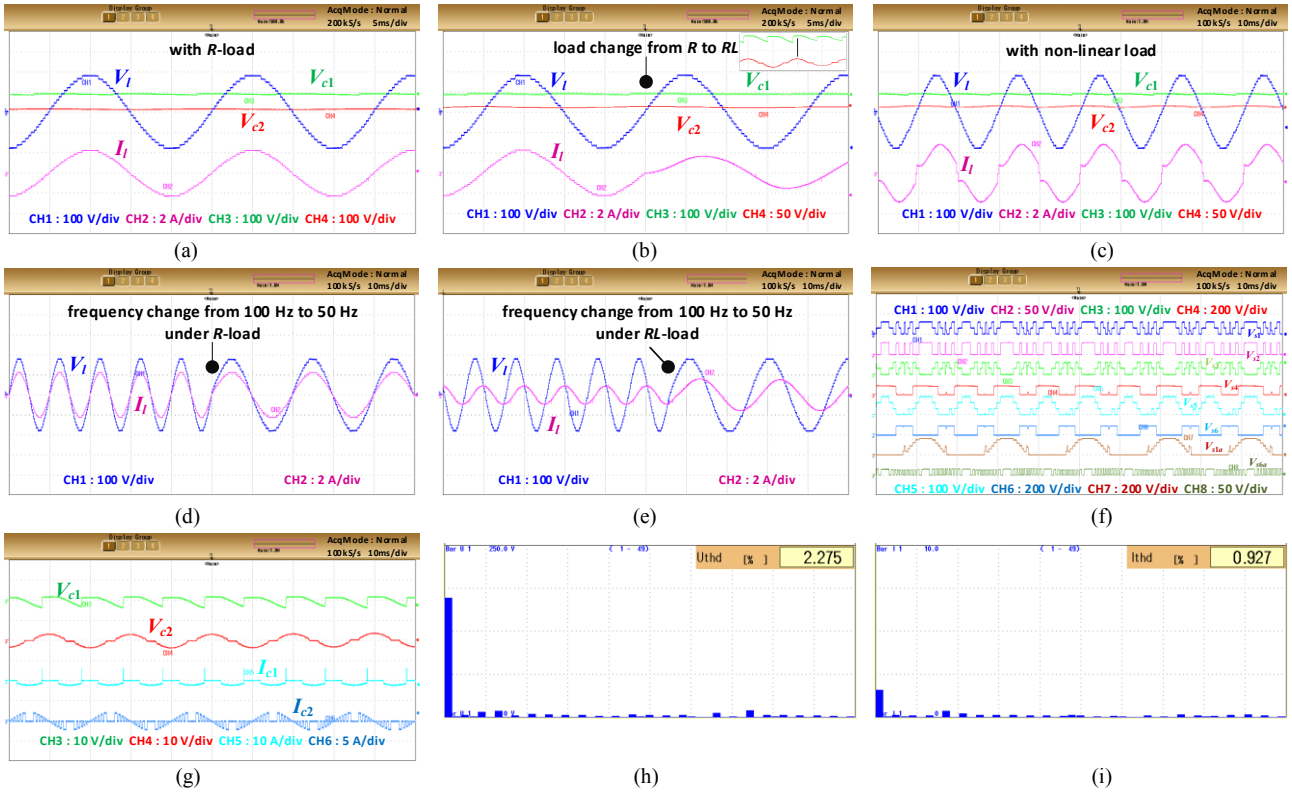

Fig.9. Experimental results using NLC scheme (a) V_l, I_l, V_{c1}, V_{c2}, under *R*-load, (b) V_l, I_l, V_{c1}, V_{c2}, with varying load, (c) V_l, I_l, V_{c1}, V_{c2}, with non-linear load, (d) V_l, I_l, V_{c1}, V_{c2}, with varying frequency under *R*-load, (e) V_l, I_l, V_{c1}, V_{c2}, with varying frequency under *RL*-load, (f) Voltage stress across the switches (S_1, S_2, S_3, S_4, S_5, S_6, S_{1a}, and S_{6a}), (g) Capacitor voltage ripple with current through the capacitors, (h) Voltage harmonics, (i) Current harmonics under *RL*-load

With the SPWM control scheme, test results are illustrated in Fig. 11. The output voltage shown in Fig. 10(a) is obtained under changing M_i condition with 80 Ω loading. Capacitor voltages are maintained constant, however fundamental value of load voltage and current changes. The loading is changed from *R*-load to *RL*-load in Fig. 10(b). The current waveform obtained is a clean sinusoidal waveform due to the high-switching and low-pass filter type load characteristics. The capacitor voltage ripples are also very less under the SPWM control method. Fig. 10(c) and (d) depicts the harmonic analysis of the load voltage and current, respectively. Fig. 10(e) presents the theoretical efficiency evaluation of the

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proposed MLI in comparison with the topologies T2, T4 and T7. Proposed topology has significantly higher efficiency due to the reduced total number of devices and low power losses. Fig. 10(f) shows the efficiency plot obtained using the WT 1800 power analyzer for a range of output capacity of the proposed MLI. The experimental result closely matches with the theoretical evaluation.

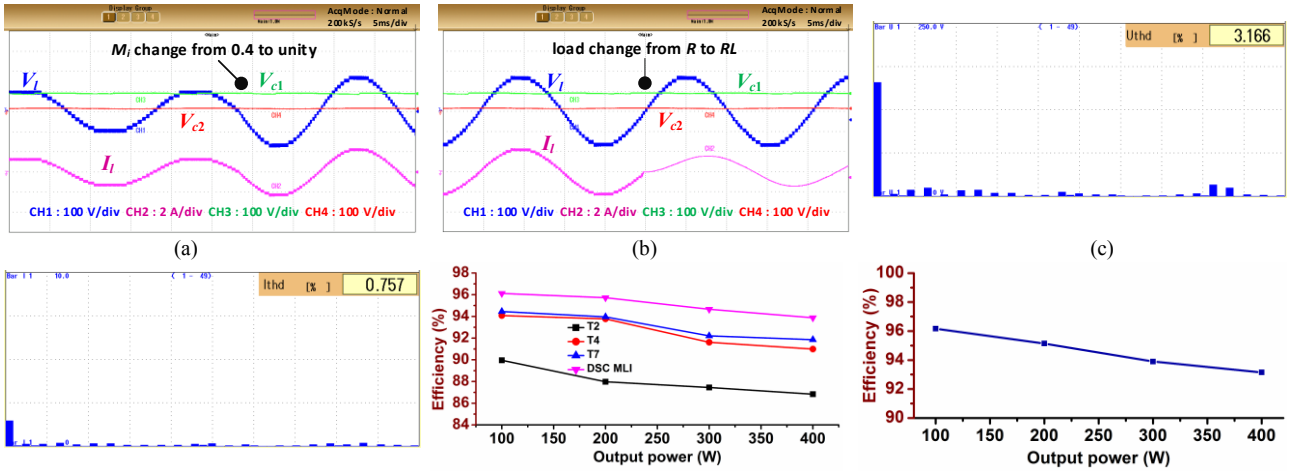

Fig.10. Experimental results using SPWM control (a) V_l, I_l,V_{c1},V_{c2}, with resistive loading and under varying *Mi* condition, (b) V_l, I_l, V_{c1}, andV_{c2} with variable loading condition, (c) Voltage harmonics, (d) Current harmonics under *RL*-load, (e) Theoretical efficiency comparison, (f) Experimental efficiency evaluation

VIII. Conclusion

In this work, a novel DSC MLI has been presented using a reduced number of switches and only two dc sources, which produce a 25-level staircase output. Capacitors are utilized to synthesize the voltage levels, which in turn reduces the source count significantly. The SCs are arranged in such a way that voltage boosting is achieved with no additional voltage balancing circuits. Thus, the proposed DSC MLI optimizes the overall size and the cost. Three possible extensions of the proposed structure for enhancing the number of voltage levels have been analyzed in detail. Comparative assessment with the well-known MLI topologies confirms the proposed topology utilizes fewer components and has low switch stress. Moreover, less than 50 % of the switches are in conduction for synthesizing any voltage level, which signifies lower conduction loss of the proposed MLI. Extensive simulation has been carried out under different dynamic test cases to verify the workability of the proposed MLI. Experimental test results further verify the feasibility of the 25-level MLI under different loading conditions, dynamic change in frequency and dynamic change in M_i. The proposed topology works satisfactorily under linear, non-linear loading and using different PWM control schemes.

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