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Virtual Resistance Trade-off Design for DCMG Grid-Forming Converters Considering Static and Large-Signal Dynamic Constraints

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***Abstract*—This study brings forward a design method of virtual resistance for droop-controlled dc microgrids (DCMGs). Although droop control is widely employed in coordinated DCMGs to coordinate different energy sources, few works address thoroughly the principles for a proper virtual resistance design. In this paper, dynamic stability and static voltage deviation constraints are taken into consideration as the main criteria to be complied with by the virtual resistance design. In critical cases, constant power loads (CPLs) may substantially decrease system damping and adversely affects the stability of the system. In this sense, the large-signal stability model is developed including CPLs by using the Lyapunov function and it is subsequently analyzed to infer the stability criterion. In studies, bus voltage is the most important index when addressing the DCMG control, hence the impact of virtual resistance on the voltage deviation is explored as well. This research founds out that virtual resistance influence on system stability is opposite to that on voltage deviation, thus a trade-off method based on the containment principle is developed. Throughout the proposed compromised design, we can adjust the weight coefficient to satisfy different performance requirements of DCMGs. The effectiveness of the proposed scheme is validated through experimental results.**

***Index Terms*—dc microgrids, droop control, compromised design, stability constraint, voltage deviation, Lyapunov function, containment-based method.**

I. Introduction

DCMG has been recognized as an effective approach of renewable energy seamless inclusion due to its simple structure, localized application, absence of power quality problems, and increased efficiency [1]-[2]. It has been used in many fields, including the power grid, industry, traffic, residential and commercial buildings, etc. [3]-[5]. A typical structure of DCMG is shown in Fig. 1, where distributed energy source, energy storage system, and terminal users are integrated together. Coordination among these components is becoming more attractive, resulting in many control strategies proposed, which can be broadly categorized into two groups, namely constant dc voltage control scheme also called master-slave control scheme [6]-[8]and droop control scheme [9]-[12]. The main drawback of the master-slave scheme is that a single-point failure may wear down the operation of the entire system, because it extremely relies on the master converter. Droop-controlled DCMG can operate with higher reliability since dc voltage regulation does not depend on a single converter.

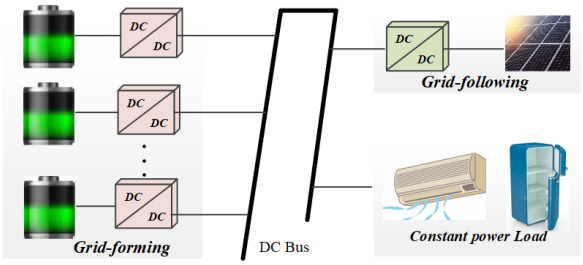

Fig. 1. Typical structure of a dc microgrid.

The objectives of coordination control mainly include power sharing and voltage regulation. By applying the droop-controlled scheme, it is easier for converters to provide power proportional to their power capacities avoiding overloaded or unreliability. Meanwhile, multiple converters are operated cooperatively to regulate bus voltage although it cannot maintain the voltage at the nominal value. With the expansion of DCMG's scale, more than one grid-forming converters (GC) are connected in parallel to provide enough capacity. Hence, the droop controller becomes more appropriate [13]-[16], since it is easier to eliminate the circulating current and to realize voltage compensation.

The hierarchical distributed control framework is widely employed in current researches, which is constituted by primary, secondary, and tertiary layers, and their different schemes are defined in [10-12], [15], and [16]. The droop controller is designed in the primary level to achieve roughly basic operation,

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and in the secondary level to achieve accurate power sharing and voltage regulation. The undertaking of the tertiary level mainly focuses on energy management, like power dispatching and economic optimization. The goals of the secondary and tertiary levels are achieved by generating adjusting strategies on virtual resistance. Hence, a reasonable range of virtual resistance should be specified.

By a careful investigation, the existing literature about virtual impedance design can be divided into two groups. The first group focus on dealing with the transient or steady properties of an ac microgrid, and the proposed methods are employed in a dc/ac converter [18]-[22], and the utilized model is commonly a small signal model. For example, [18] devotes to alleviating the voltage distortion firstly by a robust virtual resistance design and implementation, then further to improve the power control performance during the transient and grid faults by employing an adaptive resistance in a dc/ac converter. [19] prevents the coupling between the real and reactive powers through virtual impedance design, and then achieve accurate reactive power sharing. The virtual impendence is designed resistive in [20]-[22] to achieve better power sharing by reducing the sensitivity to the line impedance unbalances, not only active and reactive powers but also the harmonic content of the total loads. However, there is no frequency distortion and reactive power in dc microgrids, and the above method is not quite appropriate for dc microgrids.

The second group focus on power sharing and voltage regulation in dc microgrids in the hierarchical control structure, which generally only considers the static constraint and employed in dc/dc converters [9]-[17]. The virtual impedance in dc microgrids shows as a virtual resistance, which is designed proportionally to the capacity of converters to achieve power sharing and regulated in the secondary and tertiary levels to optimize voltage deviation [9]-[11], [14]. The original value is generally determined through voltage deviation divided by maximum current, without considering the dynamic influence of system components [12], [15], [17]. Even though if dynamic performance is considered in some works, virtual resistance is never the main objective, more efforts will be paid into improving the dynamic response by optimizing proportional and integral parameters [13], [16]. Besides, the relationship between virtual resistance and voltage deviation in these papers is generally reveled linear without considering the linearity of CPLs.

Different from previous works, the aim of this paper is to develop a proper method of virtual resistance design by considering static voltage deviation and dynamic stability constraints even in the case of CPL. The primary aim of controller design is to ensure the stability of the system, which is also a crucial issue for DCMG that cannot be ignored because of its weak inertia and damping [23]-[25]. Hence stability criterion is taken as one of the constraints. Regulating bus voltage operating in a reasonable range is the premise of the system normal operation, thus voltage deviation is taken as another criterion of virtual resistance design. It is easy to reveal the essence of how virtual resistance influences bus voltage, as discussed in Section IV, whereas stability not. Thus, more efforts will be paid in exploring the stability constraint in this paper.

Many studies about stability have been conducted, and the analysis method can be divided as small-signal analysis (SSA) [15], [26]-[28] and large-signal stability analysis (LSA) [29]-[34], but seldom of them engages in droop control. SSA generally analyzes system characteristics by studying the eigenvalues, Nyquist, and Routh-Hurwitz criterion, from which are not easy to figure out a quantitative relationship. On the other hand, LSA is applied in [29]-[34], but they are dedicated to designing proportional and integral parameters for a certain converter or a single-source system, not involved in virtual resistance design. [29]-[31] focus on the large-signal stability of dc/ac converters instead of dc/dc converters. [32] and [33] analyzes the large-signal stability of dc microgrids based on dc/dc converters, but not involved in the droop control strategy. [34] studies the large-signal stability of droop-controlled dc microgrids, but it does not reveal the relationship between virtual resistance and stability and not provide a method to design it.

Therefore, the feasible domain of virtual resistance design considering the constraints of large-signal stability and voltage deviation is researched in this paper, and the main contributions can be summarized as the following aspects.

1) Large-signal stability analysis model (LSM) considering CPL: CPL is considered in this paper since it will weaken down system damping and makes system nonlinear [8], [25]. SSA is based on linearizing the nonlinear system around an equilibrium point, and its validity and effectiveness are limited to a tiny domain around an equilibrium point, without an accurate indication of how large the tiny domain is. Hence, LSM based on the Lyapunov function [29] is established without that drawback.
2) Interaction analysis between CPL and virtual resistance: The stability criterion is derived, and the coupling of CPL and virtual resistance is further discussed, which is nonlinear and not easy to make out intuitively but can be dealt with by figure and numeral calculations in four typical situations. The relationship between these two items can not only provide guidance in the primary level, but also in the secondary and tertiary levels.
3) Comprised design of the virtual resistance value: Static voltage deviation constraints are taken into account, and the feasible domain of virtual resistance is then explored. Since the upper bound and low bound is determined, and stability margin related to virtual resistance is reduced when voltage deviation is smaller, hence a comprised design method to deal with this trade-off is developed based on the containment principle [35], and different system requirements can be satisfied by tuning weight coefficient.

This paper is structured as follows. Section II simplifies the structure of DCMGs and develops LSM based on the Lyapunov function. Section III derives the coupling relationship between CPL and virtual resistance by analyzing stability criterion. Comprised design based on the containment method is proposed in Section IV. Experimental results are presented to prove the validity of the proposed design method in Section V.

Finally, conclusions are drawn in Section VI.

II. Large Signal Model of DC Microgrid

A. Description of the Microgrid System

In a multi-GC paralleled operation DCMG, the droop control strategy is widely employed. For instance, when having n paralleled converters in parallel, each of them can be controlled by using a droop scheme, implemented in an equivalent resistance form. For the k_{th} GC, in the steady-state, its output characteristics can be described as

$$u = U_{\text{rate}} - r_k i_k , \tag{1}$$

where U_{rate} is the nominal voltage, u is the bus voltage, i_k is the output current, and r_k is the sum of the virtual resistance (r_{vk}) and the feeder resistance (r_{fk}), that is

$$r_k = r_{vk} + r_{fk} . \tag{2}$$

According to (1), the external characteristic of the k_{th} GC can be conceived as a Thevenin equivalent circuit consisting of a dc source and a comprehensive resistance.

In the hierarchical distributed control strategy of DCMG, voltage regulation and current sharing are two important objectives [12], [16]. The current sharing of GCs should be achieved proportionally to their capacity, which means their virtual resistances should be chosen proportional to the feeder resistances [17]. However, the feeder resistances of GCs are usually the fixed values, and the proportion of them is fixed and not certainly the same as the proportion of the GCs' capacity. Therefore, to get rid of the limitation of the feeder resistances, the virtual resistances are usually designed much larger than the feeder resistances [32] in a relatively small system. It can be illustrated by

$$\begin{aligned} i_1 : i_2 : \cdots : i_n &= \frac{1}{r_{v1}+r_{f1}} : \frac{1}{r_{v2}+r_{f2}} : \cdots : \frac{1}{r_{vn}+r_{fn}} \\ &\overset{r_f \ll r_v}{=} \frac{1}{r_{v1}} : \frac{1}{r_{v2}} : \cdots : \frac{1}{r_{vn}} \end{aligned} . \tag{3}$$

It can be seen that, when r_{vk} is much larger than r_{fk}, the influence of feeder resistances can be ignored. As for the larger-feeder DCMGs, since the feeder resistances are considerable, it is not recommended to design much larger virtual resistance, otherwise the system stability will be challenged. Thus, to ensure the design freedom and system stability, some insightful solutions, e.g. the average-voltage method in [12] and [17], can be deployed to eliminate the influence of feeder resistances. Therefore, in the following analysis, r_{fk} is ignored and let r_k only denote r_{vk}.

For a multi-GC parallel operation system as shown in Fig. 1, assuming i is the sum of the output current of all GCs, it can be expressed as

$$i = \sum_{k=1}^{n} i_k = \left(U_{\text{rate}} - u\right) \sum_{k=1}^{n} \frac{1}{r_k} . \tag{4}$$

Hence, the equivalent virtual resistance can be expressed as

$$r = 1 \Big/ \sum_{k=1}^{n} \frac{1}{r_k} . \tag{5}$$

Considering the condition [14] that

$$\frac{r_1}{L_1} \approx \frac{r_2}{L_2} \approx \cdots \approx \frac{r_n}{L_n} , \tag{6}$$

we can obtain the equivalent current dynamics by combining (4), (5), and (6), as

$$\frac{\mathrm{d}i_{\text{eq}}}{\mathrm{d}t} = \left(U_{\text{rate}} - u\right) \sum_{k=1}^{n} \frac{1}{L_k} - i_{\text{eq}} \sum_{k=1}^{n} \frac{1}{L_k} \Big/ \sum_{k=1}^{n} \frac{1}{r_k} . \tag{7}$$

Thus, the equivalent inductance L can be approximately given by

$$L = 1 \Big/ \sum_{k=1}^{n} \frac{1}{L_k} . \tag{8}$$

Then, substituting (8) into (7), it can be reformulated as

$$\frac{\mathrm{d}i}{\mathrm{d}t} = \frac{1}{L}\left(U_{\text{rate}} - u - ri\right) . \tag{9}$$

Therefore, a droop-controlled multi-GC parallel operation storage system can be also equivalent to the series connection of a dc source, a virtual resistance, and an inductance.

Due to the inner tight feedback controller, most of the loads in DCMG exhibiting constant power characteristics, and their capacity is much more than that of the resistance loads. Besides, the transient negative resistance of CPL will weaken the stability of the system, whereas the resistance loads will enhance its stability [36], and with the development of power electronic technologies, CPL will account for an increasing proportion in DCMG. Therefore, the worst condition should be considered in stability analysis and parameter design. Hence, the loads in DCMG modeled as CPLs. In terms of the distributed sources mostly operating in the MPPT mode, it can be modeled with the loads together as the equivalent CPLs. Therefore, the model of DCMG can be described as Fig. 2, where P is the value of CPL, and C is the equivalent capacitance connected parallel to the dc bus. Besides, u_{C} is capacitance voltage, i.e., the bus voltage, i_{L} is inductance current, $i=P/u_{\text{C}}$ is equivalent load current, and $i=i_{\text{L}}$ in the steady-state.

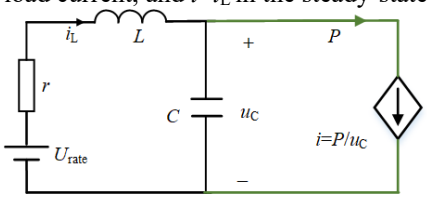

Fig. 2. The equivalent model of a dc microgrid.

B. Lyapunov-based model of a dc Microgrid

Since the studied DCMG with CPL connection exhibits nonlinear characteristics from Fig. 2, the Lyapunov-based method is employed to explore its large-signal stability. Assuming $\boldsymbol{x}_{\text{e}}=[i_{\text{Le}}, u_{\text{Ce}}]^{\text{T}}$ is the equilibrium point of the system, and $\boldsymbol{x} = [i_{\text{L}}, u_{\text{C}}]^{\text{T}}$ is the state variables, the mathematical model of the system can be derived as

$$\dot{\boldsymbol{x}} = \boldsymbol{J}\boldsymbol{x} + \boldsymbol{B} \tag{10}$$

where

$$\boldsymbol{J} = \begin{bmatrix} -r/L & -1/L \\ \dfrac{1}{C} & \dfrac{P}{Cu_{\text{C}}^2} \end{bmatrix}_{x_{\text{e}}} , \quad \boldsymbol{B} = \left[\frac{U_{\text{rate}}}{L} \quad \frac{-P}{Cu_{\text{C}}} \right]^{\text{T}}_{x_{\text{e}}} \tag{11}$$

According to the Lyapunov's second method, for a given

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nonlinear system, if a Lyapunov function $\boldsymbol{V}(\boldsymbol{x})$ is found to be a positive definite matrix and meanwhile its derivative is a negative definite matrix, then the system can be judged small-signal stable at the equilibrium point. Especially, if the condition that $\boldsymbol{V}(\boldsymbol{x})\to\infty$ when $\|\boldsymbol{x}\|\to\infty$ could be further satisfied, the system is believed large-signal stable. Hence in this study, the stability analysis can be processed as follows.

To employ the Lyapunov-based method, the model of the system can be reformed as

$$\dot{\boldsymbol{x}} = \boldsymbol{\Phi}(\boldsymbol{x}) = \begin{bmatrix} \phi_1 & \phi_2 \end{bmatrix}^{\mathrm{T}}, \tag{12}$$

and

$$\dot{\boldsymbol{\Phi}}(\boldsymbol{x}) = \frac{\partial \boldsymbol{\Phi}(\boldsymbol{x})}{\partial \boldsymbol{x}} \dot{\boldsymbol{x}} = \boldsymbol{J}\boldsymbol{\Phi}(\boldsymbol{x}). \tag{13}$$

The Lyapunov function can be constructed as

$$V(\boldsymbol{x}) = \dot{\boldsymbol{x}}^{\mathrm{T}} \boldsymbol{H} \dot{\boldsymbol{x}} = \boldsymbol{\Phi}(\boldsymbol{x})^{\mathrm{T}} \boldsymbol{H} \boldsymbol{\Phi}(\boldsymbol{x}), \tag{14}$$

where $\boldsymbol{H}$ is positive definite, thus $\boldsymbol{V}(\boldsymbol{x})$ is also positive definite. The full derivative of $\boldsymbol{V}(\boldsymbol{x})$ for t can be calculated as

$$\dot{V}(\boldsymbol{x}) = -\boldsymbol{\Phi}(\boldsymbol{x})^{\mathrm{T}} \boldsymbol{Q}(\boldsymbol{x}) \boldsymbol{\Phi}(\boldsymbol{x}), \tag{15}$$

and

$$\boldsymbol{Q}(\boldsymbol{x}) = -[\boldsymbol{J}^{\mathrm{T}}\boldsymbol{H} + \boldsymbol{H}\boldsymbol{J}]. \tag{16}$$

To ensure the progressive stability of the system under small disturbance, the negative definiteness of $\dot{\boldsymbol{V}}(\boldsymbol{x})$ must be guaranteed. Therefore, we select $\boldsymbol{Q}(\boldsymbol{x})=\boldsymbol{I}$, and then $\boldsymbol{H}$ can be derived as

$$\boldsymbol{H} = \begin{bmatrix} h_{\mathrm{a}} & h_{\mathrm{b}} \\ h_{\mathrm{c}} & h_{\mathrm{d}} \end{bmatrix} = \frac{\boldsymbol{I} + det(\boldsymbol{J})(\boldsymbol{J}\boldsymbol{J}^{\mathrm{T}})^{-1}}{-2Tr(\boldsymbol{J})}, \tag{17}$$

where $det(\boldsymbol{J})$ is the determinant of $\boldsymbol{J}$, $Tr(\boldsymbol{J})$ is the trace of $\boldsymbol{J}$, and $\boldsymbol{I}$ is the unit matrix. The symbolic expression of $\boldsymbol{H}$ is provided in the Appendix, and easy to find $h_{\mathrm{b}}=h_{\mathrm{c}}$. To ensure the positive definiteness of $\boldsymbol{H}$, its elements should satisfy

$$\begin{cases} \Delta_1 = h_{\mathrm{a}} > 0 \\ \Delta_2 = h_{\mathrm{a}} h_{\mathrm{d}} - h_{\mathrm{b}}^2 > 0 \end{cases}, \tag{18}$$

which means

$$\begin{cases} rP/u_{\mathrm{Ce}}^2 < 1 \\ rP/u_{\mathrm{Ce}}^2 < r^2 C/L \end{cases}. \tag{19}$$

That is, under this condition the system will be of small-signal stability. To further verify the stability under large disturbance, $\boldsymbol{H}$ can be rewritten as

$$\boldsymbol{H} = \begin{bmatrix} h_{\mathrm{a0}} + h_{\mathrm{a1}} & h_{\mathrm{b}} \\ h_{\mathrm{b}} & h_{\mathrm{d0}} + h_{\mathrm{d1}} \end{bmatrix}. \tag{20}$$

It can be seen from (18) and (19) that, there are $h_{\mathrm{a0}}h_{\mathrm{c0}}=h_{\mathrm{b}}^2$ and $min\{h_{\mathrm{a0}}, h_{\mathrm{a1}}, h_{\mathrm{d0}}, h_{\mathrm{d1}}\}\geq 0$ simultaneously existing, therefore $\boldsymbol{V}(\boldsymbol{x})$ can be calculated as

$$\begin{aligned} \boldsymbol{V}(\boldsymbol{x}) &= h_{\mathrm{a}}\phi_1^2 + 2h_{\mathrm{b}}\phi_1\phi_2 + h_{\mathrm{d}}\phi_2^2 \\ &= (\sqrt{h_{\mathrm{a0}}}\phi_1 + \sqrt{h_{\mathrm{d0}}}\phi_2)^2 + h_{\mathrm{a1}}\phi_1^2 + h_{\mathrm{d1}}\phi_2^2 \end{aligned}. \tag{21}$$

Obviously, $\boldsymbol{V}(\boldsymbol{x})$ will tend to positive infinity when $\|\boldsymbol{x}\|\to\infty$. It means the system is of large-signal stability under the condition of (19).

III. Stability Constraint Analysis

From (19), the feasible domain of virtual resistance is related to x_{e}, but a nonlinear system may have more than one equilibrium point. The possible equilibrium points are shown in Fig. 3. Considering the resistance loads are much less than the CPLs in the practical situations, the characteristics of loads can be approximately shown by an inversely proportional curve. Due to droop control characteristic, the output current corresponding to bus voltage is a linear function, whose slope is r and the intercept is U_{rate}, shown by the straight line.

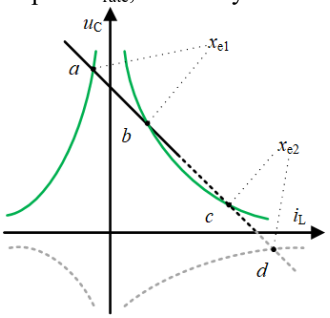

Fig. 3. The distribution of dc microgrid equilibrium points.

The equilibrium points of system can be derived as

$$\begin{cases} \boldsymbol{x}_{\mathrm{e1}} = \begin{bmatrix} P/u_{\mathrm{Ce1}} & (U_{\mathrm{rate}} + w)/2 \end{bmatrix} \\ \boldsymbol{x}_{\mathrm{e2}} = \begin{bmatrix} P/u_{\mathrm{Ce2}} & (U_{\mathrm{rate}} - w)/2 \end{bmatrix} \end{cases}, \tag{22}$$

where

$$w = \sqrt{U_{\mathrm{rate}}^2 - 4rP}. \tag{23}$$

From the derivation process, it can be easily known that a and $b \in x_{\mathrm{e1}}$, whereas c and $d \in x_{\mathrm{e2}}$. However, the dc bus voltage should be positive, thus only the upper half-plane makes sense. Since r is positive, from (19) it can be seen that the system is always stable when $P<0$, that is, point a is a stable equilibrium point. Therefore, only points b and c will be further studied in the following discussion.

A. Stability Analysis of Point c

Under the condition of $r^2C/L>1$, to make the system stable, point c has to satisfy the constraint of the first sub-formula of (19). Therefore, substitute x_{e2} into (19), and it can be derived

$$w - U_{\mathrm{rate}} > 0, \tag{24}$$

which is contrary to (23), leading to no real solution existing in (22). Hence, point c cannot satisfy the constraint and it is unstable.

B. Stability Analysis of Point b

The analysis is similar for point b. When $r^2C/L>1$, to make the system stable, point b has to satisfy the constraint of the first sub-formula of (19). Therefore, substitute point b into the first sub-formula of (19), and it can be simplified as

$$w + U_{\mathrm{rate}} > 0. \tag{25}$$

It is always been satisfied under the condition of (23). That is, when $r^2C/L>1$, point b is always stable.

On the other hand, when $r^2C/L<1$, point b has to satisfy the constraint of the second sub-formula of (19). Therefore, substitute x_{e1} into (18), and it can be derived

$$\frac{2L + 2r^2C}{rC} \cdot P - U_{\mathrm{rate}}^2 < U_{\mathrm{rate}} w. \tag{26}$$

If the left part formula is negative, that is,

$$(L+r^2C)P < 2r^2C\cdot\frac{U_{\text{rate}}^2}{4r}. \tag{27}$$

Then, (26) will always be satisfied. Else, P needs to satisfy

$$2r^2C\cdot\frac{U_{\text{rate}}^2}{4r} < (L+r^2C)P < \frac{2L}{L+r^2C}\cdot 2r^2C\cdot\frac{U_{\text{rate}}^2}{4r}. \tag{28}$$

Particularly, it is easy to prove that

$$2L/(L+r^2C) > 1. \tag{29}$$

Hence, the inequality relationship of (28) is correctly established. To summarize, when $r^2C/L<1$, point b is large-signal stable under the following condition, that

$$\left(L+r^2C\right)^2 P < rCL\cdot U_{\text{rate}}^2. \tag{30}$$

IV. Trade-off Design of Virtual Resistance

According to the analysis in Section III, when $P>0$, the selection of virtual resistance should satisfy both of the two following conditions, that

$$\begin{cases} 4rP < U_{\text{rate}}^2, & r > r_0 \\ \left(L+r^2C\right)^2 P < rCL\cdot U_{\text{rate}}^2, & r < r_0 \end{cases}. \tag{31}$$

where $r_0=\sqrt{L/C}$. It is not easy to intuitively observe how to select the value of r, but many mathematical solutions such as Newton iteration and Graphical method can be used to solve it.

A. Feasible Domain of Virtual Resistance

In the hierarchical distributed control strategy of DCMG, voltage regulation is one of the optimized objectives. Thus, the voltage deviation should be taken into account in the parameter design. To illustrate the feasible domain under different conditions, four circumstances are analyzed under both the constraints of stability and voltage deviation as shown in Fig. 4.

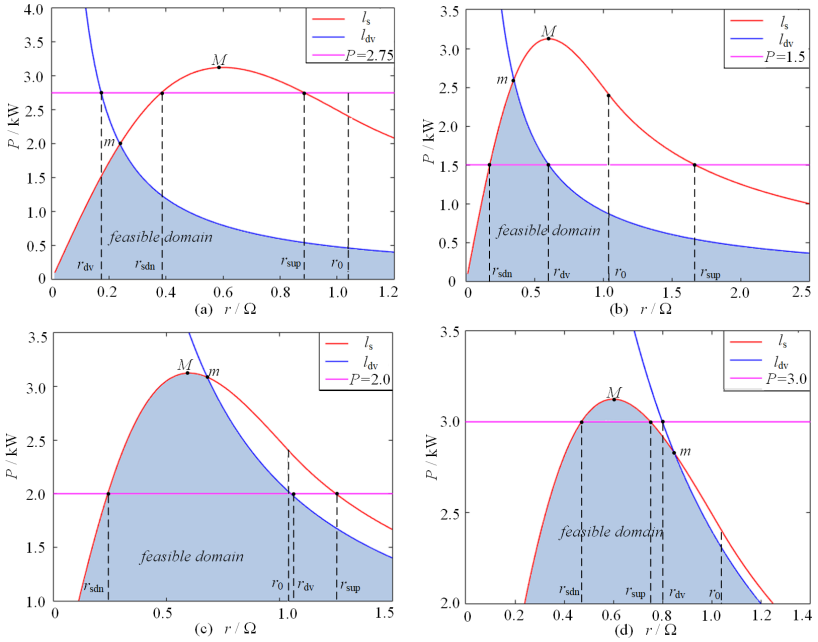

Fig. 4. The feasible domain of virtual resistance under constraints of stability and voltage deviation simultaneously. (a) $r_m<r_{\text{sdn}}$, and system is unstable. (b) $r_{\text{sdn}}<r_m<r_M$, and system is stable. (c) $r_M<r_m<r_{\text{sup}}$, system is stable. (d) $r_{\text{sup}}<r_m$, system is stable.

The parameters are listed in Table I. It can be seen that under both constraints, the feasible domain will be narrowed down to the intersection below the two curves, as shown in the shaded area.

TABLE I
Parameters of Cases

Case	*a*	*b*	*c*	*d*
Voltage deviation	5V	10V	20V	30V
P	2.75kW	1.5kW	2.0kW	3.0kW

L is 0.54mH, *C* is 0.50mF, and U_{rate} is 100V.

For the convenience of expression, the intersection point of the stability constraint curve (l_s) and the voltage deviation constraint line (l_{dv}) is defined as m (r_m, P_m). In this situation, intersection points will differ from each other under different voltage deviation constraints, as shown in Fig. 4. In addition, from the second sub-formula of (31), it can be derived the following relationship that

$$\frac{\partial P}{\partial r} = \frac{CLU^2}{\left(L+r^2C\right)^2}\cdot\frac{L-3r^2C}{L+r^2C}. \tag{32}$$

Let (32) be zero, and it can be got that l_s will achieve the peak value when $r=r_M=r_0/\sqrt{3}$, where M (r_M, P_M) is the peak point.

Further analysis shows that the shadowed area is the largest feasible domain under both constraints. However, the feasible domain will be reduced to [r_{sdn}, r_{sup}] at a certain load condition, where r_{sdn} and r_{sup} are the abscissa of the two intersections of l_s and the CPL curve. The initial CPL curve can be got by load capacity evaluation in the design stage of a dc microgrid to calculate an initial r_{sdn}. And in the operation stage, the hierarchical control structure of a dc microgrid will collect power information from GCs to dynamically modify the curve to achieve an accurate r_{sdn}. It can be seen from Fig. 4 that point m may distribute at both sides of point M under different voltage deviation constraint, resulting in the following circumstances.

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1) In Fig. 4(a), $r_m<r_{sdn}$. The requirement by voltage deviation constraint is $r<r_{dv}$, which does not belong to $[r_{sdn}, r_{sup}]$, where r_{dv} is the abscissa of the intersection of l_{dv} and CPL curve, hence no suitable virtual resistance can be selected.
2) In Fig. 4(b), $r_{sdn}<r_m<r_M$, where $r_{dv}\in[r_{sdn}, r_{sup}]$, the feasible domain decreases as $[r_{sdn}, r_{dv}]$, and the maximum allowable CPL occurs at $r=r_m$.
3) In Fig. 4(c), $r_M<r_m<r_{sup}$, and $r_{dv}\in[r_{sdn}, r_{sup}]$. The feasible domain is $[r_{sdn}, r_{dv}]$, and the maximum allowable CPL occurs at $r=r_M$.
4) In Fig. 4(d), $r_{sup}<r_m$, and $r_{dv}>r_{sup}$. In this circumstance, deviation constraint does not influence the feasible domain, and the range is $[r_{sdn}, r_{sup}]$. The maximum allowable CPL occurs at $r=r_M$.

From the above analysis, the maximum allowable CPL occurs at $r=r_M$ or $r=r_m$. Let P_{max} denote the maximum value, then it can be calculated in the following two situations.

1) If $r_m>r_M$, the maximum power point is at point M, that is, $P_{max}=P_M$. It can be derived that

$$r_M = r_0/\sqrt{3} = \sqrt{\frac{L}{3C}}. \tag{33}$$

Therefore, P_{max} can be calculated as

$$P_{max} = \left.\frac{rCL\cdot U_{rate}^2}{\left(L+r^2C\right)^2}\right|_{r=r_M} = \frac{3\sqrt{3}}{16}\sqrt{\frac{C}{L}}U_{rate}^2,\ r_m>r_M. \tag{34}$$

2) If $r_m<r_M$, the maximum power point is at point m, that is $P_{max}=P_m$, which is the mathematical solution of

$$\begin{cases} r=\Delta u\left(U_{rate}-\Delta u\right)/P \\ \left(L+r^2C\right)^2 P = rCL\cdot U_{rate}^2 \end{cases},\ r_m<r_M, \tag{35}$$

where $\Delta u=U_{rate}-u_C$ is the voltage deviation. It is not easy to directly figure out the solution, but it can be easily solved by the Graphical method.

Therefore, the P_{max} can be summarized as

$$\begin{cases} P_{max}=P_M,\ r_m>r_M \\ P_{max}=P_m,\ r_m<r_M \end{cases}. \tag{36}$$

To estimate the stability level under a certain circumstance, we define the stability margin (M_P) to illustrate how many additional loads the system can tolerate. Therefore, it can be depicted as

$$\Delta P=P_{max}-P,\ M_P=\Delta P/P_{max} \tag{37}$$

Let r_{P_max} denote the abscissa of P_{max}. To maximize the stability margin, r_{P_max} should be selected as r_m in Fig. 4(b) and r_M in Figs. 4(c) and (d).

B. Trade-off Design of Virtual Resistance

Minimizing voltage deviation is an important objective of optimization in the hierarchical control system, hence it is considered in virtual resistance design. From (35), the relationship between virtual resistance and voltage deviation can be expressed as

$$rP=\left(U_{rate}-\Delta u\right)\Delta u,\ \Delta uP>0, \tag{38}$$

and the schematic diagram is shown in Fig. 5. From this figure, it can be seen that whether CPL is positive or negative, the absolute value of voltage deviation will become larger as virtual resistance increases. Hence, it is necessary to select a possibly smaller value for virtual resistance in the feasible domain, which is not completely the same as the selected value when only considering the stability margin.

However, it is easy to nail down the upper bound and low bound of the feasible domain of virtual resistance. Combining the analysis of Fig. 5, and in the sense of decreasing voltage deviation, the feasible domain should be reduced to $[r_{sdn}, r_{P\_max}]$. It is easy to understand that, when $r\in[r_{sdn}, r_{P\_max}]$, increasing r will increase the stability margin (see Fig. 4), and reducing r will decrease the voltage deviation (see Fig.5). Therefore, to achieve different requirements of the system, a compromised design method [12] based on containment theory [28] is properly adopted to balance this trade-off.

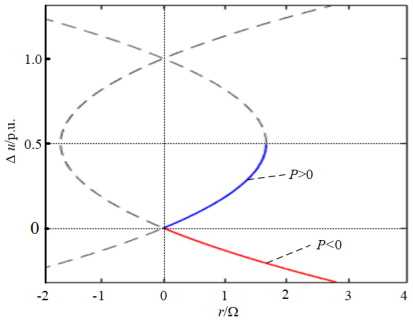

Fig. 5. The relationship between voltage deviation and virtual resistance.

According to containment theory, for a real vector space $\Re^n$, where $\overrightarrow{OB_d}, \overrightarrow{OB_u} \subseteq \Re^n$, if variable $\overrightarrow{Ov}$ satisfies

$$\overrightarrow{Ov} = \omega\overrightarrow{OB_d}+(1-\omega)\overrightarrow{OB_u} \tag{39}$$

there must be point v on $\overrightarrow{B_dB_u}$, where $\omega\in[0, 1]$. The theory can be clearly explained in a two-dimensional plane, as shown in Fig. 6, where $\overrightarrow{OB_d}$, $\overrightarrow{OB_u}$ are two boundary vectors, and $\overrightarrow{B_dB_u}=\overrightarrow{OB_u}-\overrightarrow{OB_d}$ is another boundary. It can be seen that when the variable $\overrightarrow{Ov}$ satisfies (29), the point v must be contained in $\overrightarrow{B_dB_u}$.

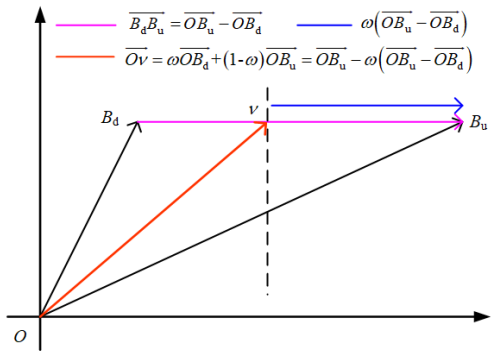

Fig. 6. The explanation for the containment theory.

Particularly, if n=1, point v must be contained in the segment $\overrightarrow{B_dB_u}$, that is $v\in[B_d, B_u]$. Therefore, we can design the virtual resistance as

$$r=\omega r_{sdn}+(1-\omega)r_{P\_max} \tag{40}$$

to satisfy different requirements of the system, where we can

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increase ω to reduce the voltage deviation, or reduce it to enlarge the stability margin. Then, we can define $P'_{\max}$ to denote the maximum allowed power loads when r is designed by (40), which can be easily got from the Graphical method or the second sub-formula of (31). And when r is designed by (40), the current stability margin M'_P can be defined as

$$M'_P = \left(P'_{\max} - P\right) / P'_{\max} . \quad (41)$$

C. Case-Explanation of the Proposed Method

Taking the circumstance in Fig. 4(b) as an example to illustrate the usage of the proposed method, where the minimized voltage limited by l_{dv} is set as 90V, and the original loads are 1.5kW (the 1.8kW and 2.2kW CPLs are only used in the following experimental tests in Section V). The bounds that r_{sdn}=0.24 and r_{P_max}=0.60 can be got from that figure.

Three cases (*A*, *B*, and *C*) are used to explain how the method functions. In these cases, ω is successively set as 0.6, 0.9, and 0.2, and the virtual resistance can be calculated by (40). The P'_{max} can be figured out by the second sub-formula of (31). The M'_p can be calculated by (41), and Δu can be calculated by (38). All the calculation results are listed in Table II, and they can also be easily figured out by Fig. 7.

From Table II and Fig. 7, it can be seen that the voltage deviation and stability margin decrease simultaneously as ω increases. That means, we can decreaseω to increase the stability margin, and increase ω to achieve less voltage deviation. Detailly, compared to case A, case B has a less voltage deviation because it has the larger ω, and case C has a larger stability margin because it has the smaller ω. Therefore, we can achieve different requirements of the system by adjusting ω.

TABLE II
PARAMETERS OF CASES *A*, *B*, AND *C*

Boundary	Case	ω	r	$P'_{\max}$	M'_P	Δu
r_{sdn}=0.17 r_{P_max}=0.35	*A*	0.6	0.24Ω	2.01kW	0.25	3.8V
	B	0.9	0.19Ω	1.63kW	0.08	3.0V
	C	0.2	0.31Ω	2.43kW	0.38	4.8V

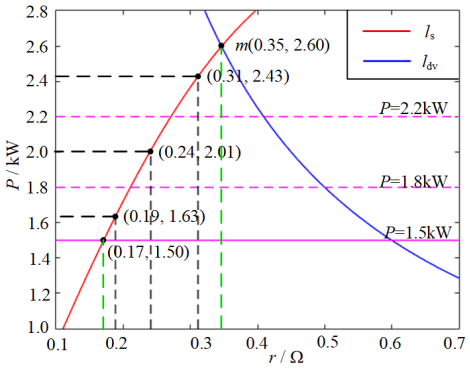

Fig. 7. Feasible domain analysis of cases *A*, *B*, and *C*.

D. The Influence of Resistive Loads

Considering that in the practical situation a few resistive loads and CPLs may exist simultaneously, therefore, the influence of resistance loads is analyzed. As studied in [36], the resistance loads will increase the damping of the system. Hence, the allowable maximum CPLs constrained by stability increases when resistance loads are connected. Taking case A as an example, when some resistive loads are connected the bus, the system can carry more CPLs under the stability constraint. The constraints can be expressed by reformulating (31) and (38) as

$$\begin{cases} 4rP < \dfrac{R}{R+r} U_{\text{rate}}^2, \ r > r_0 \\ \left(r^2CR + r + LR + rL\right)^2 P < LR\left(rCR+1\right)U_{\text{rate}}^2, \ r < r_0 \\ P + \left(U_{\text{rate}} - \Delta u\right)^2 / R = \left(U_{\text{rate}} - \Delta u\right)\Delta u / r, \ \Delta u P > 0 \end{cases} . \quad (42)$$

For the convenience of illustration, take case D as an example, where R=50Ω resistance loads are taken into consideration and the other physical parameters are the same as those of case A. The comparison is shown in Fig. 8. It can be seen the allowed maximum CPLs of case *D* is larger than that of case A. However, in practical situations, the resistive loads are much less than CPLs, hence the stability constraints of before and after considering resistive loads should be very close.

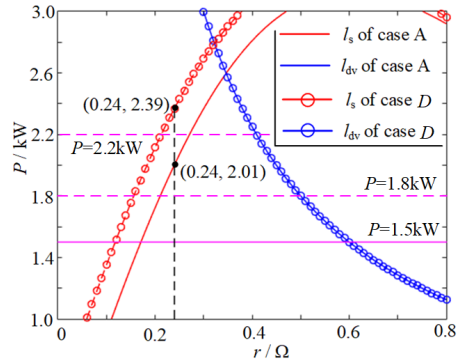

Fig. 8. Feasible domain comparison of cases *D* and *A*.

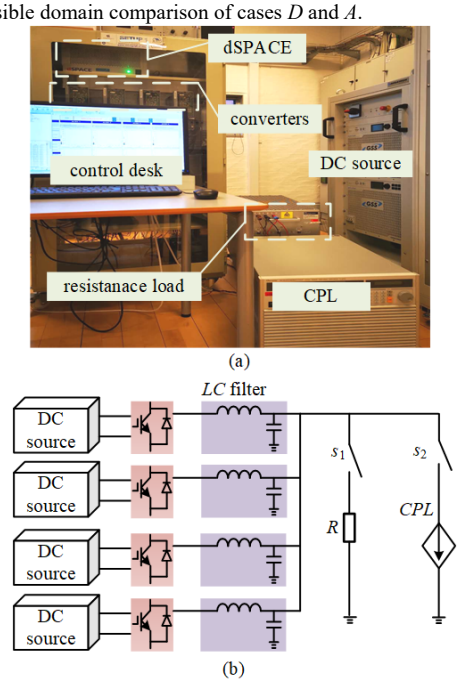

Fig. 9. Experimental setup and its circuit diagram. (a) Experimental setup in AAU-MG research laboratory. (b) Physical connection of the testing setup. (c) Feasible domain for experiments.

V. EXPERIMENTAL RESULTS

An experimental islanded DCMG setup, shown in Fig. 9 (a),

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is used to validate the proposed design method, which consists of a dc source, four parallel-connected DC/DC converters (GCs), *LC* filters, electronic loads (CPLs), resistance loads, and a dSPACE controller and monitoring platform. The physical connection of this setup is shown in Fig. 9(b), and *L*, *C*, and U_{rate} are the same as these in Table I.

In the following experiments, four cases (*A*, *B*, *C*, and *D*) are conducted to make comparisons. In cases *A*, *B*, and *C*, only CPLs are connected to the dc bus to verify the effectiveness of the trade-off design. Whereas considering a few resistive loads may exist in DCMG, some resistive loads and CPLs are simultaneously connected to the bus in case *D* to imitate a practical situation, to enhance the proposed method.

The corresponding parameters of cases *A*, *B*, and *C* are calculated and gathered in Table II, and the comparisons of them are vividly shown in Fig. 7. Apart from the 1.0 kW CPLs, 1.8kW and 2.2 kW CPLs are used to test the stability bound. The experiment results of these three cases are shown in Figs. 10, 11, and 12, and their detailed illustrations are provided in the following part *A*, *B*, and *C* of this Section. The influence of the resistive loads is analyzed in Fig. 8 and parameters keep unchanged in experiment. The experimental results are shown in Fig.13 and the detailed illustrations are provided in the following part *D*.

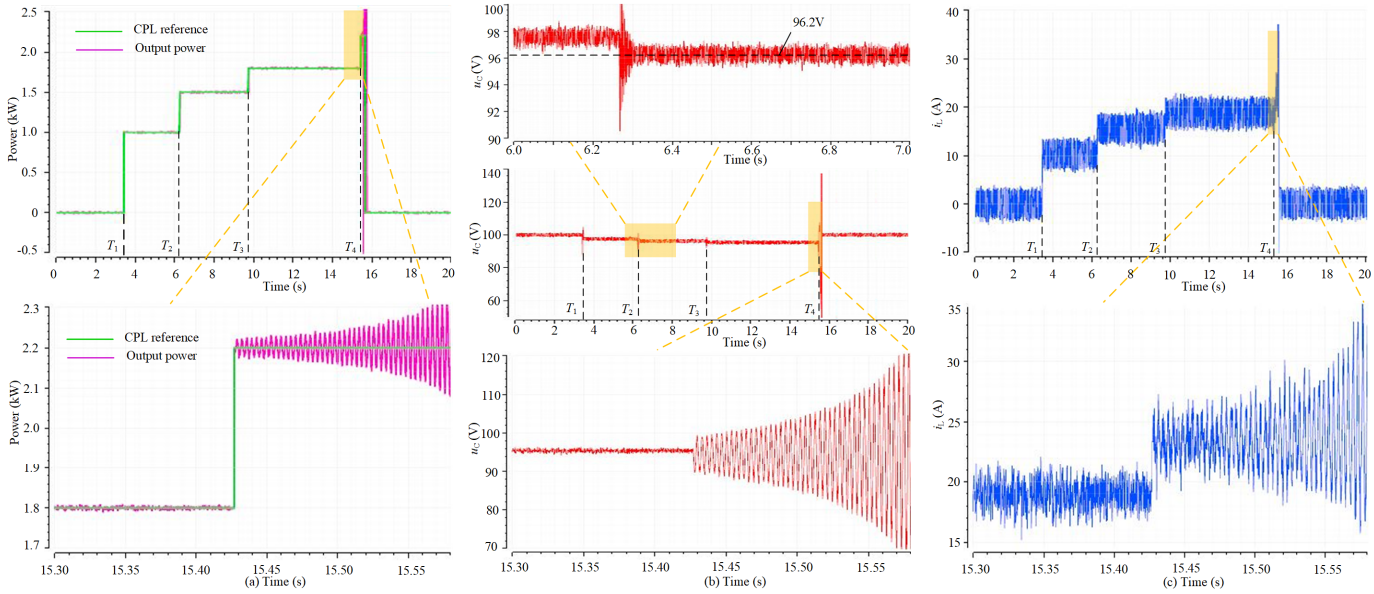

Fig. 10. Experimental waveforms of ω =0.6, virtual resistance is 0.24Ω. (a) Experimental waveforms of CPL reference and output power. (b) Experimental waveforms of the bus voltage. (c) Experimental waveforms of load current.

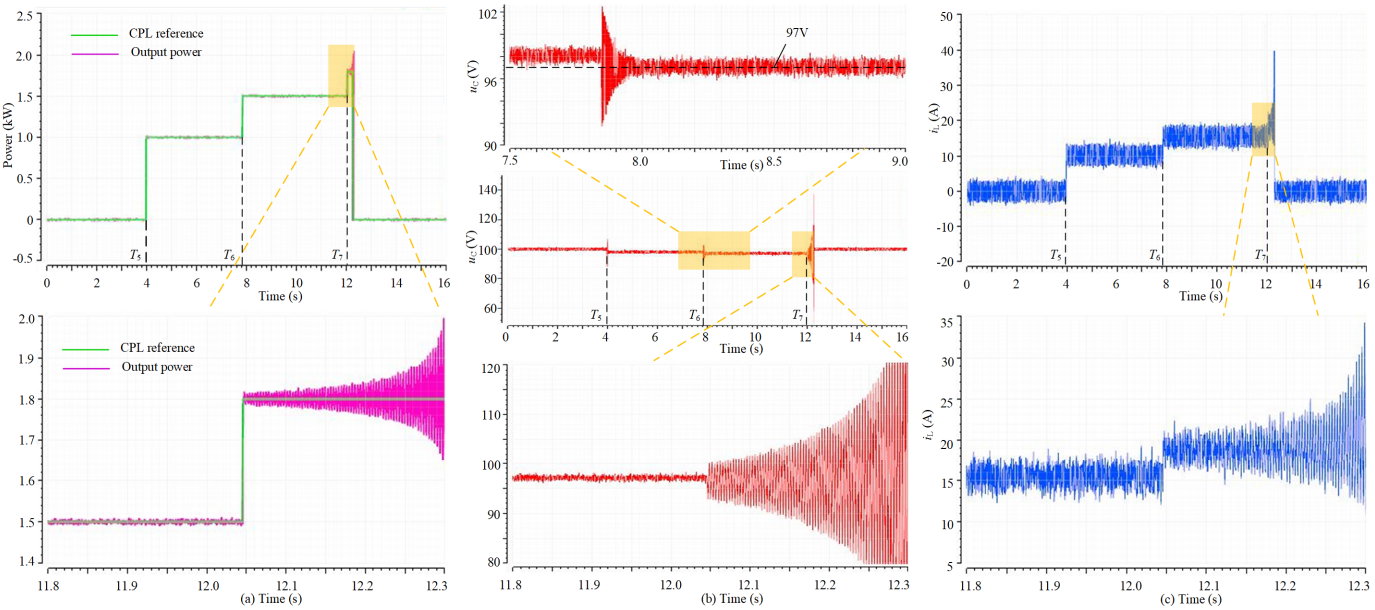

Fig. 11. Experimental waveforms of ω =0.9, virtual resistance is 0.19Ω. (a) Experimental waveforms of CPL reference and output power. (b) Experimental waveforms of the bus voltage. (c) Experimental waveforms of load current.

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A. *Case A: ω =0.6, virtual resistance is 0.24Ω.*

Fig. 10 shows experimental waveforms of ω =0.6, where P'_{max} is 2.01kW, and virtual resistance is calculated as 0.24Ω by (30). At t=T_2, 1.5kW CPL is connected to DCMG, the system is stable, and the average value is about 96.2V as shown in Fig. 10(b). At t=T_3, 1.8kW CPL is connected to DCMG less than P'_{max}, hence the system is still stable. At t=T_4, 2.2kW CPL is connected to DCMG exceeding P'_{max}, where the waveforms cannot converge. In that case, due to the huge transient current, protections are triggered, the current turns to be zero, and the bus voltage goes back to its nominal value.

B. *Case B: ω =0.9, virtual resistance is 0.19Ω.*

To achieve a lower voltage deviation, ω is adjusted to 0.9, and virtual resistance is calculated as 0.19Ω by using (30). Fig. 11 shows the waveforms of ω=0.9, and the P_{max} is 1.63kW. As shown in Fig. 11(a), 1.0kW, 1.5kW, and 1.8kW CPLs are connected to the DCMG at t=T_5, t=T_6, and t=T_7 respectively. The bus voltage and load current waveforms are shown in Figs. 11(b) and (c). At T_6, the system is stable, and the average value is about 97V as shown in Fig. 11(b), where the voltage deviation is smaller than that of ω =0.6 in Fig. 10(b). At t=T_7, the system cannot maintain stability as CPL reference exceeds 1.63kW, and the waveforms of output power, bus voltage, and load current are becoming divergent until protections are triggered making load current be zero and bus voltage be the nominal value.

C. *Case C: ω =0.2, virtual resistance is 0.31Ω.*

To achieve a higher stability margin, ω is adjusted to be 0.2, and virtual resistance is calculated as 0.31Ω by (30). As shown in Fig. 12(a), 1.0kW, 1.5kW, and1.8kW CPLs are connected to the DCMG at t=T_8, t=T_9, and t=T_{10} respectively, and the system is always stable. It is noted when 2.2kW CPL is connected to the DCMG at t=T_{11}, the system is still stable as the value of CPL is smaller than P_{max}. In this sense, its stability margin is larger than that of ω =0.6.

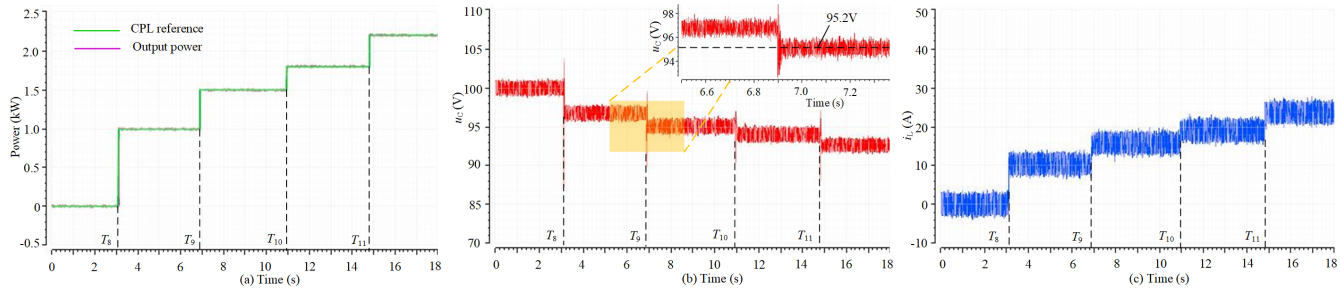

Fig. 12. Experimental waveforms of ω =0.2, virtual resistance is 0.31Ω. (a) Experimental waveforms of CPL reference and output power. (b) Experimental waveforms of the bus voltage. (c) Experimental waveforms of load current.

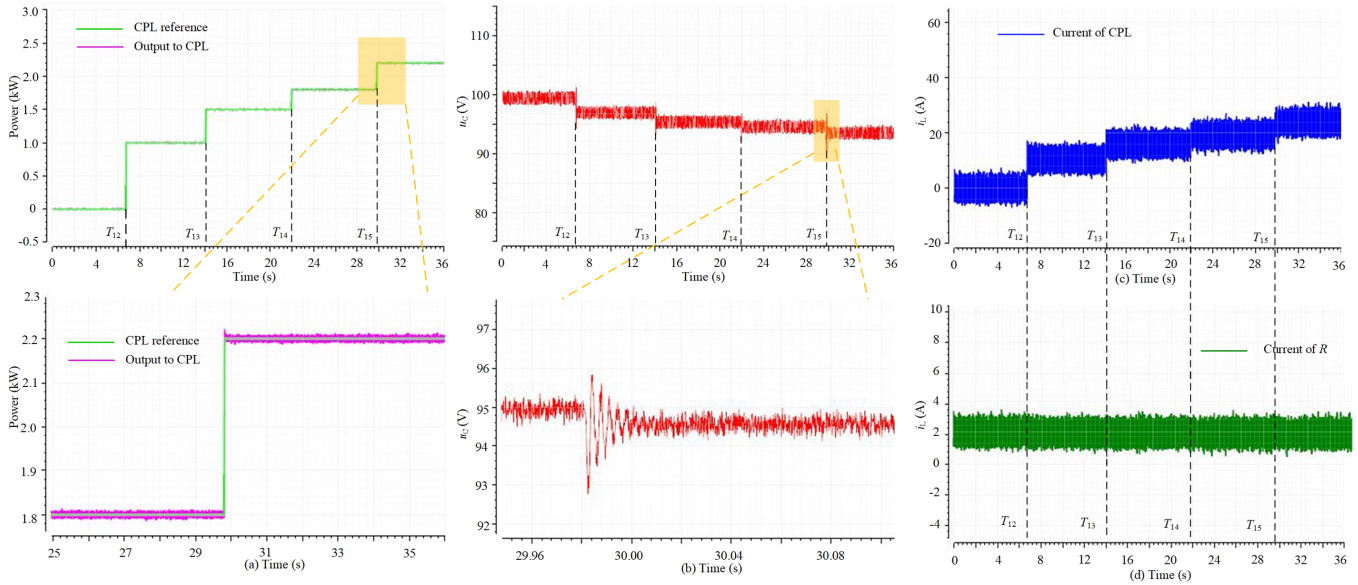

Fig. 13. Experimental waveforms of case *D*. (a) Experimental waveforms of CPL reference and the output power to CPL. (b) Experimental waveforms of the bus voltage. (c) Experimental waveforms of the CPL current. (d) Experimental waveforms of resistance current.

D. *Case D: Both resistive loads and CPLs are considered.*

To illustrate the influence of the resistive loads in practical situation, 0.2kW(R=50Ω) resistance loads are connected to the dc bus in this case, and all the other physical parameters are the same as those of case A. As analyzed in Fig. 8, when ω is 0.6, the allowed maximum CPLs of case *D* is about 2.4kW larger than that of case A (2.0kW). Therefore, when 2.2kW loads are connected to the dc bus, case *D* should be stable whereas case A is unstable, which is validated by an experiment as shown in Fig. 13. In this experiment, at t=T_{12}, t=T_{13}, and t=T_{14}, 1.0kW, 1.5kW, and 1.8kW CPLs are connected to the dc bus, respectively, and the waveforms of this case are similar to those of case A, except the current of R is about 2 A. However, when

2.2kW CPLs are connected to the dc bus at $t=T_{15}$, case D is still convergent, although case A is divergent (see Fig. 9 at $t=T_4$). Therefore, the proposed method is still effective even if a few resistive loads is connected to the dc bus.

E. Summary

To summarize, the proposed method is effective, even if a few resistive loads exist in DCMGs. However, with the development of power electronic technologies, CPLs will account for an increasing proportion in DCMGs. Therefore, the worst condition should be considered in stability analysis and parameter design. Through the proposed design, we can adjust ω to achieve different control aims, such as increasing ω to reduce the voltage deviation and decreasing ω to enlarge the stability margin. All the experimental results are consistent with the theoretical analysis done.

VI. Conclusion

Due to the absence of a virtual resistance design guideline in droop-controlled DCMGs considering large-signal stability, this paper proposes a trade-off design method. The stability margin and voltage deviation are chosen as two pivotal factors in the design. Hence the large-signal model based on the Lyapunov function is established, and the stability criterion is introduced. Besides, the negative influence of virtual resistance on the voltage deviation is taken into consideration. Finally, a compromised design based on the containment theory is developed considering the aforementioned constraints. The proposed method can achieve different system design requirements by tuning the weight coefficient, validated by the experimental results. Furthermore, it can give some instructions in voltage regulation and energy management if achieved by adjusting virtual resistance.

Appendix

The symbolic expression of $\boldsymbol{H}$ can be expressed as

$$h_{\mathrm{a}} = \frac{(L(Cu_{\mathrm{C}}^4 + LP^2 + Lu_{\mathrm{C}}^4) - CLPu_{\mathrm{C}}^2 r)/}{(2(LP - Cu_{\mathrm{C}}^2 r)(Pr - u_{\mathrm{C}}^2))}, \tag{1}$$

$$h_{\mathrm{b}} = h_{\mathrm{c}} = \frac{CLu_{\mathrm{C}}^2 (ru_{\mathrm{C}}^2 + P)/}{(2(LP - Cu_{\mathrm{C}}^2 r)(Pr - u_{\mathrm{C}}^2))}, \tag{2}$$

and

$$h_{\mathrm{d}} = \frac{Cu_{\mathrm{C}}^2 (Cu_{\mathrm{C}}^2 + Lu_{\mathrm{C}}^2 + Cu_{\mathrm{C}}^2 r^2 - LPr)/}{(2(LP - Cu_{\mathrm{C}}^2 r)(Pr - u_{\mathrm{C}}^2))}. \tag{3}$$

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