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Passivity-Based Dual-Loop Vector Voltage and Current Control for Grid-Forming VSCs

Heng Wu, *Member, IEEE*, and Xiongfei Wang, *Senior Member, IEEE*

***Abstract*—This letter proposes a passivity-based dual-loop vector voltage and current control method for grid-forming voltage-source converters (GFM-VSCs). A passive output impedance of GFM-VSC is guaranteed in both the voltage control mode and the current-limiting mode with a wide range of time delay. The frequency-domain analysis, simulation and experimental tests validate the effectiveness of the approach.**

***Index Terms*—Passivity, grid-forming, stability, voltage control, current control, delay.**

I. Introduction

The frequency-domain passivity-based control of voltage-source converters (VSCs) emerges as a promising solution to mitigate harmonic instability caused by dynamic interactions between VSCs and their connected electrical systems [1], [2]. By imposing a nonnegative-real-part in the closed-loop output impedance of VSC, i.e., $\mathrm{Re}\{Z_{VSC}(j\omega)\geq 0\}$ or $\angle Z_{VSC}(j\omega)\in$ [-90°, 90°], $\forall\omega$, the VSC will not destabilize the connected electrical system [2].

There are two general control structures of VSCs, i.e., grid-following (GFL)-VSCs and grid-forming (GFM)-VSCs [3]. The GFL-VSC is controlled as a current source through the current control (CC), while the GFM-VSC is controlled as a voltage source during the normal operation, and is switched to the current-limiting control during the fault/overload conditions [3]. Hence, the dual-loop control scheme, i.e., the outer voltage control (VC) loop + inner CC loop is commonly adopted with GFM-VSCs [4].

The time delay involved in the digital control of VSC has been identified as the main cause of the negative-real-part of Z_{VSC} in the high-frequency range (e.g. from around 200 Hz to the Nyquist frequency) [2]. The passivity-based stabilization of the CC loop for GFL-VSCs has been extensively investigated [5]-[7], where several active damping schemes are discussed to partially mitigate [5], [6], or fully eliminate [7], the negative-real-part of Z_{VSC} that is caused by the time delay. In contrast, very few works can be found on the passivity-based design of VC and CC loops for GFM-VSCs [8], [9]. By compensating the phase lag introduced by the time delay, the passive Z_{VSC} of GFM-VSCs in the voltage control mode with the typical one and a half sampling period ($1.5T_s$) time delay can be achieved by the direct-pole-placement-based state feedback control [8], or by adding the virtual impedance control [9]. Yet, the performance of those methods is degraded when subjecting to the larger phase lag introduced by longer time delay [8], [9]. In fact, those methods can no longer guarantee the passive behavior of Z_{VSC} when the time delay is longer than $1.5T_s$, which is the case in the control of high-voltage VSCs, e.g., modular multilevel converters (MMCs) and static synchronous compensators [10]. Moreover, the passivity of GFM-VSCs operating in the current-limiting mode is overlooked in those works, and consequently, the instability might still occur during the fault/overload conditions even if the time delay is limited to $1.5T_s$.

This letter thus proposes a passivity-based VC and CC for GFM-VSCs. By directly implementing the reference-tracking transfer function in the forward path of two control loops, the dynamic impact of time delay on Z_{VSC} can be eliminated, and thus, a dissipative behavior of Z_{VSC} in the high-frequency range (from around 200 Hz to the Nyquist frequency) can be guaranteed in both the voltage control mode and the current-limiting mode under any time delay. The frequency-domain modeling and experimental tests are presented, which corroborate the effectiveness of the proposed method.

II. System Description

Fig. 1(a) shows the single-line diagram of a three-phase GFM-VSC that can be operated in both the standalone and grid-connected mode [3]. L_f, Z_{load} and Z_g represents the filter inductor, load impedance and grid impedance, respectively. v_o and i_o are the output voltage and current of VSC, respectively. The VC loop is used to regulate v_o to follow the voltage reference generated by power control loops, which is further cascaded with the inner CC loop for the current limitation [4]. Moreover, a backup phase-locked loop (PLL) is needed for grid synchronization during the fault-ride through [11]. Yet, the power control loops and the PLL are usually designed with low bandwidth, which have little impact on the high-frequency (from around 200 Hz up to the Nyquist frequency) dynamics of GFM-VSC [1], [2]. Since the focus of this letter is eliminating the risk of high-frequency oscillation caused by the time delay in the VC and CC loops, the power control loops and the PLL are not included in the following analysis due to their limited impact [8], [9].

It should be noted that the LC/LCL filter is usually used in low-voltage GFM-VSCs like two/three-level VSCs [9], while the L-filter is commonly used with MMC-based GFM-VSCs [4]. For the sake of generality of the analysis, the L-filter is considered in this work. The filter capacitor and the grid-side inductor, if exist, can be categorized as part of the load and/or

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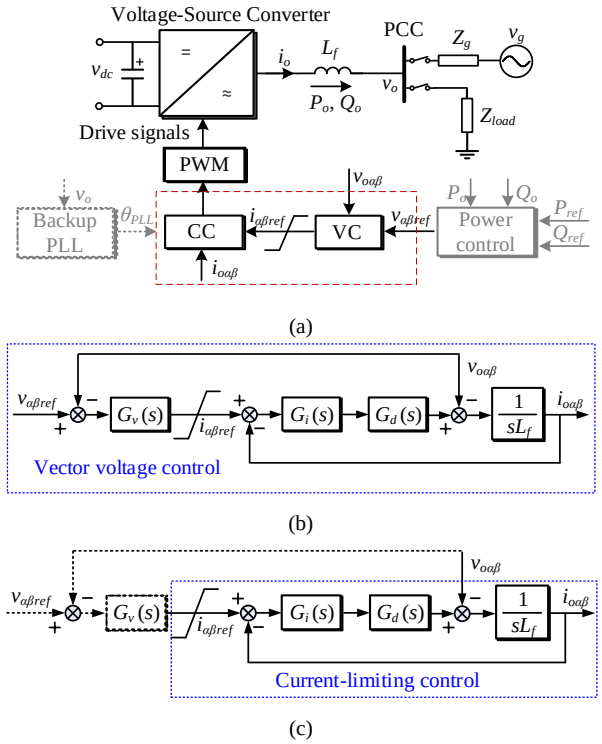

Fig. 1. GFM-VSC with the VC and CC implemented in the $\alpha\beta$-frame. (a) System diagram. (b) Vector-voltage control mode. (c) Current-limiting control mode.

grid impedance. With this configuration, the current after the filter capacitor (if exists) is assumed not to be controlled, which is not a problem as controlling i_o is enough for the current limitation [4].

Fig. 1(b) shows the block diagram of the vector voltage control during the normal operation of GFM-VSC. $G_d(s)$ represents the transfer function of the time delay, i.e., $G_d(s) = e^{-sTd}$, where T_d is the time delay [2]. $G_v(s)$ and $G_i(s)$ denote the proportional + resonant (PR) voltage and current regulator, respectively, which are expressed as:

$$G_v(s) = K_{pv} + \frac{K_{rv}s}{s^2 + 2\zeta\omega_g s + \omega_g^2} = K_{pv} + G_{Rv}(s). \tag{1.1}$$

$$G_i(s) = K_{pi} + \frac{K_{ri}s}{s^2 + 2\zeta\omega_g s + \omega_g^2} = K_{pi} + G_{Ri}(s). \tag{1.2}$$

where K_{pv}, K_{pi}, K_{rv} and K_{ri} are P gains and R gains of the corresponding voltage and current regulator, respectively. ω_g represents the grid fundamental frequency and ζ is the damping factor. During the overload condition, the output of the PR voltage regulator is saturated due to the persistent error between $v_{\alpha\beta ref}$ and $v_{o\alpha\beta}$, which leads to $i_{\alpha\beta ref}$ being equal to the limit value, and GFM-VSC is naturally switched to the current-limiting control mode, as shown in Fig. 1 (c).

Based on Figs. 1(b) and (c), the output voltage (current) of GFM-VSC in the voltage control (current-limiting) mode can be expressed as [4],[7]

$$v_{o\alpha\beta} = \underbrace{\frac{G_v G_i e^{-sT_d}}{1 + G_v G_i e^{-sT_d}}}_{H_v} v_{\alpha\beta ref} - \underbrace{\frac{sL_f + G_i e^{-sT_d}}{1 + G_v G_i e^{-sT_d}}}_{Z_{vVSC}} i_{o\alpha\beta}. \tag{2.1}$$

$$i_{o\alpha\beta} = \underbrace{\frac{G_i e^{-sT_d}}{sL_f + G_i e^{-sT_d}}}_{H_i} i_{\alpha\beta ref} - \underbrace{\frac{1}{sL_f + G_i e^{-sT_d}}}_{1/Z_{iVSC}} v_{o\alpha\beta}. \tag{2.2}$$

where H_v (H_i) is the closed-loop transfer function between $v_{\alpha\beta ref}$ and $v_{o\alpha\beta}$ ($i_{\alpha\beta ref}$ and $i_{o\alpha\beta}$), which is named as the reference tracking transfer function hereafter. Z_{vVSC} (Z_{iVSC}) is the output impedance of VSC in the voltage control (current-limiting) mode. Since R controllers are merely designed to eliminate the steady-state voltage/current tracking error at the grid fundamental frequency, it can be neglected when analyzing the high-frequency characteristic of VSC impedance [6], i.e., $G_v(s) \approx K_{pv}$ and $G_i(s) \approx K_{pi}$ in the high-frequency range. Consequently, Z_{vVSC} and Z_{iVSC} can be simplified as

$$Z_{vVSC} \overset{\text{high } f}{\approx} \frac{sL_f + K_{pi}e^{-sT_d}}{1 + K_{pv}K_{pi}e^{-sT_d}}. \tag{3.1}$$

$$Z_{iVSC} \overset{\text{high } f}{\approx} sL_f + K_{pi}e^{-sT_d}. \tag{3.2}$$

Fig. 2 shows the bode diagram of Z_{vVSC} and Z_{iVSC} with parameters given in Table I, where multiple negative-real-part regions can be observed due to the impact of long time delay (T_d =3.5T_s) considered in this work [7].

III. Passivity-Based Design of VC and CC

A. General Idea

It is well known that the open-loop impedance of VSC is merely the filter reactance, which is always passive. Yet, the open-loop control has no reference tracking capability, and hence, cannot be used in practice. This letter thus proposes a general control scheme that enables to shape the closed-loop output impedance of VSC as the passive reactance, while

TABLE I
Main Circuit and Controller Parameters

Symbol	Description	Value (p.u.)
V_{PCC}	PCC voltage (RMS value)	110 V (1 p.u.)
P	Power rating of the VSC	3 kW (1 p.u.)
f_g	Grid frequency	50 Hz (1 p.u.)
L_f	Filter inductance	3 mH (0.08 p.u.).
f_{sw}	Switching frequency	10 kHz (20 p.u.)
T_s	Sampling (control) period	100 μs (0.05 p.u.)
T_d	Time delay in the control loop	3.5T_s (0.175 p.u.)
K_{pv}	P gain of the voltage regulator	2.16 p.u.
K_{rv}	R gain of the voltage regulator	322.59 p.u.
K_{pi}	P gain of the current regulator	0.37 p.u.
K_{ri}	R gain of the current regulator	55.5 p.u.

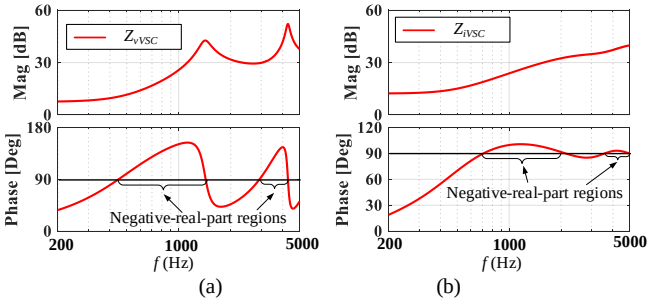

Fig. 2. Output impedance of GFM-VSC. (a) Voltage control mode. (b) Current-limiting mode.

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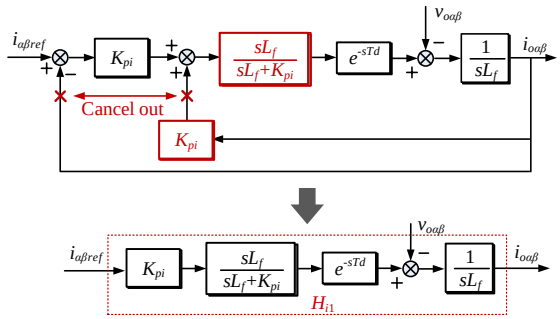

Fig. 3. High-frequency equivalent representation of the proposed CC loop.

retaining the reference tracking capability. The core idea of the method is that the reference tracking transfer functions [H_v and H_i in (2)] are directly implemented in the forward path of the control loop, rather than being formed with the feedback path, which will be detailed in the following.

B. Passivity-Based Design of CC Loop

First, the passivity-based design of the CC loop is introduced. With $G_i \approx K_{pi}$, it is known from (2.2) that H_i can be approximated as $K_{pi}e^{-sTd}/(sL_f+K_{pi}e^{-sTd})$ in the high-frequency range. Since the delay term in the denominator of H_i dose not bring in any benefit to the reference tracking, $H_{i1}=K_{pi}e^{-sTd}/(sL_f+K_{pi})$ is selected and implemented in the forward path of the CC loop. As shown in Fig. 3, the positive feedback of $i_{o\alpha\beta}$ with the control gain K_{pi} is added to cancel out the original negative feedback loop, and a high-pass filter $sL_f/(sL_f+K_{pi})$ is further inserted into the forward path to guarantee the overall transfer function as H_{i1}.

Based on Fig. 3, $i_{o\alpha\beta}$ can be expressed as:

$$i_{o\alpha\beta} = \underbrace{\frac{K_{pi}e^{-sT_d}}{sL_f + K_{pi}}}_{H_{i1}} i_{\alpha\beta ref} - \underbrace{\frac{1}{sL_f}}_{1/Z_{iVSC}} v_{o\alpha\beta}\,. \tag{4}$$

It is known from (4) that the proposed method shapes the output impedance of VSC as the passive filter reactance while remaining the current reference tracking capability.

However, the gain of $1/sL_f$ at the fundamental frequency is usually not low enough to eliminate the impact of $v_{o\alpha\beta}$ on $i_{o\alpha\beta}$. This side-effect can be avoided by adding additional notch filters to minimize the impact of the proposed control around the fundamental frequency, as shown in Fig. 4. The transfer function of the notch filter is expressed as

$$G_{notch}(s) = \frac{s^2+\omega_g^2}{s^2+2\omega_c s+\omega_g^2}\,. \tag{5}$$

where $\omega_c = \pi$ rad/s is selected to guarantee the adaptation of $G_{notch}(s)$ to the variation of ω_g in the range of ±0.5 Hz.

Based on Fig. 4, $i_{o\alpha\beta}$ can be expressed as:

$$i_{o\alpha\beta} = \underbrace{\frac{G_i e^{-sT_d}}{sL_f + K_{pi}G_{notch} + \left(G_i - K_{pi}G_{notch}\right)e^{-sT_d}}}_{H_{i2}} i_{\alpha\beta ref} - \underbrace{\frac{sL_f + K_{pi}G_{notch}}{sL_f\left[sL_f + K_{pi}G_{notch} + \left(G_i - K_{pi}G_{notch}\right)e^{-sT_d}\right]}}_{1/Z_{iVSC2}} v_{o\alpha\beta}\,. \tag{6}$$

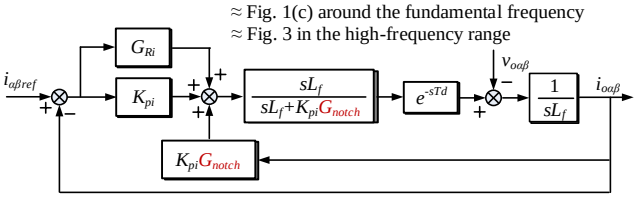

Fig. 4. Complete diagram of the proposed CC loop.

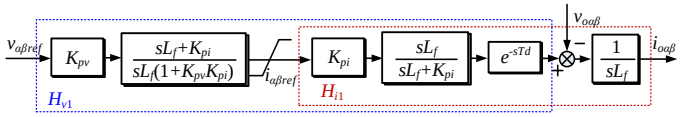

Fig. 5. High-frequency equivalent representation of the proposed VC+CC loop.

Since $G_{notch}(s)\approx 0$ around the fundamental frequency and $G_{notch}(s)\approx 1$, $G_i(s) \approx K_{pi}$ in the high-frequency range. Eq. (6) can be simplified as (2.2) around the fundamental frequency [corresponds to Fig. 1(c)], while can be approximated as (4) in the high-frequency range (corresponds to Fig. 3). Therefore, both the passivity and current tracking performance can be guaranteed.

C. Passivity-Based Design of VC Loop

Following the passive CC loop given in Fig. 4, the same passivity-based control method is further extended to the VC loop. It is known from (2.1) that H_v can be approximated as $K_{pv}K_{pi}e^{-sTd}/(sL_f+K_{pv}K_{pi}e^{-sTd})$ in the high-frequency range. By neglecting the time delay term in the denominator of H_v, $H_{v1}=K_{pv}K_{pi}e^{-sTd}/(sL_f+K_{pv}K_{pi})$ is directly implemented in the forward path of the VC loop, as shown in Fig. 5, which leads to:

$$v_{o\alpha\beta} = \underbrace{\frac{K_{pv}K_{pi}e^{-sT_d}}{1+K_{pv}K_{pi}}}_{H_{v1}} v_{\alpha\beta ref} - \underbrace{sL_f}_{Z_{vVSC}} i_{o\alpha\beta}\,. \tag{7}$$

from which, the passive output impedance of VSC in the voltage control mode can be clearly observed.

Similarly, the notch filter is further added to avoid the negative impact of the proposed control on the fundamental voltage tracking performance. Then, the complete diagram of the passivity-based VC+CC loops is given in Fig. 6, which leads to

$$v_{o\alpha\beta} = \underbrace{\frac{G_v G_i e^{-sT_d}}{G_i e^{-sT_d}\left(G_v - K_{pv}G_{notch}\right) + K_{pv}K_{pi}G_{notch} + 1}}_{H_{v2}} v_{\alpha\beta ref} - \underbrace{\frac{sL_f\left(1+K_{pv}K_{pi}G_{notch}\right)\left[sL_f + K_{pi}G_{notch} + \left(G_i - K_{pi}G_{notch}\right)e^{-sT_d}\right]}{\left(sL_f + K_{pi}G_{notch}\right)\left[\left(G_v - K_{pv}G_{notch}\right)G_i e^{-sT_d} + K_{pv}K_{pi}G_{notch} + 1\right]}}_{Z_{vVSC2}} i_{o\alpha\beta}\,. \tag{8}$$

which approximates to (2.1) [corresponds to Fig. 1(b)] around the fundamental frequency, yet it can be simplified to (7) (corresponds to Fig. 5) in the high-frequency range. Hence, both the passivity and the voltage tracking performance can be guaranteed.

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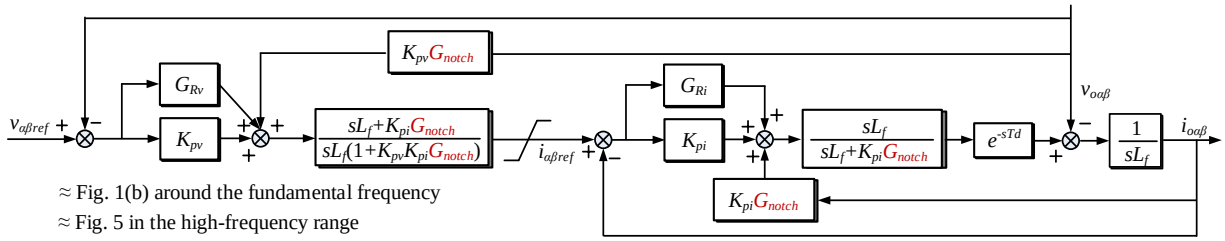

Fig. 6. Complete diagram of the proposed VC+CC loop.

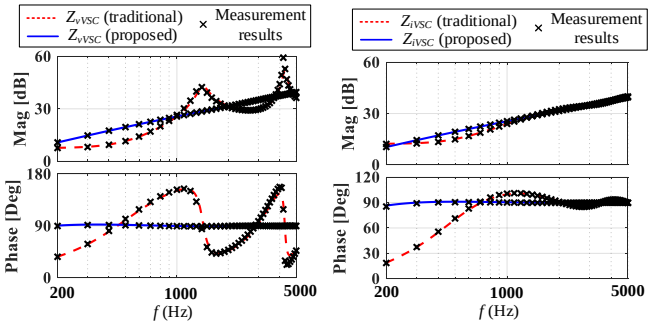

Fig. 7. Comparison of output impedance of GFM-VSC. (a) Voltage control mode. (b) Current-limiting mode.

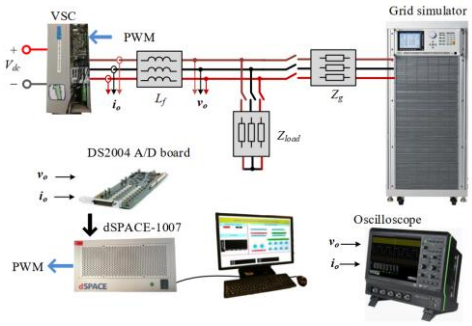

Fig. 8. Configuration of the experimental setup.

D.Robustness Analysis

It is known from Fig. 6 that implementing the proposed VC and CC requires the knowledge of L_f, whose actual value might have ±10% deviation from its nominal value due to the component tolerance [12]. Yet, it is known from Fig. 5 that this inductance deviation would not affect the effectiveness of the proposed method in shaping VSC impedance as a passive reactance. Moreover, the voltage reference tracking performance is also not affected as H_{v1} is independent of L_f [see (7)]. On the other hand, it is known from Fig. 3 and (4) that H_{i1} is affected by L_f, indicating that the inductance deviation does have some impacts on the current reference tracking dynamics. Yet, the steady-state current tracking performance is still not affected as the impact of the proposed control around the fundamental frequency is minimized by the notch filter.

IV. Simulation and Experimental Results

To validate the proposed method, time-domain simulations are carried out in the MATLAB/Simulink and PLECS block set by using VSC with parameters in Table I. The output impedance of VSC with the traditional [shown in Fig. 1(b)] and the proposed (shown in Fig. 6) VC and CC are measured through the numerical simulations and compared with each other, and the results are given in Fig. 7. It can be seen that the VSC impedance is shaped as the passive reactance in both the voltage control and current-limiting mode with the proposed method. The close match between the measured and calculated impedance also corroborates the correctness of the theoretical analysis.

Fig. 8 shows the configuration of the experimental setup, where the performance of GFM-VSC with the traditional and proposed VC and CC loops are tested in both the standalone and grid-connected operation mode. For the standalone operation mode, two types of loads, i.e., paralleled *RC* load and paralleled *RLC* load, are considered. The load parameters are selected such that VSC is operated in the voltage control mode with the paralleled *RC* load (R=60 Ω, C=10μF), and is switched to the current-limiting mode (the limit value is selected as 1.2 pu in this letter) with the paralleled *RLC* load (R=120 Ω, L=6mH, C=10μF) due to the small load inductance. For the grid-connected operation mode, grid impedance is represented by a *CL* filter with L_g=6 mH and C_g=10 μF.

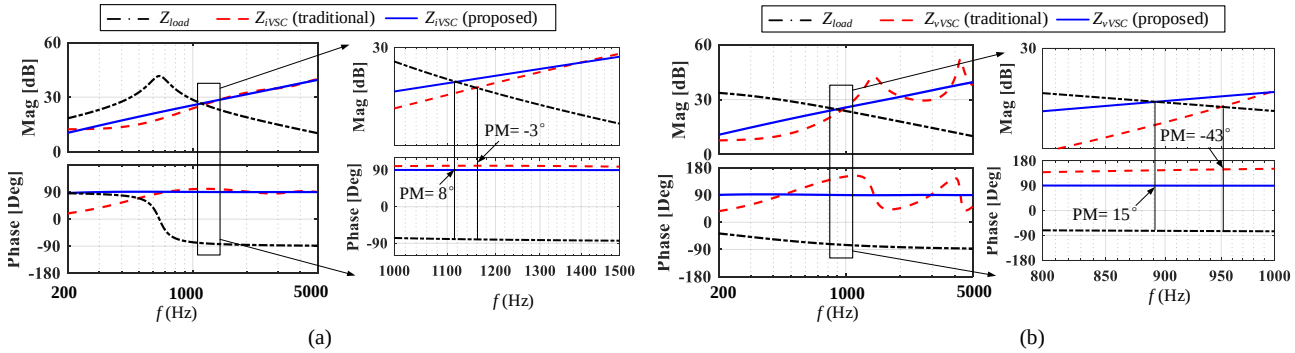

Fig. 9. Output impedance of the standalone-operated GFM-VSC and the load impedance. (a) Paralleled *RLC* load, R=120 Ω, L=6mH, C=10μF, and VSC operates in the current-limiting mode. (b) Paralleled *RC* load, R=60 Ω, C=10μF, and VSC operates in the voltage control mode.

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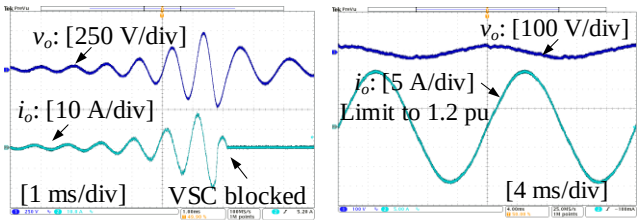
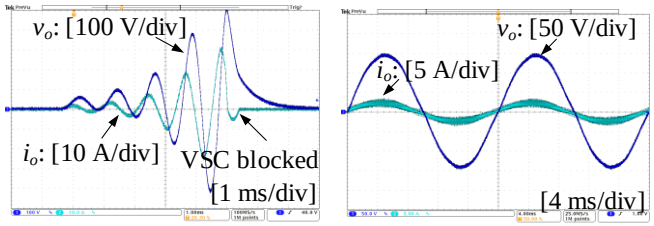


(a) (b)

Fig. 10. Experimental results of the standalone GFM-VSC operating in the current-limiting mode with the paralleled *RLC* load, R=120 Ω, L=6mH, C=10μF. (a) Traditional VC+CC loops, unstable. (b) Proposed VC+CC loops, stable.



(a) (b)

Fig. 11. Experimental results of the standalone GFM-VSC operating in the voltage control mode with the paralleled *RC* load, R=60 Ω, C=10μF. (a) Traditional VC+CC loops, unstable. (b) Proposed VC+CC loops, stable.

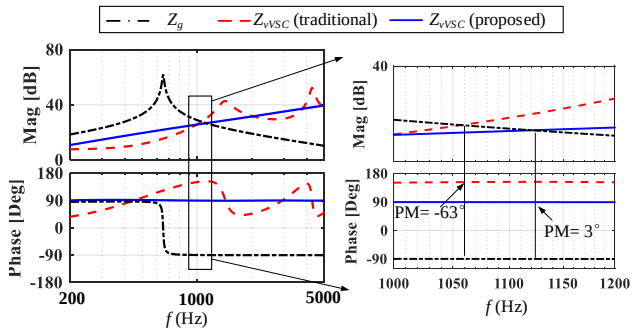
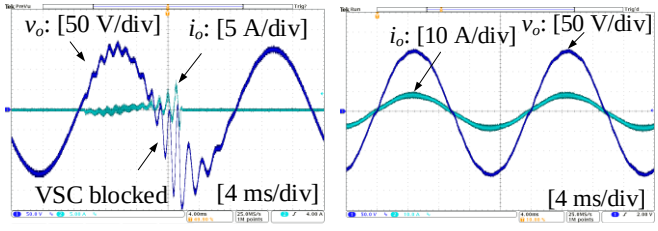


Fig. 12. Output impedance of the grid-connected GFM-VSC and the grid impedance with L_g=6 mH and C_g=10 μF.



(a) (b)

Fig. 13. Experimental results of the grid-connected GFM-VSC with L_g=6 mH and C_g=10 μF. (a) Traditional VC+CC loops, unstable. (b) Proposed VC+CC loops, stable.

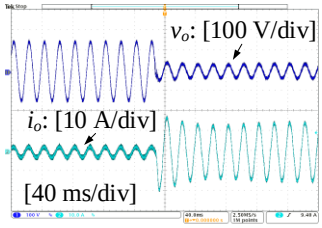


Fig. 14. Experimental results of GFM-VSC switched from the voltage control mode to the current-limiting mode.

Fig. 9 (a) plots the output impedances of the standalone-operated GFM-VSC in the current-limiting mode, as well as the paralleled *RLC* load impedance. It is clear that the load impedance intersects VSC impedance in its negative-real-part region if the traditional control scheme is used, which leads to -3° phase margin (PM), and thus the system is unstable. This analysis is verified by experimental results shown in Fig. 10 (a). It can be seen that the oscillations in the voltage and current of VSC are amplified, and VSC is finally blocked to avoid the damage. Yet, the system can be stabilized with the proposed method, as shown by the experimental results in Fig. 10 (b), where the load current is limited to 1.2 pu as expected.

Fig. 9 (b) plots the output impedances of the standalone-operated GFM-VSC in the voltage control mode, as well as the paralleled *RC* load impedance. It can be seen that VSC is unstable with the traditional VC+CC loops (PM= -43°), but is stabilized with the proposed VC+CC loops (PM=15°). These stability analyses are further verified by the experimental results given by Fig. 11.

Fig. 12 plots the output impedances of the grid-connected GFM-VSC in the voltage control mode, as well as the grid impedance. It can be seen that VSC can operate stably with the proposed VC+CC loops, but will be destabilized if the traditional VC+CC loops are used. These stability analyses are further verified by the experimental results given by Fig. 13. The theoretical analysis and experimental tests confirm the effectiveness of proposed VC+CC loops in stabilizing GFM-VSC in the grid-connected operation mode.

Fig. 14 shows the experimental results of GFM-VSC with the proposed VC and CC loops under the control mode switching. The GFM-VSC is initially operated in the voltage control mode with the paralleled *RC* load (R_1=60 Ω, C=10 μF). Then, the overload condition is triggered by suddenly connecting a new paralleled resistive load with very low resistance (R_2=2.5 Ω), after which GFM-VSC is switched to the current-limiting mode. It can be observed from Fig. 14 that GFM-VSC is operated stably in both control modes, and the steady-state current is limited to 1.2 p.u. in the current-limiting mode as expected. The current overshoot with a peak value around 1.6 p.u. can be observed at the instant of control mode switching. This is acceptable as VSC is usually designed with the capability to withstand 2.0 p.u. current within a short period [13]. The experimental results confirm the proposed VC and CC loops can guarantee the system stability in both control modes without jeopardizing the current-limiting performance.

V. Conclusion

This letter has presented a passivity-based dual-loop vector-voltage and current control method for GFM-VSCs. The unique advantage of the method lies in its effectiveness under a wide range of time delay in the control system, which is critical for the MMC-based GFM-VSCs. Frequency-domain analyses and impedance measurements through the numerical simulations have confirmed this superior feature. Experimental tests have verified the performance of the proposed approach for stabilizing the system.

VI. References

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