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Separation and Validation of Bond-Wire and Solder Layer Failure Modes in IGBT Modules

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Abstract- **Thermal stress of the power semiconductor is one of the most important indicators for the reliability assessment of power electronics based power systems. The mapping of the IGBT junction temperature is usually required to analyze the thermal stress and loss dissipation. However, it is difficult to identify inherent mechanisms of the bond-wire and solder layer failure modes in IGBT power modules. In order to solve the problem, an on-line method to identify inherent mechanisms of the bond-wire and solder layer failure modes in IGBT power modules is proposed. This method can separate the root causes of the bond-wire lift-off and solder layer fatigue by measuring the on-state voltage drop through a sinusoidal loading current based on an H-bridge circuit, as well as its corresponding control and measurement. By comparing the on-state voltage drop at the intersection current and the peak current of the converter, the wear-out conditions of the IGBT power modules can be monitored in real-time with the determination of different failure modes. Finally, experimental results are presented in order to verify the effectiveness and feasibility of the proposed method.**

***Index terms*- power semiconductor, reliability, bond-wire lift-off, solder layer fatigue, converter.**

I. Introduction

Power electronics based grid-connected converters and their dominating components are main considerations in respect to reliability analysis for reducing the maintenance cost of the renewable energy system as reported in [1], [2]. In general, the power electronics converter consists of various components such as power devices, PCBs, gate drivers, capacitors and inductors. Among them, the power semiconductor devices are taking a great portion of the primary failure sources of the converter [3], The failures in power switching semiconductors are mainly caused by thermo-mechanical fatigues, thereby the relevant thermal analysis is very essential for reliability testing in terms of a variety of industrial applications.

In practical cases, the IGBTs are widely developed in a form of packaged modules, and they can be divided into two categories: press-pack and wire-bonded IGBTs. The latter usually draws more attentions due to its cost advantage. In the case of the wire-bonded IGBT modules, there are mainly two types of package-related wear-out failure modes.

As shown in Fig. 1 [4], the bond-wire lift-off is one of the typical failures in this mechanism. The other dominant failure mechanism is the solder layer fatigue between direct bonded copper substrate and the chip or the baseplate. It may usually occur at the edge and center parts of the solder layer [4]. Both the failure modes are caused by the large coefficient of thermal expansion mismatch among materials, which are generally affected by the thermal loading conditions and periodical commutation of power switching devices as well as the ambient temperature variations for the power electronics based systems [5].

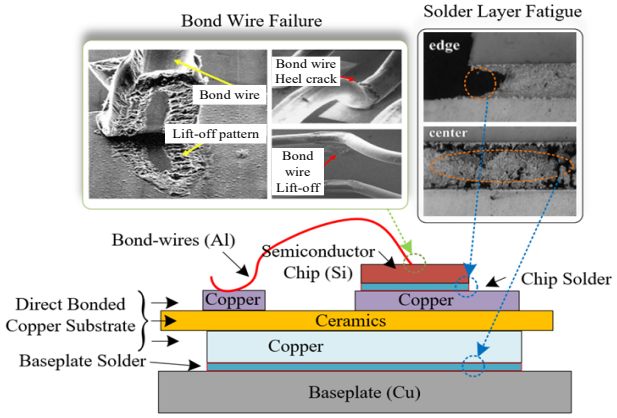

Fig. 1. Diagram of a standard IGBT module and its dominant package-related wear-out failure mechanisms [4].

In fact, the bond-wire failure will slightly increase the equivalent electrical resistance and it appears as an increase in the on-state collector-emitter voltage of transistors [5]. Even a small number of failures in the bond-wire may alter the power/current distribution in the power devices and further accelerate the wear-out failures to the remaining parts of bond-wire and finally lead to an open-circuit fault.

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On the other hand, the solder layer fatigue may increase the internal thermal impedance of the IGBT module. The on-state collector-emitter voltage increases with a higher junction temperature and may induce hot spots and thermal run away in the IGBT modules [6]. Consequently, the increased thermal impedance will accelerate more failures including the bond-wire fatigue. It is worthwhile to note that the on-state collector-emitter voltage will be varied due to the bond-wire and solder layer failure modes, thereby it is widely used to monitor the wear-out conditions of IGBT modules in cases of both failures. However, the complete simulation for the solder degradation are still very challenging, because the solder aging speed is very slow and sensitive to many uncertainty factors, and requiring accurate real-time monitoring. A real-time wear-out monitoring of IGBT modules with the determination of failure modes can provide information for further performing proactive control strategies, such as thermal control and load management, which can be applied to the power converters. For example, fault-tolerant control methods can be used when wear-out failure occurs in bond-wires [7]–[11] and active thermal control strategies can be applied when the degradation in solder joint occurs [12]–[15] to reduce the highest temperature of the failed device in order to improve the reliability of the power electronic systems.

However, the separation of the inherent mechanisms between bond-wire and solder layer failures is very difficult. For a further understanding, if the bond-wire fatigue occurs in the IGBT, the measured on-state collector-emitter voltage is increasing and leads to an increase in the estimated junction temperature. Meanwhile, if the solder fatigue occurs, it also results in an increase in the on-state collector-emitter voltage. Therefore, the I-V characteristic of the IGBT needs to be updated in order to further identify the failure modes and determine the on-state collector-emitter voltage increase. Several methods have been proposed to analyze the impact of failure modes in IGBT modules [16], [17]. However, in these methods, additional monitoring parameters are required to estimate the junction temperature in order to monitor the solder layer fatigue to distinguish bond-wire failure modes, and extra measurement circuits increase the system cost. Therefore, it is necessary to develop a more cost-effective approach to separate the failure modes of IGBT modules.

This paper proposes a new on-line method to separate the failure modes of IGBT power modules. The novel aspects are summarized in the following three aspects:

1) The proposed method is achieved by monitoring the on-state voltage drop at the intersection current of initial I-V characterization curves and the peak current of converter, which does not need the extra parameters and measurement circuits, and thus simplifies the identification process of failure modes in IGBTs.

2) It enables a fast estimation of junction temperature and thermal impedance variations in case of the failure modes, and the wear-out status of IGBTs in the converter can be monitored in real time.

3) Based on the on-line analysis, the proposed method contributes to reduce the proactive maintenance cost of power electronics based power system, and it is useful for industrial application.

II. Proposed Thermal Characterization Method

This section starts with the control structure of a testing H-bridge converter and the measurement circuit for its IGBT power modules. Then, a preliminary I–V characterization of IGBT is presented in order to separate the failure modes by using the V_{ce_on} values measured at two loading points. Finally, three case studies are carefully designed to explain how to distinguish the IGBT failure mechanisms.

A. Control structure and measurement circuit for the testing IGBT module

In order to distinguish the aforementioned failure mechanisms, an H-bridge circuit operating in the inverter mode is applied, which is beneficial to introduce the highest conduction loss of IGBT [18]. Fig. 2 shows the control structure of both legs (i.e. the test leg and the load leg) in the H-bridge circuit. The test leg provides the reference voltage by using an open-loop control. The voltage amplitude u_m is limited by the modulation index from dc-link voltage, while the voltage angle θ_u is related to its fundamental frequency. Meanwhile, for the load leg, the current amplitude I_m and angle θ_i are used to generate the current profile. Furthermore, a closed-loop control for the loading current is used to obtain the load leg reference voltage u_{lo}.

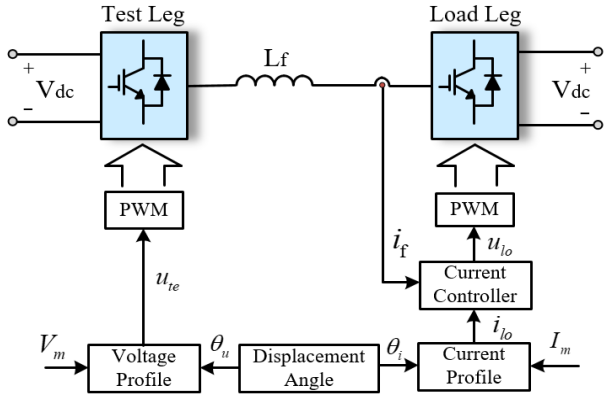


Fig. 2. Control structure of H-bridge converter for testing power modules.

In general, the thermal impedance is used to benchmark the dynamic thermal characteristics of IGBTs in the tested converter. The JESD51-14 standard provides a method to extract this thermal metric [20]–[22]. Based on its definition and standard, a widely used testing bench for the thermal impedance characterization of the IGBT devices can be applied in an H-bridge converter [19].

Fig. 3 shows the measurement circuit for the real-time V_{ce_on} of the IGBT in the experimental test based on previous work in [4], [19]. It is noted that the magnitude of the clamping voltage V_{cc} should be larger than V_{ce}. Taking T_{vh} as an example, when T_{vh} is turned on, the open-circuit

voltage $V_c = V_{ce\_on} < V_{cc}$, and the current I_m will not flow through the MOSFET because the collector voltage and the input impedance of the op-amp is high. Consequently, the MOSFET is turned on since it has a negative threshold voltage ($V_t < V_{gs} = 0$ and $V_{out\ vh} = V_{ce\_on}$).

Furthermore, when V_c increases above V_{cc}, as T_{vh} is turned off, I_m starts to flow and generate a voltage drop on R. As I_m increases, V_{gs} becomes negative and the MOSFET is turned off when $V_{gs} < V_t$. Therefore, V_{cc} is measured at the output during this period. It is also worth mentioning that this test method can be applied with other IGBTs located at upper or lower sides of the half-bridge structure.

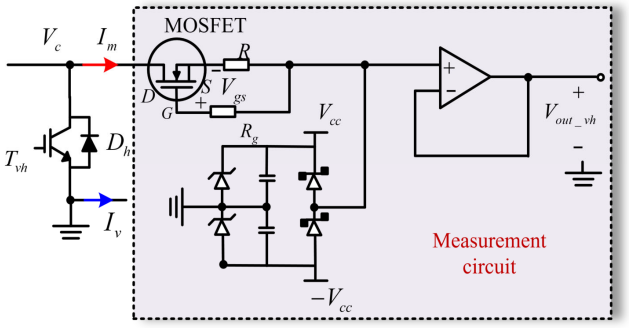


Fig. 3. V_{ce_on} measurement circuit used for real-time condition monitoring.

B. Characterization of an IGBT module

In order to separate the failure modes by using the V_{ce_on} values measured at two points from the I-V characterization curves, the I-V characterization of the IGBT module is performed by using a sinusoidal loading current.

Fig. 4 shows the I-V characterization curves of an IGBT under a sinusoidal loading current at junction temperature T_j =20 ºC, 40 ºC, and 60 ºC, respectively. Note that the $V_{ce@int}$ is independent of T_j, which can be used to determine the bond-wire fatigue. Moreover, if the loading current is higher than the intersection value, the increased T_j leads to a higher on-state voltage. However, if the loading current is lower than the intersection value, it will be located in the negative thermal coefficient range.

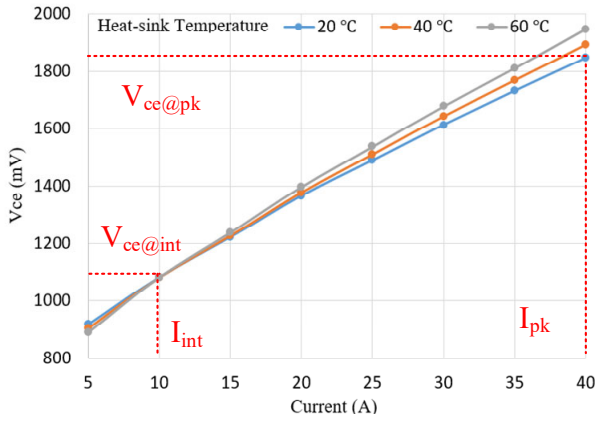


Fig. 4. I-V characterization of IGBT: On-state voltage drop using sinusoidal loading currents under different temperature.

On the other hand, a parameter of K_i is defined to illustrate the relationship between $V_{ce@pk}$ and T_j as shown in Fig. 5. It is worthwhile to note that K_i is almost linear with the loading current, while the V_{ce_int} is kept constant at the intersection current. This feature can be used to distinguish the bond-wire and solder layer fatigues.

The relationship between V_{ce_me} and junction temperature can be obtained as

$$V_{ce\_me} - V_{ce\_B} = K_i \left(T_H - T_B\right) \quad (1)$$

where V_{ce_me} is the measured on-state collector-emitter voltage at the heatsink temperature T_H of 20 ºC; V_{ce_B} is the on-state collector-emitter voltage at baseplate heatsink junction temperature T_B; K_i is K-coefficient as a function of current.

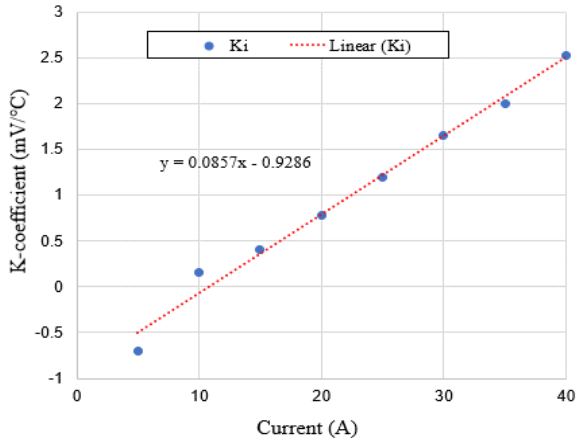


Fig. 5. K-coefficient from I-V characterization of IGBT using sinusoidal loading current.

C. Proposed separation method for failure modes of IGBT

The following will discuss the identification mechanism for the possible case studies. The proposed separation method is using the V_{ce_on} measured at the intersection point and peak current point of the converter, which is defined as $V_{ce\_me@int}$ and $V_{ce@pk}$.

Case 1: Bond-wire fatigue

During the IGBT testing, the measurement/monitoring between the collector and emitter pins consists of the chip itself and some inter-connection elements, so the measured V_{ce_on} can be calculated as

$$V_{ce\_on} = V_{ce\_on(\text{chip})} + I \cdot R_{eq} \quad (2)$$

where $V_{ce\_on\ (chip)}$ is on-state collector-emitter voltage in the chip, I is the collector current, and R_{eq} is the equivalent resistance of the inter-connection elements in the IGBT.

The bond-wire fatigue introduces the electrical resistance increase as ΔR_{eq}, which can be calculated as

$$\Delta R_{eq} = \frac{V_{ce\_me@int} - V_{ce@int}}{I_{int}} \quad (3)$$

where $V_{ce\_me@int}$ is the measured collector-emitter voltage at the intersection current, $V_{ce@int}$ and I_{int} are the intersection values as shown in Fig. 4.

The expected value under the bond-wire fatigue at the peak current $V_{ce\_ex@pk}$ can be calculated as

$$V_{ce\_ex@pk} = V_{ce@pk} + I_{pk} \cdot \Delta R_{eq} = V_{ce\_me@pk} \quad (4)$$

where $V_{ce\_ex@pk}$ is the expected voltage at peak current I_{pk}, which can be obtained from the I-V characteristics obtained by the sinusoidal current loading; $V_{ce\_me@pk}$ is the measured voltage at the peak current; $V_{ce@pk}$ is the reference value.

Therefore, it can be expected that, in the case of the bond-wire fatigue, the equivalent electrical resistance variations $\Delta R_{eq}>0$ and $V_{ce\_ex@pk}$ is approximately the same with $V_{ce\_me@pk}$ as follows

$$\begin{cases} V_{ce\_me@int} > V_{ce@int} \\ V_{ce\_me@pk} \approx V_{ce\_ex@pk} \end{cases} \quad (5)$$

Case 2: Solder layer fatigue

In the case of solder layer fatigue, the $V_{ce@pk}$ is varied when T_j changes. However, $V_{ce@int}$ is independent on the temperature variations. From Fig. 4, the $V_{ce@pk}$ can easily be determined. Therefore, if the solder layer fatigue occurs, it can be expected that there is no equivalent electrical resistance variations $\Delta R_{eq}=0$ and $V_{ce\_ex@pk}$ is smaller than $V_{ce\_me@pk}$:

$$\begin{cases} V_{ce\_me@int} = V_{ce@int} \\ V_{ce\_me@pk} > V_{ce\_ex@pk} \end{cases} \quad (6)$$

Furthermore, the junction temperature variations ΔT_j caused by the solder layer fatigue can be calculated as

$$\Delta T_j = \frac{V_{ce\_me@pk} - V_{ce\_ex@pk}}{K_i} \quad (7)$$

Case 3: Combined both bond-wire and solder layer fatigues

Furthermore, if both the bond-wire and solder layer fatigues occur simultaneously, the bond-wire fatigue will result in an increase of electrical resistance ($\Delta R_{eq}>0$), while the solder layer fatigue leads to $V_{ce\_ex@pk} < V_{ce\_me@pk}$. Therefore, it can be recognized that both failures occur in the IGBT module at the same time by using (8)

$$\begin{cases} V_{ce\_me@int} > V_{ce@int} \\ V_{ce\_me@pk} > V_{ce\_ex@pk} \end{cases} \quad (8)$$

III. Experimental Validation

In order to identify the inherent mechanisms of the aforementioned fatigue cases, an experimental H-bridge circuit converter is built and the overall setup is shown in Fig. 6. The test and load legs of H-bridge circuit are controlled by using TI DSP28335 board. The heatsink temperature is regulated by using the refrigerated circulator. The operation conditions of the experimental setup are presented in Table I.

During the test, it is assumed that the bond wire failure is the main reason to introduce a resistance increase of the IGBT modules and the effect of metallization degradation is ignored since it usually takes more aging time. The bond-wire lift-off is simulated by cutting bond wires of the IGBT module also as suggested in [4], [23-26]. However, it is very difficult to exclude the other failures/degradation in an IGBT module, which can lead to an obvious thermal resistance increase, since it is sometimes very sensitive to different thermal interface materials. As a result, the material analysis is beyond the main scope of this paper, which will thus be future research considerations.

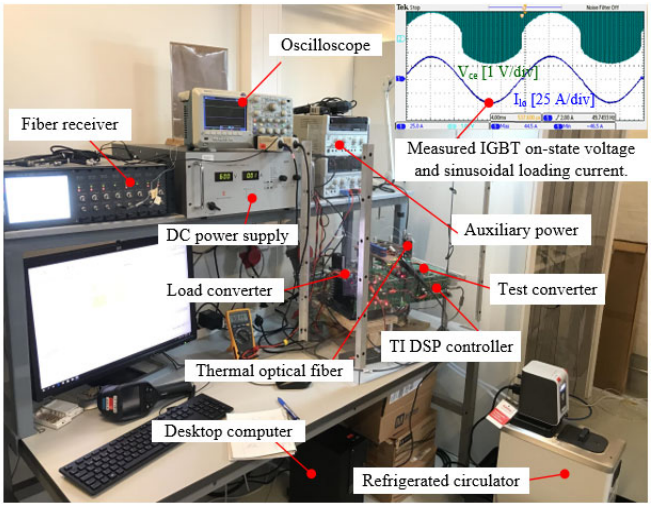
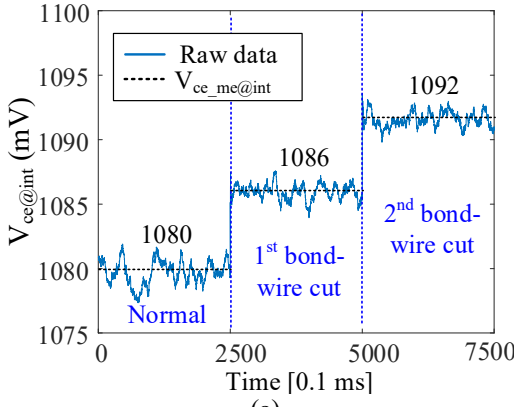


Fig. 6. Configuration of the experimental setup and its waveform.

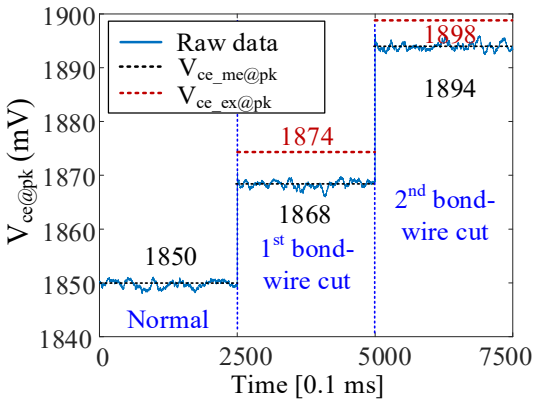
Table I. Operation Conditions of the H-bridge Circuit.

DC-link voltage V_{dc}		50 V
Filter inductor L_f		300 μH
Switching frequency f_{sw}		10 kHz
Test leg	Voltage amplitude V_m	10 V
	Fundamental frequency f_1	50 Hz
	Heat-sink temperature T_H	20-60 °C
Load leg	Current amplitude I_m	40 A
	Displacement angle θ_i	180°

Fig. 7 shows the experimental results for bond-wire lift-off where two bond-wires are cut in sequence in an open IGBT module. It can be seen that the increased voltage caused by the 1st bond-wire cut $\Delta V_{ce@int}$ is 6 mV, while the 2nd bond-wire cut increases the voltage 12 mV as shown in Fig. 7(a).



(a)



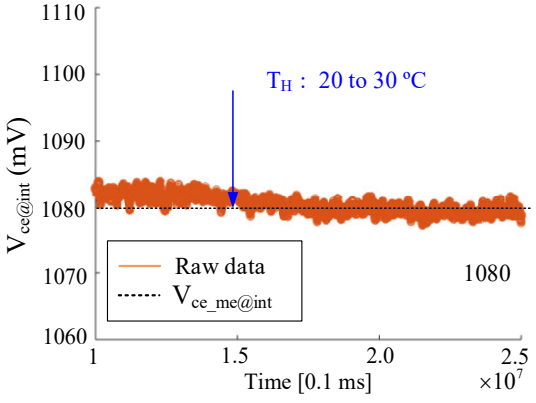
(b)

Fig. 7. Emulation and validation for the bond-wire fatigue: (a) On-state voltage at intersection current ($V_{ce@int}$); (b) On-state voltage at peak current ($V_{ce@pk}$).

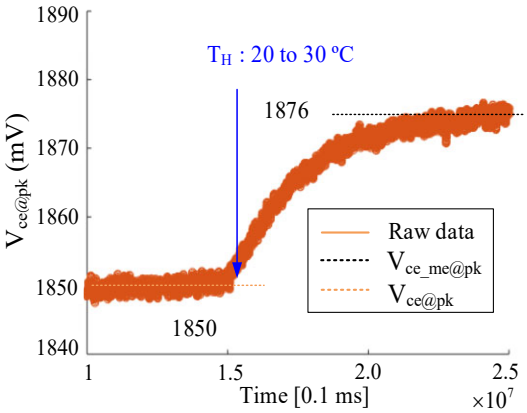
In Fig. 7(b), the $V_{ce@pk}$ is 1850 mV for the original IGBT module; then the $V_{ce\_ex@pk}$ can be calculated as 1874 mV and 1898 mV for the 1st and 2nd bond-wire cut based on (4). Furthermore, the measured $V_{ce\_me@pk}$ for the 1st and 2nd bond-wire cut are 1868 mV and 1894 mV. Considering I_{int}=10 A, the ΔR_{eq} can be calculated as 0.6 mΩ and 1.2 mΩ based on (3). Ignoring the test errors, these results indicate the bond-wire fatigue, which agrees well with the criteria corresponding to (5).

In addition, in order to emulate the solder-layer fatigue, the heatsink temperature T_H is changed from 20 ºC to 30 ºC by using the refrigerated circulator. Fig. 8 presents the experimental result simulating the solder-layer fatigue. In Fig. 8(a), the $V_{ce@int}$ remains the same at 1080 mV in despite of T_H variations. Meanwhile, Fig. 8(b) shows $V_{ce@pk}$ increases from expected value 1850 mV to 1876 mV when the T_H changes from 20 ºC to 30 ºC. These phenomena agree well with the solder layer fatigue as presented in (6).

In addition, the K-coefficient at the current I=40 A can be obtained as 2.5 mV/ºC in Fig. 5, thereby ΔT_j can be calculated by (7) [(1876-1850)/K_{40}=10.3 ºC, where K_{40}=2.5], which matches well with the emulated temperature rise of 10 ºC.



(a)



(b)

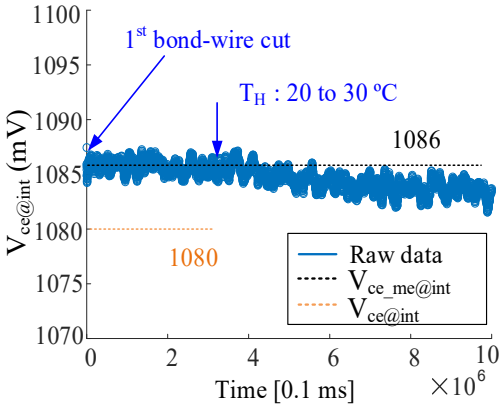
Fig. 8. Emulation and validation for the solder layer fatigue: (a) On-state voltage drop at intersection current ($V_{ce@int}$); (b) On-state voltage drop at peak current ($V_{ce@pk}$).

On the other hand, the experimental validation of both bond-wire and solder layer fatigues occurring simultaneously, which are emulated by using the bond-wires cut and the heat-sink temperature rise together as shown in Fig. 9.

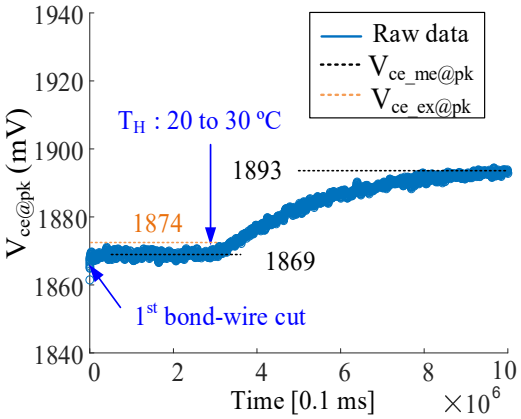
In Fig. 9(a), the increase of $V_{ce@int}$ is due to the solder layer fatigues, which is simulated by the heatsink temperature T_H changed from 20 ºC to 30 ºC. In case of the 1st bond-wire cut, the $V_{ce\_me@int}$ value is kept at 1086 mV, which is obviously higher than the normal value of 1080 mV, Therefore, ΔR_{eq} is calculated as 0.6 mΩ using (3) and $V_{ce\_ex@pk}$ can be obtained as 1874 mV with (4).

On the other hand, $V_{ce\_me@pk}$ increases from 1869 mV to 1893 mV, as shown in Fig. 9(b). $\Delta V_{ce@pk}$ is 24 mV, then ΔTj can be calculated with (1893-1869)/K_{40} =9.5 ºC, (K_{40}=2.5 obtained in Fig. 5), which indicates that there is about 10 ºC rise in T_j of the IGBT due to the solder layer fatigue. The results agree well with (8).

The method is also validated in the 2nd bond-wire fatigue case as shown in Fig. 10. In this case, $V_{ce\_me@int}$ value remains at 1092 mV in despite of a heatsink temperature change from 20 ºC to 30 ºC, and the initial value is 1080 mV, which means ΔR_{eq}=1.2 mV.



(a)

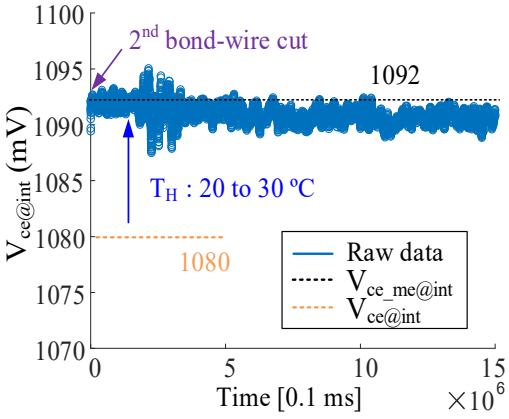


(b)

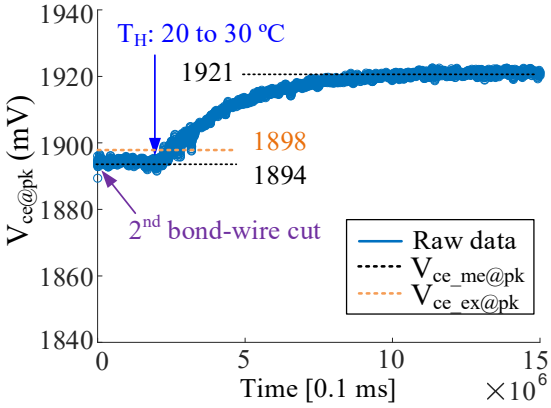
Fig. 9. Emulation and validation in the case of both fatigues (1st bond-wire fatigue case). (a) On-state voltage drop at intersection current ($V_{ce@int}$); (b) On-state voltage drop at peak current ($V_{ce@pk}$)

However, note the $V_{ce@pk}$ is changed from 1894 mV at 20 ºC heatsink temperature to 1921 mV at 30 ºC heatsink temperature in Fig. 10(b), and the junction temperature rise ΔT_j can be calculated (1921-1894)/K_{40}=10.7 ºC, which matches well with the emulated temperature rise of 10 ºC due to solder layer fatigue at the same time.

Furthermore, the measured and calculated values in these cases have been summarized in Table II. The obtained errors between the measurements and calculations are quite small (only 6 mV and 4 mV for the aforementioned test cases), which validated the effectiveness of the proposed method.



(a)



(b)

Fig. 10. Emulation and validation for in the case of both fatigues (2nd bond-wire lift-off fatigue case). (a) On-state voltage drop at intersection current ($V_{ce@int}$); (b) On-state voltage drop at peak current ($V_{ce@pk}$)

IV. Conclusions

This paper proposes an estimation approach to separate the inherent mechanisms of the bond-wire lift-off and solder layer fatigues in IGBT power modules. The method does not need a re-characterization of I-V curves when the IGBTs are worn-out. It is achieved by on-line monitoring the on-state collector-emitter voltage drops at the intersection point of the preliminary I-V characterization curve and the peak current point of the running converter, which simplifies the identification process of different failure modes.

Several study cases of fatigues have been carefully emulated in the experimental setup, where bond-wire fatigue is simulated by cutting bond wires, and solder layer fatigue is emulated by changing the heatsink temperature. Experimental results show that the errors between the measurements and calculations are very small, and it demonstrates the effectiveness and feasibility of the proposed detection method. The method is expected to improve the reliability and availability of power electronic based power systems depending on the different wear-out failure modes of IGBT to extend the lifetime of the converter.

Table II. Results of both Bond-wire and Solder Layer Fatigues (I_{int}=10 A, I_{pk}=40 A and T_H changes from 20 ºC to 30 ºC).

Test Cases	$V_{ce\_me@int}$ [mV]	$\Delta V_{ce@int}$ [mV]	ΔR_{eq} [mΩ]	$V_{ce\_me@pk}$ [mV] (T_H =20 ºC)	$V_{ce\_me@pk}$ [mV] (T_H =30 ºC)	$V_{ce\_ex@pk}$ [mV]	Error [mV]
Normal	1080	---	---	1850	---	---	---
1st bond-wire cut	1086	6	0.6	1868	1893	1874	-6
2nd bond-wire cut	1092	12	1.2	1894	1921	1898	-4

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