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A Model-Free Capacitor Voltage Balancing Method for Multi-Level DAB Converters

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***Abstract*—Capacitor voltage balancing is of importance in the neutral-point-clamped (NPC)-based dual-active-bridge (DAB) converters. Most of traditional voltage balancing methods adopt the transformer current models in the balancing process, as the direction of the neutral-point current is affected by the transformer current polarity. However, this approach requires heavy and repetitive offline pre-calculation for the transformer current polarity under various operating modes, and thus, leading to complicated implementation. To overcome this, a model-free voltage balancing scheme based on a fixed-switching-state (FSS) method is proposed in this letter. Two switching states are employed during the voltage balancing process in the proposed method, where the direction of the neutral-point current is independent on the transformer current polarity. Hence, the implementation can be simplified without the pre-calculation of transformer current polarity. Furthermore, the model-free feature of the proposed method is more robust against parameter variations or operating mode changes. Experimental tests are performed, which verify that the proposed method can achieve voltage balancing in terms of easy implementation and fast dynamics.**

***Index Terms*—Multi-level converters, dual active bridge (DAB), neutral point clamped (NPC), capacitor voltage balancing.**

I. Introduction

TWO-three (2/3)-level dual-active-bridge (DAB) converter is considered as a promising solution for medium-voltage DC (MVDC) applications, e.g., large-scale photovoltaic (PV) systems and energy storage systems, due to high power density, galvanic isolation, and higher blocking voltage capability compared to the traditional two-level DAB converters [1]–[3]. As shown in Fig. 1, a 2/3-level DAB converter is composed of a two-level full-bridge, a three-level neutral-point-clamped (NPC) bridge, and an isolation transformer.

Five-level control is one of the most advantageous control schemes to improve the performance (e.g., efficiency) of the NPC-based DAB converters [4], [5]. However, the capacitor voltage imbalance is commonly seen with this control scheme when the gate-driving signals fail to synchronize due to asymmetry in the pulsewidth-modulator in the microcontroller [6]. Besides, unbalancing may also be induced by the tolerances or uneven degradation of the DC-link capacitors, and asymmetrical hardware layouts [6]–[8]. The unbalanced voltages will increase the voltage stress on certain devices, and may cause failures if the voltage stress exceeds the blocking voltage of the device, which significantly affects the reliability of the 2/3-level DAB converters.

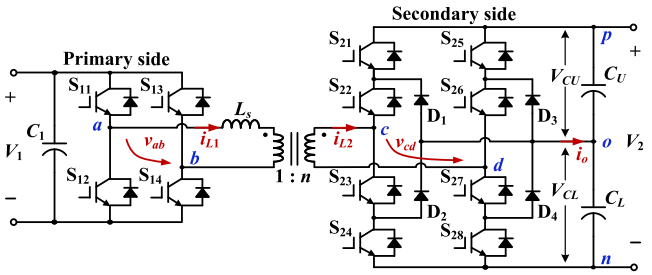

Fig. 1. A two-three (2/3)-level dual-active-bridge (DAB) DC-DC converter.

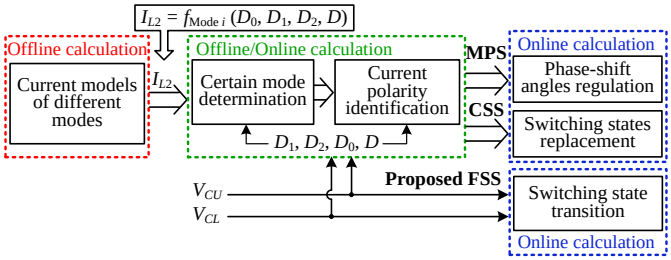

Fig. 2. Control structures of different voltage balancing methods.

To avoid these issues, two methods for capacitor voltage balancing have been proposed for the NPC-based DAB converters, i.e., modified-phase-shift (MPS) method [9]–[11] and complementary-switching-state (CSS) method [12], and their general implementation structure is shown in Fig. 2. In the MPS method, the phase-shift angles are regulated dynamically to increase the charges injected into a certain capacitor. As for the CSS method, the switching states which are adverse for balancing are replaced by their CSSs to achieve the required neutral-point current, while keeping the voltage v_{cd} unchanged. Therefore, the transformer current will not fluctuate anymore. However, these methods are highly dependent on the transformer current models as the direction of the neutral-point current i_o is affected by the polarity of the transformer current i_{L2}. There are various operating modes divided by different relationships among the control variables (i.e., D_1, D_2, D_0, and D, defined in Fig. 3), and the current polarity models are changing under various modes. It is therefore not practically feasible to obtain a generic model to identify the current polarity since: 1) for a certain modulation strategy,

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different operating modes will be applied during various power ranges, and 2) for various modulation strategies, different modes will be applied to achieve different control objectives. Consequently, heavy and repetitive offline pre-calculation for the current models under different modes is required, which increases the implementation complexity significantly. Furthermore, these model-based methods are affected by the current model accuracy, parameter variations, and operating mode changes. Accordingly, a voltage balancing method which is independent of the transformer current polarity was developed in [13]. However, the three-level control applied in the steady state cannot decouple the voltage v_{cd} from the transformer current polarity. Thus, the transformer current still has to be determined to avoid voltage distortions, which significantly hinders its practical applications.

To address the above issues, this letter proposes a model-free voltage balancing control based on a fixed-switching-state (FSS) approach. Two switching states are explored to decouple the direction of the neutral-point current from the transformer current polarity. Then, a voltage balancing control scheme based on the two switching states is developed. The proposed method is simple and generic, being independent of the current polarity models, as shown in Fig. 2. Furthermore, its model-free feature can enhance the robustness against parameter variations and operating mode changes.

II. Proposed FSS Voltage Balancing Method

A. Basic Characteristics With the Five-Level Control

Fig. 3 shows the typical waveforms of the 2/3-level DAB converters using the five-level control. The current will flow through the neutral point o only during the intervals of $v_{cd} = \pm 0.5V_2$, i.e., [A, B], [C, D], [a, b], and [c, d] in Fig. 3. Thus, the four intervals are regulated dynamically in most of the traditional voltage balancing methods to achieve the required neutral-point current. However, for the switching states during these intervals, the direction of the neutral-point current will be reversed if the polarity of the transformer current i_{L2} changes. Therefore, to achieve a required neutral-point current, i.e., $i_o > 0$ (injected into o) when $V_{CU} > V_{CL}$, and $i_o < 0$ when $V_{CU} < V_{CL}$, the transformer current polarity should be determined first, which requires offline pre-calculation and complex implementation. To avoid this, a method to apply certain switching states that can decouple the direction of i_o from the polarity of the transformer current i_{L2} is required.

B. Switching State Determination

To achieve a positive neutral-point current i_o for the condition $V_{CU} > V_{CL}$, if the transformer current i_{L2} is positive (from the primary side to the secondary side), there are two possible current conduction paths, i.e., P1 and P2, for the NPC bridge, as shown in Fig. 4 (a). Similarly, if the transformer current is negative, P3 and P4 are two possible current conduction paths to obtain a positive i_o, as shown in Fig. 4 (b). The switching states for each NPC-bridge arm are defined in Table I. Accordingly, the switching states under the four possible paths can be summarized in Table II. It can be determined from Table II that S_{23} is ON for P1 and P2

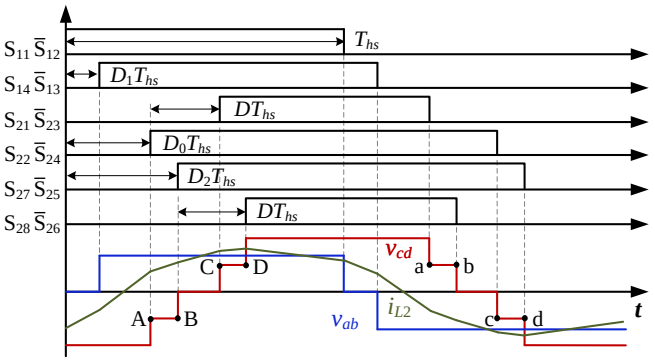


Fig. 3. Waveforms of the 2/3-level DAB converters with five-level control: T_{hs} is half of a switching period, D_0, D_1, and D_2 are the phase-shift ratios, and D is the duty-cycle ratio of the secondary side.

TABLE I
Switching States for NPC Bridge

Switching state	ON switches (first arm)	ON switches (second arm)
[P]	$\{S_{21}, S_{22}\}$	$\{S_{25}, S_{26}\}$
[O]	$\{S_{22}, S_{23}\}$	$\{S_{26}, S_{27}\}$
[N]	$\{S_{23}, S_{24}\}$	$\{S_{27}, S_{28}\}$
$[P_{(+)}]$	$\{S_{21}\}$	$\{S_{25}\}$
$[P_{(-)}]$	$\{S_{22}\}$	$\{S_{26}\}$
$[N_{(+)}]$	$\{S_{23}\}$	$\{S_{27}\}$
$[N_{(-)}]$	$\{S_{24}\}$	$\{S_{28}\}$

TABLE II
Switching States of the Possible Current Paths

Polarity of i_{L2}	Current paths	Possible switching states
$i_{L2} > 0$	P1	$[N_{(+)}P]$ or [OP]
	P2	$[N_{(+)}N]$ or [ON]
$i_{L2} < 0$	P3	$[PN_{(+)}]$ or [PO]
	P4	$[NN_{(+)}]$ or [NO]

during $i_{L2} > 0$. Thus, P3 is not possible any more since S_{23} is OFF in this path, meaning that P4 is the correct current path during $i_{L2} < 0$. Similarly, P2 is the correct current path during $i_{L2} > 0$ since S_{27} is ON for P4. Therefore, by combining the states of P2 and P4, the switching state which can achieve a positive neutral-point current i_o regardless of a positive or negative current i_{L2} can be obtained as $[N_{(+)}N_{(+)}]$. With a similar analysis, the switching state for the condition $V_{CU} < V_{CL}$ can be obtained as $[P_{(-)}P_{(-)}]$, as shown in Fig. 5, which can ensure a negative i_o, independent of the transformer current polarity.

C. Implementation of the Proposed FSS Method

After determining the specific switching states applied in the balancing state, the implementation, i.e., the intervals where the two switching states are employed during a switching cycle, should also be considered. The implementation of the proposed FSS method should take into account:

- The voltage v_{cd} during the balancing state should be symmetrical to avoid DC bias in the transformer current.
- The dwell time of the applied switching state $[N_{(+)}N_{(+)}]$ or $[P_{(-)}P_{(-)}]$ should be determined by the existing control variables, i.e., D_0, D_2, and D. Otherwise, the

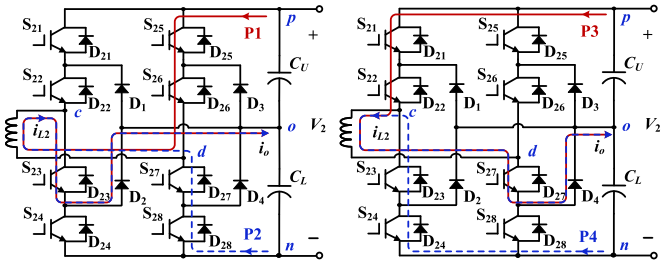


Fig. 4. Possible current conduction paths to achieve a positive neutral-point current i_o when the transformer current i_{L2} is: (a) positive and (b) negative.

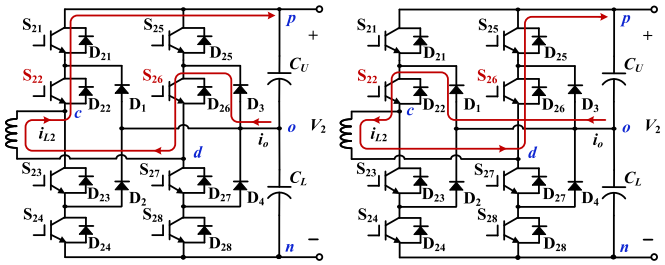


Fig. 5. Current conduction paths under the switching state $[\mathrm{P}_{(-)}\mathrm{P}_{(-)}]$ when i_{L2} is: (a) positive and (b) negative.

additional control variable during the voltage balancing will affect the overall control performance.

- It would be better to maintain certain gate-driving signals unchanged during the balancing process, which can be applied as the basic signals, and other gate-driving signals can be obtained easily based on them. Otherwise, the duty cycles and phase-shift angles are needed to be regulated in the pulse generator, which will increase the control complexity.

With the above, the proposed FSS method can be implemented as shown in Fig. 6, where the dotted lines denote the steady-state waveforms, and the solid lines represent the waveforms after applying the FSS method. As shown in Fig. 6, a fixed switching state is employed during the two intervals [E, F] and [e, f], i.e., $[\mathrm{N}_{(+)}\mathrm{N}_{(+)}]$ for the condition $V_{CU} > V_{CL}$, and $[\mathrm{P}_{(-)}\mathrm{P}_{(-)}]$ for the condition $V_{CU} < V_{CL}$. Under such a switching sequence, the gate-driving signals of S_{21} and S_{24} remain unchanged for both $V_{CU} > V_{CL}$ and $V_{CU} < V_{CL}$, which can be utilized as the basic signals, and those of the other switches can be obtained as

$$\begin{aligned} V_{CU} > V_{CL}: &\begin{cases} \mathrm{S}_{22} = \mathrm{S}_{21}, \mathrm{S}_{23} = \overline{\mathrm{S}}_{21}, \mathrm{S}_{28} = \mathrm{S}_{21} \\ \mathrm{S}_{25} = \mathrm{S}_{24}, \mathrm{S}_{26} = \mathrm{S}_{24}, \mathrm{S}_{27} = \overline{\mathrm{S}}_{24} \end{cases} \\ V_{CU} < V_{CL}: &\begin{cases} \mathrm{S}_{26} = \overline{\mathrm{S}}_{21}, \mathrm{S}_{27} = \mathrm{S}_{21}, \mathrm{S}_{28} = \mathrm{S}_{21} \\ \mathrm{S}_{22} = \overline{\mathrm{S}}_{24}, \mathrm{S}_{23} = \mathrm{S}_{24}, \mathrm{S}_{25} = \mathrm{S}_{24} \end{cases} \end{aligned} \tag{1}$$

In addition, as shown in Fig. 6, the balancing-state waveforms are controlled by the existing variables D_0 and D. For instance, D can be kept unchanged with the steady state, and D_0 can be applied as the output of the proportional-integral (PI) controller to achieve the reference output voltage/transferred power in the closed-loop control system. Thus, the control

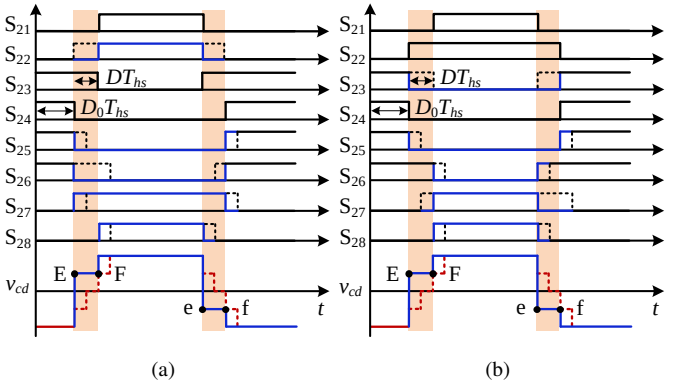


Fig. 6. Transient waveforms with the FSS method with the switching state: (a) $[\mathrm{N}_{(+)}\mathrm{N}_{(+)}]$ when $V_{CU} > V_{CL}$, and (b) $[\mathrm{P}_{(-)}\mathrm{P}_{(-)}]$ when $V_{CU} < V_{CL}$.

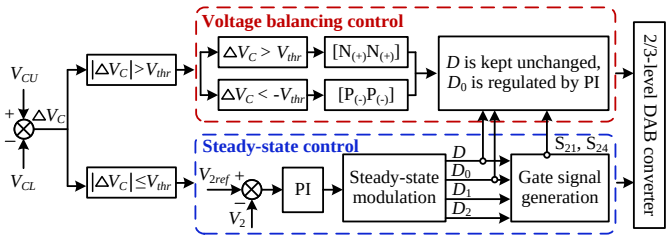


Fig. 7. Implementation of the proposed voltage balancing control scheme.

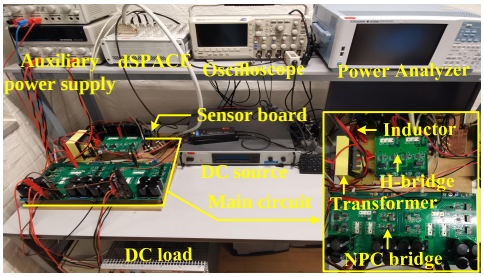


Fig. 8. Prototype of the 2/3-level DAB converter.

variables will not be increased, and the implementation of the FSS method meets the above three constraints.

Accordingly, the control structure of the proposed FSS method is given in Fig. 7. If the voltage difference (i.e., $\triangle V_C = V_{CU} - V_{CL}$) exceeds the threshold V_{thr}, the proposed FSS method will be employed. According to the polarity of $\triangle V_C$, $[\mathrm{N}_{(+)}\mathrm{N}_{(+)}]$ or $[\mathrm{P}_{(-)}\mathrm{P}_{(-)}]$ will be applied during the balancing state. The gate-driving signals of S_{21} and S_{24} are kept unchanged, and others are obtained according to (1).

III. Simulation and Experimental Results

Experimental tests are performed on a downscaled 2/3-level DAB prototype to validate the performance of the proposed FSS method, as shown in Fig. 8. The main parameters and prototype components are shown in Table III. To comprehensively verify the proposed method in different parameters and operating conditions including the mismatched conditions $nV_1 > V_2$ and $nV_1 < V_2$, the input voltage is applied from 100 V to 200 V, and the output voltage is 300 V in the experimental tests. In addition, simulations are performed based on MATLAB/Simulink and PLECS, and the parameters are the same as the experimental parameters.

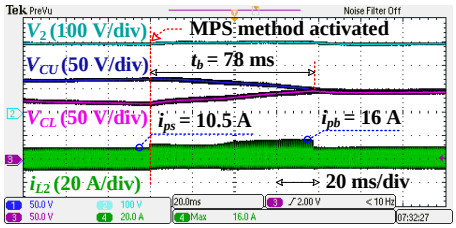
TABLE III
MAIN PARAMETERS OF THE EXPERIMENT AND SIMULATION SYSTEMS

Parameters	Values
Rated input/output voltage V_1/V_2	200/400 V
Rated transferred power P	2.5 kW
Transformer turns ratio n	2
Series inductor L_s	100 μH
DC-link capacitors C_1, C_U, C_L	680 μF
Switching frequency f_s	10 kHz
Power switches (IGBT)	Semikron SK35GB12T4
Gate driver	Infineon 1ED020I12-F2
Voltage sensor	LV 25-P
Control system	dSPACE MicroLabBox
DC source	Delta Elektronika SM330

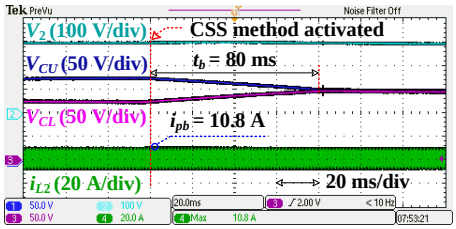
Fig. 9 shows the experimental results with the traditional MPS [9] and CSS [12] methods, and the proposed FSS method under V_1 = 140 V, V_2 = 300 V, P = 1580 W, D_1 = 0.05, D_2 = 0.2, D = 0.15, and D_0 is regulated by the closed-loop control system to track the reference output voltage. These methods are all enabled with the same initial unbalanced condition, i.e., $V_{CU} - V_{CL} = 50$ V. It is worth to mention that the transformer current models are calculated and the beneficial/adverse switching states are identified offline for the traditional MPS and CSS methods, which are not needed for the proposed FSS method.

As shown in Fig. 9 (a), the two capacitor voltages can be balanced after a balancing period of t_b = 78 ms with the MPS method. Due to the changed voltage v_{cd}, the peak transformer current will be increased from 10.5 A in the steady state (i.e., i_{ps}) to 16 A in the balancing state (i.e., i_{pb}), i.e., 52.4% current increment, which is defined as $(i_{pb} - i_{ps})/i_{ps}$. As for the traditional CSS method, the voltage balancing can be completed around 80 ms, and there is no significant current fluctuation, as shown in Fig. 9 (b). By contrast, the balancing time can be decreased to 57 ms with the proposed FSS method, as shown in Fig. 9 (c), and the peak current is 11.2 A (i.e., 6.7% current increment). Therefore, the proposed FSS method can achieve the fastest balancing dynamics under this operating condition.

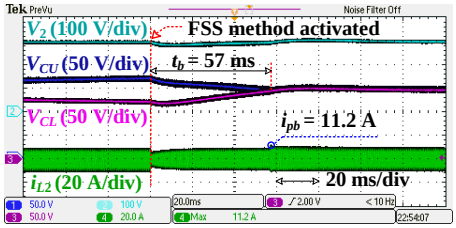
In addition, the power losses breakdown and efficiency during steady state, and the balancing state under the three voltage balancing methods are shown in Fig. 10, where various parts of the power losses are tested by the simulations in PLECS. Since the transformer current during the balancing state with the CSS and the proposed FSS methods is similar to that of the steady state, as shown in Fig. 9, the conduction, diode, and magnetic losses are similar for the three states that are mainly determined by the root-mean-square (RMS) transformer current [14]. In addition, the switching losses will also be similar since the switching times of the semiconductors during the balancing state in each switching period are the same as the steady state. Therefore, the total power losses and efficiency during the balancing state with the CSS and FSS methods are similar to those in steady state. On the other hand, the transformer current increases significantly during the balancing state for the MPS method, which will increase the conduction losses and reduce the efficiency of the converter.



(a)



(b)



(c)

Fig. 9. Experimental results with various capacitor voltage balancing methods for the condition $V_{CU} > V_{CL}$ with: (a) MPS method, (b) CSS method, and (c) proposed FSS method.

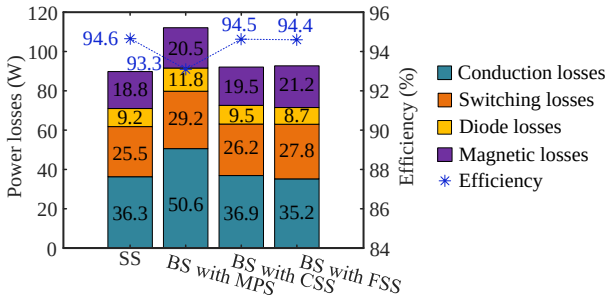
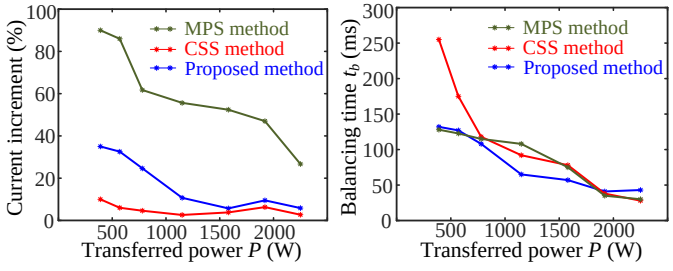


Fig. 10. Power losses breakdown and efficiency during the steady state (SS) and the balancing state (BS) with various voltage balancing methods.



(a) (b)

Fig. 11. Comparative experimental curves among different capacitor voltage balancing methods under various transferred power levels: (a) peak current increment curves and (b) balancing time curves.

Comparative experimental tests under various transferred power are shown in Fig. 11, where the input and output voltages are 140 V and 300 V, respectively, and the load changes from 235 Ω to 40 Ω. Fig. 11 (a) demonstrates the increased peak current with the three methods, where it can

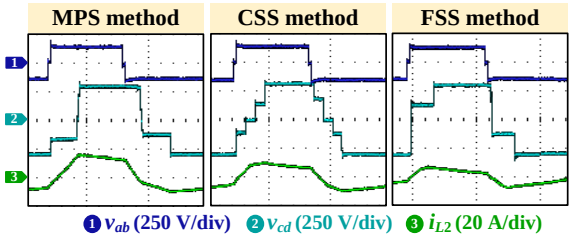


Fig. 12. Experimental waveforms during the balancing state with various voltage balancing methods.

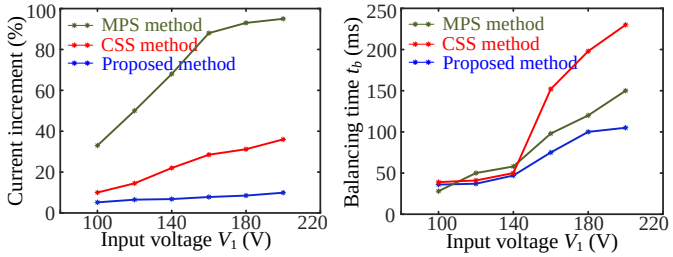


Fig. 13. Comparative experimental curves among different capacitor voltage balancing methods under various input voltages: (a) peak current increment curves and (b) balancing time curves.

be seen that the traditional CSS method can achieve the lowest increased peak current since the voltage v_{cd} can be kept unchanged during the balancing state. On the other hand, the peak current will be increased under the other two methods due to the changed voltage v_{cd}. However, since v_{cd} can be maintained symmetrical during balancing with the proposed FSS method, the current fluctuation will be less than that of the traditional MPS method, whose balancing-state waveform is asymmetrical, as shown in Fig. 12. Fig. 11 (b) shows the comparative curves of the balancing time, where it can be seen that the proposed FSS method has relatively fast dynamics during the entire power range. That is because the charge flowing through the neutral point is determined by the neutral-point current i_o and the balancing time t_b. For the traditional MPS method, although the neutral-point current during balancing is increased, a relatively short efficient balancing interval during each switching period (less than DT_{hs} [12]) and large current fluctuation will slow down the voltage balancing. On the other hand, the neutral-point current is kept unchanged for the CSS method. Since the efficient balancing interval (i.e., $(D_2 - D_0)T_{hs}$ [12]) is generally short during the low power range, the balancing period will be increased. Compared to them, the neutral-point current will not be changed significantly and the efficient balancing interval (i.e., DT_{hs}) is relatively long for the proposed method, and thus it can achieve fast balancing during the entire power range. In addition, Fig. 13 demonstrates the comparative curves among the three voltage balancing methods under different input voltages, where the output voltage is 300 V and the transferred power is maintained at 1000 W. It can be seen from Fig. 13 that the proposed FSS method can achieve fast balancing and relatively low current fluctuation (compared to the MPS method) with various DC voltages.

Fig. 14 (a) shows the simulation results when the load changes from 57 Ω to 75 Ω during the balancing process

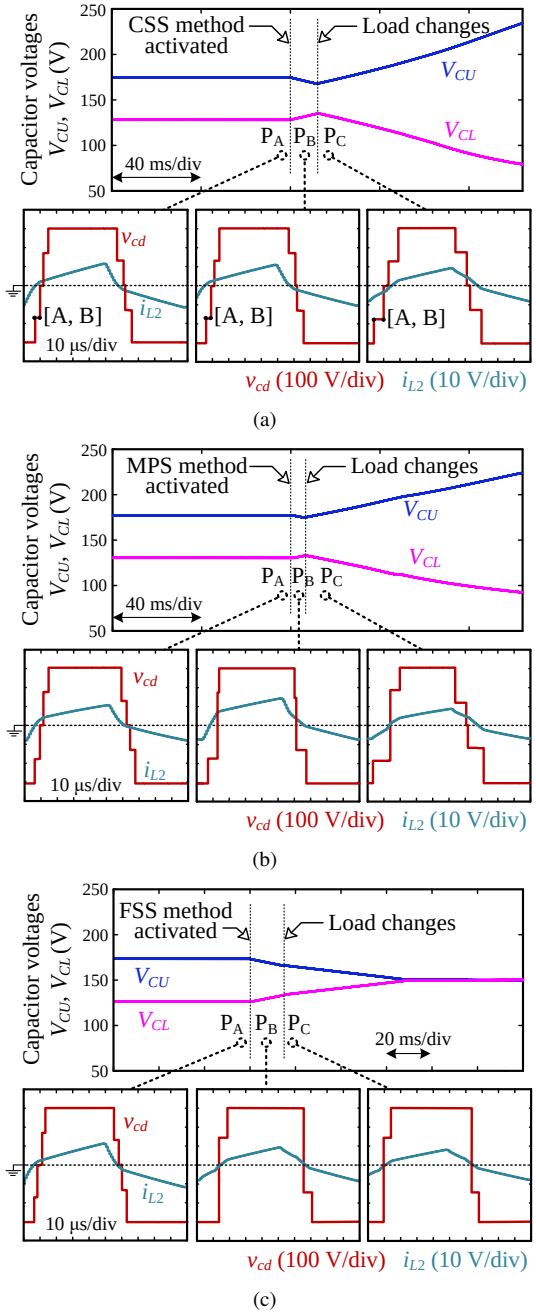


Fig. 14. Simulation waveforms when the load changes from 57 Ω to 75 Ω during the voltage balancing process under V_1 = 200 V and V_2 = 300 V with: (a) the traditional CSS method, (b) the traditional MPS method, and (c) the proposed FSS method.

under the traditional CSS method (MPS method has similar characteristics, as shown in Fig. 14 (b)). The switching states which are beneficial/adverse for voltage balancing are determined by the current polarity when the voltage balancing method is enabled, i.e., P_A, where the current is positive during the interval [A, B]. However, the current polarity is reversed after the step load change (see the current i_{L2} at P_C in Fig. 14 (a)). Since the current polarity will generally not be re-determined until the voltage balancing is completed (the two capacitor voltages become equal), the beneficial/adverse switching states will be wrongly identified. Consequently, the effective voltage balancing intervals cannot provide sufficient

required charges to the neutral point, which will cause a longer balancing period or even worse voltage imbalance, e.g., Fig. 14 (a). Furthermore, the performance of the traditional MPS and CSS methods will also be affected by the step change on the input/output voltage, the fluctuated phase-shift angles in the closed-loop control system, and so on. On the other hand, these issues can be avoided by the proposed FSS method due to the model-free feature, as shown in Fig. 14 (c). Thus, the proposed method is more robust against parameter variation, operating mode change, and inaccurate current models.

IV. Conclusion

This letter has proposed a model-free capacitor voltage balancing control scheme based on the FSS method. Two fixed switching states are explored and then applied during the balancing, without the transformer current polarity identification. In addition, the balancing-state control is determined by the existing control variables in steady state, which means that no additional control variables are introduced. With these characteristics, the proposed voltage balancing control method can simply be implemented in practice without pre-calculation of the current polarity models, and the robustness against the parameter variations can be enhanced. Experimental tests have verified that the proposed method can achieve easy and fast balancing without significant current overshoots.

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