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*Occurrence Mechanism, Instability Analysis, and Oscillation Suppression*

Xue, Peng; Iannuzzo, Francesco

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# Self-sustained Turn-off Oscillation of Cascode GaN HEMTs: Occurrence Mechanism, Instability Analysis and Oscillation Suppression

Peng Xue, *Member, IEEE* and Francesco Iannuzzo, *Senior Member, IEEE*

***Abstract*—This paper presents a comprehensive study on the occurrence mechanism, instability analysis and suppression methods of self-sustained turn-off oscillation which occurs on cascode gallium nitride high electron mobility transistors (cascode GaN HEMTs). In the beginning, the oscillation waveforms are analyzed, which indicate that the occurrence of the oscillation is determined by test circuit instability. Based on the double pulse test, the impact of the load current $I_L$, DC-bus voltage $V_{DC}$ and gate resistance $R_G$ on the self-sustained oscillation is identified. To investigate the instability of the resonant circuit, a small-signal ac model of the resonant circuit is derived. Based on the model, the influences of various parameters on the self-sustained oscillation are analyzed. The analyses reveal the possible methods which can suppress the oscillation. The effectiveness of the proposed methods is validated by the experimental data and simulation results in the end.**

***Index Terms*—gallium nitride (GaN), GaN cascode HEMTs, self-sustained oscillation, turn-off oscillation**

## I. Introduction

The cascode gallium nitride high electron mobility transistors (cascode GaN HEMTs) have quickly matured from research-grade devices to commercially available products in the past few years. Thanks to the superior properties of GaN semiconductor, the cascode GaN HEMTs have emerged as a promising candidate for high-frequency and high-density power conversion. The fundamental depletion-mode HEMTs (DHEMTs) are normally-on devices, which are not suitable for power electronics applications in terms of fail-safe operation [1]. To tackle the problem, the cascode GaN HEMTs and enhanced-mode HEMTs (EHEMTs) are introduced as the normally-off solutions for the GaN switches. In the cascode GaN HEMTs, a low voltage (LV) MOSFET is connected in series to drive a normally-off GaN DHEMT, as shown in Fig. 1. For the GaN EHEMTs, the gate is modified to achieve a positive threshold voltage. Compared to the GaN EHEMTs, the cascode GaN HEMTs have faster turn-off speed thanks to the intrinsic current accelerating mechanism [2], [3]. This makes the cascode GaN HEMTs a perfect choice for converter applications with high turn-off current.

Despite the high switching speed, the cascode GaN HEMT still has some unwanted drawbacks. One of the major drawbacks is the underdamped current and voltage oscillation during the switching transient [4]. Under certain test conditions, the switching oscillation can become self-sustained [5]–[8].

The authors are with the Energy Technology Department, Aalborg University, Aalborg East 9220, Denmark. (E-mail: pexu@energy.aau.dk).

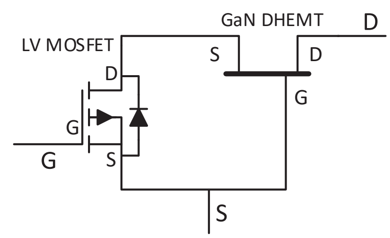



Fig. 1. The structure of cascode GaN HEMTs.

The self-sustained oscillation causes severe electromagnetic Interference (EMI) problems, which can disrupt the converter operation. In the worst-case scenario, the oscillation can even induce the device and circuit failure [8]. Unfortunately, the underdamped switching oscillation of cascode GaN HEMTs has not received the proper attention it deserves [9]. Only a few studies are proposed to investigate the switching oscillation [4]–[7], [10]–[13] of cascode transistors. The paper [10] proposed three reasons which give rise to the underdamped turn-off oscillation of SiC-JFET cascode. Firstly, the LV MOSFET and JFET work in saturation mode simultaneously during turn-off transient, which can generate a positive feedback process to amplify the turn-off oscillation. Secondly, during the turn-off process, the increase in the width of the space-charge region causes the reduction of the device's stray capacitances. This gives rise to the reduced attenuation of the turn-off oscillation. Thirdly, the stray inductances induce the voltage overshoot across the cascode, which can trigger the turn-off oscillation. In [4], the underdamped switching oscillation of parallel-connected cascode GaN HEMTs is studied. The paper claims that the underdamped switching oscillation is related to the resonant tank formed by the gate loop of the GaN DHEMT. In the gate loop, the parasitic inductances of the internal wire bonds and stray capacitances of cascode GaN HEMT form an LC tank without effective damping. During switching transient, the LC tank can be excited and the oscillation is generated. The research [11] implies that the self-sustained oscillation can be excited due to the feedback action between the gate loop and the additional loop introduced by external gate-drain couple capacitance. However, the detail of the feedback action is not presented in [11]. In [6]–[8], the self-sustained oscillation is observed during the switching transients of the cascode GaN HEMT in the half-bridge circuit. However, the studies [6]–[8] do not provide further analysis on the self-sustained oscillation. The [13] reports that high dV/dt excites gate voltage bounce of cascode GaN HEMT during the turn-off transient, which triggers underdamped oscillation. The [5] claims that the cascode GaN HEMT has the capacitance mismatch between its internal GaN DHEMT and LV MOSFET during turn-off transient. This gives rise to a time-varying equivalent resonant capacitance in the test circuit, which can excite the self-sustained oscillation. By adding an additional capacitor $C_X$ in parallel with the LV MOSFET, the mismatched charge can be compensated. The test is performed in [5] to validate the effectiveness of capacitor $C_X$ on the oscillation suppression. The theory presented in [5] is also utilized in [12] to explain the origin of the self-sustained oscillation that appears in the cascode GaN HEMTs based half-bridge circuit.

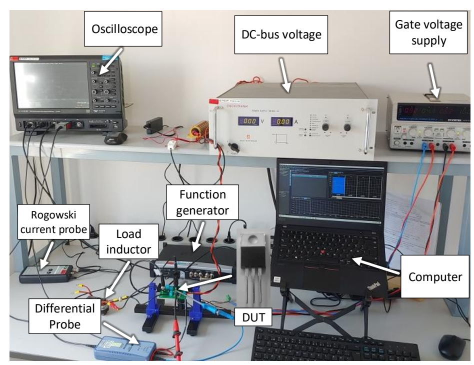
The studies presented above [4], [5], [10], [11] provide diverse explanations on the switching oscillation of the cascode GaN HEMTs. The studies [4], [10], [11] indicate that the underdamped switching oscillation of the cascode GaN HEMTs is due to the RLC resonance. However, the articles [4], [10], [11] only provide brief discussions on the possible root causes of the switching oscillation. No further analysis on the instability of the resonant circuit was performed to prove the RLC resonance can self-sustain. [5] claims that the time-varying resonant capacitances can cause the self-sustained oscillation. However, the research [5] did not provide any experimental or simulation results to demonstrate that the proposed mechanism actually occurs during the turn-off transient. It is also unclear whether the additional energy drawn by the mechanism can compensate for the power consumption of the resistive components in the resonant circuit so that the oscillation can self-sustain. The paper [5] shows that the self-sustained oscillation can be suppressed with an additional capacitor $C_X$ connected in parallel with the LV MOSFET. However, since the $C_X$ can disrupt the RLC resonant circuit and dampen the oscillation, the validation is not convincing enough. The research on the self-sustained switching oscillation of the cascode GaN HEMTs is far from conclusive.

Recently, many studies [14]–[18] show that the self-sustained switching oscillation of the wide bandgap power devices is determined by the instability of resonant circuit. When the circuit is unstable, self-sustained oscillation can be excited in the SiC MOSFETs [14], [15], SiC JFETs [16] and GaN EHEMTs [17], [18] based half-bridge circuits during the switching transient. With an underdamped LC tank in the gate loop of the GaN DHEMT, the GaN cascode HEMTs based half-bridge circuit can also be unstable and excite the self-sustained oscillation [19]. Therefore, it is of interest to identify the instability of the GaN cascode HEMTs based half-bridge circuit.

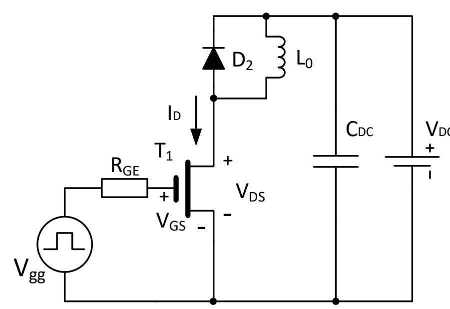
In this paper, the self-sustained oscillation which occurs during the turn-off transient of the cascode GaN HEMTs is studied. The remainder of this paper is structured as follows. In section II, the self-sustained turn-off oscillation appearing in the commercially available cascode GaN HEMTs is presented. In section III, the unique characteristics of the self-sustained turn-off oscillation are presented. In section IV, a small-signal model of the resonant circuit is proposed to derive the transfer function of the oscillatory system. In section V, the poles of the system transfer function are studied to identify the dominant poles which determine the occurrence of the oscillation. The damping ratio of the dominant pole is analyzed in section VI. The analyses reveal several methods to suppress the oscillation, which are proposed in section VII. In the end, the simulation is performed in section VIII to validate some of the unverified oscillation suppression methods.

## II. Self-Sustained Turn-Off Oscillation of Cascode GaN HEMT

To reproduce the self-sustained turn-off oscillation, the 650V/20A Transphorm cascode GaN HEMTs with part number TPH3208PS are utilized to perform the double-pulse test. Fig. 2 shows the test platform and its corresponding schematic circuit. In the test circuit, $T_1$ is the device under test. A 650V/26A SiC Schottky with part number CVFD20065A is utilized as the freewheeling diode $D_2$. $L_0 = 380\mu H$ is the load inductor. $R_{GE}$ is the external gate resistance. $V_{DC}$ is the DC-bus voltage, which is connected to a power capacitor $C_{DC} = 390\mu F$. A function generator is controlled by the computer to send a pulse signal to the gate driver, which switches the gate drive voltage $V_{gg}$ with 0V/10V.




(a) The test platform.




(b) The schematic circuit.

Fig. 2. The SC test setup. (a) Test platform. (b) Schematic circuit.

In the double pulse test, self-sustained oscillation is observed during the turn-off transient of cascode GaN HEMT, as shown in . When the device turns off, the self-sustained oscillation appears in the waveforms of $I_D$, $V_{DS}$ and $V_{GS}$. The oscillation holds for 1.3 $\mu s$ before it vanishes. To investigate the behaviour of cascode GaN HEMT during the oscillatory transient, the $V_{GS}$ waveform is zoomed, as shown in Fig. 4. During the turn-off transient, the $V_{gg}$ drives the $V_{GS}$ to

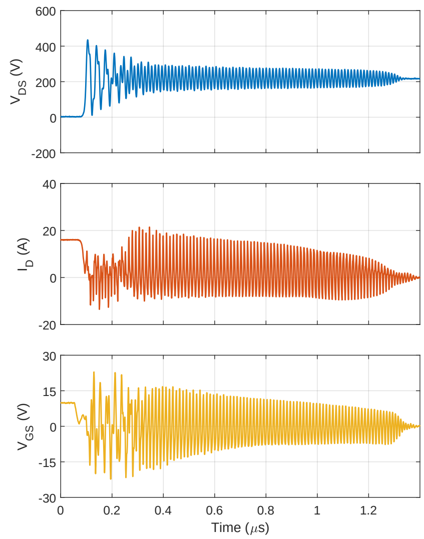



Fig. 3. Experimental turn-off waveforms of $I_D$, $V_{DS}$ and $V_{GS}$ with $V_{DC} = 220V$ and $R_{GE} = 16\Omega$.

drop. When the $V_{GS}$ drops down the threshold voltage $V_{th}$, it rings back and surpasses the threshold voltage $V_{th}$. This phenomenon is well known as false turn-on [11], [20], [21].

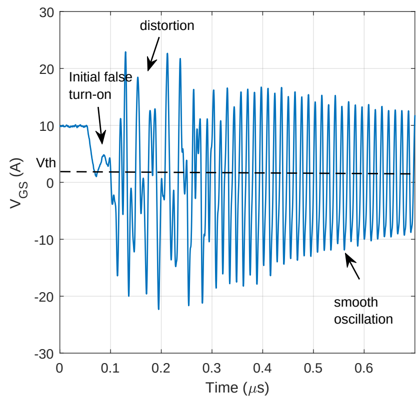



Fig. 4. The zoomed waveform of $V_{GS}$ presented in Fig. 3.

As shown in Fig. 3, when the device turns off, $dv/dt = 28kV/\mu s$ and $di/dt = 773A/\mu s$ are achieved. The steep $dv/dt$ and $di/dt$ induce the initial false turn-on of the cascode GaN HEMTs. During the turn-off transient, the cascode drain current is utilized to discharge the output capacitance of the LV MOSFET and the gate-source capacitance of the DHEMT so that the GaN DHEMT can turn off [2], [3]. This phenomenon is well-known as intrinsic current accelerating mechanism [2], [3]. The mechanism can greatly accelerate the turn off process [2], which induce very steep $dv/dt$ and $di/dt$ to generate triggering pulses $V_S$ and $V_G$ on common sourse inductance $L_S$ and gate loop impedance $Z_G$ respectively, as shown in Fig. 5. When the device turns off, the steep negative $di/dt$ generates positive $V_S$ on the common source inductance $L_S$, which can drive the gate to turn on [11], [13]. The steep positive $dv/dt$ can capacitively couple into the gate through the $C_{GD\_M}$ of LV MOSFET [22], which generates a displacement current $I_{disp}$, as shown in Fig. 5. The $I_{disp}$ flows through the gate loop impedance $Z_G$, which generates positive $V_G$ to drive the gate to turn on [22].

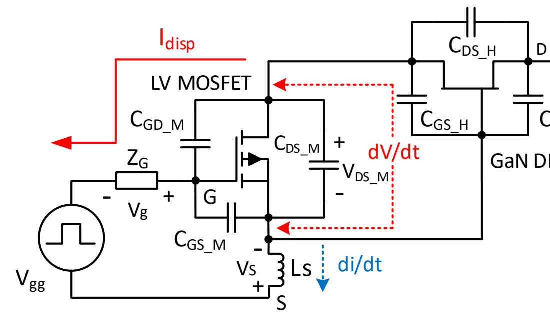



Fig. 5. Mechanism of the initial false turn-on for cascode GaN HEMT.

After the initial false triggering, the LV MOSFET and DHEMT both turn on, which generates additional conductive channels in the LV MOSFET and DHEMT. Since the LV MOSFET and DHEMT operate under saturation mode, the channel currents can be considered as gate voltage-controlled current sources $I_{CH1}$ and $I_{CH2}$ [14]–[17], which drive the RLC circuit to resonate, as shown in Fig. 6. When the device turns on, the currents $I_{CH1}$ and $I_{CH2}$ give rise to the positive $di/dt$. The channel current $I_{CH1}$ charges the output capacitances of LV MOSFET, which induces a negative $dv/dt$ on LV MOSFET. This generates negative $V_S$ and $V_G$ to drive the device to turn off again. The $I_{CH1}$ and $I_{CH2}$ reduce, which in turn excites positive $V_S$ and $V_G$ to drive the device to turn on. As a result, the device can turn on and turn off repetitively, which generates a positive feedback mechanism to draw additional energy from the DC-bus voltage. If the resonant circuit is unstable, the additional energy can compensate for the power losses dissipated by the resistive components in the resonant circuit and the oscillation can self-sustain [14].

In Fig. 4, after the initial false turn-on, the resonant circuit shown in Fig. 6 is activated, which disrupts the natural resonance and induces the distortion in the oscillation. After a few oscillatory cycles, an equilibrium is achieved between the damping effect induced by the resistive components and the driving force provided by the positive feedback mechanism. A smooth sinusoidal oscillation is thereby generated in the end, as shown in Fig. 4.

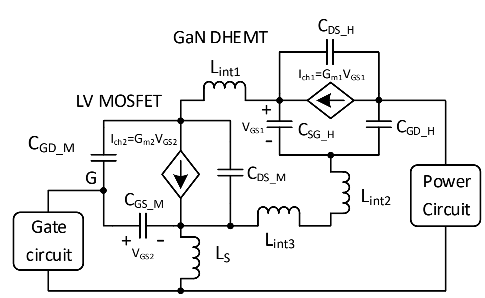



Fig. 6. Equivalent resonant circuit after the initial false turn-on.

From the analysis presented above, it can be noticed that the occurrence of the self-sustained oscillation requires two fundamental conditions:

1) The false triggering pulse can reopen the gate and causes the false turn-on in the initial turn-off oscillation cycles.

2) The resonant circuit is unstable. If the resonant circuit is unstable, the energy drawn by the positive feedback mechanism can compensate for the power dissipation. The triggering pulses are thereby generated repetitively, which drives the oscillation to self-sustain.

It should be noticed that the first condition triggers the onset of self-sustained oscillation. The second condition determines whether the oscillation can self-sustain. In this study, the instability of the resonant circuit is studied to avoid the occurrence of the second condition.

## III. Characteristics of the Self-Sustained Oscillation

In this study, the double-pulse test is performed under various test conditions to identify the impact of load current $I_L$, gate resistance $R_G$ and DC-bus voltage $V_{DC}$ on the self-sustained oscillation. The test results are provided in the following subsections.

### A. Impact of $I_L$ on the self-sustained oscillation

Fig. 7 shows the influence of load current $I_L$ on the turn-off oscillation. When $I_L$ is 10A, the turn-off oscillation rapidly attenuates. When $I_L$ rises to 15 A, the oscillation sustains for 1.2$\mu s$. The duration of the self-sustained oscillation does not have significant changes when $I_L$ further increases to 20 A.

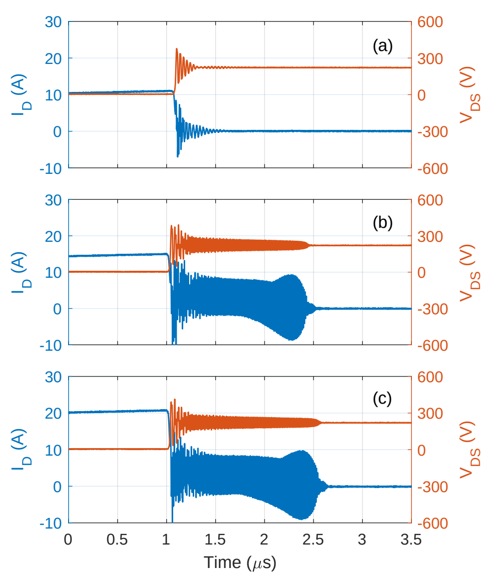



Fig. 7. Experimental turn-off waveforms of the cascode GaN HEMT with $V_{DC} = 220V$ and $R_{GE} = 26\Omega$ when $I_L$ is (a) 10 A, (b) 15 A and (c) 20A.

This phenomenon is due to the initial false triggering turn-on. As shown in Fig. 5, with the increase of load current, the steeper $di/dt$ induces higher $V_S$ voltage on the common source inductance to trigger the initial turn-on. Due to the intrinsic current accelerating mechanism, the larger load current also accelerates the turn-off speed. A steeper $dv/dt$ is thereby achieved to generate higher $V_G$. Therefore, with the increase of load current, the false triggering pulse becomes higher and the initial false turn-on is excited when $I_L \geq 15A$. However, since $di/dt$ and $dv/dt$ can not affect the instability of the resonant circuit, the self-sustained oscillation does not have significant changes when $I_L$ further increase to 20 A. This phenomenon proves that the initial false turn-on acts as a triggering mechanism for the onset of self-sustained turn-off oscillation.

### B. Impact of $V_{DC}$ on the self-sustained oscillation

The impact of the DC-bus voltage $V_{DC}$ on the turn-off oscillation is presented in Fig. 8. With $V_{DC} = 200V$, the turn-off oscillation quickly attenuates. When $V_{DC}$ increases to 220V, the self-sustained oscillation holds for 1.2$\mu s$. When $V_{DC}$ increases to 280V, the duration of the oscillation prolongs to 5 $\mu s$. When $V_{DC} = 320V$, the oscillation self-sustains all the time. Therefore, the turn-off oscillation becomes more unstable when the $V_{DC}$ becomes higher.

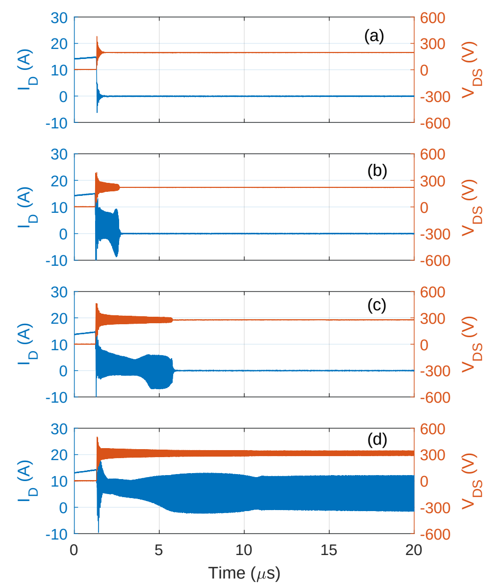



Fig. 8. Experimental turn-off waveforms of the cascode GaN HEMT with $R_{GE} = 26\Omega$ $I_L = 15A$ when $V_{DC}$ is (a) 200V, (b) 220V, (c) 280V and (d) 320V.

Previous research [17], [18] shows that the self-sustained oscillation can also occur during the switching transient of GaN EHEMTs. However, in [17], [18], the self-sustained oscillation of GaN EHEMTs is observed when $V_{DC}$ ranges from 60V to 100V. The GaN EHEMTs only suffer from self-sustained oscillation under low-voltage operation conditions. For the cascode GaN HEMTs, the turn-off oscillation becomes self-sustained when $V_{DC} \geq 220V$ and tends to be more unstable when the $V_{DC}$ becomes higher. This characteristic makes the turn-off oscillation of cascode GaN HEMTs a threat for real power converter applications.

### C. Impact of gate resistance on the self-sustained oscillation

Fig. 9 shows the impact of gate resistance on the self-sustained oscillation. The duration of the self-sustained oscillation becomes longer when $R_{GE}$ increases from 16$\Omega$ to 26$\Omega$.

When $R_{GE}$ increases to 46Ω, the duration further extends. The self-sustained oscillation becomes more unstable with the increase of $R_{GE}$. This phenomenon contradicts the conventional knowledge presented in [14]–[17], [23]. In the previous studies, the gate resistance is widely acknowledged to have a very strong damping effect on the self-sustained switching oscillation of GaN EHEMTs [17], SiC MOSFET [14], [15], [23] and SiC JFET [16]. The self-sustained oscillation can be suppressed when few ohms of gate resistance is utilized [15], [17]. In this case, since the self-sustained switching oscillation of cascode GaN HEMTs becomes more unstable with the increase of $R_{GE}$, the oscillation can not be suppressed by increasing the gate resistance.

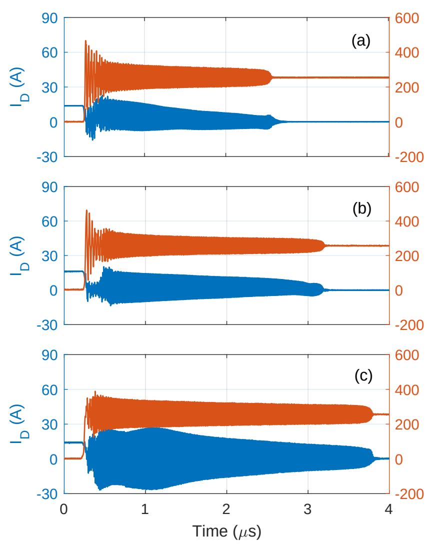



Fig. 9. Experimental turn-off waveforms of the cascode GaN HEMT with $V_{DC} = 260V$ and $I_L = 15A$ when $R_{GE}$ is (a) 16Ω, (b) 26Ω and (c) 46Ω.

## IV. SMALL-SIGNAL AC MODEL

The analyses in section II show that the instability of the resonant circuit determines whether the turn-off oscillation can self-sustain. Therefore, the instability of the resonant circuit should be analyzed. This can be achieved by analyzing the equivalent small-signal model of the resonant circuit [14]–[18]. Following the approach presented in [14]–[18], a small-signal model of the test circuit is derived, which is shown in Fig. 10. In the model, the $C_{DC}$ and $V_{DC}$ are short-circuited. The freewheeling diode $D_2$ is replaced by its junction capacitance $C_{D2}$. The gate drive voltage $V_{gg}$ is replaced by its small-signal model $V_P$. $L_P$ is the power loop inductance, which includes the stray inductance at the power circuit and drain terminal of the device. $L_G$ is the gate loop inductance, which includes the stray inductance of the gate circuit and gate terminal of the device. $L_S$ is the common source stray inductance. $R_G$ is the total gate resistance, which is the combination of internal gate resistance $R_{GI}$ and external gate resistance $R_{GE}$. $R_P$ is the stray resistance of the power loop, which includes the stray resistances of the device and power circuit. The GaN cascode is replaced by its equivalent small-signal model. In the model, $L_{int1(2,3)}$ are the stray inductances of the bond wire interconnections between the LV MOSFET and DHEMT. $R_{GH}$ is the internal gate resistance of the DHEMT. $C_{GD\_M(H)}$, $C_{DS\_M(H)}$ and $C_{GS\_M(H)}$ are the gate-drain, drain-source and gate-source capacitances of the LV MOSFET and DHEMT. $i_{CH1(2)} = G_{m1(2)} \cdot v_{GS1(2)}$ is the small-signal model of the channel current $I_{CH1(2)}$.

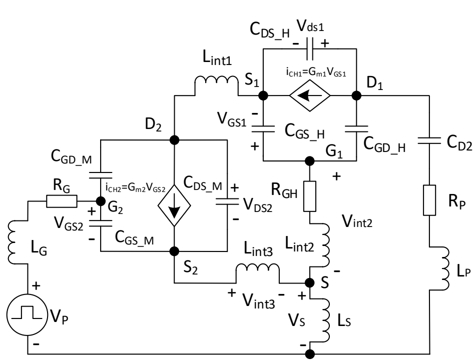



Fig. 10. The small-signal model of the test circuit.

In the small-signal model, by analyzing the node current in $G_2$, $S_2$, $D_2$, $G_1$, $D_1$, $S_1$ and $S$, the equations (1)-(7) can be obtained, which are presented as follows:

$$\frac{V_P - (V_{GS2} + V_{int3} + V_S)}{R_G + sL_G} - sV_{GS2}C_{GS\_M} - s(V_{GS2} - V_{DS2})C_{GD\_M} = 0 \quad (1)$$

$$\frac{V_{int3}}{sL_{int3}} - sV_{GS2}C_{GS\_M} - G_{m2}V_{GS2} - sV_{DS2}C_{DS\_M} = 0 \quad (2)$$

$$s(V_{DS2} - V_{GS2})C_{GD\_M} + sV_{DS2}C_{DS\_M} + G_{m2}V_{GS2} - (V_{int2} - V_{GS1} - V_{DS2} - V_{int3})/sL_{int1} = 0 \quad (3)$$

$$V_{int2}/(sL_{int2} + R_{GH}) - s(V_{DS1} - V_{GS1})C_{GD\_H} + sV_{GS1}C_{GS\_H} = 0 \quad (4)$$

$$sV_{DS1}C_{DS\_H} + sV_{GS1}C_{GS\_H} + G_{m1}V_{GS1} - (V_{int2} - V_{GS1} - V_{DS2} - V_{int3})/sL_{int1} = 0 \quad (5)$$

$$sV_{DS1}C_{DS\_H} + s(V_{DS1} - V_{GS1})C_{GD\_H} + G_{m1}V_{GS1} + \frac{(V_S + V_{int2} - V_{GS1} + V_{DS1})}{sL_P + R_P + 1/(SC_{D2})} = 0 \quad (6)$$

$$V_{int3}/sL_{int3} + V_{int2}/(sL_{int2} + R_{GH}) - V_S/sL_S = 0 \quad (7)$$

Where the definition of the voltage components $V_{GS1(2)}$, $V_{DS1(2)}$, $V_{int2(3)}$ and $V_S$ are presented in Fig. 10. By solving the equations (1)-(7), the $V_{GS2}$ can be obtained as a function of $V_P$. In the oscillatory circuit, the gate drive voltage $V_P$ provides the initial disturbance signal in the gate. Therefore, $V_P$ can be considered as the input of the oscillatory system. Considering the $V_{GS2}$ as the output of the oscillatory system, the transfer function $H(s)$ can be obtained as:

$$H(s) = \frac{V_{GS2}}{V_P} \quad (8)$$

In this case, the transfer function $H(s)$ is of seventh order. The function is very complex, which make it impossible to be solved analytically. Therefore, the $H(s)$ and its poles are

TABLE I
PARAMETERS OF THE DEVICE UNDER TEST

| Symbol | Value | Symbol | Value | Symbol | Value |
|---|---|---|---|---|---|
| $R_{GI}$ | 2.2 Ω | $R_P$ | 0.5 Ω | $R_{GH}$ | 0.12 Ω |
| $C_{D2}$ | 1.09 nF | $G_{m1}$ | 0.08 S | $G_{m2}$ | 0.07 S |
| $L_P$ | 6.7 nH | $L_S$ | 0.8 nH | $L_G$ | 5.9 nH |
| $L_{int1}$ | 0.26 nH | $L_{int2}$ | 0.2 nH | $L_{int3}$ | 0.33 nH |
| $C_{GD\_M}$ | 71.8 pF | $C_{GS\_M}$ | 653.7 pF | $C_{DS\_M}$ | 66.9 pF |

derived numerically by MATLAB.

To obtain the transfer function $H(s)$, the dc operating point should be clarified for linearization. In the cascode GaN HEMT under test, a silicon LV MOSFET with part number IRF8707 is utilized to drive a GaN DHEMT with part number TPH3208. The stray capacitances of the LV MOSFET should be linearized at it is off-state voltage $V_{DS\_M(off)}$. The SPICE simulation study identifies that the $V_{DS\_M(off)} \approx 24V$. The stray capacitances of the GaN DHEMT are thereby linearized at $V_{DC} - V_{DS\_M(off)}$. Since the freewheeling diode $D_2$ forward conducts during the turn-off transient, its junction capacitance $C_{D2}$ is linearized at 0V. Following the approach presented in [14], [15], the $G_{m1}$ and $G_{m2}$ are linearized at the threshold voltages of DHEMT and LV MOSFET, respectively. At the dc operating point, the device parameters are extracted base on the data provided by the device manufacturer. The external stray inductances are extracted by the Q3D extractor. The internal stray elements $L_{int1(2,3)}$ and $R_{GH}$ are obtained from the SPICE model provided by the device manufacturer. The values of all the parameters are summarized in Table I. The C-V curves of the GaN DHEMT's stray capacitances provided by the device manufacturer are presented in Fig. 11. With the increase of $V_{DS\_H}$, the $C_{GD\_H}$ greatly decreases, whereas the $C_{DS\_H}$ and $C_{GS\_H}$ do not have significant changes except for the initial step down. In this study, the $C_{DS\_H}$ and $C_{GS\_H}$ are approximately considered as a constant, $C_{DS\_H} = 40pF$ and $C_{GS\_H} = 130pF$.

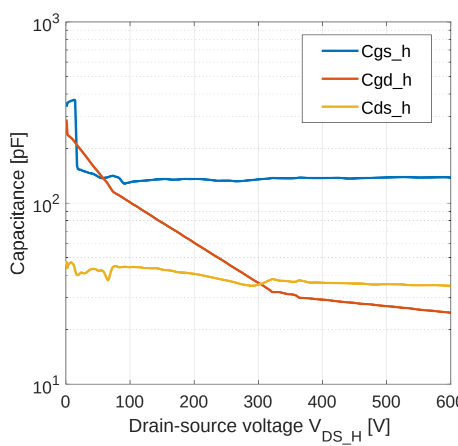



Fig. 11. The C-V curves of the GaN DHEMT stray capacitances.

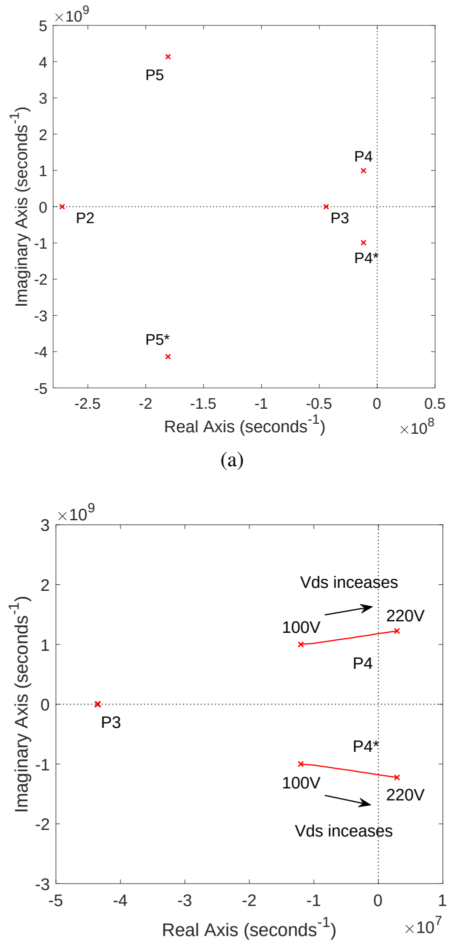
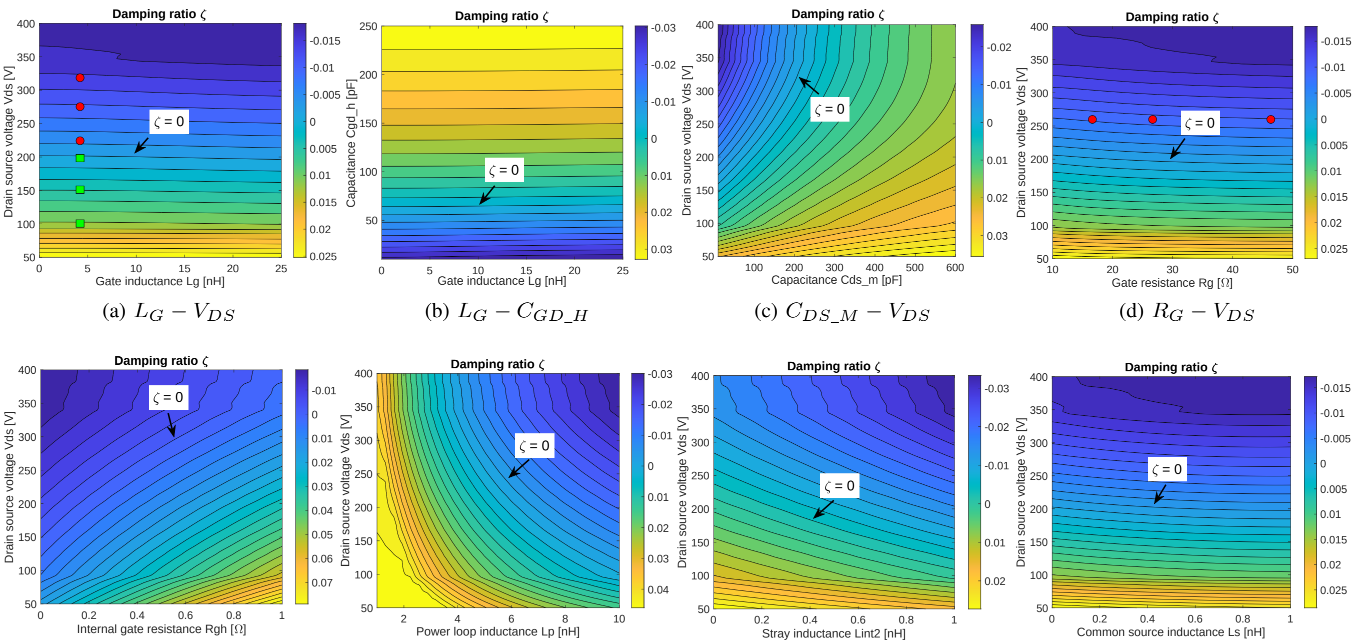



Fig. 12. The poles of transfer function $H(s)$: (a) Plot of poles P2 - P5 with $V_{DS} = 100V$ and $R_{GE} = 26\Omega$; (b) Loci of the P3 and P4 when $V_{DC}$ increase from 100V to 220V.

## V. ANALYSIS ON POLES OF TRANSFER FUNCTION $H(s)$

Since the instability of turn-off oscillation is determined by the transfer function $H(s)$, the poles of $H(s)$ are analyzed in this section. With $V_{DS} = 100V$ and $R_{GE} = 26\Omega$, five poles of $H(s)$ are obtained. The real pole P1$= -4.1 \times 10^9$ seconds$^{-1}$, which locates far away from the imaginary axis. Its impact on the system instability is thereby negligible. Fig. 12a shows the other poles. Compared with real pole P2 and conjugate pole pair P5, real pole P3 and conjugate pole pair P4 locate much closer to the imaginary axis. Therefore, the system instability is dominated by P3 and P4.

To clarify the impact of P3 and P4 on the system instability, the loci of P3 and P4 are plotted when $V_{DS}$ increases from 100V to 220V, as shown in Fig. 12b. Compared to the P3, the P4 locates closer to the imaginary axis. Moreover, with the increase of $V_{DS}$, the real pole P3 stays unchanged, while the conjugate pole pair P4 moves to the right and lies on the right half of the s-plane when $V_{DS} = 220V$. According to the well-known Routh-Hurwitz stability criterion, the oscillation is unstable when the system has a conjugate pole pair at the right half of the s-plane. The impact of P4 on the system instability agrees with the test results presented in Fig. 8. The instability




(a) $L_G - V_{DS}$ (b) $L_G - C_{GD\_H}$ (c) $C_{DS\_M} - V_{DS}$ (d) $R_G - V_{DS}$

(e) $R_{GH} - V_{DS}$ (f) $L_P - V_{DS}$ (g) $L_{int2} - V_{DS}$ (h) $L_S - V_{DS}$

Fig. 13. The contour plots of the damping ratio $\zeta$.

of $H(s)$ is thereby mainly determined by the conjugate pole pair P4. In this study, the damping ratio $\zeta$ of P4 is utilized to analyze the instability of the test circuit. $\zeta = \sigma/(\sigma^2 + \omega^2)$, where the -$\sigma$ and $\omega$ are the real and imaginary parts of the poles. When $\zeta < 0$, the oscillatory system is unstable and the turn-off oscillation becomes self-sustained. When $\zeta > 0$, the oscillatory system is stable. $\zeta = 0$ indicates a constant-amplitude oscillation.

## VI. Analysis on Instability of Turn-off Oscillation

In this section, the impact of various parameters on the damping ratio $\zeta$ of the pole pair P4 is analyzed to clarify the occurrence condition of the self-sustained oscillation. As shown in Fig. 13, the contour plots of $\zeta$ as a function of various parameters are presented. The contour lines with $\zeta = 0$ are indicated in the plots.

In Fig. 13a, the $\zeta$ is plotted as a function of $L_G$ and $V_{DS}$. The contour plot shows that $L_G$ does not have a significant impact on the $\zeta$. With the increase of $L_G$, $\zeta$ only slightly decreases. The Fig. 13a also shows the impact of $V_{DS}$ on $\zeta$. The test results presented in Fig. 8 are included in the figure. The red dots indicate the self-sustained oscillation and the green squares denote the damped ring-down. When $V_{DS} < 202V$, $\zeta$ is positive and the turn-off oscillation rings down. When $V_{DS} > 202V$, $\zeta$ becomes negative and self-sustained oscillation thereby occurs. With the increase of $V_{DS}$, $\zeta$ greatly reduces and the oscillation becomes more unstable. The calculated $\zeta$ aligns with the test results.

The impact of $V_{DS}$ on the $\zeta$ is related to the $C_{GD\_H}$. As shown in figures 11 and 13b, with the increase of $V_{DS}$, the reduced $C_{GD\_H}$ gives rise to the reduction of $\zeta$. When $C_{GD\_H}$ drops below $66pF$, $\zeta$ becomes negative and self-sustained oscillation is excited. Therefore, the self-sustained turn-off oscillation can be suppressed by slightly increasing the $C_{GD\_H}$.

The previous research [5] shows that the self-sustained turn-off oscillation can be suppressed with an additional capacitor $C_X$ connected in parallel with the LV MOSFET. The introduction of the capacitor $C_X$ is equivalent to increase the drain-source capacitance $C_{DS\_M}$ of the LV MOSFET. Therefore, it is of interest to investigate the impact of the $C_{DS\_M}$ on the $\zeta$. As shown in Fig. 13c, with the increase of $C_{DS\_M}$, $\zeta$ rises drastically. Therefore, with capacitor $C_X$ utilized, the self-sustained oscillation is suppressed due to the larger equivalent drain-source capacitance of the LV MOSFET. Due to the merit of the cascode structure, the larger $C_{DS\_M}$ only slightly increases the switching loss of the device [3], [5], [24]. Therefore, increasing $C_{DS\_M}$ is a good option to suppress the oscillation.

The impact of the gate resistance $R_G$ and the internal DHEMT gate resistance $R_{GH}$ on the $\zeta$ are presented in Figs. 13d and 13e, respectively. The test results proposed in Fig. 9 are also indicated as red dots in Fig. 13d. With the increase of $R_G$, the $\zeta$ slightly reduces, the turn-off oscillation thereby becomes more unstable. The analytical results align with the experimental data. The resistance $R_{GH}$ shows a very strong damping effect on the $\zeta$. As shown in Fig. 13e, $\zeta$ greatly increases when $R_{GH}$ becomes larger. The oscillation can thereby be suppressed by increasing the $R_{GH}$.

Figs. 13f and 13g show that the stray inductances $L_P$ and $L_{int2}$ have a very strong impact on the $\zeta$. With the increase of $L_P$ or $L_{int2}$, $\zeta$ greatly drops. With higher $V_{DS}$, the $\zeta$ drops even faster. The oscillation can thereby be suppressed by reducing the $L_P$ and $L_{int2}$. As shown in 13h, with the increase common source inductance $L_S$, $\zeta$ slightly decreases. Th $L_S$ has relatively minor impact on the $\zeta$.

## VII. Suppression methods of the self-sustained oscillation

The theoretical analysis presented in the previous section shows that some parameters can be optimized to achieve a positive damping ratio $\zeta$, which are discussed as follows:

1. Increasing the stray capacitances $C_{GD\_H}$ and $C_{DS\_M}$: The analytical results presented in Figs. 13b shows that $\zeta$ greatly increases when $C_{GD\_H}$ becomes larger. The oscillation can be suppressed when $C_{GD\_H}$ becomes larger than $66pF$. The optimized $C_{GD\_H}$ can be achieved by optimizing the structure of the field plate and gate in GaN DHEMT. As shown in Fig. 13c, to suppress the oscillation, the required $C_{DS\_M}$ should be much larger than its original value. To achieve the required $C_{DS\_M}$, an external capacitor $C_X$ can be connected in parallel with the LV MOSFET. In the test, the impact of $V_{DC}$ on the turn-off oscillation validates that increasing $C_{GD\_H}$ is an effective oscillation suppression method. The effectiveness of the $C_X$ on the oscillation suppression is also verified by the previous research [5]. It should be noticed that the large $C_{GD\_H}$ and $C_{DS\_M}$ can also slow down the switching speed of the device. Therefore, the capacitances of the $C_{GD\_H}$ and $C_{DS\_M}$ should be optimized based on the proposed model so that the device can avoid the self-sustained turn-off oscillation with an acceptable reduction in the switching performance. The parameter optimization procedure is presented in Fig. 14.

2. Increasing the internal gate resistance $R_{G\_H}$ and decreasing the stray inductance $L_{int2}$: As shown in Fig. 13e, $\zeta$ greatly increases when $R_{G\_H}$ becomes larger. With smaller $L_{int2}$, $\zeta$ also greatly increases, as shown in Fig. 13g. In the cascode GaN HEMTs, the gate loop of the DHEMT does not have effective damping due to the cascode configuration. The gate loop of the DHEMT resonates with the power loop, which causes turn-off oscillation. With large $R_{G\_H}$ and small $L_{int2}$ utilized, the gate loop resonance is greatly damped, which can greatly suppress the self-sustained turn-off oscillation. The $L_{int2}$ can be minimized by optimizing the packaging layout of the cascode GaN HEMTs. Despite the strong damping effect, a large $R_{G\_H}$ can also greatly increase the switching loss [25] and cause some severe reliability issues [10]. Therefore, $R_{G\_H}$ should be optimized to suppress the self-sustained oscillation while avoiding the unwanted side-effect. The parameter optimization procedure presented in Fig. 14 can be utilized to obtain the optimized $R_{G\_H}$.

3. Minimizing the stray inductance $L_P$: As shown in Figs. 13f, the $\zeta$ greatly increases with the by the reduction of $L_P$. With small $L_P$, the resonant in the power loop is damped, which can greatly suppress the turn-off oscillation. Therefore, the $L_P$ should be minimized under any circumstances. The reduction of $L_P$ can be achieved by optimizing the circuit design and reducing the package stray inductance.

In the test circuit, the stray elements $R_{G\_H}$, $L_P$, and $L_{int2}$ can not be modified. Therefore, the effectiveness of the oscillation suppression methods 2 and 3 can only be validated by SPICE simulation. In the SPICE model, the C-V characteristics are approximately modeled by a simple analytical expression, which can not accurately replicate the C-V characteristics of the real device. Moreover, the self-sustained oscillation is very unstable and can cause divergence in the simulation. To avoid the divergence, the solver tends to damp the turn-off oscillation. Therefore, the simulation can not perfectly reproduce the test results. In this simulation, some of the circuit parameters utilized in the test are modified to trigger the self-sustained oscillation. However, from the previous discussion, it can be noticed that the impact of the stray elements $R_{G\_H}$, $L_P$, and $L_{int2}$ on the turn-off oscillation is universal, which can be validated by the simulation despite the changes in the parameters.

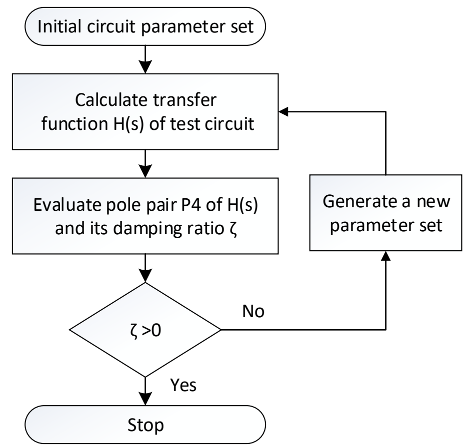



Fig. 14. Flow chart showing the parameter optimization procedure.

## VIII. The simulation validation

In this section, the SPICE simulation is performed to validate the impact of $R_{G\_H}$, $L_P$ and $L_{int2}$ on the turn-off oscillation. Fig. 15 shows the test circuit utilized in the simulation. In the circuit, the cascode GaN HEMT is composed of a LV MOSFET $T_{1a}$ and a GaN DHEMT $T_{1b}$. The Spice model of the $T_{1a}$, $T_{1b}$ and freewheeling diode $D_2$ are provided by the device manufacturer. In the test circuit, the circuit parameters presented in Table I are used in the simulation. To trigger the self-sustained oscillation, $V_{DC} = 320V$ and $R_{GE} = 16\Omega$. $I_L = 28A$ are utilized. With $L_P = 6.7nH$, $L_{int2} = 0.2nH$ and $R_{GH} = 0.12\Omega$, the self-sustained oscillation is reproduced in the turn-off waveforms, as shown in Fig. 16.

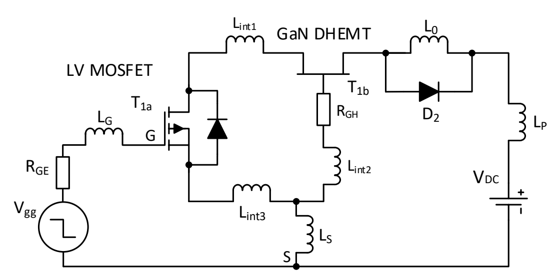



Fig. 15. The circuit utilized for the simulation.

To validate the impact of $L_P$ on the self-sustained oscillation, the simulation is performed utilizing smaller $L_P$ while the other parameters remain unchanged. As shown in Fig. 17(a), when $L_P = 5.7nH$, the self-sustained turn-off oscillation is suppressed to a ring-down. When $L_P$ further decreases to 4.7nH, the turn-off oscillation is further dampened, as shown in Fig. 17(b). This demonstrates that reducing $L_P$ is an effective way to dampen the self-sustained turn-off oscillation.

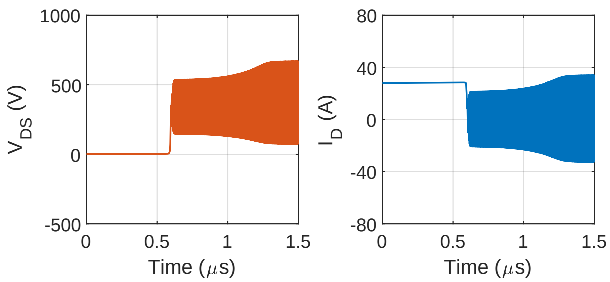



Fig. 16. Simulated waveforms of $V_{DS}$ and $I_D$ with $L_P = 6.7nH$, $L_{int2} = 0.2nH$ and $R_{GH} = 0.12\Omega$.

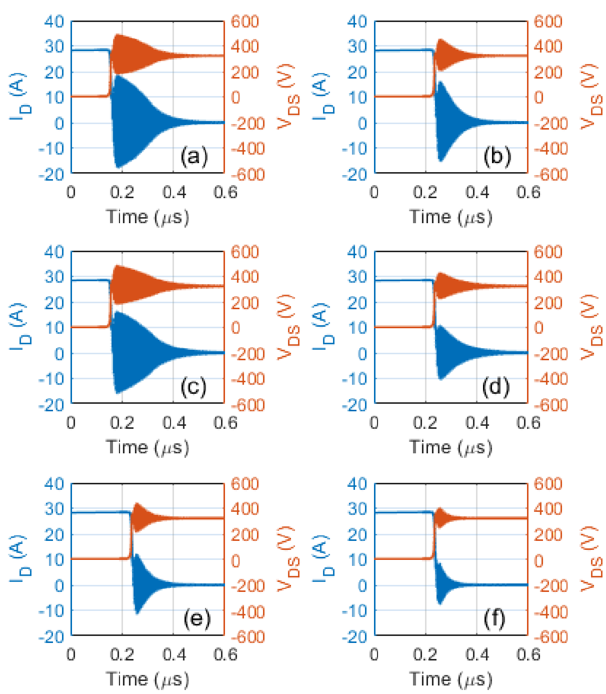



Fig. 17. Simulated waveforms with stray element modified as: (a) $L_P = 5.7nH$, (b) $L_P = 4.7nH$, (c) $L_{int2} = 0.15nH$, (d) $L_{int2} = 0.1nH$, (e) $R_{GH} = 0.32\Omega$ and (f) $R_{GH} = 0.52\Omega$.

To validate the impact of $L_{int2}$ on the self-sustained oscillation, the simulation is also performed with $L_{int2}$ reduced to 0.15nH and 0.1nH. As shown in Figs. 17(c) and 17(d), the turn-off oscillation is greatly dampened when $L_{int2}$ becomes smaller. The self-sustained turn-off oscillation can thereby be dampened by reducing the $L_{int2}$.

In the end, the $R_{GH}$ is increased to validate its damping effect. As shown in Fig. 17(e), the self-sustained turn-off oscillation is greatly suppressed when $R_{GH}$ increases to 0.32 $\Omega$. The oscillation is further dampened when $R_{GH}$ increases to 0.52 $\Omega$, as shown in 17(f). This validates the damping effect of $R_{GH}$ on the self-sustained turn-off oscillation. The oscillation can thereby be dampened by increasing $R_{GH}$.

## IX. Conclusion

This paper presents a comprehensive investigation on the self-sustained oscillation which appears in the turn-off transient of GaN cascode HEMTs. The analyses on the test waveforms show that the occurrence of the self-sustained oscillation requires two fundamental conditions. Firstly, the false triggering pulse should reopen the gate, which triggers the onset of the self-sustained oscillation. Secondly, the resonant circuit under test should be unstable. The first condition triggers onset of the oscillation, while the second condition determines whether the oscillation can self-sustain.

The test results also reveal the characteristics of the self-sustained oscillation. To trigger the self-sustained turn-off oscillation of GaN cascode HEMTs, the load current should be large enough. However, when the oscillation is excited, the load current does not have a significant impact on the instability of the oscillation. With the increase of DC-bus voltage, the self-sustained oscillation becomes more unstable. The gate resistance does not show effective damping on the self-sustained oscillation. In contrast, the self-sustained oscillation unexpectedly becomes more unstable when the gate resistance becomes larger.

To investigate the instability of the resonant circuit, the transfer function of the oscillatory system is derived. Based on the model, the impact of various parameters on the turn-off oscillation is analyzed. The analyses reveal that the self-sustained turn-off oscillation can be suppressed by increasing the stray capacitances $C_{GD\_H}$, $C_{DS\_M}$ and gate resistance $R_{G\_H}$ or reducing the stray inductances of the $L_P$ and $L_{int2}$. The effectiveness of the proposed methods is validated by the experimental data and simulation results.

## References


[1] Y. Niiyama, S. Ootomo, H. Kambayashi, N. Ikeda, T. Nomura, and S. Kato, "Normally-off operation GaN based MOSFETs for power electronics," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2009, pp. 1–4, DOI: 10.1109/csics.2009.5315770.

[2] X. Huang, Z. Liu, Q. Li, and F. C. Lee, "Evaluation and application of 600 v GaN HEMT in cascode structure," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2453–2461, 2014, DOI: 10.1109/TPEL.2013.2276127.

[3] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2208–2219, DOI: 10.1109/TPEL.2013.2267804.

[4] L. He, Z. Xuan, L. Wen, J. A. Brothers, and W. Jin, "Paralleled operation of high voltage Cascode GaN HEMTs," *IEEE Journal of Emerging & Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 815–823, 2017, DOI: 10.1109/JESTPE.2016.2557316.

[5] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding divergent oscillation of a cascode GaN device under high-current turn-off condition," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 593–601, 2017, DOI: 10.1109/TPEL.2016.2532799.

[6] Z. Xu, W. Zhang, F. Xu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Investigation of 600 V GaN HEMTs for high efficiency and high temperature applications," in *Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 131–136, DOI: 10.1109/JESTPE.2016.2563220.

[7] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," in *IEEE Applied Power Electronics Conference and Exposition*, 2014, pp. 1484–1489, DOI: 10.1109/APEC.2014.6803503.

[8] T. Ryo, A. Takamasa, H. Bernhard, Z. Michael, and H. Mike, "Cascode GaN FET Dynamic Characterization," *Bodo's Power Systems*, pp. 34–37, Mar. 2021.

[9] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A review of switching oscillations of wide bandgap semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 182–13 199, 2020.

[10] R. Siemieniec, G. Nöbauer, and D. Domes, "Stability and performance analysis of a sic-based cascode switch and an alternative solution," *Microelectronics Reliability*, vol. 52, no. 3, pp. 509–518, 2012, DOI: 10.1016/j.microrel.2011.12.006.

[11] Z. Huang and J. Cuadra, "Preventing GaN Device VHF Oscillation," presented at APEC 2017 Industry Session, March 2017.

[12] F. Zhao, Y. Li, Q. Tang, and L. Wang, "Analysis of oscillation in bridge structure based on GaN devices and ferrite bead suppression method," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 391–398, DOI: 10.1109/ECCE.2017.8095809.

[13] Z. Chen and J. R. Guitart, "dV/dt Immunization limit of LV MOSFET in cascode GaN FET and dV/dt safe chart for MOSFETs," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2017, pp. 1946–1949.

[14] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2380–2392, 2014, DOI: 10.1109/TPEL.2013.2273275.

[15] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Self-Sustained Turn-Off Oscillation of SiC MOSFETs: Origin, Instability Analysis, and Prevention," *Energies*, vol. 12, no. 11, p. 2211, 2019, DOI: 10.3390/en12112211.

[16] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE transactions on Power Electronics*, vol. 28, no. 10, pp. 4453–4459, 2012, DOI: 10.1109/TPEL.2012.2226473.

[17] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability analysis and oscillation suppression of enhancement-mode gan devices in half-bridge circuits," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1585–1596, 2018, DOI: 10.1109/TPEL.2017.2684094.

[18] K. Umetani, R. Matsumoto, and E. Hiraki, "Prevention of oscillatory false triggering of GaN-FETs by balancing Gate-Drain capacitance and common-source inductance," *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 610–619, 2019, DOI: 10.1109/TIA.2018.2868272.

[19] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Investigation on the short-circuit oscillation of Cascode GaN HEMTs," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6292–6300, 2020, DOI: 10.1109/TPEL.2019.2947274.

[20] H. Umegami, A. Nishigaki, F. Hattori, and M. Yamamoto, "Investigation of false triggering mechanism," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 9, no. 1, pp. 102–104, 2014, DOI: 10.1002/tee.21943.

[21] A. Nishigaki, H. Umegami, F. Hattori, W. Martinez, and M. Yamamoto, "An analysis of false turn-on mechanism on power devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2014, pp. 2988–2993, DOI: 10.1109/ECCE.2014.6953806.

[22] Z. Wang, J. Honea, Y. Shi, and H. Li, "Investigation of driver circuits for GaN HEMTs in leaded packages," in *IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2014, pp. 81–87, DOI: 10.1109/WiPDA.2014.6964629.

[23] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Analysis on the Self-Sustained Oscillation of SiC MOSFET Body Diode," *IEEE Transactions on Electron Devices*, vol. 66, no. 10, pp. 4287–4295, 2019, DOI: 10.1109/TED.2019.2937059.

[24] X. Huang, W. Du, F. C. Lee, Q. Li, and Z. Liu, "Avoiding Si MOSFET avalanche and achieving zero-voltage switching for cascode GaN devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 593–600, 2016, DOI: 10.1109/TPEL.2015.2398856.

[25] P. J. Garsed and R. A. McMahon, "Understanding the cascode switching process," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2013, pp. 186–189, DOI: 10.1109/WiPDA.2013.6695593.

**Peng Xue** received the M.S., and Ph.D. degrees from Beihang University, Beijing, China in 2013 and 2017, respectively.
From 2017 to 2019, he works as a Post-Doctoral Research Fellow at University of Naples Federico II, Italy. He is currently a Post-Doctoral researcher at the Aalborg University, Denmark. His research interests include modeling, simulation, and experimental characterization of power semiconductor devices.

**Francesco Iannuzzo** (IEEE Senior member) received the M.Sc. degree in Electronic Engineering and the Ph.D. degree in Electronic and Information Engineering from the University of Naples, Italy, in 1997 and 2002, respectively.
He is currently a professor of reliable power electronics at the Aalborg University, Denmark, where he is also part of CORPE, the Center of Reliable Power Electronics. His research interests are in the field of reliability of power devices, condition monitoring, failure modelling and testing up to megawatts under extreme conditions. He is author or co-author of +250 publications on journals and international conferences, three book chapters and four patents, and has edited a book on Modern Power Electronic Devices (2020, IET). Besides the publication activity, over the past years he has been contributing +20 technical seminars about reliability at top-tier conferences as ISPSD, IRPS, EPE, ECCE, PCIM and APEC.
Prof. Iannuzzo currently serves as the vice-chair of the IEEE IAS Power Electronic Devices and Components Committee. In 2018 he was the general chair of the 29th ESREF, the first European conference on the reliability of electronics, and has recently been appointed general chair for the 2023 EPE-ECCE Europe conference in Aalborg.