# Switching Stability Analysis of Paralleled RC-IGBTs with Snapback Effect

Diaz Reigosa, P.; Rahimo, M.; Minamisawa, R.; Iannuzzo, F.

*Published in:*
IEEE Transactions on Electron Devices

*DOI (link to publication from Publisher):*
10.1109/TED.2021.3081614

*Publication date:*
2021

*Document Version*
Accepted author manuscript, peer reviewed version

# Switching Stability Analysis of Paralleled RC-IGBTs with Snap-Back Effect

P. Diaz Reigosa[a], M. Rahimo[b], R. Minamisawa[a] and F. Iannuzzo[c]
[a] University of Applied Sciences and Arts Northwestern Switzerland, Windisch, Switzerland
[b] MTAL GmbH, Gaensbrunnen, Switzerland
[c] Department of Energy Technology, Aalborg University, Denmark

***Abstract*—In this paper, a study of the snap-back behaviour of reverse conducting RC-IGBTs by means of 2D TCAD simulations is carried out. Half-cell TCAD models of 1200V RC-IGBT structures with different snap-back voltage levels were generated by varying the peak doping concentration of the punch-through N-buffer region. First observations show that snap-back could be an issue for low current switching commutations of paralleled RC-IGBTs operating at low temperatures, where one device falls back into unipolar mode and current is completely mis-shared. Results show that the RC-IGBT snap-back voltage level, circuit variations and operating conditions play a critical role for determining if the parallel RC-IGBTs operate in a stable or un-stable mode.**

***Index Terms*—Reverse Conducting IGBT, snapback, switching, instability**

## I. Introduction

Development trends continue to improve Reverse Conducting IGBTs (RC-IGBT) [1]–[3] where the integration of the IGBT and the freewheeling diode into a single structure allows for higher power per package footprint [4]–[6]. Due to the fact that both transistor and diode share the same chip area, there are challenges related to plasma distribution optimization that need to be considered. For example, a high plasma on the emitter side (p -well) reduces the on-state losses in IGBT mode, however a low plasma during diode mode is needed to reduce reverse recovery losses. This would be different in separate IGBT/diode chips since they allow optimization of each device independently [7], [8]. The challenges do not end here, apart from the power losses optimization, another challenge faced in the design of RC-IGBTs is the on-state snap-back behavior during IGBT mode [9]–[12]. The basic RC-IGBT structure has been implemented with collector shorts, and since then, different design concepts have been proposed to reduce or eliminate the snapback voltage without sacrificing the total available diode area [6], [13]. The introduction of a pilot IGBT collector region (i.e., no collector short) referred to as the Bimode Insulated Gate Transistor (BIGT), provided an easy to implement design to mitigate the snap-back behavior while still offering good diode characteristics [14]. The aim was to suppress the primary snap-back effect occurring at low current levels, as shown in the IV curves in Fig. 1 [15]. However, the BIGT output characteristics exhibited secondary snap-backs at high current levels which were also eliminated with an optimized radial layout design [15].

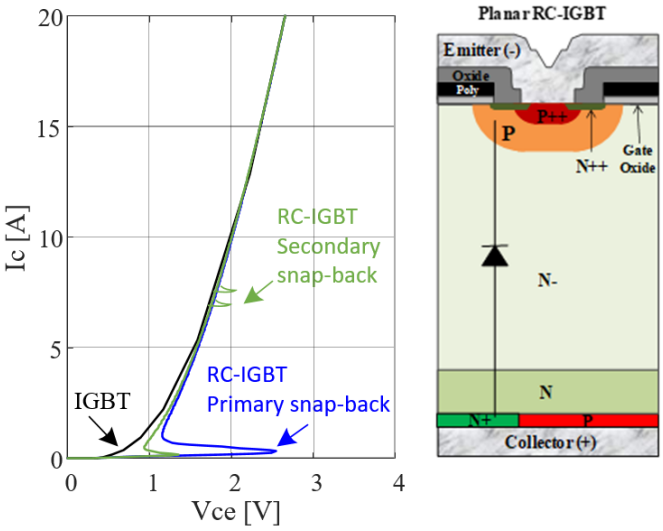


Fig. 1. IGBT and RC-IGBT IV on-state curves showing the primary and secondary snap-backs. The structure of the RC-IGBT with the $N^+$ collector short is presented on the right [16].

Many efforts have been made to mitigate the snap-back behavior [6]. One aspect of study is that a Negative Differential Resistance NDR zone [17]–[19] in the IV output characteristics is particularly harmful when devices are operating in parallel (i.e. some devices will fail to turn-on during switching transients). While many of the research has been focused on quantifying the snap-back voltage level during static conditions (i.e., IV characteristics) [20]–[22], the authors of this paper did not find previous work with respect to the effects of the snap-back phenomenon on device operation or a quantification of the snap-back magnitude (i.e. snap-back voltage $V_{SB}$) to which the effect becomes destructive in real applications [9]. So far, there is no published data of parallel High Voltage RC-IGBTs malfunction which can be attributed to the primary or secondary snap-back voltages. Improving our knowledge in this area is important while also maintaining the development trend towards designing snap-back free RC-IGBT concepts. The first investigation made by the authors [9] did not identify the root cause of the instability mechanism due to the snap-back effect. In this paper, the snap-back behavior of RC-IGBTs operating in parallel is investigated while attempting to analyze and understand the root causes

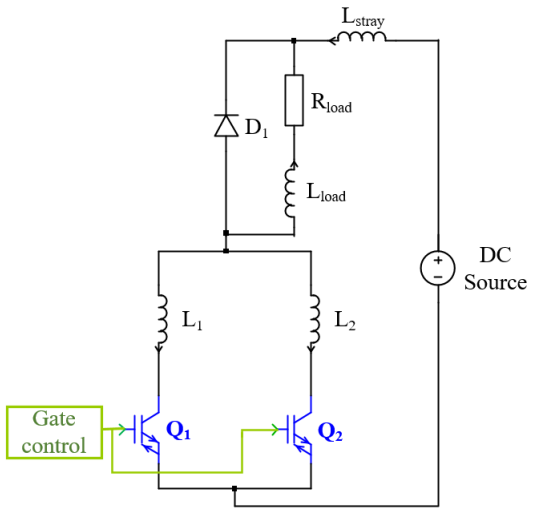


Fig. 2. Mixed mode circuit simulation model for obtaining double pulse waveforms for two parallel RC-IGBT devices $Q_1$ and $Q_2$. The stray inductances $L_1 = L_2$, unless specified.

leading to current mis-sharing between parallel devices.

The paper is organized as follows: Section II presents the RC-IGBT turn-on transient. Section III focus on the paralleling of RC-IGBTs having variations in snap-back voltage levels $V_{SB}$. Section IV demonstrates the behavior of identical parallel RC-IGBTs but with variations in circuit parameters such as circuit stray inductances. Finally, conclusions are given.

## II. The RC-IGBT Turn-on Transient

### A. Circuit and device model

The focus of this investigation is on the primary snap-back under dynamic conditions. To explore the phenomenon and its impact in real applications, TCAD device/circuit simulations were carried out for a 1,200V enhanced-planar RC-IGBT with a field-stop type buffer having a total thickness of 135 $\mu$m and a cell pitch of 18 $\mu$m. The simulations were carried out on a half-cell RC-IGBT model scaled to 1 cm$^2$ with a small n+ short region of 1 $\mu$m adjacent to the P collector. For a half-cell model, 25°C IV simulations will typically result in high snap-back voltages $V_{SB}$. Therefore, all simulations were carried out at 125°C to produce reasonable snap-back voltages for the purpose of this work. A mixed mode circuit model, as shown in Fig. 2, is used to evaluate the switching commutations of parallel RC-IGBTs. Two identical RC-IGBTs with slight variations in $V_{SB}$ levels can lead to full current missharing, which is only observed during the first turn-on pulse of a double pulse test, as it is shown in Fig. 3 [9]. One device takes all of the current ($I_{C1}$) and the second device fails to turn-on ($I_{C2}$ = 0 A), however for the second turn-on pulse both conduct current. In the next section we will therefore focus on the first turn-on phase. It is worth to mention that the second turn-on event does not show full current miss-sharing, demonstrating that the snap-back phenomenon has a negligible impact when the device turns on under high current.

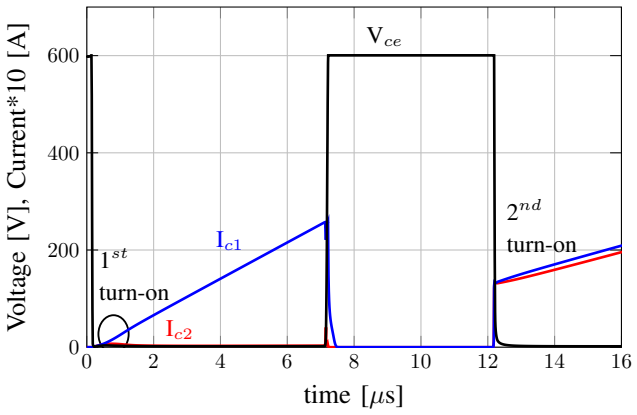


Fig. 3. Switching behavior of parallel RC-IGBTs with full current mis-sharing during first turn on.

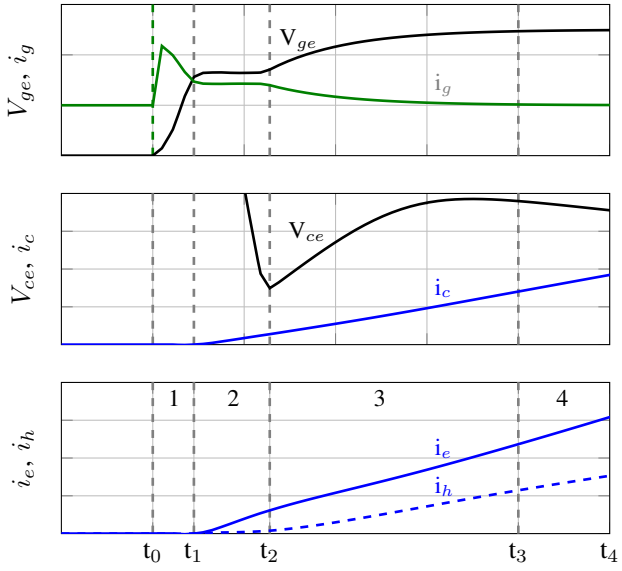


Fig. 4. First turn-on event of a Double Pulse Test for the RC-IGBT at 125°C and nominal voltage $V_{CE}$ = 600 V.

### B. First turn-on analysis

Fig. 4 shows the voltage and current waveforms associated with the first turn-on transient of a RC-IGBT. The first turn-on period of the classic double pulse test is analysed since the snap-back voltage phenomenon can only be observed when the RC-IGBT turn-on under low currents. The turn-on period can be divided into four phases depending on the RC-IGBT modes of operation and the initial snap-back voltage.

- Delay phase (1): initially the RC-IGBT is operating in the blocking or cut-off region and supports the full supply voltage, while the load current is zero. At $t_0$ the voltage $V_{gg}$ is applied to the gate-emitter terminals of the RC-IGBT. By injecting a constant current $i_g$ into the gate terminal, the input capacitance $C_{iss}$ begins to charge and $V_{ge}$ increases [16]. When $V_{ge} = V_{th}$, the collector current does not increase as the load current needs time to build up through the circuit inductance. Therefore, even though the RC-IGBT is turned on, it does not yet conduct any

current. Therefore, there is no carrier injection in this phase.

- Unipolar phase (2): the load current across the circuit builds up and the RC-IGBT, which is operating in the active region, begins to conduct electron current and the $V_{ce}$ falls more rapidly. The typical Miller effect comes into account due to a lower collector voltage across $C_{gc}$. During this phase, the RC-IGBT is conducting in unipolar mode, since the collector voltage has not dropped sufficiently for the bipolar action to take place.
- Quasi-bipolar phase (3): during this phase, the collector-emitter voltage rises up to the peak snap-back voltage of the RC-IGBT, whereas $V_{ge}$ continues to increase above the Miller plateau level. The RC-IGBT starts to inject holes from $P^+$ collector regions, however due to the $n^+$ short regions at the collector side, the RC-IGBT does not directly conduct in bipolar mode. The RC-IGBT conducts in a quasi-bipolar mode, where the hole carrier concentration is sufficiently strong at the PiN region of the RC-IGBT, however the hole injection is weak in the PNN region. The resulting hole carrier injection RC-IGBT is therefore below the background doping but above the intrinsic doping concentration. Hence, this mode is named as quasi-bipolar.
- Bipolar phase (4): after the voltage reaches the snap-back peak value, the RC-IGBT enters the voltage fall transient characterized with a negative dv/dt. The RC-IGBT is operated in bipolar mode as the collector voltage falls and enough hole injection is provided by the $P^+$ collector.

## III. Parallel RC-IGBT with variations in $V_{SB}$ levels

### A. Switching Analysis of RC-IGBTs with Low $V_{SB}$

The snap-back behavior of reverse conducting IGBTs is studied through TCAD simulations of 1200 V RC-IGBTs with the double pulse circuit presented in Fig. 2, where two RC-IGBTs have been simulated in parallel at a DC link voltage of 600V at 125°$C$. The investigation of this effect under switching conditions is relevant for real life applications since the device has to operate reliably under normal conditions. For the main circuit parameters; $L_{stray}$=100 nH, $L_{load}$ =50 $\mu$H, $R_{load}$ =0.1 ohm and $L_1$ = $L_2$ = 0 nH unless specified. For the gate circuit, the gate control voltage was switched between $V_{ge}$ = 15 V (on-state) and $V_{ge}$ = -15V (off-state). To instigate the current mis-sharing between parallel RC-IGBTs, the two devices were simulated with small variations in $V_{SB}$ levels. Different $V_{SB}$ values between parallel RC-IGBTs can occur due to variations in the silicon resistivity, collector/short/buffer processing or operating temperatures. The snap-back voltage is in general very sensitive to all above parameters and therefore a number of simulations were carried out to assess the impact of these mis-sharing instigating factors. In this study, the snap-back voltage level has been varied by adjusting the RC-IGBT buffer peak concentration. Fig. 6 shows the IV output characteristics for different RC-IGBT buffer peak concentrations compared to a standard IGBT.

Parallel RC-IGBTs with a small snap-back voltage $V_{SB}$, show some current mis-sharing as illustrated in Fig. 5.

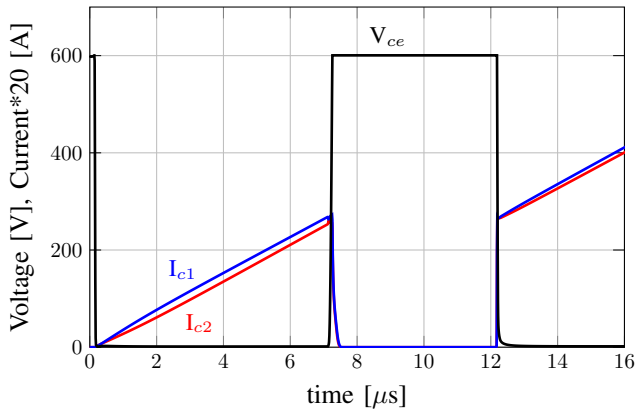


Fig. 5. Switching behaviour of parallel RC-IGBTs with low $V_{SB}$ levels ($Q_1$, $V_{SB1}$ = 1.2V and $Q_2$, $V_{SB2}$ = 1.65V) at 125°C.

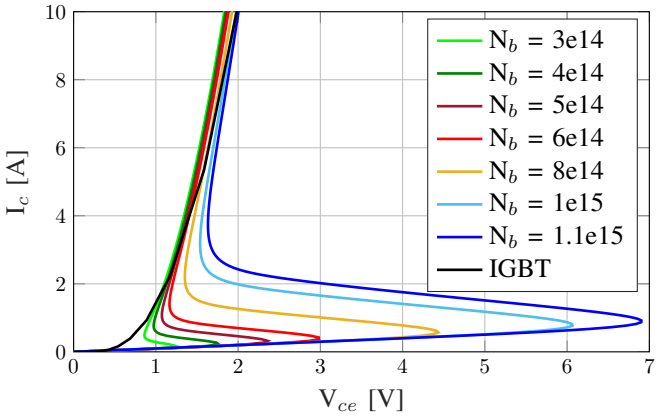


Fig. 6. Simulation IV output curves for 1.2kV RC-IGBTs with different peak buffer concentrations ($N_b$) at 125°C ($N_b$ in /cm$^3$).

The buffer concentrations are for $Q_1$ ($3{\cdot}10^{14}$/cm$^3$) and $Q_2$ ($4{\cdot}10^{14}$/cm$^3$) with snap-back voltage levels of 1.2V and 1.65V, respectively. The current mis-sharing can be observed for both turn-on events, under low and high load currents, however, it only becomes critical for the first turn-on event as presented in [9] with devices having a larger snap-back voltage. It is therefore important to conclude that the snap-back behavior has negligible impact on subsequent turn-on events if the conducting device during the ramp-up phase can survive the first turn-off transient.

### B. Instability of RC-IGBTs with large $V_{SB}$

While RC-IGBT with low snap-back voltage levels (i.e, below 3V) show mis-sharing current effects but both parallel devices are still able to conduct the load current, RC-IGBT having high snap-back voltage levels (i.e., 4V and above) result in one device carrying all of the load current and the second device failing to turn on.

Fig. 7 shows the current and voltage waveforms for two RC-IGBTs in parallel with buffer concentrations of ($Q_1$) $6{\cdot}10^{14}$/cm$^3$; $V_{SB1}$= 3V and ($Q_2$) 8x$10^{14}$/cm$^3$; $V_{SB2}$= 4.5V. Both devices turn-on following the phases explained in Section II (i.e., delay phase, commutation phase, unipolar phase...).

The difference comes into the bipolar phase, where the RC-IGBT will be operated in bipolar mode if the collector voltage falls bellow its snap-back voltage level and enough hole injection is supplied to the N-drift region. By looking at the hole current through each device in Fig. 7, $Q_1$ enters the bipolar phase when $V_{ce}$ reaches its snap-back voltage peak. On the other hand, the device $Q_2$ having a higher snap-back voltage level still operates in the quasi-bipolar mode, where not enough holes are supplied from the collector. Therefore, device $Q_2$ never enters the bipolar conduction mode. Fig. 8 shows the 2D hole current distribution of the two parallel RC-IGBTs with variations in $V_{SB}$ levels. The devices are plotted during the first turn-on event at the time instant t = 1 $\mu$s, where both devices are supposed to operate in bipolar mode.

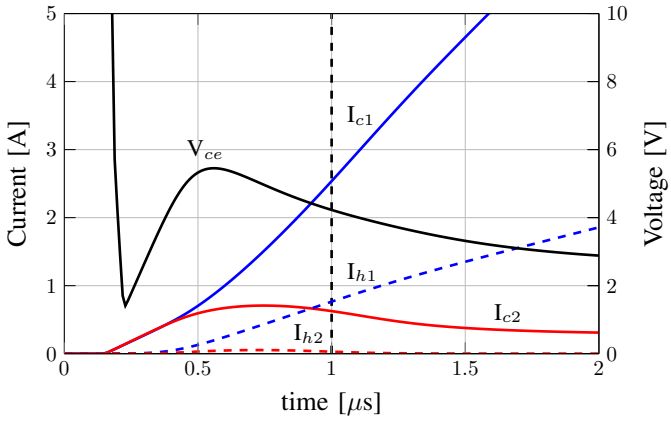


Fig. 7. First turn-on event for RC-IGBTs with high $V_{SB}$ levels (Q1 $N_b$=6·10$^{14}$/cm$^3$ and Q2 $N_b$=8·10$^{14}$/cm$^3$) at 125°C. The two RC-IGBTs are evaluated at t = 1 $\mu$s in Fig. 8.

Fig. 8 shows that the hole current density is above the background doping level (5·10$^{13}$/cm$^3$) for device Q1, which indicates that it is conducting in bipolar mode, but device Q2 is not flooded immediately and remains in the quasi-bipolar mode. A vertical cut along the PNN region (i.e., carrier accumulation between the cells) and PNP region (i.e., carrier drainage at the cells) of both devices is presented in Fig.9 (vertical cuts are highlighted in Fig. 8). It is clearly observed that for device $Q_1$, a large number of holes from the collector are injected into the N-drift region constituting a quasi-neutral plasma in the drift region as the collector current flows during conduction. On the other hand, device $Q_2$ shows a smaller hole injection, which is weakened in the PNP region due to the effect of the collector shorts. The device remains in a quasi-bipolar mode, eventually falling back into unipolar mode, and is subsequently turned off in practical terms. Thus, $Q_1$ will carry all the of the current.

The small difference in snap-back voltage levels appears to play a critical role when RC-IGBT devices are designed with a relatively high snap-back voltage. Results prove that for a given design and set of conditions, mis-sharing can be instigated with small modifications in device parameters and they appear to be critical when the RC-IGBT turns on under low loads.

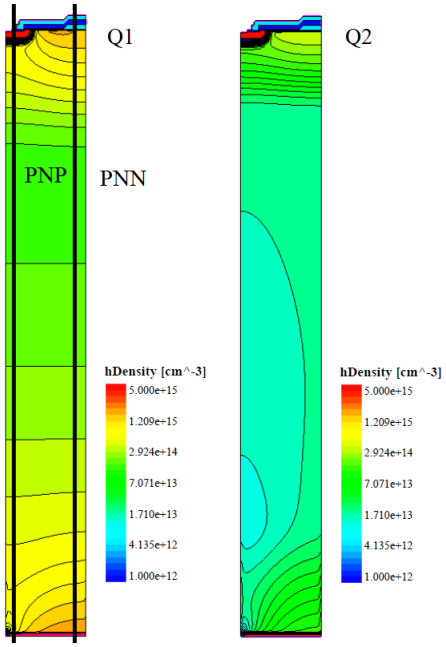


Fig. 8. Hole density during first turn-on event for the paralleled RC-IGBTs with $V_{SB}$ = 3V ($Q_1$) and $V_{SB}$ = 4.5V ($Q_2$) at 125°C. The 2D plots are shown at t = 1 $\mu$s in Fig. 7.

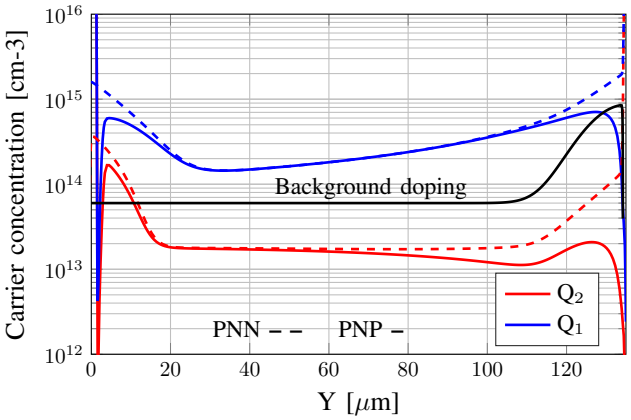


Fig. 9. The hole density of the paralleled RC-IGBTs with variations in $V_{SB}$ levels across the PNN (hole accumulation effect) and PNP (hole drainage effect) regions. Time instant is t = 1 $\mu$s in Fig.7.

## IV. Parallel RC-IGBT with Variations in Circuit Parameters

In High-Voltage RC-IGBT modules, chips are commonly arranged in parallel to increase the power capability. The stray inductances among parallel chips are therefore not the same for each parallel branch. The effect of the stray inductance on the snap-back phenomemon for parallel RC-IGBTs will be investigated in the following. Two stray inductances were inserted in each parallel RC-IGBT path having a small difference in value ($L_1$ = 9 nH and $L_2$ = 11 nH), as presented in Fig. 2. All the devices shown in Fig. 6 were evaluated with a double pulse simulation with identical structures for $Q_1$ and $Q_2$. RC-IGBTs with $N_b > 1.5\cdot10^{15}$/cm$^3$ resulted in $Q_2$ (with the higher $L_2$) eventually falling back to the unipolar mode and the device bipolar mode is turn off.

Fig.10 shows the simulated waveforms during the first turn-on event for $Q_1$ = $Q_2$, $N_b$ = $1.0{\cdot}10^{15}$/cm$^3$ and $V_{SB}$ = 5.5V. In this case, both $Q_1$ and $Q_2$ have the same snap-back voltage, so they enter into bipolar mode at the same IV point. This effect can be observed in Figs. 11 and 12 for devices $Q_1$ and $Q_2$, respectively. Subsequently, the current mis-sharing is initiated as the RC-IGBT enters the voltage fall phase characterized with a negative dv/dt. Despite $Q_2$ conducting for some time in bipolar mode, it eventually falls back into unipolar more as illustrated with the hole density time evolution shown in Fig. 12. The small difference in inductance appears to play a critical role to enable stable operation. Hence, results prove that for a given design and set of conditions, mis-sharing can be instigated with small modifications in the circuit parameters.

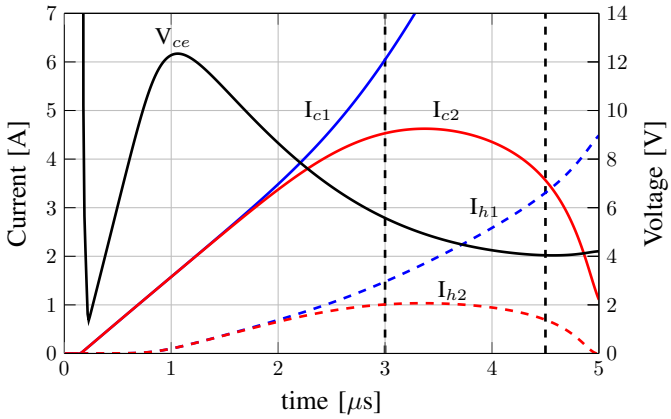


Fig. 10. First turn-on event for RC-IGBTs with $N_b$=$1.5{\cdot}10^{15}$/cm$^3$ ($Q_1$ with $L_1$ = 9nH and $Q_2$ with $L_2$ = 11nH) at 125°C.

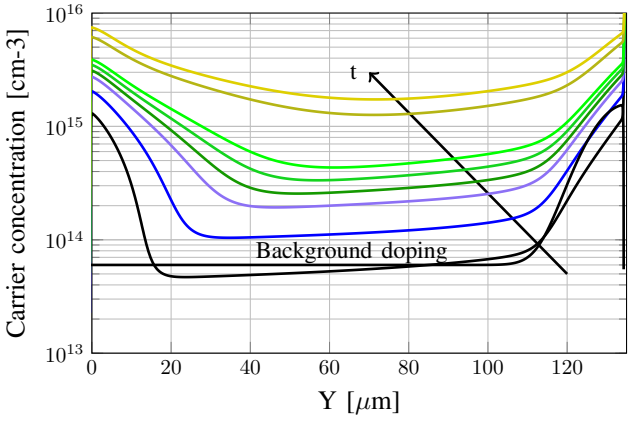


Fig. 11. Hole carrier density of device $Q_1$ ($L_1$ = 9 nH) during the first turn-on of paralleled RC-IGBTs with variations in $L_{stray}$. The cut along the vertical axis is done in the PNN region.

## V. Discussion

Based on the previous results, current mis-sharing due to snap-back behavior will lead into two operational modes (a) a stable mode where all parallel devices remain in bipolar mode with acceptable levels of current mis-sharing or (b) unstable mode where all devices will enter initially into a bipolar or quasi-bipolar mode but some would fall back into unipolar operation, which can lead to potential failures. Results have also shown that the above modes are determined after the voltage reaches the peak value when devices enter the voltage fall phase characterized with a negative dv/dt. Even if the devices are able to operate stable with some current mis-sharing, at the second pulse when the RC-IGBT turns on under the load current (i.e., several amps), the current mis-sharing does not take place.

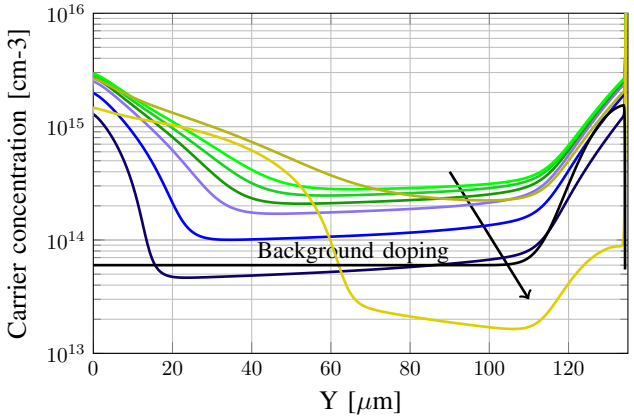


Fig. 12. Hole carrier density of device $Q_2$ ($L_2$ = 11 nH) during the first turn-on of paralleled RC-IGBTs with variations in $L_{stray}$. The cut along the vertical axis is done in the PNN region.

To instigate current mis-sharing in parallel RC-IGBTs, two parameter variations have been investigated (1) devices with variations in $V_{SB}$ levels and (2) devices with variations in circuit parameters. The results prove that for a given design and set of conditions, mis-sharing can be instigated, however, the small variations in the snap-back voltage level appear to show a different failure mechanism if compared to the small variations in circuit parameters.

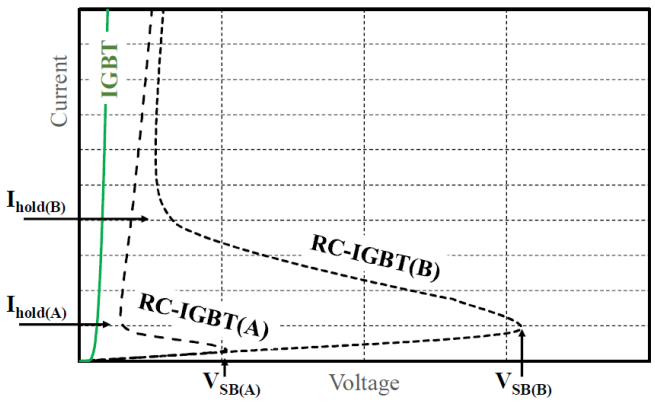


Fig. 13. Typical RC-IGBT output IV curves with variations in snap-back voltage levels $V_{SB}$ [9].

### A. Variations in $V_{SB}$ levels

The snap-back voltage level can be varied by adjusting the RC-IGBT buffer peak concentration as illustrated in Fig. 13

in the output IV curve of RC-IGBTs having different buffer designs. A similar effect can be obtained when devices operate under different temperatures since the snapback voltage level becomes more critical at low temperatures [9]. Also, the uneven internal current distribution will cause temperature distribution to become inhomogeneous, which may produce local overheating resulting in reliability problems. During the turn-on and after reaching the snap-back peak voltage, two operation modes are possible (a) a stable mode where both devices enter the bipolar mode showing some current mis-sharing or (b) unstable mode where one device reaches its $V_{SB(A)}$ (Fig. 13), whereas the second device does not reach its $V_{SB(B)}$. Subsequently, the second device having a higher $V_{SB}$ level remains in a quasi-bipolar mode and instead of conducting in bipolar mode, falls back to unipolar and turns off.

### *B. Variations in circuit parameters*

The variations in circuit parameters when paralleling identical RC-IGBTs can also lead to unstable mode, which is related to the snap-back voltage level and the holding current ($I_{hold}$, see Fig. 13). In this case, both devices enter the bipolar mode since they have the same snap-back voltage level. Due to the differences in stray circuit parameters, current mis-sharing is initiated and one device conducts more current which means that is more likely to reach the holding current earlier during the negative dv/dt zone. If the other devices is not able to reach that point within a very short time during the voltage fall phase, it will fall back into unipolar mode, as the simulations prove so.

## VI. Conclusions

The effects of the primary snap-back voltage in the parallel connection of high voltage RC-IGBTs are investigated to understand whether small snap-back could be problematic for the application. The snap-back phenomenon has been investigated by means of TCAD simulations of paralleled 1200V RC-IGBT structures with different snap-back voltage levels and variations in circuit parameters, showing that RC-IGBTs can tolerate small primary snap-back levels. Devices with large snap-back voltages at certain operating conditions could be problematic due to current mis-sharing between parallel RC-IGBTs, which is happening in the first current ramp-up turn-on period and not in the subsequent turn-on events. The physical phenomena behind the snap-back instability is not clear but becomes more critical as a high $V_{SB}$ level occurs at low temperatures. Additionally, the uneven internal current distribution may deserve further investigation, as it will cause inhomogeneous temperature distribution. So far, there is no published data of parallel high voltage RC-IGBTs failures which can be attributed to the primary or secondary snap-back voltages, therefore, as the next steps would be to seek a potential industrial partner to carry out the experimental work.

## References


[1] Takahashi, Yamamoto, Aono, and Minato, "1200V reverse conducting IGBT," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, 2004, pp. 133–136.

[2] H. Ruthing, F. Hille, F. . Niedernostheide, H. . Schulze, and B. Brunner, "600 V Reverse Conducting (RC-)IGBT for Drives Applications in Ultra-Thin Wafer Technology," in *Proceedings of the 19th International Symposium on Power Semiconductor Devices and IC's*, 2007, pp. 89–92.

[3] M. Rahimo, U. Schlapbach, A. Kopta, J. Vobecky, D. Schneider, and A. Baschnagel, "A high current 3300v module employing reverse conducting igbts setting a new benchmark in output power capability," in *2008 20th International Symposium on Power Semiconductor Devices and IC's*, 2008, pp. 68–71.

[4] K. Takahashi, S. Yoshida, S. Noguchi, H. Kuribayashi, N. Nashida, Y. Kobayashi, H. Kobayashi, K. Mochizuki, Y. Ikeda, and O. Ikawa, "New reverse-conducting IGBT (1200V) with revolutionary compact package," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 2569–2574.

[5] A. Kopta, M. Rahimo, C. Corvasce, M. Andenna, F. Dugal, F. Fischer, S. Hartmann, and A. Baschnagel, "Next Generation IGBT and Package Technologies for High Voltage Applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 753–759, 2017.

[6] E. M. Findlay and F. Udrea, "Reverse-Conducting Insulated Gate Bipolar Transistor: A Review of Current Technologies," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 219–231, 2019.

[7] M. T. Rahimo and N. Y. A. Shammas, "Freewheeling diode reverse-recovery failure modes in IGBT applications," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 661–670, 2001.

[8] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413–2426, 2015.

[9] M. Rahimo, P. D. Reigosa, N. Schulz, and F. Iannuzzo, "Analysis of the RC-IGBT snap-back phenomenon on the switching performance of parallel devices," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2020, pp. 482–485.

[10] H. Jiang, B. Zhang, W. Chen, Z. Li, C. Liu, Z. Rao, and B. Dong, "A Snapback Suppressed Reverse-Conducting IGBT With a Floating p-Region in Trench Collector," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 417–419, 2012.

[11] M. Antoniou, F. Udrea, F. Bauer, and I. Nistor, "A new way to alleviate the RC IGBT snapback phenomenon: The Super Junction solution," in *2010 22nd International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2010, pp. 153–156.

[12] X. Zhang, Y. Wang, X. Wu, M. Bao, C. Yu, and F. Cao, "An Improved Vce - Eoff Tradeoff and Snapback-Free RC-IGBT With P Pillars," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2859–2864, 2020.

[13] W. Chen, W. Wang, Y. Liu, and P. Liao, "Separated reverse-conducting insulated-gate bipolar transistor with snapback-free characteristics," *Micro and Nano Letters*, vol. 10, no. 7, pp. 330–333, 2015.

[14] M. Rahimo, A. Kopta, U. Schlapbach, J. Vobecky, R. Schnell, and S. Klaka, "The Bi-mode Insulated Gate Transistor (BIGT) a potential technology for higher power applications," in *2009 21st International Symposium on Power Semiconductor Devices IC's*, 2009, pp. 283–286.

[15] L. Storasta, M. Rahimo, M. Bellini, A. Kopta, U. R. Vemulapati, and N. Kaminski, "The radial layout design concept for the Bi-mode insulated gate transistor," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 56–59.

[16] F. Iannuzzo, *Modern Power Electronic Devices: Physics, applications, and reliability*, 2020, vol. ISBN-13: 978-1-78561-917-5.

[17] M. R. Simpson, "Analysis of negative differential resistance in the I-V characteristics of shorted-anode LIGBT's," *IEEE Transactions on Electron Devices*, vol. 38, no. 7, pp. 1633–1640, 1991.

[18] P. Spirito, G. Breglio, A. Irace, L. Maresca, E. Napoli, and M. Riccio, "Physics of the Negative Resistance in the Avalanche $I-V$ Curve of Field Stop IGBTs: Collector Design Rules for Improved Ruggedness," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1457–1463, 2014.

[19] H. Schulze, F. Niedernostheide, F. Pfirsch, and R. Baburske, "Limiting Factors of the Safe Operating Area for Power Devices," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 551–562, 2013.

[20] W. Chen, Z. Li, B. Zhang, M. Ren, Y. liu, and Z. Li, "A snapback suppressed reverse-conducting IGBT with soft reverse recovery characteristic," *Superlattices and Microstructures*, vol. 61, pp. 59 – 68, 2013.

[21] U. Vemulapati, N. Kaminski, D. Silber, L. Storasta, and M. Rahimo, "Reverse conductingIGBTs initial snapback phenomenon and its analytical modelling," *IET Circuits, Devices and Systems*, vol. 8, no. 3, pp. 168–175, 2014.

[22] L. Zhu and X. Chen, "An Investigation of a Novel Snapback-Free Reverse-Conducting IGBT and With Dual Gates," *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 3048–3053, 2012.