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Analysis of a New Soft-Switched Step-Up Trans-Inverse DC/DC Converter Based on Three-Winding Coupled-Inductor

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***Abstract*— This paper introduces a new non-isolated full soft-switching step-up DC/DC converter based on SEPIC structure. The proposed topology utilizes a Three-Winding Coupled-Inductor (TWCI) to increase the voltage gain, but unlike other coupled-inductor-based converters, its voltage gain is increased by reducing its magnetic turns ratio. Moreover, the secondary and tertiary turns ratios of the TWCI can be used as an additional design freedom to extend the voltage gain, which indicates more converter flexibility. Due to the continuous input current, the proposed converter can be used for many types of renewable energy sources. Also, the leakage energy from the TWCI has further been recycled and transferred to the output with the help of a regenerative passive clamp circuit. Due to the soft-switching performance, the proposed converter has no switching losses at the turn-on instant for the power switch and reverse recycling losses of the diodes. Furthermore, the use of a small number of components along with the soft-switching performance offer high efficiency. Steady-state analysis and design considerations are discussed thoroughly. Finally, a 200 W prototype with 200 V output voltage is provided to verify the theoretical analysis.**

I. INTRODUCTION

For Renewable Energy Sources (RES) applications, there has been a continuous push for higher efficiency and higher power density step-up gain DC-DC converters. For this purpose, step-up DC-DC converters as an interfacing circuit convert the input DC voltage (typically <50 V) to the demanded regulated high output voltage. Moreover, high voltage gain, low voltage stress, and continuous input current are other critical requirements for RES applications [1-2]. The non-isolated structures of such converters with small volume and low cost are more desirable for low power applications [1]. In addition, Some other applications of high voltage gain converters include energy harvesting, implantable medical devices, portable devices, gadgets, and appliances, lighting technology.

Due to the low voltage gain ratio, high voltage stress, and considerable diode reverse recovery losses of the conventional step-up converters, such as boost and SEPIC, improving the performance key indicators of such converters is imperative. To achieve a higher voltage gain ratio, some voltage boosting techniques such as voltage lift, Voltage Multipliers (VMs), Switched Capacitors, Switched Inductors, and cascading connections are widely used in step-up converters [1-3]. However, the high voltage conversion ratio of these modified structures is often achieved under hard switching conditions and by using many components [4].

In recent years, to further improve the key indicators, the magnetic devices in the form of coupled-inductor (CI) along with other voltage boosting methods are broadly employed in different configurations of step-up topologies [5]. In these types of circuits, the turns ratio of the CI, as an additional degree of freedom, further increases the voltage gain of the circuit with lesser components. However, creating a voltage spike across the switching devices in high turns ratio is a problem with the use of CIs, which can be solved using clamp techniques (active or passive) [6, 7]. It is noteworthy that in high step-up converters, often hard-switching performance and diode reverse recovery problems compromise the conversion efficiency. In such situation, a soft-switch design is highly recommended to improve both power efficiency and density.

In recent years, some non-isolated CI-based step-up DC-DC structures with proper performance have been presented. In the step-up converters in [8-10], two-winding CI along with VMs are used to increase the voltage gain. Despite an ultra-high voltage conversion ratio under soft-switching performance, these circuits suffer from a high input current ripple, which limits their applications for RESs. Moreover, new types of step-up converters with regenerative clamp techniques have been introduced in [11-15]. In these converters, the power switch is driven at soft-switching conditions (ZCS) with low voltage stress. Besides, the leakage inductor of the CI alleviates the reverse recovery issue of the diodes. However, these converters cannot provide a wide range of voltage conversion ratios. Furthermore, several SEPIC-based converters with low input current and high efficiency are suggested in [16-18]. In these converters, to further reduce the switching power loss, a resonant tank is designed without any additional auxiliary components. However, the problem with these converters is the limitation of the voltage gain ratio. Also, two types of ultra high-gain DC-DC converters using two-winding CI are presented in [5, 19]. Using two active switches without soft-switching performance are the main disadvantages of these converters. Two types of trans-inverse step-up converter using two-winding CI are suggested in [20-23]. In these converters, a higher voltage gain is obtained by reducing the turns ratio of the CI under low number of components and soft-switching performance.

Employing Three-Winding CI (TWCI) in step-up converters increases the degrees of freedom to obtain the voltage gain in a wider range [24-26]. In these circuits, the

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voltage gain ratio is a function of three parameters, including duty cycle, secondary and tertiary windings turns ratio. Nevertheless, the series connection of TWCI with the input DC voltage source leads to create a high input current ripple. For this purpose, in [27-29], TWCI-based converters with high voltage gain and continuous input current are presented. In these single switch topologies, using a regenerative passive clamp circuit, the leakage inductor energy is recycled. Moreover, the leakage inductor helps to eliminate the diodes reverse recovery issue of the converters.

Based on the above discussions, a new single switch trans-inverse high gain DC/DC Converter using a Three-Winding Coupled-Inductor is proposed. A unique feature of the proposed topology is its inverse relationship between the voltage gain ratio and turns ratio of the TWCI (Trans-Inverse). Thus, the converter voltage gain can raise the voltage gain by reducing its turns ratio. The main benefits of this structure are categorized as follows:

1- Capability to provide an ultra High voltage gain under lower a number of turns ratio (Transe –Inverse);
2- High voltage gain ratio per number of components;
3- Low input current ripple;
4- Low voltage stress;
5- Low Reverse Recovery (LRR) problem;
6- Soft-switching performance for all switching components;
7- Low number of components (10 components);

This paper is organized as follows. The topology description, steady-state analysis and mathematical derivation of the introduced topology are discussed in sections II and III. In section IV, the proposed converter is compared with its counterparts. The small-signal modelling of the proposed circuit is given in section V. Section VI then describes experimental results from laboratory prototype. Eventually, a brief conclusion are presented in Section VII.

II. THE PROPOSED CONVERTER STRUCTURE AND PERIODIC STEADY-STATE OPERATION

The structure of the proposed topology is shown in Fig. 1. This converter is formed by a TWCI, an input inductor (L_{in}), a single power switch (S), three diodes (D_c, D_1, and D_o), and four capacitors (C_c, C_1, C_2, and C_o). The turns of the primary, secondary, and tertiary windings of CI are N_1, N_2, and N_3, respectively. Moreover, L_k is the merged leakage inductance of the TWCI reflected on the primary side. Combining the secondary and tertiary sides of the TWCI along with C_2 and D_1 in the form of a VM increases the voltage gain by setting the turns ratios. The proposed converter is driven by a single switch with a low on-resistance $R_{DS\text{-}on}$ at the low-voltage side with a simple gating circuit. Also, the maximum voltage across the single power switch is limited by a regenerative passive clamp circuit, consisting of C_c and D_c. In this converter, because of applying a Quasi Reronant (QR) operation among L_k, C_1, and C_c during operating mode *II*, the current shape of the switch, TWCI, and the output diode D_o change in a sinusoidal function, which reduces the switch turn-off power loss and also eliminates the output diode reverse recovery issue. To simplify the circuit steady-state analysis, the following assumptions are made during one switching period:

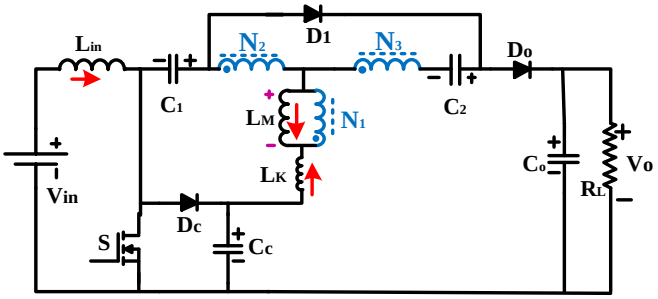


Fig. 1. Equivalent circuit of the proposed SEPIC-based high-gain DC/DC converter.

1) switches and diodes are regarded as ideal.
2) All capacitors are large enough so that their voltages are considered to be constant without any ripple.
3) The TWCI is modeled as an ideal transformer with a magnetizing inductor (L_M) and a leakage inductor (L_k).

Fig. 2 shows the theoretical waveforms of the presented converter for a switching period in Continous Conduction Mode (CCM) condition. These key waveforms are divided into five-time intervals. The current flow paths of operating modes are depicted in Fig. 3.

Mode 1 [t_0 - t_1]: At the beginning of the first time interval, the switch starts to conduct under ZCS condition. The leakage inductance of the TWCI (L_k) alleviates the rate of *di/dt* in the switch at the turn-on instant. As it is shown in Fig. 3-(a), D_1 is conducting, while D_o is reverse-biased in this time duration. In this mode, the input inductor (L_{in}) receives energy from the input voltage V_{in}. The capacitor C_2 receives energy from the secondary and tertiary sides of the TWCI. Also, in this mode, due to the negative value of i_{Lk1}, the capacitor C_1 is discharging its energy. During this short time transition, the currents of L_K and L_M decrease linearly. The leakage inductor

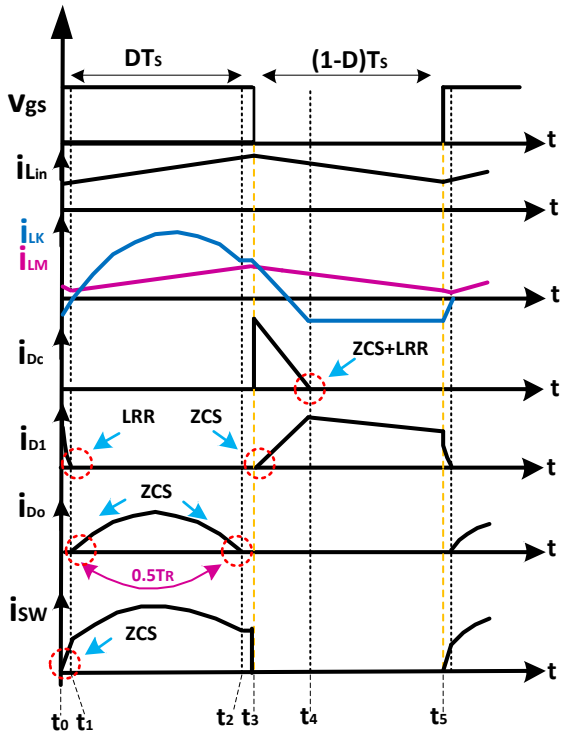


Fig. 2. Typical waveforms in the CCM operation of the converter.

of the TWCI leads to the current of the diode D_1 reaches zero at Low Reverse Recovery (LRR) condition with a minimum reverse recovery problem at the end of this mode ($t = t_1$).

Mode 2 [t_1 - t_2]: In the second time interval, the single power switch S is still on, and diode D_o starts to turn-on at ZCS condition. The input inductor is also magnetized by the input DC power supply; thus its current increase linearly. Due to the positive voltage applied across the magnetic inductor of the TWCI, its current starts to increase at a positive slope.

Also, the output capacitor C_o receives energy from the capacitors C_c, C_1, and TWCI. During this time interval, a resonant tank consisting of a leakage inductance of the TWCI and the capacitors C_c and C_1 is created in the form of QR. Due to QR performance, the current shapes of the power switch and the output diodes D_o are into a quasi sinusoidal current. As shown in Fig. 3 (b), the current value of the power switch at the end of this mode is decreased, which reduces its turn-off power dissipation. The ZCS operation of the power switch at turning on time is shown in Fig. 2. Furthermore, the QR operation leads to the current of D_o reaches zero naturally under the ZCS and LRR condition at $t=t_2$. Therefore, it can be expected that the voltage spikes of the DC output voltage at the switching instants will be significantly reduced. The resonant frequency (f_R) is obtained by applying Kirchhoff's Voltage Law on the circuit as follows:

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_{k1}[C_1 \| C_c]}} \quad (1)$$

To ensure the best performance in the presented topology, the resonant frequency (f_R) should be higher than the switching frequency. The resonant operation can create in two states, including below resonance (*BR*) area ($0.5T_R < DT_S$) and above resonance (*AR*) ($T_R/2 > DT_S$) area. However, the best state of QR operation to maintain the maximum duty cycle (D), reducing the switching and diode reverse recovery losses along with at least current stress on them is the critical mode ($0.5T_R \approx DT_S$). In this mode, the following equations can be given:

$$K = \frac{L_M}{L_M + L_K} \quad (2)$$

$$v_{Lin} = V_{in} \quad (3)$$

$$v_{LM} = K\frac{v_{C1} - v_{Cc}}{n_{21} - 1} \quad (4)$$

$$v_o = v_{Cc} + v_{C2} - (1 + n_{31})v_{LM} \quad (5)$$

Here, K is the coupling coefficient of the TWCL, $n_{21}=N_2/N_1$ and $n_{31}=N_3/N_1$. In addition, the current passed through the switch, and the secondary current side of the TWCI (i_{N2}) are given as:

$$i_{sw} = i_{in} - i_{N2} \quad (6)$$

$$i_{N2} = \frac{i_{Do}(1 + n_{31}) + i_{LM}}{n_{21} - 1} \quad (7)$$

This mode ends, when D_o turns off at the ZCS condition.

Mode 3 [t_2 - t_3]: This transient mode starts when the QR operation that happens on operating Mode 2 is finished at $t=t_2$; thus, the current of D_o reaches zero naturally under a slow slope with the LRR problem, as it is shown in Fig. 3 (c). In this mode, the current value of the leakage inductance and the secondary sides of the TWCI are identical. The capacitor C_1 is charged by the secondary side current of the coupled inductor.

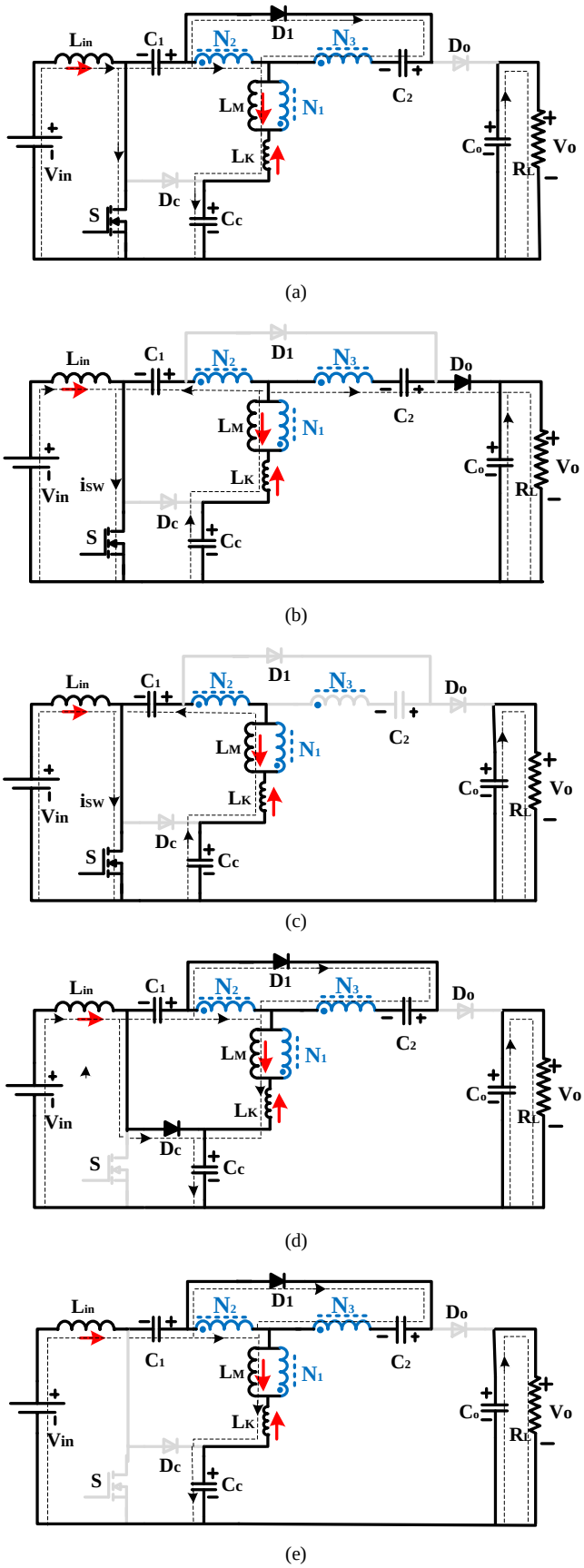


Fig. 3. Operation modes of the proposed converter, *(a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, and (e) Mode 5.*

Moreover, the same as the previous mode, the current passed through the input L_{in} and the magnetizing inductors are increased linearly. In this time interval, the current of the switch is given as:

$$i_{SW} = i_{in} + i_{LK} \quad (8)$$

Mode 4 [t_3 - t_4]: At $t = t_3$, the power switch S is turned off. Thus, the currents of the input and leakage inductors flows through the clamp diode D_c and turns it on. Thus, the maximum voltage stress across the power switch is restricted by the clamp circuit (D_c and C_c). Furthermore, the leakage inductance of the TWCI leads to the diode D_1 starts to conduct under ZCS condition as shown in Fig. 3(d). Moreover, the clamp capacitor C_c begins to charge from the input inductor current. In this mode, the capacitor C_2 received energy from the TWCI. Consequently, the current of the input and magnetizing inductors i_{Lin} and i_{LM} decrease linearly. This mode ends when the current of the diode D_c reaches zero at the ZCS condition with a LRR problem. The following equations for the voltage can be expressed in this mode:

$$v_{Lin} = V_{in} - v_{Cc} \quad (9)$$

$$v_{LM} = K\frac{v_{C1}}{n_{21}-1} = \frac{v_{C2}}{n_{31}+n_{21}} \quad (10)$$

$$v_{C2} = (n_{21} + n_{31}).v_{LM} \quad (11)$$

Mode 5 [t_4 - t_5]: In this time interval, diode D_1 is still on. The input inductor current charges the capacitor C_c. The capacitor C_2 received energy from the TWCI same as in the previous mode. Thus, the current of the input and magnetizing inductors decrease linearly. As shown in Fig. 3 (e), during this time, the current of the leakage inductance of the primary side on the TWCI and the input inductor are identical. The following equations can be obtained in this time duration:

$$v_{LM} = \frac{v_{C1}}{n_{21}-1} = \frac{v_{C2}}{n_{31}+n_{21}} \quad (12)$$

III. Steady-State Analysis of the Proposed Topology

A. Voltage Gain

The time durations of 1 and 3 are very short. Therefore, these intervals can be neglected in the steady-state analysis. The average value of the voltage on the capacitors C_c and C_1 can be derived by employing the voltage-second balance law on the input and magnetizing inductors during the switching period as follows:

$$V_{Cc} = \frac{V_{in}}{1-D} \quad (13)$$

$$V_{C1} = D.V_{Cc} = \frac{D.V_{in}}{1-D} \quad (14)$$

where D denotes the duty cycle of the switch S. Using (10), (11), and (12), the voltage of the capacitor C_2 is obtained as:

$$V_{C2} = \mathrm{K}\frac{(n_{21}+n_{31})}{n_{21}-1}.\frac{D.V_{in}}{1-D} \quad (15)$$

Finally, substituting (4), (15) into (5) and using (13) and (14), the overall voltage gain of the proposed converter in CCM is calculated as:

$$M = \frac{V_o}{V_{in}} = \frac{K(n_{31}+n_{21})+Dn_{21}-\mathrm{D}}{(n_{21}-1)(1-D)} \quad (16)$$

Because the coupling coefficient K of the TWCL has no significant effect on the conversion ratio, so it can be neglected. Consequently, the ideal voltage gain of the proposed converter with $K = 1$ is obtained as:

$$M = \frac{V_o}{V_{in}} = \frac{n_{31}+n_{21}(1+D)-\mathrm{D}}{(n_{21}-1)(1-D)} \quad (17)$$

According to (17), the voltage gain can be regulated in a wide range by adjusting three parameters consisting of duty cycle along with the turns ratios of the TWCI (n_{21} and n_{31}). Fig. 4 depicts the voltage gain ratio of the proposed converter as a function of the duty cycle and different values of n_{31} and n_{21}. From this figure, the voltage gain can be enhanced by increasing D, n_{31}, and also decreasing n_{21}. In fact, increasing the voltage gain ratio is inversely related to the number of n_{21}. Therefore, the proposed converter can achieve higher voltage gain in a smaller number of the magnetic turns ratio.

Besides, the voltage gain ratio is more sensitive to the parameter n_{21} against n_{31}. Therefore, a higher voltage gain can be obtained by properly setting the TWCI at fewer turns ratios (n_{21}+n_{31}), which leads to reduced ohmic power losses. Also, Fig. 5 shows the theoretical voltage gain as a function of n_{21} for different values of n_{31} at a constant duty cycle D=0.55. It is clear that reducing n_{21} toward unity ($n_{21}\rightarrow 1$) leads to a significant increase in the voltage gain. In other words, the performance of this converter is different from many magnetically coupled converters, where the voltage gains often increase with their turns ratios. It is important to note that the selection of very small values of n_{21}, as shown in Fig. 5, leads to a sharp increase in the slope of voltage gain ratio changes. Increasing this slope will make it more difficult to control and adjust the output voltage gain by selecting the specified number of turns ratio. Thus, choosing very small values of n_{21} (very close to unity) is not recommended. However, in the following section, the effects of n_{21} and n_{31} on the voltage and current stresses of the converter components are analyzed. Moreover, Fig. 6 presents a 3D plot of the proposed converter voltage gain as a function of n_{31} and n_{21} for the different duty cycles *D=0.3*, *D=0.55*, and *D=0.75*.

B. Voltage and Current Stress on the Power Devices

As mentioned before, the single power switch is clamped by C_c, thus using (13), drain-source voltage stress (V_{DS}) on the single power switch can be obtained as follows:

$$V_{DS} = \frac{V_{in}}{1-D} = \frac{(n_{21}-1)}{K(n_{31}+n_{21})+Dn_{21}-\mathrm{D}}V_o \quad (18)$$

Besides, the maximum repetitive peak reverse voltage across the diodes D_c, D_1, and D_o at their off-state can be expressesed as:

$$V_{Dc} = V_{DS} = \frac{(n_{21}-1)}{K(n_{31}+n_{21})+Dn_{21}-\mathrm{D}} \quad (19)$$

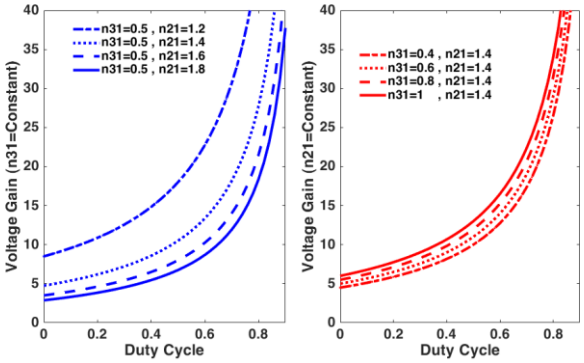


Fig. 4. The voltage gain of the proposed converter as a function of duty cycle for different values of n_{21} and n_{31} in CCM.

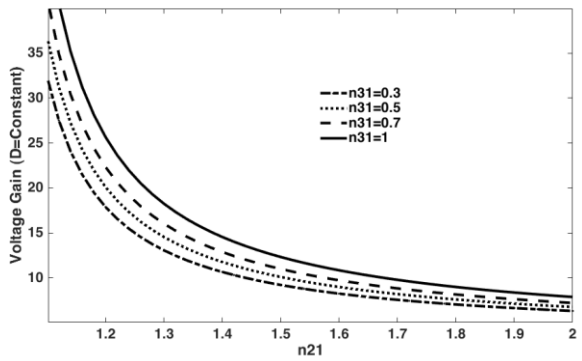


Fig. 5. The voltage gain of the proposed converter as a function of n_{21} for different values of n_{31} at a constant duty cycle (D=0.55).

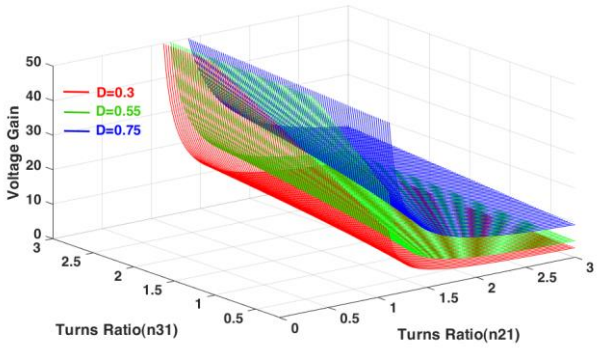


Fig. 6. 3D plot of the proposed converter voltage gain as a function of n_{31} and n_{21} for the different duty cycles D=0.3, D=0.55, and D=0.75.

$$V_{D1} = K\frac{n_{21}+n_{31}}{K(n_{31}+n_{21})+Dn_{21}-\mathrm{D}}V_o \quad (20)$$

$$V_{Do} = \frac{n_{21}(K-1)+Kn_{31}+1}{K(n_{31}+n_{21})+Dn_{21}-\mathrm{D}} \quad (21)$$

From (18) - (20), it can be seen that the maximum voltage stress of the output and clamp diodes is lower than the output voltage. Regarding (16), the average value of the input inductor current is given as:

$$< i_{in} >= MI_o \quad (22)$$

Here I_o is the output load current. Furthermore, using the ampere-second balance for the capacitors, the average current values of the converter components are calculated as:

$$< i_{Dc} >=< i_{D1} \geq =< i_{Do} >=< i_{LK1} >= I_o \quad (23)$$

$$< i_{LM} >= (n_{21}-1)I_o \quad (24)$$

Considering the critical mode operation in QR performance ($0.5T_R \approx DT_S$), and assuming a sinusoidal form of the current shape of the output diode D_o, the peak current of this diode can be estimated as follows:

$$i_{Do_{peak}} = \frac{\pi}{2D}I_o \quad (25)$$

Also, the peak current value passing through the diode D_2 is obtained as:

$$i_{D1\_peak} \approx \frac{I_o}{1-D} \quad (26)$$

Using (6), (7), (22), and (25), the peak and Root Mean Square (RMS) values of the switch current are calculated as follows:

$$i_{SW}(\mathrm{t}) \approx i_{in} + \frac{\frac{\pi}{2D}\sin(w_R t)(1+n_{31})+(n_{21}-1)}{n_{21}-1}I_o \quad (27)$$

$$i_{SW\_peak} = \left(M+1+\frac{\frac{\pi}{2D}(1+n_{31})}{n_{21}-1}\right)I_o \quad (28)$$

$$I_{SW(RMS)} = I_o\sqrt{D(M+1)^2+\frac{4D(M+1)Q}{\pi}+\frac{DQ^2}{2}} \quad (29)$$

where M is the voltage gain ratio of the proposed circuit, and Q is defined as:

$$Q = \frac{\pi}{2D}\left(\frac{1+n_{31}}{n_{21}-1}\right) \quad (30)$$

Using operating Mode 3, the switch current value in the turn-off instant is obtained as:

$$i_{SW}^{t=off} = i_{in} + \left(\frac{1}{n_{21}-1}\right)i_{LM} \quad (31)$$

Substituting (22) and (24) into (31):

$$i_{SW}^{t=off} = (M+1)I_o \quad (32)$$

Besides, the peak value of the current passing through the clamp diode D_c at the beginning of Mode 4 can be given using (31) as:

$$i_{Dc\_peak} = i_{SW}^{t=off} \quad (33)$$

Fig. 7 shows the maximum current value of the switching components as a function of the duty cycle under the turns ratios n_{21}=1.6 at n_{31}=0.35. Moreover, Fig. 8 depicts the peak and the RMS values of the switch current along with the voltage gain for different turns ratios n_{21} at n_{31}=0.4. From these figures, the minimum current stress has occurred at the duty cycle range 0.4<D<0.7.

C. Theoretical Power loss analysis

Theoretical power loss analysis of the presented circuit components is performed in this section.

Switch Loss: The switch power losses are divided into conduction and switching losses. Since the power switch is operated under ZCS condition, so the switching loss at the

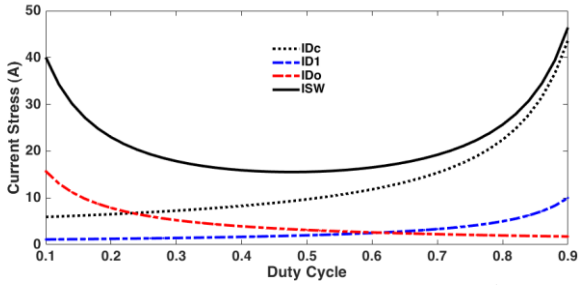


Fig. 7. Maximum current stress across the switch and diodes of the proposed converter at n_{21}=1.6 and n_{31}=0.4.

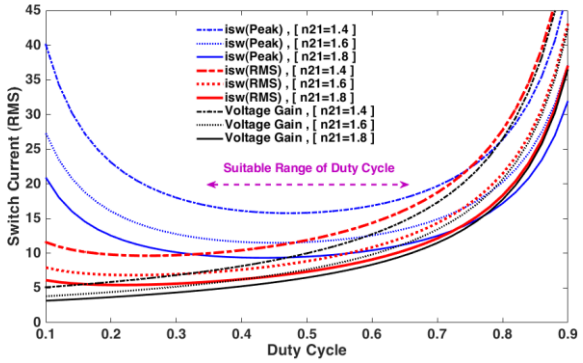


Fig. 8. Normalized current stress of the power switch as a function of the duty cycle at different turns ratio n_{21} under n_{31}=0.4.

turn-on instant is not considered in loss analysis. Therefore, the switch power loss in the proposed converter is given as:

$$P_{SW}^{loss} = \frac{1}{2T_s}.V_{DS}\left(i_{SW}^{t=off}.t_{off}\right) + \frac{1}{2T_s}(C_{oss}.V_{DS}^2) + R_{DS(on)}.I_{SW(RMS)}^2 \quad (34)$$

Here, t_{off} and C_{oss} are the switch turn-off time and the output capacitance of the MOSFET, respectivily.

Diode Losses: Diode power losses are including the forward voltage drop, conduction resistive dissipations, and reverse recovery losses. In the suggested topology, the ZCS performance for all diodes leads to eliminating the reverse recovery losses. Consequently, the diode power losses of the presented converter are calculated as:

$$P_{D_{1,2,c,o}}^{loss} = V_F.I_{D(AVG)} + r_D.I_{D(RMS)}^2 \quad (35)$$

Where V_F and r_D denote the forward voltage drop and the conduction resistance, respectively.

Capacitor Losses: Using the equivalent series resistance (r_{ESR}), the capacitor power losses can be calculated as:

$$P_{Cap.}^{loss} = r_{ESR}.I_{C(RMS)}^2 \quad (36)$$

Magnetic component Losses: The magnetic losses of the input inductor and TWCI can be expressed as:

$$P_{mag.}^{loss} = r_{L_{in}}.I_{L_{in}(RMS)}^2 + r_{eq1}.I_{lk1(RMS)}^2 + P_{Core(Lin,TWCI)} \quad (37)$$

Where r_{Lin} and r_{eq1} are the series resistances of the input inductor and TWCI, respectively.

The effect of turns ratio n_{21} of the TWCI on the theoretical efficiency is demonstrated in Fig. 9. The converter parameters are considered as: V_{in} = 25 *V*, R_L = 200 *Ω*, r_{Lin} = 65 *mΩ*, r_{LM} = 100 *mΩ*, n_{31}=*0.4*, f_s = 50 *kHz*, $t_{d(off)}$ = 50 *ns*, $t_{d(on)}$ = 26 *ns*, $R_{DS(ON)}$ = 5.6 *mΩ*, $r_{D1} = r_{D2} = r_{Dc} = r_{Do}$ = 7 *mΩ*, $r_{ESR(C1)} = r_{esrCc}$ = 25 *mΩ*, $r_{ESR(C2)}$ =50 *mΩ*, $r_{ESR(Co)}$ =100 *mΩ*, VF_{Dc} =0.45, $VF_{D1}=VF_{Do}$ =0.55. Regarding this figure, with increasing duty cycles or decreasing n_{21}, the converter efficiency is decreased. In fact, due to the high voltage and current levels at higher duty cycles, the maximum power-handling capability is limited, which also happens in other step-up topologies. However, converters such as the proposed converter, which have a high voltage gain, low number of components and soft switching function, can provide higher power-handling capacities.

IV. Performance Comparison

In order to show the merits of the proposed converter, an analytical comparison is performed in this section. Table *I* summarizes an analytical comparison of the proposed converter with its non-isolated counterparts.

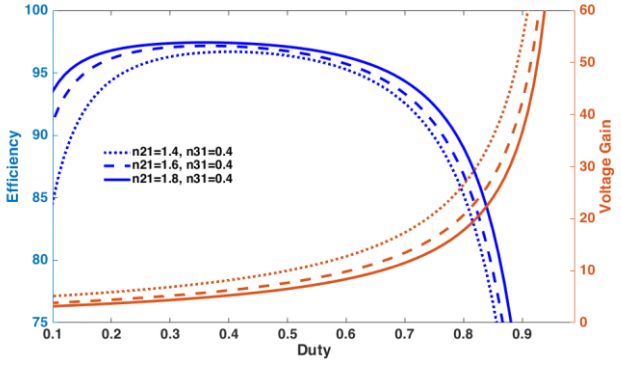


Fig. 9. Estimated efficiencies and voltage gains as a function of the duty cycle under different values of n_{21} at n_{31}.

Fig. 10 shows voltage gain comparison of the proposed converter and the converters mentioned in Table *I* versus duty cycle under the same conditions of turns ratios as n_{21} = 1.3, n_{31} = 0.35 (for converters with three-winding CI), n = n_{21}+n_{31}=1.65 (for converters with two-winding CI). One can see that only the proposed converter, along with the topology proposed in [29], can provide a higher voltage gain than the other converters. It is noteworthy that in the step-up topology in [29], the high voltage gain is obtained by using more components than the proposed converter. The ratio of the voltage gain to the whole number of components is a reasonable indicator to evaluate the power density of the converter. For this purpose, a comparison between the voltage gain ratio to the number of converter components (*M/N*) for converters referred to in Table *I* is demonstrated in Fig. 11. As it is shown, the presented circuit exhibits a higher value of *M/N* compared with the others in the total range of duty cycles, which indicates a higher power density.

Furthermore, the normalized maximum voltage across the main power switch of the converters in Table *I* is compared in Fig. 12. Similarly, Fig.13 depicts the normalized total voltage stress across the diodes of the converters in the comparison Table. It can be seen that the voltage stress of the switching components of the suggested topology is at the lowest level. The comparisons indicate that the proposed circuit possesses small semiconductor voltage stresses. Thus, MOSFET and diodes with lower-rated voltages can be selected, which leads to an efficiency improvement. Furthermore, the full soft-switching performance of the presented converter reduces the switching losses. For this purpose, the theoretical efficiency of the proposed topology compared to their conventional competitors under the same specific conditions (20 V/200 V, 200 W, 50 kHz, n_{21}=1.3, n_{31} =0.35, n=n_{21}+n_{31}=1.65) is carried out and presented in Table *I*. The parasitic resistors are selected based on related catalogs from aluminum electrolytic for capacitors (Vishay), Schottky barrier rectifier (SR series) for diodes, IRFP4310 (international IOR rectifier) for MOSFETs, and also EE Ferrite core, and iron powder toroidal core for CL and inductors, respectively. Also, the wire AWG24 specifications are used to obtain the Ohmic resistance of magnetic devices. Because of a full soft-switching

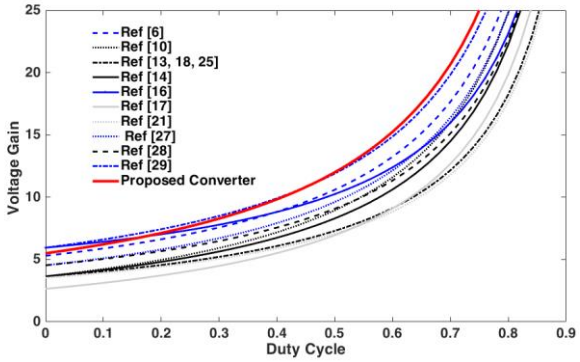


Fig. 10. The voltage gain comparison of converters given in Table *I*.

TABLE I. PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER RELATED CONVERTERS.

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	L.I.C.R	Voltage Stress on Main Switch	Voltage Stress on Diodes	Soft-Switching (Main Switch)	Reverse Recovery Loss	Eff. 200 W (50 kHz)
[6]	1/5/6/1^{2w} +1/14	$\frac{2(1+n)}{(1-D)}$	Yes	$\frac{V_o}{2(1+n)}$	$\frac{V_i}{1-D}, 4\times\frac{(1+n)V_i}{1-D}$	ZCS	Low	95.1%
[10]	1/4/4/1^{2w} +0/10	$\frac{2+n+nD}{(1-D)}$	No	$\frac{V_o}{2+n+nD}$	$\frac{V_i}{1-D}, 2\times\frac{(1+nD)V_i}{1-D}, \frac{nV_i}{1-D}$	ZCS	Low	96.8%
[13]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{V_i}{1-D}, 2\times\frac{(1+n)V_i}{1-D}$	ZCS	Medium	96.0%
[14]	1/4/5/1^{2w} +1/12	$\frac{2+n+D}{(1-D)}$	Yes	$\frac{V_o}{2+n+D}$	$2\times\frac{V_i}{1-D}, 2\times\frac{(1+n)V_i}{1-D}$	ZCS	Low	95.9%
[16]	1/4/5/1^{2w} +1/12	$\frac{1+(1+n)D}{(1-D)}+2n$	Yes	$\frac{V_o}{1+D+n(2-D)}$	$\frac{V_i}{1-D}, 2\times\frac{nV_i}{1-D}, \frac{(1+n)V_i}{1-D}$	ZCS+QR	Very Low	96.4%
[17]	1/4/5/1^{2w} +1/12	$\frac{1+n(1+D)}{(1-D)}$	Yes	$\frac{V_o}{1+n(1+D)}$	$\frac{V_i}{1-D}, 3\times\frac{nV_i}{1-D}$	ZCS+QR	Very Low	96.1%
[18]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{V_i}{1-D}, 2\times\frac{(1+n)V_i}{1-D}$	ZCS+QR	Very Low	96.5%
[21]	2/2/4/1^{3W} +1/10	$\frac{2n-1}{(n-1)(1-D)}$	Yes	$2\times\frac{(n-1)V_o}{2n-1}$	$2\times\frac{nV_i}{(n-1)(1-D)}$	ZVS	Very Low	96.6%
[25]	1/4/4/1^{3W}+0/10	$\frac{2+n_{21}+n_{31}}{(1-D)}$	No	$\frac{V_o}{2+n_{21}+n_{31}}$	$\frac{V_i}{1-D}, \frac{n_{31}V_i}{1-D}, \frac{(1+n_{21}+n_{31})V_i}{1-D}, \frac{(1+n_{21})V_i}{1-D}$	-	Low	95.8%
[27]	1/3/4/1^{3W} +1/10	$\frac{2+n_{21}-n_{31}(1-D)}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{2+n_{21}-n_{31}(1-D)}$	$\frac{V_i}{1-D}, \frac{(1+n_{21}+n_{31}(1-D))V_i}{(1-n_{31})(1-D)}, \frac{(1+n_{21}-2n_{31}D)V_i}{(1-n_{31})(1-D)}$	ZCS	Medium	96.2%
[28]	1/3/4/1^{3W} +1/10	$\frac{2+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+n_{31}-n_{21}}$	$\frac{V_i}{1-D}, 2\times\frac{(1+n_{31})V_i}{(1-n_{21})(1-D)}$	ZCS	Low	96.6%
[29]	1/5/6/1^{3W}+1/14	$\frac{3+2n_{21}+n_{31}}{(1-D)}$	Yes	$\frac{V_o}{3+2n_{21}+n_{31}}$	$\frac{V_i}{1-D}, 2\times\frac{(1+n_{21})V_i}{(1-D)}, 2\times\frac{(1+n_{21}+n_{31})V_i}{(1-D)}$	ZCS	Low	95.3%
Proposed Converter	1/3/4/1^{3W} +1/10	$\frac{n_{31}+n_{21}(1+D)-\mathrm{D}}{(n_{21}-1)(1-D)}$	Yes	$\frac{(n_{21}-1)V_o}{n_{31}+n_{21}(1+D)-\mathrm{D}}$	$\frac{V_i}{1-D}, \frac{(n_{31}+n_{21})V_i}{(n_{21}-1)(1-D)}, \frac{(1+n_{31})V_i}{(n_{21}-1)(1-D)}$	ZCS+QR	Very Low	96.7%

S=Switch, **D**=Diode, **C**=Capacitor, **CI** =Coupled-Inductor, **L**=inductor, **T**=Total Device Count, **L.I.C.R**= Low Input Current Ripple, **Eff**=Efficiency

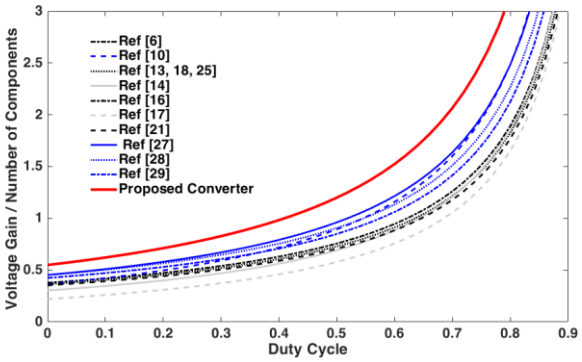


Fig. 11. The voltage gain per number of components comparison of converters given in Table *I*.

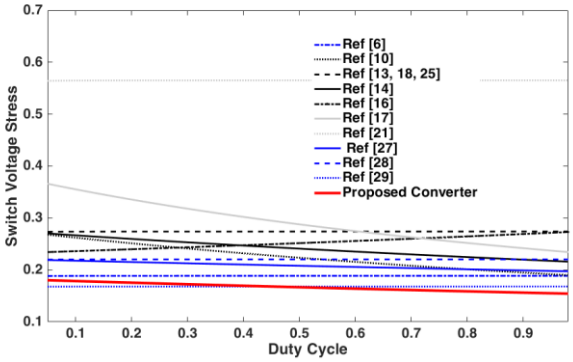


Fig. 12. Comparison of normalized voltage stress across the power switch of the converters given in Table *I* .

performance, along with the low number of components and low voltage stress, the proposed converter can provide high efficiency.

According to the above discussions, the suggested converter with a low number of components can offer relatively good performance for the RES cases.

V. DERIVATION OF THE SMALL-SIGNAL MODEL

In this section, an analysis of the low-frequency behavior of the proposed circuit is provided. The time durations 1 and 3 of the proposed converter are neglected because they are very

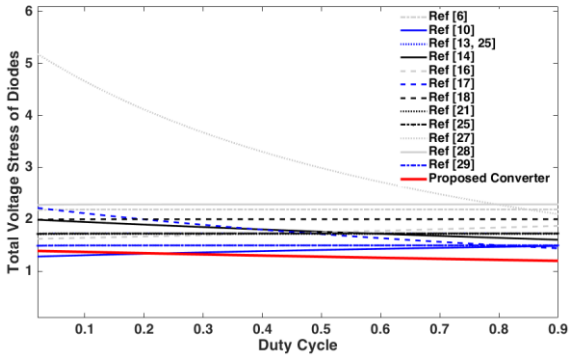


Fig. 13. Comparison of normalized total voltage stress of the diodes of the converters given in Table *I* .

short. To obtain the state equations, it is necessary to consider the parasitic resistances r_{c2} in series with the capacitor C_2. Also, for the non-conservative of the model, the parasitic resistance of the input inductor (r_{Lin}) is considered because of the high input current level in the input section of the converter. The state vector of the proposed converter is defined as:

$$x(t) = [i_{Lin}\ \ i_{LM}\ \ v_{Cc}\ \ v_{C1}\ \ v_{C2}\ \ v_{Co}\ ] \tag{38}$$

The state equations of Mode 2 are expressed as:

$$L\frac{di_{Lin}}{dt} = V_{in} - r_{Lin}i_{Lin} \tag{39}$$

$$L_M\frac{di_{LM}}{dt} = V_{c1} - V_{Cc} \tag{40}$$

$$C_2\frac{dV_{c2}}{dt} = \frac{1}{r_{c2}}[-W_1(V_{Cc} - V_{C1}) - V_{Cc} - V_{C2} + V_{Co}] \tag{41}$$

$$C_c\frac{dV_{cc}}{dt} = W_2 i_{LM} + (1 - W_1).C_2\frac{dV_{c2}}{dt} \tag{42}$$

$$C_1\frac{dV_{c1}}{dt} = -W_2 i_{LM} - W_1.C_2\frac{dV_{c2}}{dt} \tag{43}$$

$$C_o\frac{dV_{co}}{dt} = -C_2\frac{dV_{c2}}{dt} - \frac{V_{Co}}{R} \tag{44}$$

The state equations of Mode 4, are given as:

$$L_{in}\frac{di_{Lin}}{dt} = V_{in} - V_{Cc} - r_{Lin}i_{Lin} \tag{45}$$

$$L_M\frac{di_{LM}}{dt} = W_2.V_{c1} \tag{46}$$

$$C_2\frac{dV_{c2}}{dt} = \frac{1}{r_{c2}}(-V_{C2} - W_3V_{C1}) \tag{47}$$

$$C_c\frac{dV_{Cc}}{dt} = i_{Lin} \tag{48}$$

$$C_1\frac{dV_{c1}}{dt} = -W_2 i_{Lm} - (1 - W_1)C_2\frac{dV_{c2}}{dt} \tag{49}$$

$$C_o\frac{dV_{co}}{dt} = -\frac{V_{Co}}{R} \tag{50}$$

Where, W_1, W_2 and W_3 are defined as:

$$W_1 = \frac{n_{31}+1}{1-n_{21}}\ ,\quad W_2 = \frac{1}{1-n_{21}}\ ,\quad W_3 = \frac{n_{31}+n_{21}}{1-n_{21}} \tag{51}$$

Also, the state equations of Mode 5 are expressed as:

$$\frac{di_{Lin}}{dt} = V_{in} - i_{Lin}(-r_{Lin} - W_4) + W_5 i_{Lm} - V_{Cc} + V_{C1} + \frac{V_{C2}}{W_3} \tag{52}$$

$$C_2\frac{dV_{c2}}{dt} = \frac{-1}{W_3}i_{Lin} + \frac{1}{n_{31}+n_{21}}i_{Lm} \tag{53}$$

$$L_M\frac{di_{LM}}{dt} = -\frac{1}{n_{31}+n_{21}}(r_{c2}.C_2\frac{dV_{c2}}{dt} + V_{C2}) \tag{54}$$

$$C_c\frac{dV_{Cc}}{dt} = i_{Lin} \tag{55}$$

$$C_1\frac{dV_{c1}}{dt} = -i_{Lin} \tag{56}$$

$$C_o\frac{dV_{co}}{dt} = -\frac{V_{Co}}{R} \tag{57}$$

Where W_4, W_5 are defined as follows:

$$W_4 = \left(\frac{1}{n_{31}+n_{21}}\right)^2 r_{c2}(n_{21}-1)^2\ \ ,\quad W_5 = \frac{-r_{c2}}{W_3(n_{31}+n_{21})} \tag{58}$$

After applying the weighting factors on the state equations and then superimposing small ac perturbations same (as the procedure described in [30]), the transfer functions input-to-output voltages (v_o/v_{in}) and control-to-output voltage (v_o/d) are obtained. The bode plot diagrams of transfer functions v_o/v_{in} and v_o/d of the proposed converter along with conventional SEPIC are illustrated in Fig.14 and Fig.15. From these curves, the gain crossover frequency of the proposed converter is smaller than the SEPIC. Also, both converters are stable with a non-minimum phase behaviors. It should be noted that the non-minimum phase behavior is one of the most prominent features of the step-up converters, which is due to the presence of the right half-plane (RHP) zero of the control to the output transfer function. In fact, RHP zeros impose an extra phase shift to the loop gain of the transfer function and limited bandwidth.

VI. Converter Design Considerations

A. Input and Magnetizing Inductors Design

The input inductor L_{in} is designed to limit the input current ripple to be approximately 20% of the average input current (to prolong the usage life of the PV and FC), which is derived as:

$$L_{in} = \frac{V_{in}.D}{\Delta I_{in}.f_s} \tag{59}$$

where ΔI_{in} represents the permitted input current ripple. Also, the magnetizing inductor of the TWCI can be designed by:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM}.f_s} \tag{60}$$

where ΔI_{LM} is the current ripple. It is necessary to mention that choosing a very small ΔI_{LM} will increase the value of L_m, which increases the wire consumption and consequently increases the conduction loss significantly.

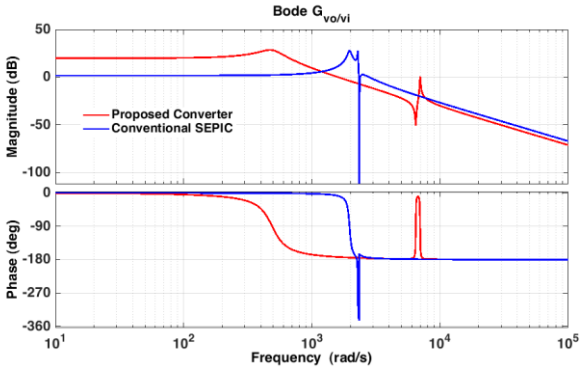


Fig. 14. Comparison of frequency response of the input-to-output transfer function between the proposed circuit and a conventional SEPIC.

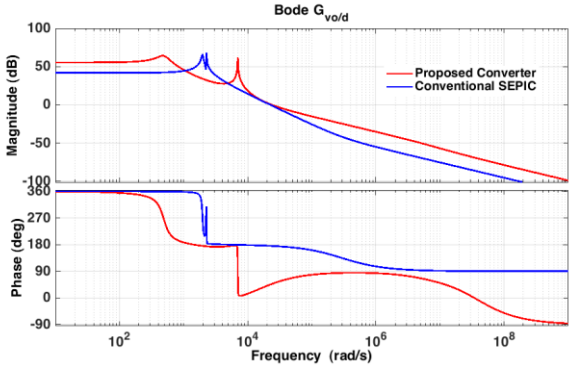


Fig. 15. Comparison of frequency response of the control-to-output transfer function between the proposed circuit and conventional SEPIC.

B. *Capacitors Design*

In order to suppress the voltage ripple across the output load, the output capacitor can be selected as:

$$C_o = \frac{DV_{out}}{R_L.\Delta V_{Co}.f_s} \quad (61)$$

Here ΔV_{Co} is the maximum tolerant voltage ripple, which usually is 1% of the output voltage. Furthermore, the suitable values of the other capacitors can be determined as follows:

$$C_c = \frac{i_{in}(1-D)}{\Delta V_{Cc}.f_s} > \frac{(1-D).M.V_{out}}{\Delta V_{Cc}.R_L.f_s} \quad (62)$$

$$C_1 = \frac{i_{in}(1-D)}{\Delta V_{C1}.f_s} > \frac{(1-D).M.V_{out}}{\Delta V_{C1}.R_L.f_s} \quad (63)$$

$$C_2 = \frac{i_{Do}.(1-D)}{\Delta V_{C2}.f_s} > \frac{\pi(1-D)V_{out}}{\Delta V_{C2}.2DR_L.f_s} \quad (64)$$

where ΔV_{Cc}, ΔV_{c1} and ΔV_{c2} denote the voltage ripple. Moreover, according to operation Mode *II*, the quasi-resonant duration is related to the capacitors C_c and C_1. Consequently, these capacitors are also designed as:

$$\pi\sqrt{L_{k1}[C_c \| C_1]} = DT_S \quad (65)$$

It is noteworthy that the middle capacitors of the proposed converter are not performing any filtering effect. Thus their design can be done at larger allowable voltage ripples, which leads to cost and volume saving. Also, selecting small values for these capacitors will not affect the output DC voltage quality. Therefore, the simplest way to adjust the resonant frequency is by properly choosing the capacitors C_c and C_1.

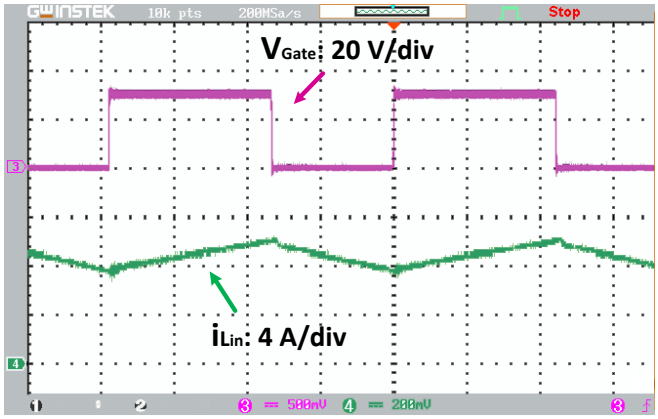
VII. EXPERIMENTAL RESULTS

To verify the theoretical analysis of the presented topology, a sample prototype is provided in the laboratory. The main components are listed summarized in Table *II*. Due to the low voltage stress across the power switch, a MOSFET with a very low $R_{DS(on)}$ is employed. The current and voltage waveforms of the converter components were measured by the help of a high-frequency current probe *PA-667 1 MHz* and a differential voltage probe *GDP-025*. Moreover, it is necessary to make three short-circuit tests to obtain the leakage inductance of the TWCI for the equivalent circuit of the proposed converter.

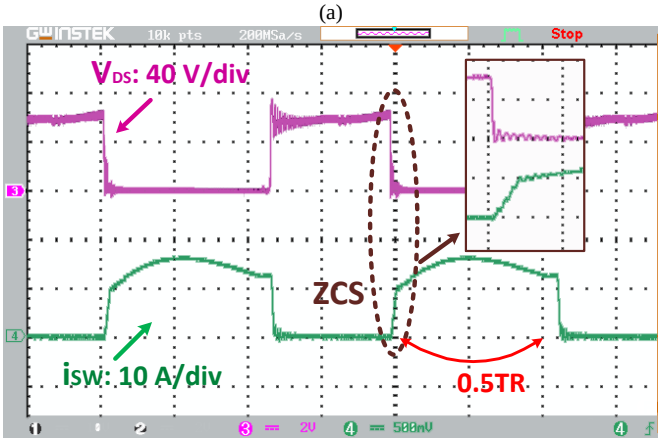
Fig. 16 (a) represents the input current waveforms of the proposed converter in steady-state, which is continuous with a low ripple. According to Fig. 16-(b), the power MOSFET turns-on under ZCS conditions with low voltage stress. Due to QR operation in Mode 2, the switch current value is reduced at the turn-off instant, which is decreasing switching power

Table *II*: PARAMETERS OF PROTOTYPE SETUP.

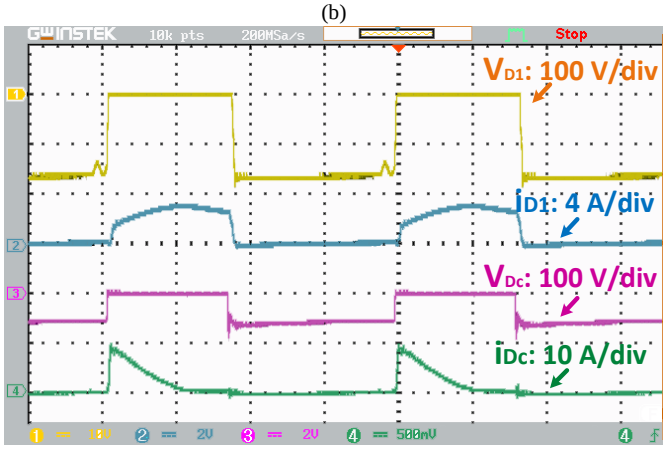
Parameter	Values
Output Power (P_{out})	200 W
Input Voltage (V_{in})	25 V
Output Voltage (V_{out})	200 V
Switching Frequency (f_s)	50 kHz
Capacitor C_1	4.7 µF / 250 V
Capacitor C_c	3.9 µF / 250 V
Capacitors C_2	47 µF / 250 V
Capacitor C_o	100 µF / 250 V
Power Switch	IRFB4310 / $R_{DS(on)}$=5.6 mΩ
Input Inductors L_{in}	170 µH / T184-52
Magnetizing Inductor of the CL (L_m)	160 µH
Turns Ratios of the TWCI *(N1:N2:N3)*	(18:29:7) / EE42/21/20
Leakage Inductances L_{K1}	3.6 µH
Diodes D_1 and D_2	MUR420 ($V_{F\,(Max)}$=0.88 V)
Diodes D_c	SR360 ($V_{F\,(Max)}$=0.7 V)



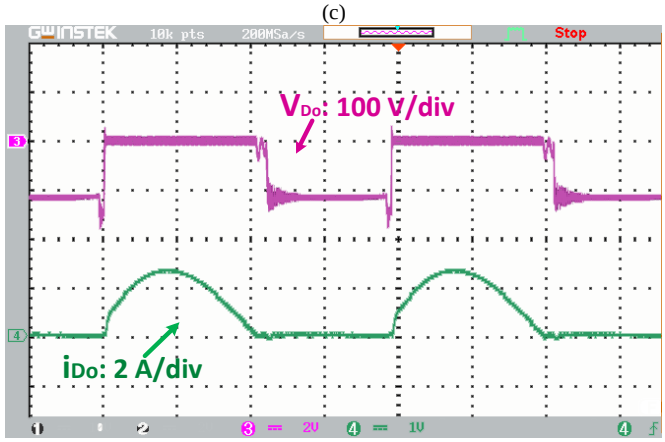
(a)



(b)



(c)



(d)

Fig. 16. Experimental results of the proposed topology at 200 W, *(a) Input inductor current, (b) MOSFET S, (c) Diodes D_c and D_1, and (d) Diode D_o.*

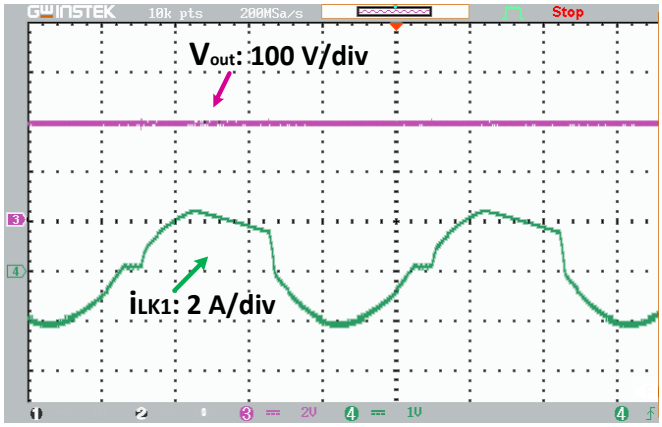


Fig. 17. Experimental results of the i_{LK} and V_{out} at 200 W.

loss. From Fig. 16 (c) and (d), the LRR condition at the turn-off instant can be realized in the current waveform of all converter diodes. Also, the voltage stress across the diodes D_1, D_c, and D_o are 170 V, 55 V, and 115 V, respectively, which are lower than the output DC voltage. Besides, the current of the leakage inductor from the primary side of the coupled inductor and the output DC voltage waveforms are depicted in Fig. 17. Due to the sinusoidal form of the output diode current (because of QR), the DC output voltage is constant with minimum voltage spike at the switching instants, which is the other merit of the presented circuit.

The measured efficiency curve of the proposed converter versus output power at V_o= 200 V is shown in Fig. 18. These diagrams for different input voltages V_{in}=20 V and V_{in}=25 V are measured under the same conditions of output voltage V_{out}=200 V, the number of turns ratios of the TWCI N1:N2:N3= 18:29:7, switching frequency f_s=50 kHz, and operating mode (BR mode near to critical mode). Due to increasing the voltage gain from *M=8* to *M=10* in equal power, the converter efficiency is decreased slightly. The overall efficiency of the presented topology at full load condition (25 V / 200 V , and 200 W) is 96.5%. Regarding Fig. 18, with increasing output power, the efficiency of the converter decreases with a light slope. Moreover, Fig. 19 illustrates by a pie graph the power loss breakdown at full load conditions. This curve is calculated based on the theoretical analysis of the proposed circuit provided in Section III by considering the real parasitic components. also, the power loss analysis is summarized in Table III. To calculate the efficiency, the parasitice resistances of the components are achieved from the prototype converter.Due to the low voltage stress and soft-switching performance (ZCS, LRR, and QR) provided for all switching components, the power loss

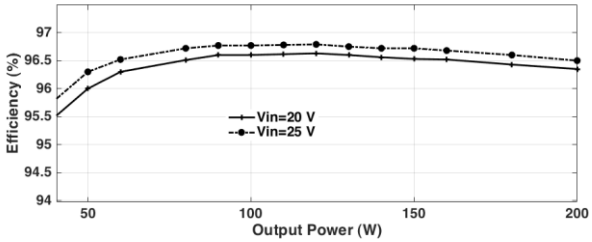


Fig. 18. Measured efficiency of the proposed converter versus output power.

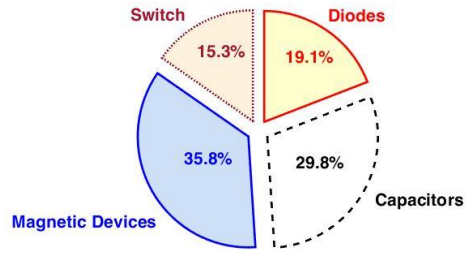


Fig. 19. Break-down of power dissipitions at full load condition (V_{in} = 25 V, V_o = 200 V, and P_{out} = 200 W).

Table *III*. THE LOSS DISTRIBUTIONS OF THE PROPOSED TOPOLOGY FOR THE NOMINAL POWER

Components	Power loss relations	Loss value (W)
Input inductor r_{lin}	$P_{ohmic}^{loss} + P_{core}^{loss}$	1.38
Coupled inductor loss		1.25
Turn-off loss (MOSFET)	$\frac{1}{2T_s}(I_{switch(\max)}.V_{DS}.t_{off})$	0.7
Conduction-loss (MOSFET)	$I_{S(RMS)}^2.R_{DS(on)}$	0.4
Capacitive turn-on loss (MOSFET)	$\frac{1}{2T_s}(C_{oss}.V_{DS}^2)$	0.03
D_1	$V_F.I_{D(AVG)}$	0.48
D_c		0.45
D_o		0.48
C_1	$I_{C(RMS)}^2.ESR$	0.8
C_2		0.38
C_c		0.91
C_o		0.11

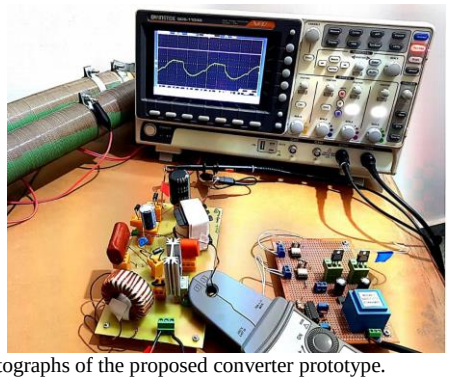


Fig. 20. Photographs of the proposed converter prototype.

share of the single power switch and diodes are lower than other losses. Photographs of the proposed converter prototype is shown in Fig. 20.

VIII. CONCLUSION

This paper has proposed a new non-isolated single-switch high voltage gain DC-DC converter for renewable energy sources applications like photovoltaic and fuel cells. Combining a three winding coupled-inductor with a multiplier circuit leads to an increase in the converter voltage gain ratio under a low number of components. A lossless regenerative clamp circuit is also employed to recycle the energy stored in the leakage inductor of the TWCI, which is restricted by the power switch voltage stress. To further decrease the switching power dissipations, a resonant tank is designed with the help of the parasitic component of the coupled-inductor and the

middle capacitors. High voltage conversion ratio, high efficiency, continuous input current with low ripple, low voltage stress on the power switch, and also the soft-switching performance for all switching components are the main merits of the suggested converter. The steady-state analysis, modeling, and design considerations have been presented. Finally, experimental results from a 25 V-200 V /200 W laboratory prototype have proved the feasibility of the proposed converter design. These results are promising for potential applications for small-scale renewable energy sources applications.

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