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Switched-Capacitor Multilevel Inverters: A Comprehensive Review

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***Abstract*—Multilevel inverters (MLIs) with switched-capacitor (SC) units have been a widely rehearsed research topic in power electronics since the last decade. Inductorless/transformerless operation with voltage-boosting feature and inherent capacitor self-voltage balancing performance with a reduced electromagnetic interference make the SC-MLI an attractive converter over the other available counterparts for various applications. There have been many developed SC-MLI structures recently put forward, where different basic switching techniques are used to generate multiple (discrete) output voltage levels. In general, the priority of the topological development is motivated by the number of output voltage levels, overall voltage gain, and full dc-link voltage utilization, while reducing the component counts and stress on devices for better efficiency and power density. To facilitate the direction of future research in SC-MLIs, this article presents a comprehensive review, critical analysis, and categorization of the existing topologies. Common fundamental units are generalized and summarized with their merits and demerits. Ultimately, major challenges and research directions are outlined leading to the future technology roadmap for more practical applications.**

***Index Terms*—Multilevel inverter (MLI), pulsewidth modulation (PWM), self-voltage balancing, step-up switched-mode dc–ac converters, switched capacitor (SC).**

I. Introduction

MULTILEVEL inverters (MLIs) have been a mature technology in power electronics owing to their many well-known benefits, such as high-quality output harmonic profiles, low-voltage stress across the switches, and low-electromagnetic interference (EMI) propagation issue [1]–[4]. Followed by the recent development in highly efficient semiconductor devices' packaging with the industrialized perspectives of MLIs, their performance has been continuously improved for different applications [4], [5].

Among many families of improved MLIs, the integration of switched-capacitor (SC)-based circuits has become one of the popular techniques [6]. Pure SC-based switching circuits contain several capacitors, power switches, and/or diodes that can convert the available fixed dc-link voltage to generate multilevel voltage using a series–parallel switching conversion technique. The integrated capacitors are charged directly through the parallel connection with another voltage source (input dc source or another charged capacitor). A discrete output voltage can be generated by discharging the capacitor(s) in series or parallel fashion with or without the input dc source. Such a single-stage inductorless/transfomerless switching operation creates a voltage step-up feature with a self-voltage balancing for the involved capacitors and makes SC-MLIs a valuable and interesting solution for many new applications [6]. Inclusion of SC-based switching circuit techniques into the dc–dc converters has already been widely studied in literature and commercialized in industry [7]–[9]; however, such integration for multilevel ac-voltage generation applications is emerging and worth investigating.

One of the initial attempts to generate a multilevel ac-voltage waveform through an SC network dates back to 1989 [10]. In that case, a series–parallel SC (SPSC) network was used to generate multiple dc-voltage levels across an unfolding classical full-bridge (FB) cell that generates ac voltage at the output. To implement this idea in practice, some old-fashion types of N-channel power MOSFETs driven by a CMOS logic control circuitry were used. The implementation of this innovative idea was hindered by the power semiconductor technology at the time. A decade later, such a concept was re-examined through the use of optocoupler and a suitable FET driver circuits. This has inspired the development of SC-MLIs with a low weight, small size, and acceptable overall efficiency [11]–[14]. Motivated by a high-voltage pulse generator in Marx converters, the concept of SC-MLIs was further developed in [15] and [16] for inductively coupled power transfer and high-voltage solid-state repetitive pulses within a wide range of output frequencies and loads. With the integration of a boost inductor placed at the front-end side of an SC network, other schemes of SC-MLIs emerged with a dynamic voltage-boosting operation [14], [17], [18].

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Since 2010, the development of SC-MLIs has been growing rapidly, in which various SC-based basic units came forward as the switched-capacitor converters (SCCs) with the capability of boosted ac-voltage level generation (discrete) have been introduced. Taking their inclusion in different circuit designs of MLIs into account, plenty of new SC-MLI topologies with diverse characteristics and performances for broad applications are explored so far. The main motivations and inclinations toward SC-MLIs can be enlisted as follows: 1) reduction in the number of required semiconductor devices with reasonable values of maximum voltage stress (MVS) across the switches, while producing the maximum number of output voltage levels; 2) enhancement in the overall output voltage gain using a single- or multiple-dc-source configurations; and 3) alleviating/controlling the current stress/loss profile of switches through soft charging or pulsewidth modulation (PWM)-based techniques. Ultimately, a topology with better power density and overall efficiency is of prime focus. Regarding these contributions, many new challenges, design considerations, and practical limitations have been reported. Accordingly, MLIs with the SC concept are developed through different circuit configurations, such as single [19]–[75] and multiple [5], [6], [73], [76]–[91] dc-source structures, mid-point-clamped techniques [92]–[120], and common-grounded (CG)-based topologies [121]–[145]. Their performance is much improved using a hybrid topological design, where other well-known integrated techniques, such as flying-capacitor (FC) [146]–[157] and switched-boost (SB) [158], [159] technologies, are merged with the SC concept.

Taking such recent trends and advancements into account, a clear overview of circuit derivations for different SC-MLIs is crucial as many of the derived topologies are complying with the same rule and concept with different performances. The aim of this review article is to investigate such recent trends/advances of the SC-MLIs and assimilate them to report a summary to future research.

The rest of this article is organized as follows. Section II introduces different SC-based basic units and their overview. The use of these basic concepts to design new SCCs is then discussed in Section III. Derivations of different SC-MLIs with single/multiple dc-source, mid-point-clamped, CG, and hybrid configurations followed by some comparative studies in various aspects and structural motivations behind each concept are explored in Section IV. Here, more than 65% of the discussed structures have been presented within 2020 and 2021. The major challenges associated with SC-MLIs and the related solutions/opportunities are discussed in Section V. A qualitative summary targeting the pros and cons of different SC-MLIs with some well-known reported applications and a future roadmap of the topic are discussed in Section VI. Finally, Section VII concludes this article.

II. Overview of Basic SC Units

A basic "SC unit" consists of a dc source and some diodes, capacitors, and switches. The existing basic SC units can be categorized into five different sub-groups such as SPSC units [19]–[24], [52], [160], [161], SC voltage doubler units [25]–[28], [70], SC half-mode units [29]–[34], SC voltage tripler units [35]–[43], [67], [71], [162], [163], and SC bipolar units [44]. A general overview of these basic SC units is shown in Fig. 1, and their details are discussed in the following subsections:

A. SPSC Units

SPSC units with two different configurations, as shown in Fig. 1, are the primary circuits that have been used in many SC-MLIs so far. As shown in Fig. 2, Type-I of this unit requires only two switches, one capacitor, and a single power diode [19], [20], [52], [160]. Considering $V_{\rm dc}$ as the value of the input dc source, two discrete positive-voltage levels, i.e., $V_{\rm dc}$ and $2V_{\rm dc}$, can be generated at the output. The same charging/discharging concept of capacitors is used in SPSC Unit-II, as depicted in Fig. 3, while an additional capacitor and a power switch instead of the diode and a four-quadrant switch, T, are used [21]–[24]. The difference between these two basic units is that SPSC Unit-I does not have bidirectional power flow capability. In addition, as opposed to SPSC Unit-I, both the discrete voltage levels in SPSC Unit-II are generated with the help of the charged capacitors voltages, which can prevent any dc offset during the output voltage level generation in SC-MLIs. Herein, depending on the configurations of some developed SC-MLIs, four-quadrant power switches with a back-to-back connection of two standard MOSFETs can also be used instead of each of paralleled normal power switches in SPSC Unit-II [23], [130]. The MVS value of all the semiconductor devices in both types of SPSC units is within the voltage of the input dc source.

B. SC Voltage Doubler Unit

An SC voltage doubler unit is a two-port converter with a single dc source, two capacitors, two complementary power switches, and two power diodes, as illustrated in Fig. 1 [25]–[28]. Similar to the basic SPSC units, both the capacitors are charged in parallel to the input dc source, as can be realized in Fig. 4. Hence, all the involved semiconductors have to tolerate the same MVS. As for each capacitor, a diode and a power switch are involved in the charging path of the capacitors. Since it is a two-port SC-based basic unit, five dc-link voltages, i.e., $0V_{\rm dc}$, $\pm V_{\rm dc}$, and $\pm 2V_{\rm dc}$, can be generated at the output. Although this basic SC unit offers a flexible operation, it lacks bidirectional power flow capability. To overcome this issue, a derived version of this SC voltage doubler unit with diodes replaced with the four-quadrant power switches has recently been proposed in [70] but at the cost of additional semiconductor devices.

C. SC Half-Mode Units

Charging the dc-link capacitors up to a fraction of the input dc-source voltage can be possible through SC half-mode units. There have been several types of SC half-mode units recently introduced, as shown in Fig. 1. Taking Fig. 5 into account, which

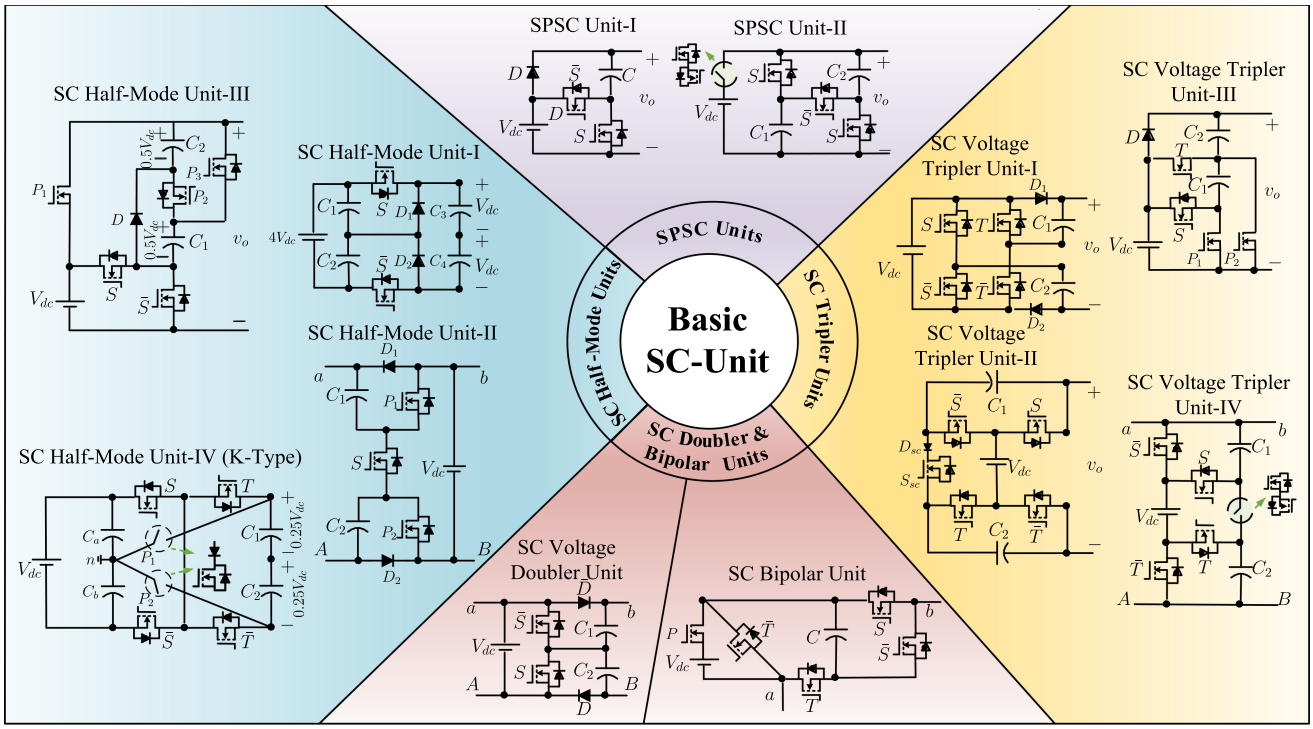

Fig. 1. Categorization of different SC-based basic units.

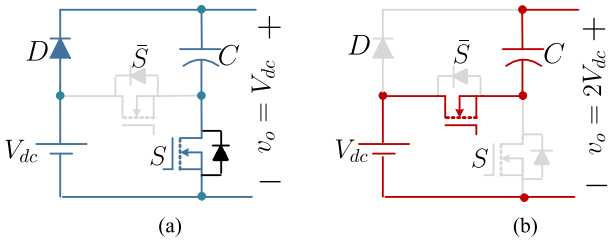

Fig. 2. Operation of the capacitor in SPSC Unit-I during the (a) charging state and (b) discharging state [19], [20], [52], [160].

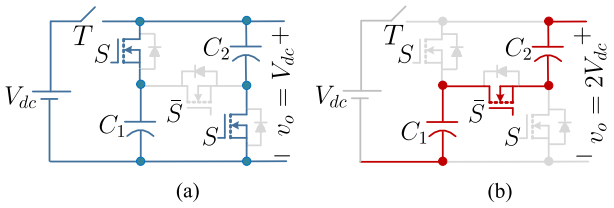

Fig. 3. Operation of the capacitor in SPSC Unit-II during the (a) charging state and (b) discharging state [21], [22], [24], [161].

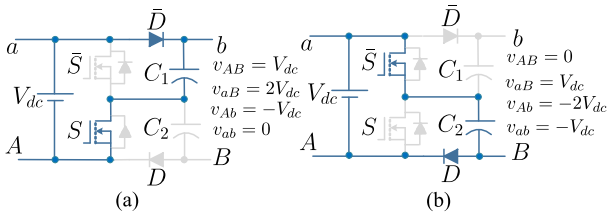

Fig. 4. Charging operation of the capacitors in the SC voltage doubler unit (a) for C_1 and (b) for C_2 [25]–[28].

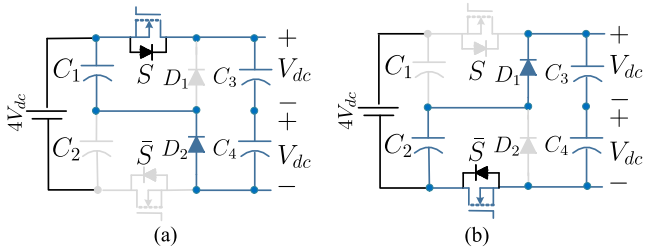

Fig. 5. Charging operation of the capacitors in the SC half-mode Unit-I [29]. (a) Discharging path of C_1. (b) Discharging path of C_2.

is related to the capacitors' charging operations in the SC half-mode Unit-I presented in [29], it can be observed that four dc-link capacitors, two complementary switches, and two diodes are needed to give two fixed values of discrete dc-link voltages at its output. As for the charging operation of each of these two dc-link output capacitors, only one diode and one power switch 188 are involved.

The presented structure in [30] uses three power switches, and the same number of power diodes as in [29] and its capacitor charging operation can be seen in Fig. 6(a). This structure is named as SC half-mode Unit-II, while each of the involved capacitors is charged at half value of the main dc-link voltage through a capacitive charging path including two diodes and a single power switch. Here, i_{ch} is the notation of charging current of the capacitors. Considering Fig. 6(b), another type of SC half-mode unit with the capability of generating four identical positive dc-voltage levels at its output, i.e., $0.5V_{\text{dc}}$, V_{dc}, $1.5V_{\text{dc}}$, and $2V_{\text{dc}}$, is introduced [31]. As can be observed

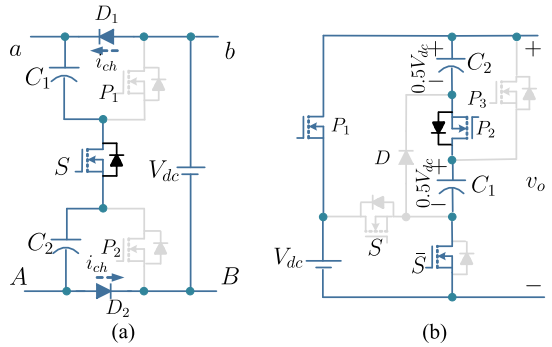

Fig. 6. Charging operation of the capacitors in (a) SC half-mode Unit-II [30] and (b) SC half-mode Unit-III [31].

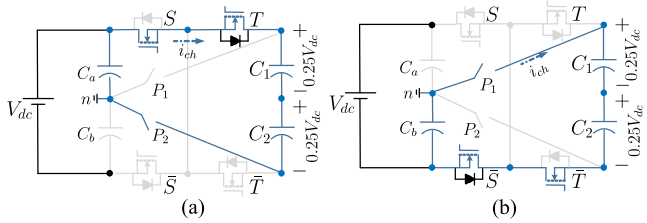

Fig. 7. Charging operation of the capacitors in SC half-mode unit K-type [34]. (a) Discharging path of C_1. (b) Discharging path of C_2.

from the capacitor charging flow path in Fig. 6(b), again, two involved capacitors are charged in parallel to the input dc source, while three power switches are integrated in the charging flow path. A similar multioutput SC-based basic unit with half-mode operation of the capacitors is also proposed in the presented SC-MLIs of [32] and [33].

The last configuration of this family of SC-based basic units is a K-type converter presented in [34]. This unit can provide two paths for the charging operation of the capacitors, as shown in Fig. 7. Similar to SC half-mode Unit-I, this structure requires four dc-link capacitors, as well, while it can output two identical positive-voltage levels, which are a quarter value of the main dc-link voltage. In all the SC-based half-mode units, capacitors, C_1 and C_2, have to be in series with each other, and then, they have to be connected in parallel to the main dc-link capacitors, C_a and C_b, through several semiconductor devices for the charging operation purpose. Therefore, considering the internal parasitic resistance of each dc-link capacitor, known as "equivalent series resistance (ESR)," a larger value of the impedance can be inserted in the charging loop of the capacitors compared to the other types of SC basic units, which helps to alleviate the charging current of the capacitor more. The details of current stress suppression solutions are later presented in Section V.

D. SC Voltage Tripler Units

These types of SC-based basic units provide a three times voltage-boosting feature to the SC-MLI topologies. The most common SC voltage tripler unit with its operating principle is depicted in Fig. 8(a). It uses two dc-link capacitors, two power diodes, and four power switches [35], [37]–[39], [67]. As can

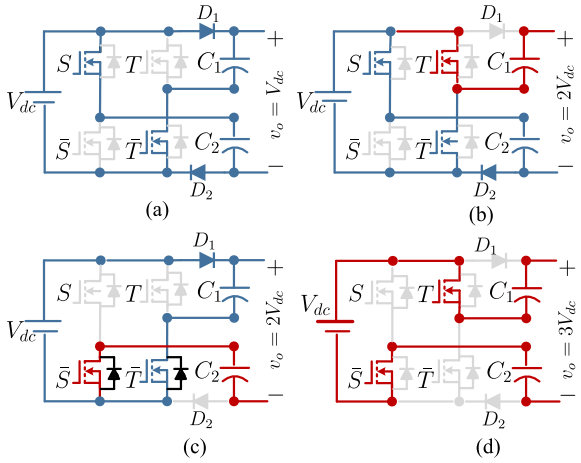

Fig. 8. Operating modes of SC voltage tripler Unit-I [35], [37]–[39], [67]. (a) Both the capacitors are charging. (b) and (c) One of the capacitors is charging and the other is discharging. (d) Both the capacitors are discharging.

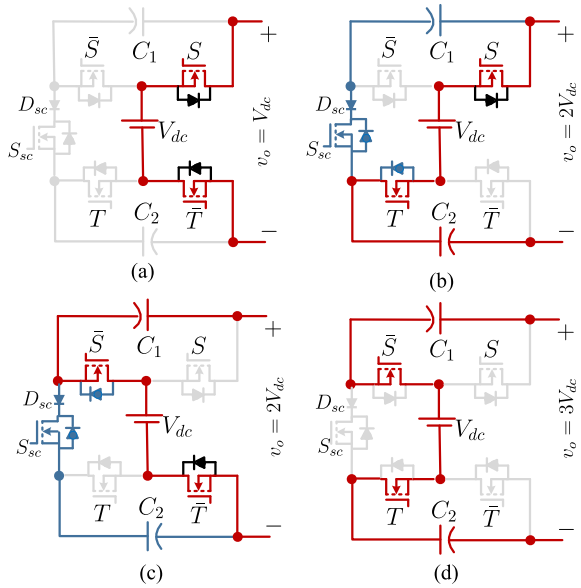

Fig. 9. Operating modes of SC voltage tripler Unit-II [71], [162]. (a) Both the capacitors are disconnected. (b) and (c) One of the capacitors is charging and the other is discharging. (d) Both the capacitors are discharging.

be seen, both the capacitors in this unit are charged to the input dc source, while for each, a single power diode with one of the involved power switches is required to be integrated in the capacitive charging path shown in blue color in Fig. 8. This basic SC unit is named as SC voltage tripler Unit-I, where the MVS of all the semiconductor devices is within the input dc-source voltage. As can be realized from Fig. 8(b) and (c), to convert the voltage level of $+2V_{\rm dc}$ to the output, two redundant switching states (RSSs) are available. These RSSs can be adopted in the modulation to effectively control the capacitor ripple voltages during the operation in its possible SC-MLI incorporation [67].

Another version of this basic SC unit named as SC voltage tripler Unit-II with its all operating modes is illustrated in Fig. 9 [71], [162]. In this case, there is no need to use

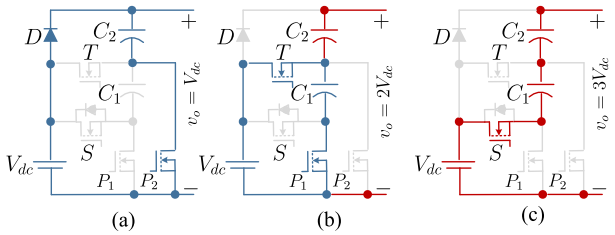

Fig. 10. Operating modes of SC voltage tripler Unit-III [163]. (a) C_2 is charging and C_1 is disconnected. (b) and (c) C_1 is charging and C_2 is discharging. (d) Both the capacitors are discharging.

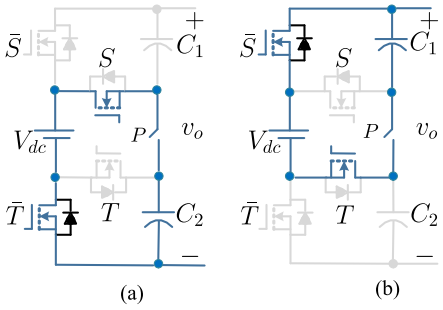

Fig. 11. Capacitors charging paths of SC voltage tripler Unit-IV [40]. (a) C_2 is charging and C_1 is disconnected. (b) C_1 is charging and C_2 is discharging.

any individual power diode; however, one additional reverse-blocking insulated gate bipolar transistor (RB-IGBT) switch in the charging path of both the capacitors is needed. Similar to SC voltage tripler Unit-I, all the involved semiconductors must tolerate the same MVS equal to the input dc-source voltage. In addition, for the $+2V_{\rm dc}$ output voltage level, there is an additional RSS that can be realized in Fig. 9(b) and (c).

The third version of these SC-based basic units named as SC voltage tripler Unit-III is introduced in [163], while its operating modes to generate different discrete output voltage levels are depicted in Fig. 10. As can be seen, again, both the capacitors charge in parallel to the input dc source, while the charging path semiconductors are only a power diode, D, and two MOSFETs without internal body diode, P_1 and P_2. Although this SC voltage tripler unit uses less number of semiconductor devices than others, it requires three reverse-blocking or RB-IGBT power switches. Similar to the previous SC voltage tripler units, the MVS of all semiconductors is within the input dc-source voltage.

SC voltage tripler Unit-IV is shown in Fig. 11, where without involving any diodes and just by the contribution of four normal MOSFETs/IGBTs and one four-quadrant power switch, three symmetrical discrete voltage levels can be generated at the output [40]. As can realized by Fig. 11, a four-quadrant power switch, P, is used in Fig. 11, where the MVS of all semiconductors is the same as the input dc-source voltage. A derived version of this type of SC voltage tripler unit with the inclusion of five normal power switches and a single power diode is also presented in [41], which inherits the same circuit characteristic as mentioned above. By replacing the switches $\bar{S}$ and $\bar{T}$, and using an RB-IGBT instead of a four-quadrant switch,

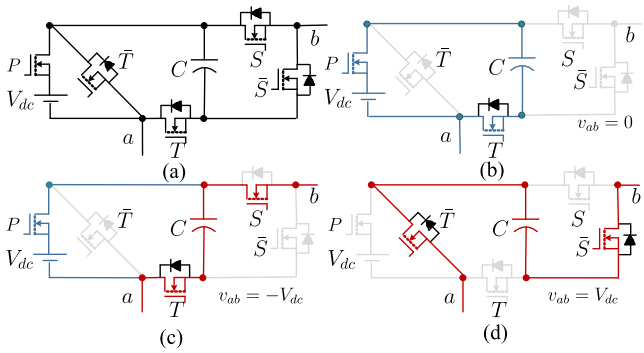

Fig. 12. Operating modes of SC bipolar unit [44]. (a) Main circuit. (b) Current flowing path when $v_{ab} = 0$. (c) Current flowing path when $v_{ab} = -V_{\rm dc}$. (d) Current flowing path when $v_{ab} = V_{\rm dc}$.

P, a passive-based design of this unit has also been recently used in [36].

E. SC Bipolar Unit

The operating modes of SC bipolar unit presented in [44] are shown in Fig. 12. This is the first available SC-based basic unit that is able to produce bipolar output voltage levels, i.e., $0V_{\rm dc}$, $\pm V_{\rm dc}$, In this unit, only a single dc-link capacitor is needed to be charged in parallel to the input dc-source voltage, while five power switches are needed for the whole operation. Herein, switch P can be chosen as an RB-IGBT or a series diode with a normal power MOSFET. Changing the polarity of the output voltage without using any classical unfolding FB cell makes this type of SC-based basic unit interesting since the MVS of all the semiconductors can be remained constant as the input dc-source voltage.

III. Derivations of Generalized SCCs

The SC-based basic units reviewed in the previous section can be used in a cascaded connection leading to interesting features such as modularity and generation of a larger number of discrete output voltages with higher overall gain. Herein, the same series–parallel switching operations are used to charge and discharge the capacitors; however, since additional SC cells are inserted in the circuit, all the switches of the generalized SCCs must be able to pass the current stress profile of the capacitive charging loops. Since each output voltage level is produced by the charged capacitor in the SCCs, any dc offset between the voltage levels can be ruled out. The generalization of SCCs has led to the development of numerous topologies suitable for high-voltage applications that are reviewed in this section.

One of the earliest generalized SCCs that is used to achieve larger voltage conversion gain by switching the capacitors in series and parallel is shown in Fig. 13(a) [19]. As all the capacitors are clamped to the input voltage level, the MVS across the switches is equal to the input dc source, which makes it suitable for high switching operation. This structure has been used just before the classical back-end FB cell to generate the positive and negative voltages in order to form an SC-MLI [19], [20], [52]. One variant of this SCC that used an active switch instead

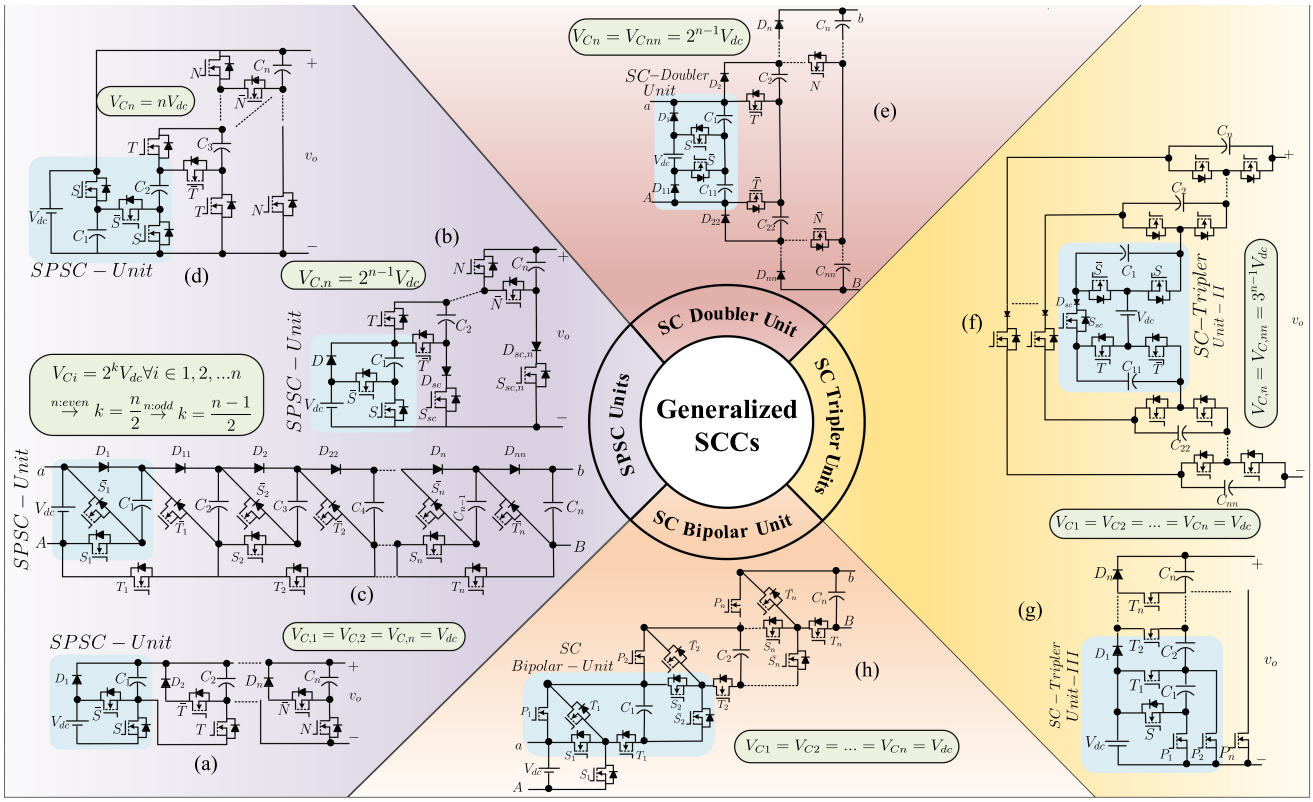

Fig. 13. Generalized SCCs based on (a) cascaded/series connection of SPSC Unit-I [19], [20], [52], (b) binary charging operation of capacitors with SPSC Unit-I [45]–[47], (c) cascaded/series connection of SPSC Unit-I [50], (d) binary charging operation of capacitors with SPSC Unit-II [21], (e) binary charging operation of capacitors with SC voltage doubler basic unit [26], (f) cascaded/series connection of SC bipolar unit [162], (g) ternary charging operation of capacitors with SC voltage tripler basic Unit-II [163], and (h) ternary charging operation of capacitors with SC voltage tripler basic Unit-III [44].

of the diode in each SC cell is proposed in [20]. This SCC has a bidirectional power flow capability; however, the use of all active switches in the SC network increases the total system cost and complexity in terms of gate driver circuit design and providing PWM signals. Another similar SCC that uses only one active switch in each SC unit is presented in [52], which simplifies the driving circuits and reduces the overall cost, while being able to achieve capacitor voltage self-balancing. However, due to the presence of diodes in this SCC, reactive power operation is not possible.

The generalized SCC using the SPSC-based basic units in Fig. 13(b) and presented in [45]–[47] can enhance the number of output voltage levels through a binary charging operation of the capacitors from $V_{\rm dc}$ to $2^n V_{\rm dc}$. As can be seen from Fig. 13(b), switches $S_{{\rm sc},i}$ are in series with diodes $D_{{\rm sc},i}$ to counteract the effect of internal body diode in the IGBT/MOSFET switches and make current unidirectional switches. To keep the capacitor charge for each voltage step, it is crucial to connect the related capacitors of the previous steps in parallel.

Fig. 13(c) illustrates an SCC with a discrete voltage step-up feature [50]. In this case, two SPSC basic units are placed in a special cascaded connection to form the main module with two capacitors, which can be connected in series to make another variant of the generalized SCCs. Hence, whether the number of capacitors is even or odd, the number of achievable voltage levels can be changed. This SCC can be used in bipolar (inverting) form with additional two switches at each end to generate all the negative-, positive-, and zero-voltage levels. In Fig. 13(d), an SPSC-based SCC is shown with all active switches that provide bidirectional power flow capability [21]. The voltage step-up is linear in this SCC, and all the capacitors are charged to the input dc source that can be connected in series and in parallel to build discrete output voltage levels. In this case, the MVS across the switches increases by the enhancement in number of SPSC units.

Fig. 13(e) illustrates another generalized SCC that is based on an SC doubler unit [26]. This topology does not need an end-side FB cell to generate negative- and zero-voltage levels, and hence, it benefits from reduced total standing voltage (TSV) index. The capacitors are charged as a binary asymmetrical pattern, and the MVS across the switches increases by the number of capacitors.

Fig. 13(f) illustrates a generalized SCC that is based on SC voltage tripler Unit-II [162]. In this topology, the capacitors are charged to ternary voltage levels, $3^n V_{\rm dc}$, as the voltage-boosting factor of a single SC unit is 3. The MVS of all the switches in each unit is equal to the input dc-source voltage of that unit, and hence, this SCC benefits from a low overall TVS in per-unit (p.u.) scale. In Fig. 13(g), a generalized SCC is illustrated that can step-up the output voltage to the number of capacitors plus the input dc source [163]. Since all the capacitors in this SCC are clamped to the input dc source, the maximum output voltage can be $(n+1)V_{\rm dc}$, where n is the number of capacitors. The main advantage

TABLE I
QUANTITATIVE COMPARISON OF DIFFERENT SCCS

Type of SCCs	No. of Components			No. of Levels	Max No. of ON-Switches	Value of MVS	Maximum TSV(pu)	Voltage Across Caps
	S	D	C					
Fig. 13(a)	$2n$	n	n	$n+1$	n	V_{dc}	$\frac{2n}{n+1}$	V_{dc}
Fig. 13(b)	$3n$-1	n	n	2^n	n	$2^{n-1}V_{dc}$	$\frac{3(2^n-1)-1}{2^n}$	$2^{n-1}V_{dc}$
Fig. 13(c) n:even	$2n$	n	n	$3\left(2^{\frac{n}{2}-1}\right)$	$2n$	$2^{\frac{n}{2}}V_{dc}$	$\frac{4(2^{\frac{n}{2}}-2)+2(2^{\frac{n}{2}}+1)}{3(2^{\frac{n}{2}}-1)}$	$2^{\frac{n}{2}}V_{dc}$
Fig. 13(c) n:odd	$2n$	n	n	$3\left(2^{\frac{n-1}{2}-1}\right)$	$2n$	$2^{\frac{n-1}{2}}V_{dc}$	$\frac{4(2^{\frac{n-1}{2}}-2)+2(2^{\frac{n+1}{2}}+1)}{3(2^{\frac{n-1}{2}}-1)}$	$2^{\frac{n-1}{2}}V_{dc}$
Fig. 13(d)	$3(n$-1)	0	n	n for $n \geq 2$	$2(n$-1)	$(n-1)V_{dc}$	$\frac{2(n-1)}{n}+\frac{n-1}{2}$	V_{dc}
Fig. 13(e)	$2n$	$2n$	$2n$	2^n	n	$2^{n-1}V_{dc}$	$\frac{2(2^n-1)}{2^n}$	$2^{n-1}V_{dc}$
Fig. 13(f)	$5n$	n	$3n$	3^n	$3n$	$3^{n-1}V_{dc}$	$\frac{2.5(3^n-1)}{3^n}$	$3^{n-1}V_{dc}$
Fig. 13(g)	$2n$	1	n+1	n	$3n$	nV_{dc}	$\frac{2.5(5^{(n^2+2n)})}{n+1}$	V_{dc}
Fig. 13(h)	$5n$	n	n	n	$2n$	V_{dc}	$\frac{7n-3}{n}$	V_{dc}

of this SCC is that it requires a minimum number of conducting switches (ON-state switches at each switching instant), which is independent of n. Moreover, only two switches are required to charge any of the capacitors, and it is not dependent on the number of output voltage levels.

Almost all of the discussed SCCs deploy a back-end FB cell in order to achieve negative- and zero-voltage levels, where all the switches in the FB cell should withstand the peak of the SCC output voltage. As high-voltage switches are costly with high $R_{\text{DS,ON}}$, all the SC-MLIs using the mentioned SCCs are limited to low/medium-power applications. In [42], a generalized bipolar SCC is proposed, where no FB cell is required to generate the negative-voltage levels as the bipolar configuration can be implemented with ease. In this SCC, all the capacitors are clamped to V_{dc}, and all the switches are required to block only V_{dc} as the MVS. A similar concept is also adopted in [42] and [43]. Although they need much larger number of switching devices, the capacitors can be charged through different RSSs, which is helpful for a proper charging operation of the capacitors with reduced ripple voltage. Table I compares some of the most important circuit features of the aforementioned SCCs. The comparative items are the number of main components, e.g., switches (S), diodes (D), and capacitors (C), the number of output voltage levels, the maximum number of ON-state switches at each switching instant, the value of MVS across the switches, the maximum value of the overall TSV in p.u. scale, and the pattern of capacitors voltage charging operation.

IV. SC-MLIs

SC-MLIs can be categorized as: single- and multiple-dc-source SC-MLIs, mid-point-clamped SC-MLIs, common-ground switched-capacitor (CGSC)-based MLIs, and hybrid SC-MLIs, as shown in Fig. 14. The categorization of the first four types of SC-MLIs is based on the type of output voltage port of inverters. Here, single- and multiple-dc-source SC-MLIs usually need two half-bridge (HB) legs to output the inverter voltage. In contrast, the output voltage of the inverters in mid-point-clamped and CGSC-based MLIs is measured with reference to the neutral point and the ground of the input dc source, respectively. The last category named as hybrid MLIs may use one of the aforementioned rules for the output voltage terminal of the inverter but with an integrated SB and/or FC-based technology. In this section, each of these SC-MLIs categories is reviewed in detail.

A. Single DC-Source SC-MLIs

The simplest solution to convert the multiple generated voltage levels of different types of SCCs as a bidirectional waveform is to use a back-end FB unfolding cell, as shown in Fig. 15(a). Similarly, plenty of single-source SCMLIs have been presented so far [19]–[21], [31], [32], [39], [46], [48], [65], [67], [69], [160], which use the generalized version of SCCs based on basic SPSC or SC voltage tripler units in the front-end side. All the four involved switches of this unfolding FB cell need to withstand the largest MVS equal to the peak of inverter output voltage, which can severely affect the TSV index of the converter. Although the recent advances in semiconductor devices have provided new types of SiC power MOSFETs with higher drain–source blocking voltage capability, this unfolding FB cell can still cause a sort of limitations for some high-voltage-based applications. Moreover, variable high-frequency common-mode voltage (HF-CMV) is another shortcoming of this type of circuit configuration, which causes EMI and leakage current propagation issues in photovoltaic (PV), motor drives, and even battery-integrated applications.

To reduce the MVS across the FB cell switches, and to improve the TSV index of the single dc-source SC-MLIs, HB-leg circuit-based architecture can also be used, as presented in [25]–[27], [30], [36], [40], [50], and [70] and as shown in Fig. 15(b). In this case, both the switches in one of these HB legs have to tolerate an MVS equal to the input dc source, and the switches incorporated in the other HB leg side must withstand the peak of the inverter output voltage. Therefore, similar to the unfolding FB cell, HB legs act as an output voltage polarity inversion unit, while their all four switches operate at a line/fundamental output frequency of the converter. Hence, from the load current

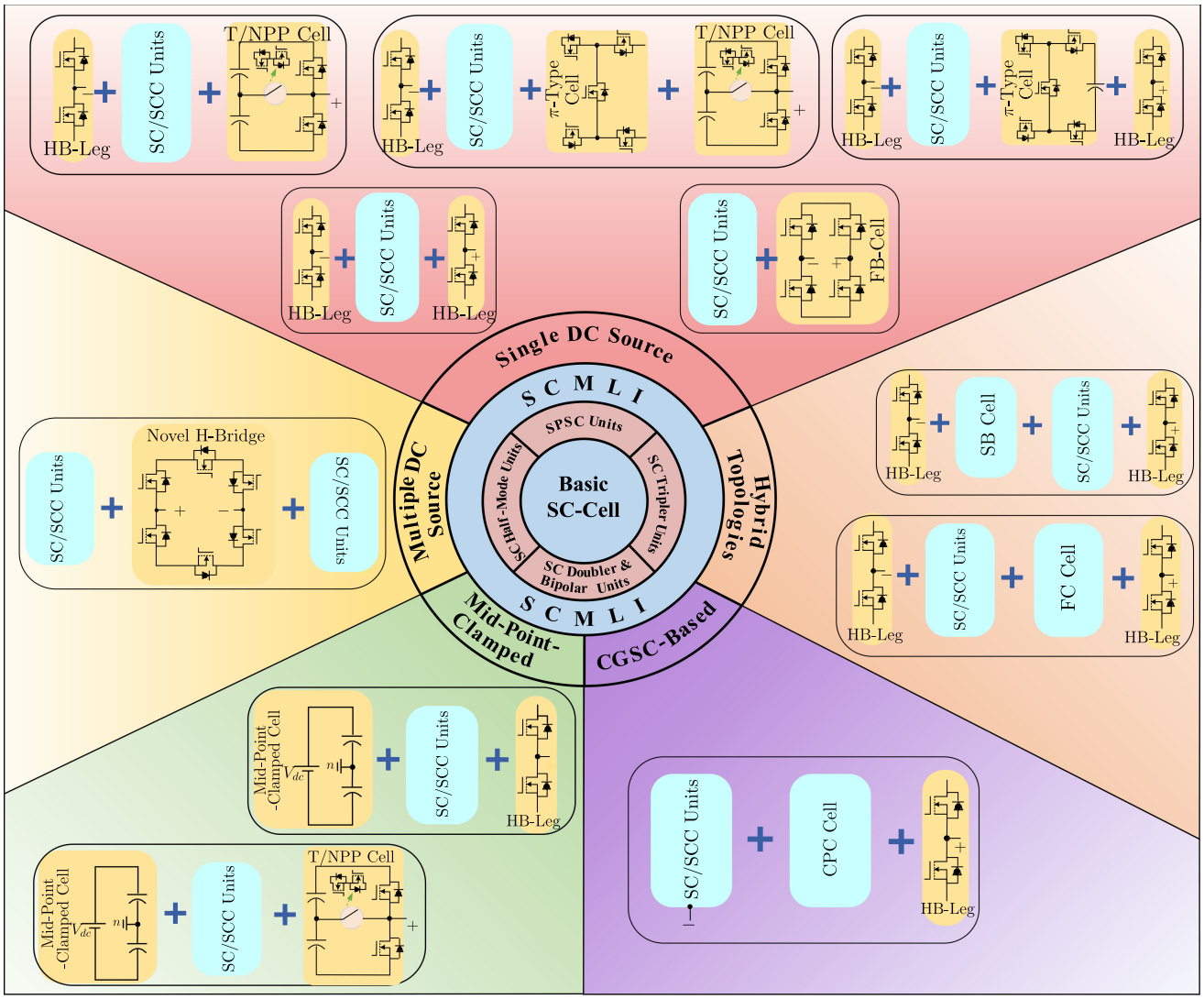

Fig. 14. Classification of SC-MLIs based on different types of SC basic units.

flowing path perspective, switches S and $\bar{T}$ must be ON during the positive half-cycle of output voltage levels, while in the negative half-cycle, switches $\bar{S}$ and T have to be in the ON-state condition. The presented SC-MLIs in [25] and [26] are based on these HB legs, while they used the SC voltage doubler unit to generate multiple dc-link voltage levels. To achieve a larger number of inverter output voltage levels, Saeedian *et al.* [26] have used a generalized SCC shown in Fig. 13(e), while Ye *et al.* [25] have placed the input dc source in the middle of the circuit and has integrated multiple SC voltage doubler units in two sides of the input dc source, as shown in Fig. 15(c). Using two identical SC voltage doubler units with opposite polarity on two sides of the input dc source, a seven-level (7L) inverter with triple output voltage conversion gain is introduced in [25]. Owing to the provided RSSs in the SC voltage doubler units, the switches of this topology can also be driven through a hybrid modulation technique, which can further improve the voltage ripple profile of the capacitors. Following this, Saeedian *et al.* [27] have used one cell of the SC voltage doubler unit with this two HB legs. Hence, a five-level (5L) double-voltage-gain SC-based inverter using six switches is achieved. Conversely, a 7L variant of this structure has recently been proposed in [70], while instead of power diodes, four-quadrant power switches are used in its basic SC voltage doubler unit. Although ten power switches are used to realize a 7L SC-based inverter with 1.5 times voltage conversion gain, a reduced value of the MVS and, in turn, reduced overall TSV index across the switches with a bidirectional power flow capability are its most important features. Apart from the SC voltage doubler unit, SC half-mode Unit-II [30] and SC voltage tripler Unit-IV [40] have also been used in this type of circuit architecture, while a 7L output voltage using seven and ten switches and with 1.5 times and triple voltage conversion gain, respectively, is attained. The triple-gain 7L inverter presented in [164], the quadruple-gain 9L inverter proposed in [51], and the generalized SC-MLIs proposed in [50], [54], and [66], respectively, are the other notable structures that have been constructed based on this HB-leg circuit design.

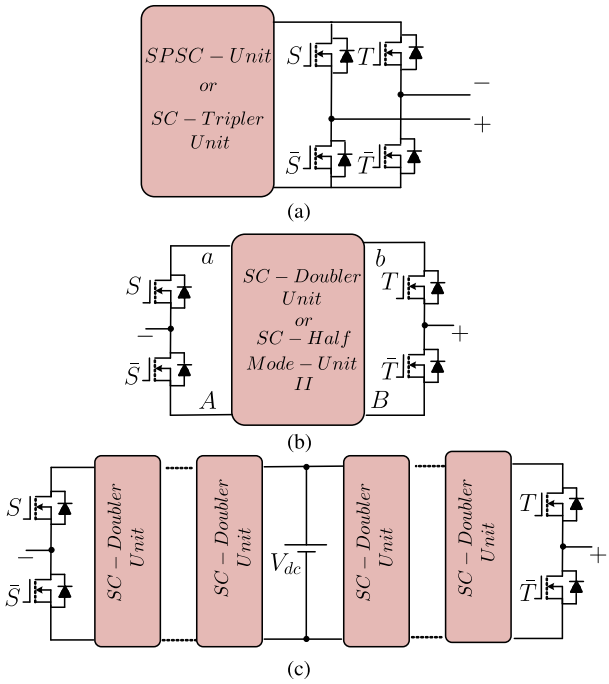

Fig. 15. (a) SC-MLIs with FB unfolding cell conceptualized in [19]–[21], [31], [32], [39], [46], [48], [67], [71], and [160]. (b) SC-MLIs using two HB legs [25]–[27], [30], [40], [70]. (c) Generalized SC-MLI using two HB legs [25].

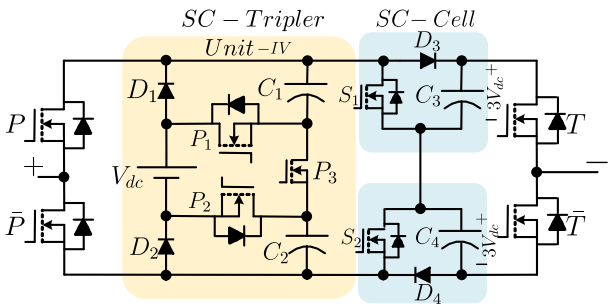

Fig. 16. 11L single-source SC-based inverter using SC voltage tripler unit integration [36].

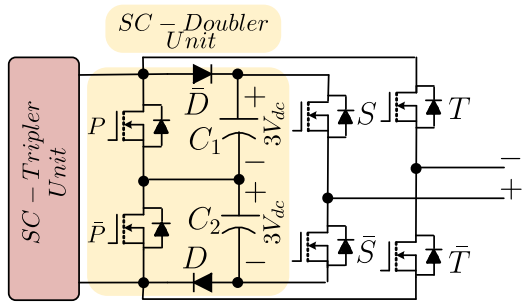

Fig. 17. 13L single source SC-based inverter using SC voltage doubler and SC voltage tripler unit integration [37].

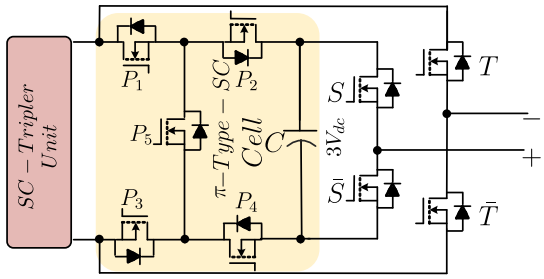

Fig. 18. 13L single-source SC-based inverter using SC voltage tripler unit and a π-type SC cell integration [35], [38].

To enhance the number of output voltage levels as well as the static voltage gain of the single dc-source SC-MLIs with the incorporation of the two-HB-leg polarity inverting technique, an 11-level (11L) SC-based inverter is proposed in [36]. This structure is illustrated in Fig. 16 and is comprised of a passive-based design of a front-end SC voltage tripler Unit-IV series with two upper and lower sides SC cells. Using a proper series–parallel switching conversion of the front SC voltage tripler Unit-IV, the voltages across capacitors C_3 and C_4 are balanced at $3V_{\rm dc}$. The overall voltage conversion gain of this structure is five, while five out of nine power switches are involved in the charging path of the capacitors. Similar to this concept, a 13-level (13L) SC-based inverter is also proposed in [37]. In this case, front-end SC voltage tripler Unit-I, that can be replaced with any other types of the available SC voltage tripler units, is in series with an SC voltage doubler unit, as shown in Fig. 17. Both the capacitors of this SC voltage doubler unit can be charged up to $3V_{\rm dc}$, which is the maximum gain of the front-end SC voltage tripler unit. As a result, the gain of these two SC-based units can be multiplied to each other to realize a maximum voltage gain of six for the whole converter. Herein, HB legs are used to invert the output voltage polarity to realize a 13L SC-based inverter. Concerning this technique, the MVS across switches S and $\bar{S}$ as one HB leg of the converter is equal to $6V_{\rm dc}$, while for the other HB-leg switches, i.e., switches T and $\bar{T}$, this MVS is only equal to $V_{\rm dc}$. The total number of required power switches for this structure is 10, while only six of them are involved in the charging path of the capacitors.

Following this voltage gain enhancement solution, Ye *et al.* [35] and Sandeep [38] use similar front-end SC voltage tripler Unit-I in series with a π-type SC network, including five normal MOSFETs/IGBTs and a floating capacitor, as illustrated in Fig. 18. Similar to [37], this topology can generate 13L output voltage with a six times overall voltage gain, while the floating capacitor, C, can be charged up to $3V_{\rm dc}$ using four switches P_1, P_2, P_3, and P_4. The advantage of these topologies over their counterpart presented in [37] is the less utilization of the floating capacitors. In this case, an HB leg has also been used to invert the output voltage levels with a reduced value of the overall TSV, whereas the number of required power switches is 12 and 13 for the presented topologies in [35] and [38], respectively. All these mentioned 13L single dc-source SC-MLIs have some RSSs during the middle output voltage level generation, which can further facilitate the incorporation of hybrid PWM methods to reduce the capacitor ripple voltages at higher range of output power. Regarding this type of SC-MLIs, Kim *et al.* [55] have proposed another 13L six-times-gain SC-based inverter with 14 power switches, while its front-end SC network is SC voltage tripler Unit-IV cascaded with a π-type SC network. Replacing this

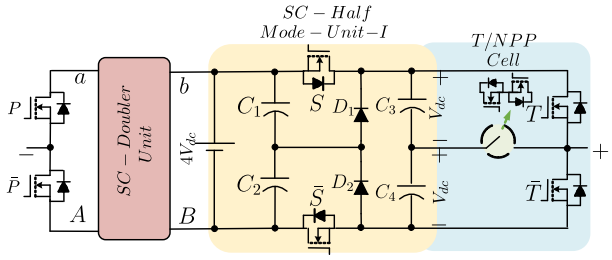

Fig. 19. 17L single-source SC-based inverter in [29].

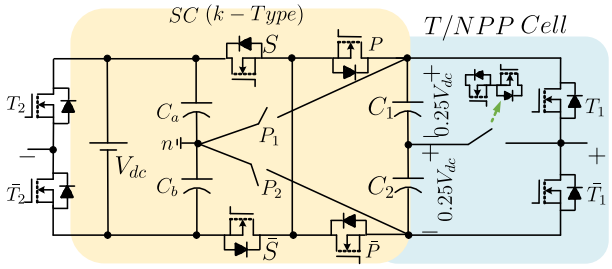

Fig. 20. 13L single-source SC-based inverter using a K-type SC unit [34].

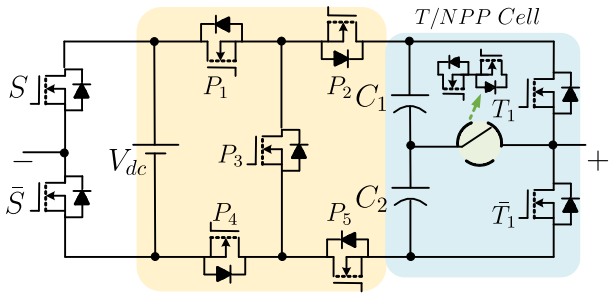

Fig. 21. 9L single-source SC-based inverter [57].

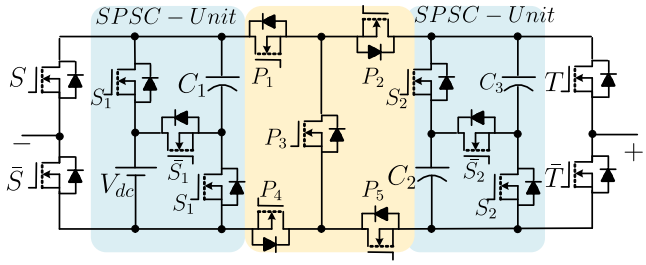

Fig. 22. 13L single-source SC-based inverter [74].

front-end SC network with the described SPSC Unit-I and following the same principle, a 9L inverter is proposed in [53], while the capacitor, C, can be charged up to $2V_{\rm dc}$, which is the maximum voltage gain of SPSC Unit-I. In contrast, Bhatnagar *et al.* [58] used simple SPSC Unit-I in the front-end side, while combining the concept of π-type SC network with a standard T/NPP cell. Using this, a 13L output voltage is achieved with 13 power switches. Although the overall voltage gain of this converter is 3, its MVS across the switches is only $2V_{\rm dc}$, while three capacitors of this structure should withstand $V_{\rm dc}$.

Owing to the utilization of the HB-leg generalized concept proposed in [25], another reduced switch-count single-input-dc-source 17-level (17L) SC-based inverter is also presented in [29]. Herein, an SC voltage doubler unit is used in the left-hand side of the input dc source, while in the right-hand side, an integration of SC half-mode Unit-I with a T/neutral-point-piloted (NPP) cell is used to realize an eight times voltage gain with 17L output voltage. This topology is shown in Fig. 19, where ten power switches and six capacitors are used to realize all the 17L output voltage. Through this structure, it can be deduced that to convert the dc-link stored voltages of the SC half-mode unit capacitors to the output, a T/NPP cell is needed. Using the K-type SC unit and the same T/NPP cell with one HB leg, another 13L SC-based inverter with triple overall voltage gain and 12 power switches is proposed in [34], as well as shown in Fig. 20.

To create a 9L inverter output voltage, the concept of the π-type SC network and the T/NPP cell is integrated to each other as a developed SC-MLI presented in [57]. This topology requires an HB leg, as shown in Fig. 21, while both the capacitors in the T/NPP cell are balanced at half value of the input dc-source voltage. This topology is derived from [63], where one more power switch is used to create the same number of inverter output voltage levels. By replacing the input dc source with SPSC Unit-I and regarding the same circuit configuration, a 13L SC-based inverter with triple voltage gain is introduced in [58]. In this case, by replacing the T/NPP cell with an HB leg and using the same single dc source with a π-type SC cell, a 5L SC-based inverter can be obtained, while through a series connection of this π-type SC cell with the similar SC network, the number of output voltage levels can be even extended, as presented in [59]. The presented 9L SC-based inverter in [72] and [73] has also used this T/NPP cell with an SC-integrated FB cell and SPSC unit, while 12 and 10 power switches are used, respectively, with a double voltage gain. Taking the structure presented in [57] into account, and using two SPSC basic units in the left- and right-hand sides of its π-type network, another 13L SC-based inverter with 15 power switches and two HB legs is also derived, as shown in Fig. 22 [74]. Here, the overall voltage gain is 6. It benefits from a bidirectional power flow capability. The value of MVS is only half value of the peak inverter output voltage, and the voltage stress across three capacitors is $V_{\rm dc}$ and $2V_{\rm dc}$. Being motivated by the same π-type network, and using the same two HB legs, another triple-gain 7L inverter is introduced in [75]. This topology is illustrated in Fig. 23; it uses nine power switches, two diodes, and three capacitors. All these three capacitors are clamped at $V_{\rm dc}$. Although the TSV index of the converter is reasonable among other 7L SC-based inverter counterparts, the topology lacks in having enough RSSs and supporting bidirectional power flow operation.

Another 7L variant of the single-dc-source SC-based inverters with the integration of the unfolding FB and T/NPP cells is proposed in [60]. As shown in Fig. 24(a), these two cells have been connected to each other through a four-quadrant power switch, while a 1.5 times voltage conversion gain is achieved. Here, both the capacitors should be in series and have to be connected in parallel to the input dc source to be charged at $0.5V_{\rm dc}$. By keeping fixed the T/NPP cell, and series connection

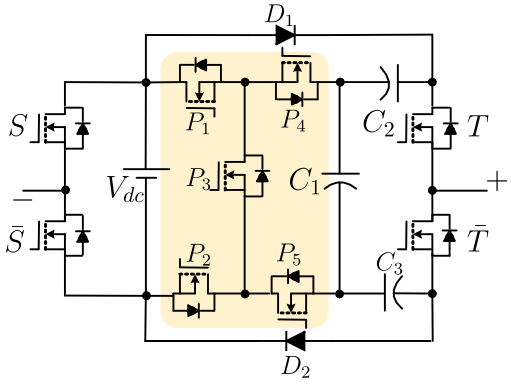

Fig. 23. 7L single-source SC-based inverter [75].

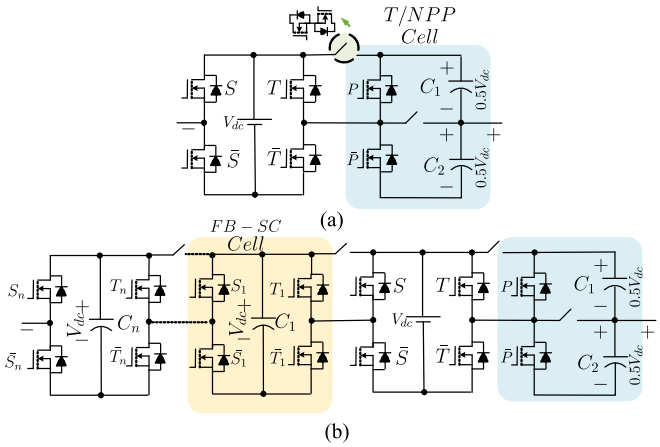

Fig. 24. (a) 7L single-source SC-based inverter [60]. (b) Generalized SC-based inverter [60].

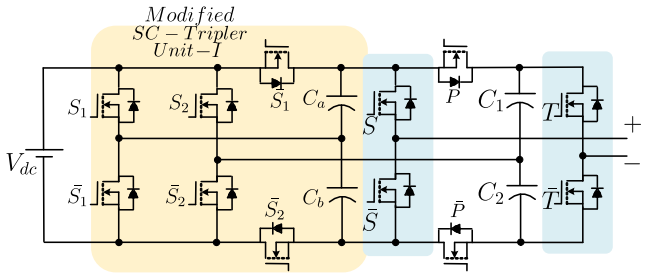

Fig. 25. 7L single-source SC-based bridge modular inverter [68].

of several SC-integrated FB cells with the help of interconnected four-quadrant switches, this topology can be generalized to achieve a larger number of inverter output voltage levels, as demonstrated in Fig. 24(b). In this regard, a similar output voltage level extension without using the T/NPP cell and just by cascaded connection of several SC-integrated FB cells is proposed in [62]. The 7L variant of this SC-based MLI requires 12 MOSFETs/IGBTs and two four-quadrant power switches, while the voltage conversion gain of the converter is triple using two dc-link capacitors.

The last structure from this category is related to a quadruple gain 7L inverter named as bridge modular SC-MLI [68]. As shown in Fig. 25, this topology comprised of 12 power switches integrated within four HB legs. Here, two out of four used HB legs highlighted with the blue color are in charge of inverting the polarity of the front-end SC network, which is based on a modified version of SC voltage tripler Unit-I. In this case, capacitors C_1 and C_2 are balanced at $2V_{\rm dc}$, which is the summation of voltages provided by the input dc source and the capacitors in the modified SC voltage tripler Unit-I. Having additional RSSs to create the output voltage levels of $\pm V_{\rm dc}$ and $\pm 2V_{\rm dc}$ can facilitate the integration of hybrid PWM techniques to further minimize the capacitor ripple voltage deviations in this structure. Although this topology cannot generate the output voltage levels of $\pm 3V_{\rm dc}$, the p.u. TSV index of the converter is 5.5, while only two switches, e.g., switches T and $\bar{T}$, should tolerate the MVS equal to $4V_{\rm dc}$. Owing to using the standard MOSFETs/IGBTs in this structure, its possible application can be further broaden if a bidirectional power flow operation is needed. Moreover, since the sources of HB-leg switches are grounded, the gate driver of the switches can be designed with a bootstrap SC-based technique, which may help for further reduction of the size and cost of its auxiliary driving circuit [165]. Using the unfolding FB cell instead of two HB legs to invert the output voltage polarity, and following the same switching principle, a generalized single dc-source derivation of this topology has also been presented in [69]. To this end, Table II summarizes all the aforementioned single-dc-source SC-MLIs in terms of the number of required power switches (S)/diodes (D), required dc-link capacitors (C), required gate drivers (G), output voltage levels with the reported total harmonic distortion (THD) percentage, overall voltage gain with the information of the voltages across the capacitors, the value of MVS with the p.u. value of the overall TSV across the switches, the maximum number of ON-state switches at each instant, and the maximum number of switches that are involved in the charging path of the capacitors. The reported efficiency of each structure at the rated power is also considered in this table. Here, the single-dc-source SC-MLIs have been categorized based on their overall circuit architecture, i.e., FB-based, HB-leg-based, or a combination of HB leg(s) and T/NPP cell-based. From the point of view of the number of output voltage levels versus the number of required power switches as well as p.u. scale of the overall TSV across the switches, the 17L inverters presented in [29] and [54] have a better condition over the others. This ratio for the 13L inverter presented in [37] is 1.3, which is another notable topology in this category of SC-MLIs with some RSSs for the middle output voltage levels. From the number of power switches involved in the charging path of the capacitors' point of view, the presented 7L SC inverter in [30] with only one switch out of seven has an optimized condition than others.

B. Multiple DC-Source SC-MLIs

Each of the described basic SC units/generalized SCCs can be connected to an unfolding FB cell, and then, through the cascaded connection, multiple-dc-source SC-MLIs can be realized, as shown in Fig. 26 [88]. In this case, adjusting the voltage magnitude of different dc sources can lead to the development of different symmetric or asymmetric input-dc-source-based

TABLE II
COMPARATIVE STUDY OF DIFFERENT SINGLE DC-SOURCE SC-MLIS

Type of SCMLI	No. of Components				No. of Levels/ THD	Overall Voltage Gain/ Caps Voltage	Max No. of ON-Switches	Max No. of Switches in Charging Path	TSV (pu)/ MVS	Reported Rated Efficiency
	S	D	C	G						
FB-based [20]	10	0	3	10	7/19.5%	$3/V_{dc}(3)$	5	6	$6/3V_{dc}$	85%@1kHz/5W
HB-based [25]	8	4	4	8	7/22.4%	$3/V_{dc}(4)$	4	4	$4/2V_{dc}$	93%@50Hz/330W
HB-based [30]	7	2	2	7	7/NA	$1.5/0.5V_{dc}(2)$	3	1	$4.33/1.5V_{dc}$	96%@50Hz/600W
HB-based [40]	9	4	2	9	7/7%	$3/V_{dc}(2)$	5	3	$5.66/3V_{dc}$	92.2%@50Hz/500W
HB-based [41]	9	1	2	9	7/NA	$3/V_{dc}(2)$	5	4	$6/3V_{dc}$	NA%@50Hz/NA
HB/NPP-based [60]	10	0	2	8	7/16.2%	$1.5/0.5V_{dc}(2)$	5	4	$6/V_{dc}$	95.5%@50Hz/250W
FB-based [65], [67]	8	2	2	8	7/23.3%	$3/V_{dc}(2)$	4	4	$5.33/3V_{dc}$	96.4%@50Hz/340W
HB-based [68]	12	0	4	12	7/11.2%	$4/V_{dc}(2),2V_{dc}(2)$	6	8	$5.5/4V_{dc}$	96.5%@50Hz/270W
HB-based [70]	10	0	2	8	7/13.7%	$1.5/V_{dc}(2)$	6	4	$5.33/V_{dc}$	96.6%@50Hz/600W
FB-based [71]	9	1	2	9	7/2.8%	$3/V_{dc}(2)$	5	5	$6/3V_{dc}$	92.1%@50Hz/150W
HB-based [75]	9	2	3	9	7/12%	$3/V_{dc}(3)$	5	5	$5.6/3V_{dc}$	93.1%@50Hz/313W
HB-based [164]	8	3	2	8	7/NA	$3/V_{dc}(1),2V_{dc}(2)$	5	2	$5.66/3V_{dc}$	98.2%@50Hz/500W
HB-based [22]	12	0	4	12	9/16.6%	$4/V_{dc}(4)$	6	6	$6/4V_{dc}$	96%@50Hz/50W
HB-based [26]	8	4	4	8	9/11.8%	$4/V_{dc}(2),2V_{dc}(2)$	6	4	$4/V_{dc}$	92.75%@50Hz/1kW
FB-based [31]	9	2	2	9	9/3.1%	$2/V_{dc}(2)$	4	4	$5.75/2V_{dc}$	94.2%@1kHz/200W
FB-based [32]	10	1	2	8	9/NA	$2/V_{dc}(2)$	4	2	$6/2V_{dc}$	96%@50Hz/600W
HB-based [44]	19	3	3	19	9/NA	$4/V_{dc}(3)$	11	9	$4.75/V_{dc}$	91.7%@50Hz/NA
FB-based [48]	9	2	2	9	9/13.8%	$4/V_{dc}(1),2V_{dc}(1)$	5	3	$5.25/4V_{dc}$	NA%@50Hz/NA
HB-based [51]	8	3	3	8	9/NA	$4/V_{dc}(1),2V_{dc}(2)$	4	4	$5.75/4V_{dc}$	93%@50Hz/500W
HB-based [53]	12	0	2	12	9/NA	$4/V_{dc}(1),2V_{dc}(2)$	6	6	$5.25/2V_{dc}$	NA%@50Hz/NA
HB/NPP-based [57]	11	0	2	10	9/12.5%	$2/0.5V_{dc}(2)$	7	4	$5.5/V_{dc}$	NA%@50Hz/400W
HB/NPP-based [63]	12	0	2	10	9/NA	$2/0.5V_{dc}(2)$	6	4	$5.5/V_{dc}$	80%@50Hz/15W
HB/NPP-based [72]	12	0	3	11	9/8.8%	$2/V_{dc}(1),0.5V_{dc}(2)$	5	2	$5.5/2V_{dc}$	97.4%@50Hz/1kW
HB/NPP-based [73]	10	1	3	9	9/10.2%	$2/V_{dc}(1),0.5V_{dc}(2)$	5	2	$5.5/2V_{dc}$	98%@50Hz/1kW
HB-based [114]	10	3	2	10	9/NA	$2/0.5V_{dc}(2)$	5	3	$6.75/2V_{dc}$	97.1%@50Hz/400W
HB-based [36]	9	4	4	9	11/6.8%	$5/V_{dc}(2),3V_{dc}(2)$	5	5	$5/6V_{dc}$	95.5%50Hz/220W
HB-based [37]	10	4	4	12	13/11%	$6/V_{dc}(2),3V_{dc}(2)$	8	6	$5.5/6V_{dc}$	95.5%@50Hz/500W
HB-based [35]	12	4	3	12	13/NA	$6/V_{dc}(2),3V_{dc}(1)$	7	8	$6/6V_{dc}$	95.5%@50Hz/500W
HB-based [38]	13	2	3	13	13/NA	$6/V_{dc}(2),3V_{dc}(1)$	8	9	$5.33/6V_{dc}$	97.3%@50Hz/1kW
HB/NPP-based [34]	12	4	3	11	13/5.3%	$3/V_{dc}(2),0.5V_{dc}(2)$	6	6	$6/3V_{dc}$	NA%@50Hz/1kW
HB/based [55]	14	1	3	14	13/NA	$6/V_{dc}(2),0.5V_{dc}(1)$	7	7	$5.5/3V_{dc}$	NA%@50Hz/NA
HB/NPP-based [58]	13	1	3	13	13/NA	$3/V_{dc}(1),0.5V_{dc}(2)$	7	5	$5.33/2V_{dc}$	96.53%@50Hz/1kW
HB-based [64]	13	2	3	13	13/7.2%	$6/V_{dc}(2),3V_{dc}(1)$	7	7	$6/3V_{dc}$	NA%@50Hz/NA
HB-based [74]	15	0	3	15	13/7.7%	$6/V_{dc}(1),2V_{dc}(2)$	8	10	$5/3V_{dc}$	94%@50Hz/1kW
HB/NPP-based [29]	10	4	6	9	17/NA	$8/V_{dc}(2),2V_{dc}(2),4V_{dc}(2)$	5	6	$4.25/8V_{dc}$	95.5%@50Hz/1kW
HB-based [54]	10	5	5	10	17/3.9%	$8/V_{dc}(1),2V_{dc}(2),4V_{dc}(2)$	5	6	$4.25/8V_{dc}$	94.5%@50Hz/80W
HB-based [50]	20	8	8	20	21/4.8%	$10/V_{dc}(2),2V_{dc}(4),4V_{dc}(2)$	10	16	$5/2V_{dc}$	NA%@50Hz/NA
HB-based [66]	20	12	10	20	21/4.5%	$10/V_{dc}(2),2V_{dc}(4),4V_{dc}(2)$	10	16	$5/2V_{dc}$	NA%@50Hz/NA

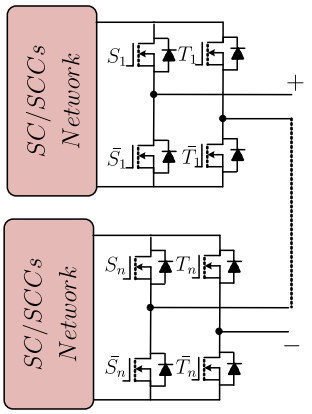

Fig. 26. Cascaded version of SC-MLIs using multiple dc sources.

MLIs [76]. Simplicity and modularity are two main features of this type of circuit extensions. Here, one of the cascaded units can be FB-based, and the remaining ones can be constructed based on any types of previously discussed SC-MLIs [20], [91]. Hence, some hybrid circuit architectures can also be generated. A 19-level (19L) SC-based inverter using two symmetric dc sources with eight times voltage conversion gain and 12 power switches is proposed in [77], which is an example of this type of multi-input SC-MLIs. A cascaded connection of a three-level (3L) FB-based cell with the 9L derived topology of [46] can also lead to a 27-level (27L) inverter with two asymmetric dc sources [91]. However, using four switches as an FB cell in the back-end side of each unit in a cascaded version of SC-MLIs can still cause the concern of large values of MVS and TSV indexes for the converter.

Fig. 27(a) shows another general circuit scheme for double-port-based SC-MLIs, which has been widely used in many research articles, such as [45], [47], [49], [78], [162], and [163]. This general circuit architecture has been derived from [167] and [168] and is called novel/developed H-bridge, as well. Herein, the HB switches in the left- and right-hand legs of the circuit have to tolerate an MVS related to their respective output voltage of the left- and right-hand sides of SC-based basic units/generalized SCCs, whereas two intermediate switches, P and $\bar{P}$, must withstand an MVS equal to the maximum voltage gain of both the incorporated SC-based basic units/generalized SCCs. Hence, the overall TSV index of the converter is reduced in comparison to unfolding FB-based cascaded technique, while only two switches must tolerate the MVS. In this case, the right- and

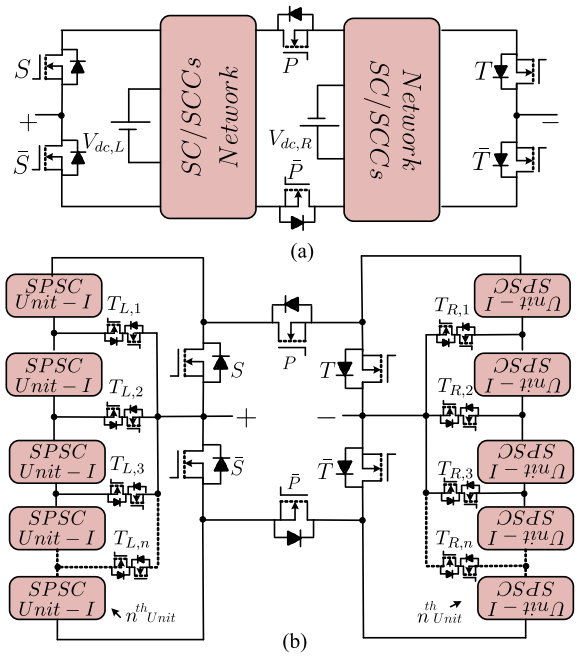

Fig. 27. Generalized configuration of SC-MLIs using a novel/developed H-bridge configuration based on (a) double-port design and (b) multiport design [166].

left-hand-side input dc-source magnitudes, i.e., $V_{\mathrm{dc},R}$ and $V_{\mathrm{dc},L}$, can be chosen based on symmetric, binary asymmetric, ternary asymmetric, or even quaternary and quinary asymmetric-based designs to realize various numbers of required output voltage levels. The SCCs used in each side of the converter have to be placed with an opposite polarity with respect to each other. Furthermore, the number of input dc sources can be integrated if a generalized multiport SC-MLI, as presented in [32], [45], and [86], is adopted. Having taken a ternary asymmetric pattern for two involved input dc sources into account, some 17L SC-based inverters using ten power switches are proposed in [45], [47], and [49], while through a quinary asymmetric-based design, 49-level (49L) output voltage with 12 power switches is developed in [32]. With a quaternary asymmetric adjustment of two input dc sources and using the generalized concept of SCCs, three different SC-MLI topologies with 31-level (31L) output voltage are proposed in [49], [162], and [163], while 14, 16, and 14 power switches are utilized, respectively. Reduced number of ON-state power switches with a reduction in the total number of required power switches and the overall value of the TSV index across the switches are three important items that can be improved by this type of circuit architecture in comparison to the cascaded version of SC-MLIs.

Taking the advantage of this novel/developed H-bridge and using series-connected SPSC Unit-I in left- and right-hand sides, a generalized multiport SC-MLI with asymmetric adjustment of the integrated dc sources is developed in [73]. This circuit architecture is depicted in Fig. 27(b), and apart from the novel/developed H-bridge as the polarity inverting cell and SPSC units, it needs several four-quadrant power switches in both the left- and right-hand sides as well as to transfer the created voltages of the SPSC units to the output. Considering $V_{\mathrm{dc},L}$ and $V_{\mathrm{dc},R}$ as the magnitude of all the input dc sources in left- and right-hand sides of the circuit, respectively, the condition of $V_{\mathrm{dc},L} = (2n+1)V_{\mathrm{dc},R}$ must be fulfilled to obtain $(8n^2+8n+1)$ levels of the output voltage. Here, "n" is the number of SPSC units employed in each side. Through this circuit configuration, the p.u. index of TSV is 5.5.

By integrating the basic unipolar SC units/generalized SCCs into other types of multiple-input-dc-source MLIs, many new topologies of SC-MLIs with different circuit characteristics have been widely investigated [5]. In this regard, six other notable topologies of double-port-based SC-MLIs presented in [79], [81], [83], [84], [85], and [89] are illustrated in Fig. 28(a)–(f), respectively. As can be seen from Fig. 28(a), in [79], an SC-integrated FB cell is used, while the voltage across C_{FC} is balanced at the left-hand-side input dc-source value. With a ternary pattern of the input dc-source magnitudes as $V_{\mathrm{dc},R} = 3V_{\mathrm{dc},L}$, 11L of the output voltage can be achieved, whereas this structure is also able to work with a binary pattern as $V_{\mathrm{dc},L} = 2V_{\mathrm{dc},R}$ to attain the same number of output voltage levels. Herein, Iqbal *et al.* [80] use a similar technique but with the integration of T/NPP cell instead of switches S and $\bar{S}$ in the current FB cell. Therefore, through the symmetric magnitude of the input dc sources, a 13L output voltage is obtained, while with a quaternary asymmetric pattern as $V_{\mathrm{dc},L} = 4V_{\mathrm{dc},R}$, a 19L inverter is achieved. The presented topology in [79] can also be extended if the same FB cell is to be adopted in the right-hand side of the circuit, as well. This topology is proposed in [80], while with a symmetric pattern of the input dc sources and 16 power switches, a 9L output voltage can be seen. Through a ternary asymmetric pattern as $V_{\mathrm{dc},L} = 3V_{\mathrm{dc},R}$, a 17L inverter can also be made.

Considering Fig. 28(b), double-port SC-MLIs can also be constructed using a series connection of different basic SC units, while a 9L output voltage is achieved using nine power switches and a ternary asymmetric pattern for the input dc-source magnitudes [81]. A 7L variant of this topology is also proposed in [82], while only one SC-based basic unit is employed. Alternatively, Arif *et al.* [83] have combined a modified SPSC unit in the left-hand side and a T/NPP cell in the right-hand side of the main double-port SC-MLI, as shown in Fig. 28(c). Herein, capacitor, C_3, in the left-hand side of the circuit is charged to the voltage of $V_{\mathrm{dc},L}$, while similar to any types of T/NPP cell, both capacitors C_1 and C_2 are charged to half value of the right-hand-side input dc-source voltage magnitude, $V_{\mathrm{dc},R}$. In this case, an asymmetric 17L inverter is made as long as the condition of $2V_{\mathrm{dc},L} = 3V_{\mathrm{dc},R}$ is to be fulfilled. Herein, 12 power switches are used, while the p.u. index of TSV for the involved switches is 4.5 with 1.6 times output voltage conversion gain.

In the following, the concept of using two HB legs and dc-link capacitors connected within an NPP configuration has been combined to rehearse another version of double-port SC-MLI, as shown in Fig. 28(d) [84]. This topology can generate 21-level (21L) output voltage using two asymmetric input dc sources with the condition of $V_{\mathrm{dc},R} = 4V_{\mathrm{dc},L}$. Through the parallel connection of each of the dc-link capacitors to their respective input dc source, they can be charged to $V_{\mathrm{dc},R}$ and $V_{\mathrm{dc},L}$. Hence, the overall

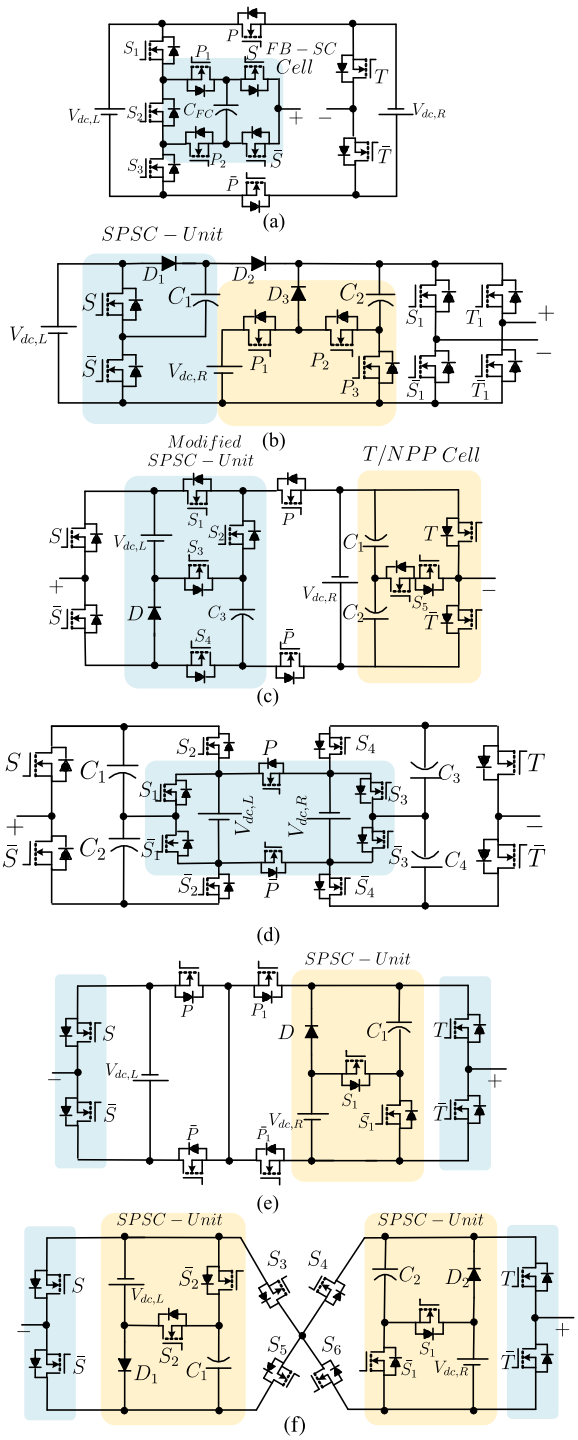

Fig. 28. Double-port SC-MLIs. (a) 11L inverter [79]. (b) 7L inverter [81]. (c) 17L inverter [83]. (d) 21L inverter [84]. (e) 15L inverter [85]. (f) 25L inverter [89].

voltage conversion gain of the converter is double, while 14 power switches are employed. Similar to the single dc-source SC-MLIs, the HB-leg switches are operated within a line frequency, while eight out of 14 power switches of this structure are involved in the capacitor charging loops. The generation of all the desired output voltage levels without recruiting any power diodes makes sense since bidirectional power flow operation can also be possible.

In contrast, the most recent improvement of double-port SC-MLIs using a simple SPSC integrated unit is proposed in [85], as shown in Fig. 28(e). Unlike the previously discussed topologies, this structure uses only two line-frequency HB legs highlighted with a blue color, as shown in Fig. 28(e), to realize different output voltage levels. Through a ternary pattern for two input dc sources, i.e., $V_{\mathrm{dc},R} = 3V_{\mathrm{dc},L}$, 15 levels (15L) of the output voltage are achieved utilizing ten power switches. Obviously, by the integration of other SC-based basic units in both the right- and left-hand sides of the input dc sources, the number of output voltage levels could have been increased more; however, Sarebanzadeh *et al.* [85] have recommended a cascaded technique to realize this feature. The total TSV index of the switches in the p.u. scale for this topology is 8.5, while its overall voltage conversion gain is 1.75. In this case, only two switches, i.e., P_1 and $\bar{P}_1$, must tolerate $7V_{\mathrm{dc}}$ as MVS.

Finally, the last structure from the double-port SC-MLIs family is a 25-level (25L) inverter shown in Fig. 28(f) [89]. As can be seen, the topology is constructed based on two integrated SPSC Units-I with two asymmetric input dc sources and 12 power switches. Excluding four switches used in SPSC units, the rest of switches are not in capacitor charging loops. To attain the maximum possible number of output voltage levels, the input dc sources must be asymmetrically designed as $V_{\mathrm{dc},R} = 5V_{\mathrm{dc},L}$. Similar to the previous case studies, the number of output voltage levels is further enhanced using the cascaded connection. It is worth noting that multiple-input-dc-source SC-MLIs with more than two symmetric or asymmetric dc sources can also be constructed using some hybrid techniques. In this case, the level-generator units can be adopted using any types of main multilevel submodule introduced in [5]. Then, through the cascaded connection of these submodules to an SC-integrated FB-based cell, the number of output voltage levels is enhanced, while the resultant SC-MLI can offer a voltage-boosting feature. An example of this circuit architecture has been presented in [87], while 15L/double-output-voltage-gain inverter is achieved using three symmetric input dc sources and one floating capacitor. A generalized version of multiport dc-source SC-MLIs to incorporate more number of symmetric dc sources and to realize a larger number of output voltage levels for HF applications with the same hybrid approach has also been investigated in [90].

In order to compare the circuit characteristics of different aforementioned double-port SC-MLIs, Table III can be considered. Herein, only the asymmetric-based topologies that are able to generate the largest number of output voltage levels are taken into account. The type of all the included topologies in Table III is based on either novel/developed H-bridge or any other techniques except the cascaded connection. Since any of the previously discussed single dc-source SC-MLIs can work as two- or multiport SC-MLIs through the cascaded connection, this type of circuit architectures has not been included in Table III. The comparable indexes are the same as what presented for the single dc-source SC-MLIs; however, the relationship between the magnitudes of the input dc sources has also been included in Table III to better realize the effectiveness

TABLE III
COMPARATIVE STUDY OF DIFFERENT SC-MLIs WITH TWO ASYMMETRIC DC SOURCES

Presented SCMLI	No. of Components				No. of Levels/ THD	Overall Voltage Gain/ Caps Voltage	Max No. of ON-Switches	Max No. of Switches in Charging Path	TSV (pu)/ MVS	Asymmetric Amplitude of DC-Sources
	S	D	C	G						
Fig.3 in [32]	18	2	4	14	49/NA	$2/V_{dc}(2), 5V_{dc}(2)$	7	4	$6/24V_{dc}$	V_{dc} and $5V_{dc}$
[45], [47] and [49]*	10	2	2	10	17/NA	$2/V_{dc}, 3V_{dc}$	5	2	$6/8V_{dc}$	V_{dc} and $3V_{dc}$
[47] with Fig. 13(a) SCC	16	4	4	16	49/NA	$4/V_{dc}, 2V_{dc}, 3V_{dc}, 6V_{dc}$	8	4	$6/24V_{dc}$	V_{dc} and $3V_{dc}$
Fig. 12 in [49]	14	2	4	14	31/NA	$4/V_{dc}(2), 4V_{dc}(2)$	7	4	$5.5/15V_{dc}$	V_{dc} and $4V_{dc}$
[79]-Mode I	11	0	1	11	11/NA	$1.25/V_{dc}$	5	4	$4.2/4V_{dc}$	V_{dc} and $3V_{dc}$
[79]-Mode II	11	0	1	11	11/9.3%	$1.67/2V_{dc}$	5	4	$4.4/2V_{dc}$	V_{dc} and $2V_{dc}$
[80]-First Structure	13	0	2	12	19/8.9%	$1.8/4V_{dc}(2)$	7	4	$4.89/9V_{dc}$	V_{dc} and $4V_{dc}$
[80]-Second Structure	16	0	2	16	17/NA	$2/V_{dc}, 3V_{dc}$	9	8	$4.5/8V_{dc}$	V_{dc} and $3V_{dc}$
[80]-Third Structure	18	0	3	17	29/NA	$2/V_{dc}(2), 2.5V_{dc}$	10	8	$4.64/14V_{dc}$	V_{dc} and $2.5V_{dc}$
[80]-Fourth Structure	20	0	4	18	49/NA	$2/V_{dc}(2), 5V_{dc}(2)$	10	8	$5/24V_{dc}$	V_{dc} and $5V_{dc}$
Fig. 1 in [83]	12	1	3	11	17/4.8%	$1.6/2V_{dc}, 1.5V_{dc}(2)$	6	3	$4.5/8V_{dc}$	$2V_{dc}$ and $3V_{dc}$
Fig. 1 in [84]	14	0	4	14	21/4.3%	$2/V_{dc}(2), 4V_{dc}(2)$	7	8	$5/10V_{dc}$	V_{dc} and $4V_{dc}$
Fig. 1 in [85]	10	1	1	10	15/4.7%	$1.75/V_{dc}$	5	1	$8.5/7V_{dc}$	V_{dc} and $3V_{dc}$
Fig.1 in [89]	12	2	2	12	25/1.8%	$2/V_{dc}, 5V_{dc}$	7	4	$10/10V_{dc}$	V_{dc} and $5V_{dc}$
[162] with Fig. 13(f) SCC	16	0	4	16	31/NA	$3/V_{dc}(2), 4V_{dc}(2)$	7	3	$5.6/15V_{dc}$	V_{dc} and $4V_{dc}$
[163] with Fig. 13(g) SCC	14	2	4	14	31/NA	$3/V_{dc}(2), 4V_{dc}(2)$	7	4	$6/15V_{dc}$	V_{dc} and $4V_{dc}$
[163] with Fig. 13(g) SCC	18	2	6	18	49/NA	$4/V_{dc}(3), 4V_{dc}(3)$	7	4	$7.25/24V_{dc}$	V_{dc} and $4V_{dc}$

*Based on [45, Fig. 7], [45, Fig. 6], and [49, Fig. 2].

of each topology in terms of the input dc-source magnitude. Owing to inadequate data reported in the literature, the overall efficiency of these types of SC-MLIs has not been included in Table III. As can be deduced from this table, the reduced number of required switching devices to realize a large number of output voltage levels is the interesting feature of these multiport SC-MLIs; however, their power density may be a prime shortcoming, since to achieve this goal, different values of asymmetric input dc sources are needed. Considering Table III, the 49L asymmetric SC inverter presented in [32] possesses better option than others in terms of the ratio between the number of output voltage levels and the number of required power switches. In addition, from the minimum number of capacitors' charging path switches and the number of required capacitors with respect to the overall voltage gain viewpoint, the recently proposed 15L SC inverter in [85] offers an optimized option.

C. Mid-Point-Clamped SC-MLIs

Owing to the utilization of different numbers of HB legs in the aforementioned single- and multiple-dc-source SC-MLIs to invert the SC unit/generalized SCC output voltage polarity, high-frequency variable CMV is one of the serious concerns, which hinders their applications, e.g., grid-tied PV systems. Mid-point-clamped MLIs are enumerated as a popular choice in this case since they are based on dc-link neutral-balanced capacitors, and their output voltage is measured with respect to this neutral point. Therefore, the leakage current concern in grid-tied PV applications can be considerably mitigated, while a multilevel output voltage waveform is provided by a single input dc source [169]. These types of MLIs can also be extended to a three-phase circuit design with the same dc-link capacitors. An example of this type of SC-MLIs is shown in Fig. 29, where the converter is designed based on a front-end T/NPP cell and several SC-integrated FB cell in series. Similar to the presented SC-MLI in [60], four-quadrant power switches or RB-IGBT are needed to connect different SC-based basic units to each other.

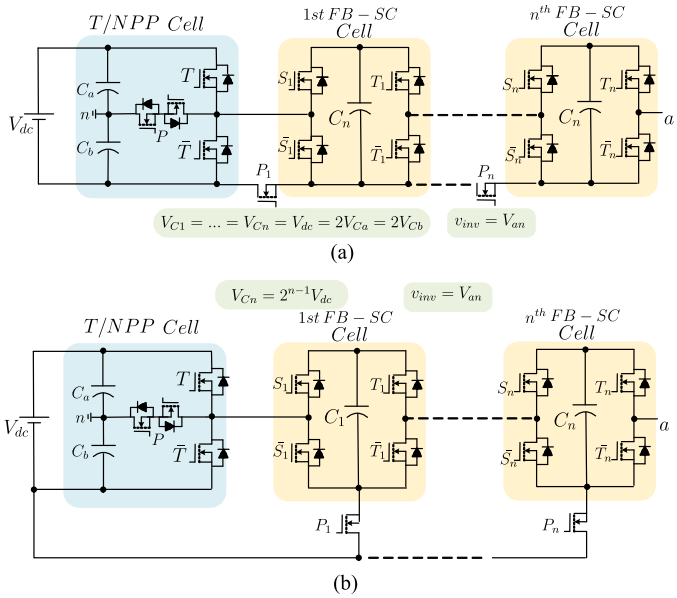

Fig. 29. Mid-point-clamped SC-MLI presented in [92]. (a) With symmetric charging operation of all the capacitors. (b) With asymmetric charging operation of all the capacitors [93].

Liu *et al.* [93] propose two different configurations based on the symmetrical and asymmetrical charging operations of the capacitors. Considering Fig. 29(a), all the capacitors in the SC-integrated FB cells can be charged symmetrically to the input dc source. Through this technique and with the use of one SC-integrated FB cell, a 7L mid-point-clamped inverter can be obtained, in which its overall voltage gain is 1.5, and it requires nine active power switches. A similar approach is also used in [61] to realize the same number of output voltage levels. Regarding Fig. 29(b), the capacitors in the SC-integrated FB cells can be charged asymmetrically, as well. Hence, considering "n" SC-integrated FB cells, the voltage balancing pattern of the capacitors can be written as $V_{C_n} = 2^{n-1}V_{\rm dc}$. Therefore, with $5n + 4$

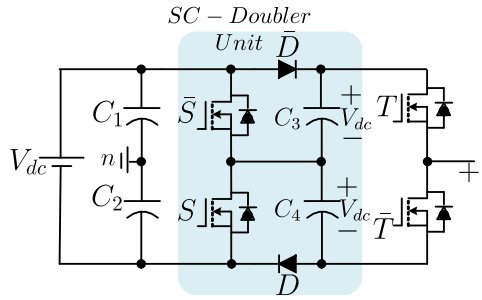

Fig. 30. 4L mid-point-clamped SC inverter [28], [94].

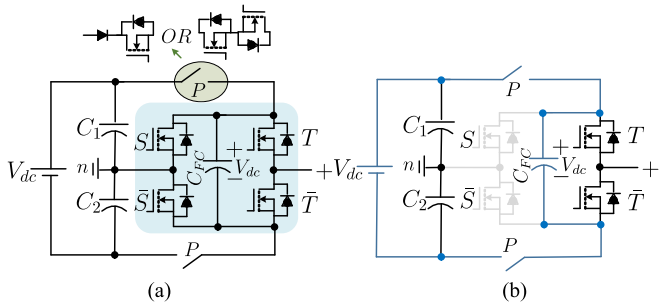

Fig. 31. 5L mid-point-clamped SC-based inverter [95], [96]. (a) Main circuit architecture. (b) Charging path of the FC capacitor.

power switches, $2^{n+2}-1$ number of output voltage levels are obtained, whereas in the symmetrical charging design, this number is $4n+3$. Through almost the same circuitry concept, Lin *et al.* [92] have developed another version of mid-point-clamped generalized SC-MLI with a symmetrical charging operation of the integrated capacitors, while more numbers of power switches are used.

The integration of the SC voltage doubler unit into a mid-point-clamped four-level (4L) inverter has also been introduced in [28] and [94], while single- and three-phase designs of the converter are the target, respectively, as shown in Fig. 30. A unity ratio between the number of inverter output voltage levels and the number of required switches and a single-stage 1.5 times overall voltage conversion gain are two important features of this topology.

Conventional mid-point-clamped MLIs, such as active-neutral point-clamped (ANPC), have a limited performance in terms of full dc-link voltage utilization. The active boost neutral point-clamped (ABNPC)-based MLI presented in [95] and [96] have improved this shortcoming using the SC incorporation technique. This structure with the SC charging flow path is shown in Fig. 31, while 5L output voltage with six power switches and unity voltage conversion gain is achieved. Here, the SC-integrated switches designated as P can be either RB-IGBT or four-quadrant power switch. Similar to [28] and [94], C_{FC} is charged to the main dc-link voltage during the middle-output-voltage-level generation. A similar technique but with two more power switches has also been conceptualized in [97], as well. Following this, to reduce the voltage stress across C_{FC}, Lee *et al.* [98] have proposed another unity-gain 5L mid-point-clamped inverter with ten power switches, as shown in Fig. 32.

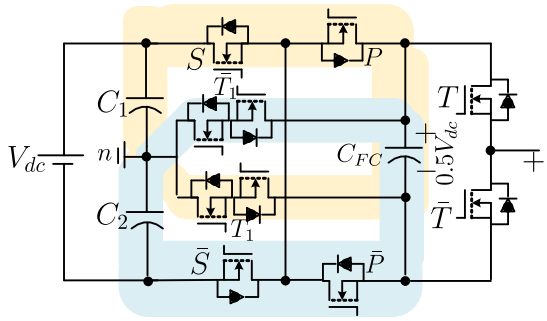

Fig. 32. 5L mid-point-clamped SC-based inverter [98].

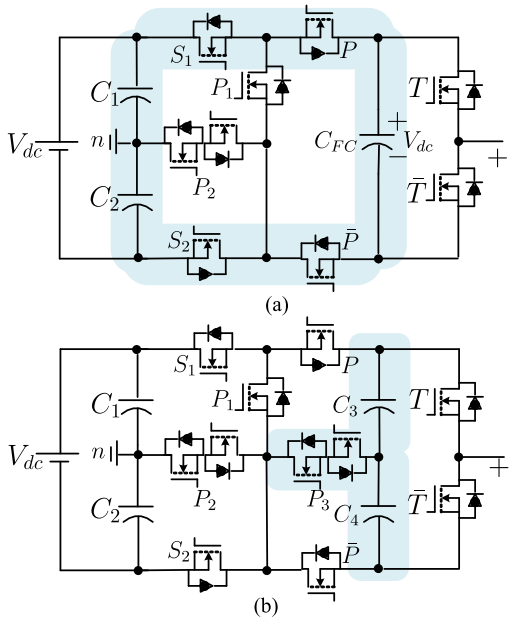

Fig. 33. (a) 7L mid-point-clamped SC-based inverter presented in [99]. (b) Dual T-type 9L/11L mid-point-clamped inverter [99].

In this case, two RSSs for charging operation of C_{FC} to half value of the main dc-link voltage are provided. Hence, some hybrid modulation-based techniques discussed in Section V can be adopted to further reduce the size of this SC network capacitor. To extend the number of output voltage levels as well as the overall voltage gain of the converter, Lee *et al.* [99] have proposed two different circuit configurations for the mid-point-clamped SC-MLIs. The first structure is illustrated in Fig. 33(a). C_{FC} is balanced at the input dc-source voltage through the highlighted current flowing path, as shown in Fig. 33, while the number of inverter output voltage levels is seven with 1.5 times overall voltage conversion gain. Replacing C_{FC} and the HB leg with a T/NPP cell constitutes to 9L and 11L inverters with unity and 1.5 times voltage conversion gain, respectively [99]. This structure is shown in Fig. 33(b), while additional capacitors in T/NPP cells are charged to half voltage value of the main dc-link voltage. The same technique is employed in [109] and [110] to realize a 9L inverter output voltage with unity voltage conversion gain. The concept of adding T/NPP cell to any conventional types of ANPCs to achieve a larger number of output voltage levels with

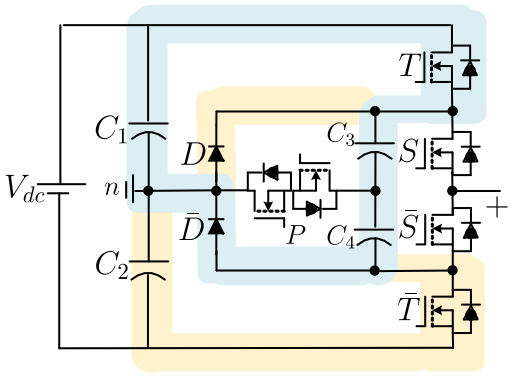

Fig. 34. 5L mid-point-clamped SC-based inverter [102].

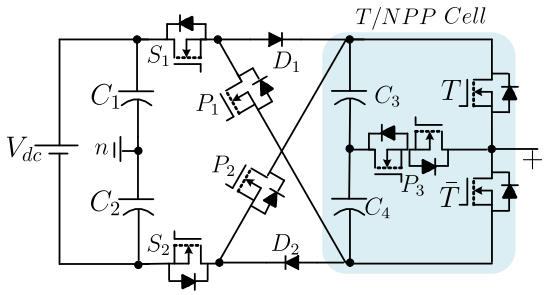

Fig. 35. 7L mid-point-clamped SC-based inverter [112].

full dc-link utilization is also introduced in [100] and [101]. An example of this technique is shown in Fig. 34, where two capacitors, C_3 and C_4, with a four-quadrant power switch, P, are inserted into the conventional 3L NPC-based inverter, and five output voltage levels are achieved [102]. Regarding the blue and yellow highlighted colors in Fig. 34, it can be discerned that these two added capacitors are charged to the voltage across C_1 or C_2 through the integration of the existing diodes and the switches T and $\bar{T}$. In contrast, instead of T/NPP cell and the back-end HB leg used in Fig. 33(b), an SC-integrated FB cell is used in [104]–[106]. Similarly, C_{FC} employed in this SC-integrated FB cell is charged to the main dc-link voltage. Hence, a 7L mid-point-clamped inverter with 1.5 times voltage conversion gain and nine power switches is introduced. This technique with ten power switches and the same number of output voltage levels and the same gain is also developed in [107]–[109]. In the following, another reduced switch-count mid-point-clamped SC-MLI with the capability of 7L output voltage generation and 1.5 times voltage conversion gain is proposed in [112] and [113], as shown in Fig. 35. As can be seen, apart from a T/NPP cell, two cross-connected switches, P_1 and P_2, are also used to transfer the charged voltages of C_3 and C_4, which are balanced at half voltage value of the main dc link, to the output. These two switches are not in the charging path of the capacitors, and only eight power switches with two additional power diodes are incorporated to realize a 7L output voltage. The same technique but with the help of an SC-integrated FB cell is also used in [103]. Although C_{FC} in that structure must be charged at full dc-link voltage, the topology can generate 7L output voltage with eight power switches and without involving

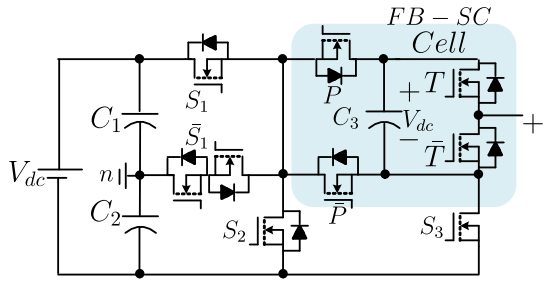

Fig. 36. 7L mid-point-clamped SC-based inverter [117].

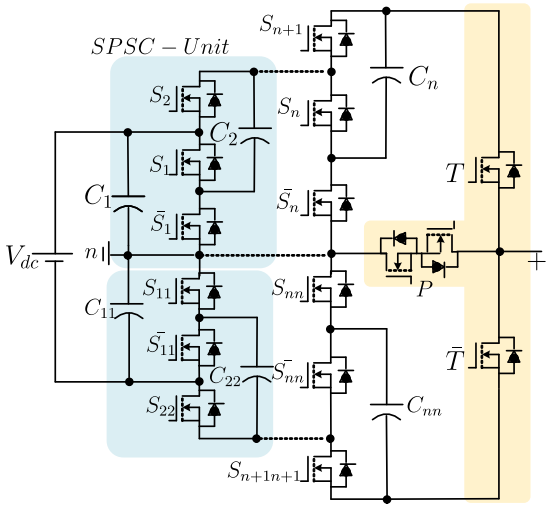

Fig. 37. Generalized mid-point-clamped SC-MLI [118].

any power diodes. Hence, bidirectional power flow operation is possible. The presented topology in [112] and [113] using T/NPP cell has a better overall TSV profile than its counterpart in [103]. In this regard, Sathik *et al.* [114] use the same circuit architecture as shown Fig. 35 but with the incorporation of HB legs rather than the mid-point-clamped one. Hence, 9L output voltage with double voltage conversion gain is achieved, however, at the expense of increased HF-CMV and leakage current. Following this, Siddique *et al.* [115] have removed the T/NPP cell of Fig. 35 and used a single capacitor charged from the main dc-link voltage. The same technique with the integration of SPSC Unit-I is used in [115]. Again, by the incorporation of HB legs, two different single-input-dc-source 7L SC-based inverters with 1.5 times and two times voltage conversion gain are attained for the presented structures in [115] and [116], respectively. The 7L mid-point-clamped inverter presented in [117] and shown in Fig. 36 is another version of this type of topologies, while it uses one extra RB-IGBT switch in comparison to its eight-switch-based 7L mid-point-clamped counterpart.

The generalized SC-based mid-point-clamped MLI presented in [118] is a recent proposed version of ABNPCs and is illustrated in Fig. 37. A modified SPSC Unit-I with the integration of a switch instead of diode and an ideal T-type cell have been used here, while Dhara *et al.* [119] have used the exact model of SPSC Unit-I to generate 5L output voltage with a unity voltage conversion gain. The capacitors in all the SPSC

TABLE IV
COMPARATIVE STUDY OF DIFFERENT MID-POINT-CLAMPED SC-MLIS

Type of SCMLI	No. of Components				No. of Levels/ THD	Overall Voltage Gain/ Caps Voltage	Max No. of ON-Switches	Max No. of Switches in Charging Path	TSV (pu)/ MVS	Reported Rated Efficiency
	S	D	C	G						
Sym SC [61], [93]	9	1	3	8	7/12.2%	$1.5/V_{dc}(1),0.5V_{dc}(2)$	4	3	$5/V_{dc}$	97%@150W
Asym SC [93]	12	2	4	11	15/5.5%	$1.5/V_{dc}(1),0.5V_{dc}(2),\ 2V_{dc}(1)$	7	7	$5/2V_{dc}$	97%@150W
Ref [28], [94]	4	2	4	4	4/41.4%	$1.5/V_{dc}(2),0.5V_{dc}(2)$	2	2	$2.66/1.5V_{dc}$	97%@1kW
ABNPC [95], [96]	6	2	3	6	5/NA	$1/V_{dc}(1),0.5V_{dc}(2)$	3	2	$5/V_{dc}$	98.5%@1.2kW
ABNPC [97]	8	0	3	8	5/NA	$1/V_{dc}(1),0.5V_{dc}(2)$	4	4	$6/V_{dc}$	NA%@1.2kW
ABNPC [98]	10	0	3	8	5/NA	$1/0.5V_{dc}(3)$	5	6	$6/0.5V_{dc}$	NA%@50W
ABNPC [99]	9	0	3	8	7/NA	$1.5/V_{dc}(1),0.5V_{dc}(2)$	4	4	$5.33/V_{dc}$	96%@50W
Dual T-Type [99]	12	0	3	10	9/NA	$1/V_{dc}(2),0.5V_{dc}(2)$	6	6	$10/V_{dc}$	96%@50W
ABNPC [102]	6	2	4	5	5/NA	$0.5/0.5V_{dc}(2),0.25V_{dc}(2)$	3	2	$6/0.5V_{dc}$	97.5%@800W
ABNPC [103]	8	0	3	8	7/NA	$1.5/V_{dc}(1),0.5V_{dc}(2)$	3	2	$7.3/V_{dc}$	96%@800W
ANPC [104]–[106]	9	0	3	8	7/19.3%	$1.5/V_{dc}(1),0.5V_{dc}(2)$	5	4	$5.3/V_{dc}$	96.7%@250W
ABNPC [107]	10	0	3	9	7/NA	$1.5/V_{dc}(1),0.5V_{dc}(2)$	5	4	$6.6/V_{dc}$	96%@450W
Dual T-Type [108]	10	0	4	8	7/NA	$1.5/V_{dc}(2),0.5V_{dc}(2)$	3	4	$7.33/2V_{dc}$	98%@100W
ABNPC [109]	10	0	4	8	7/NA	$1.5/V_{dc}(2),0.5V_{dc}(2)$	5	4	$6.66/V_{dc}$	97%@100W
ABNPC [110]	10	4	4	9	9/NA	$1/0.25V_{dc}(2),0.5V_{dc}(2)$	5	5	$5/0.5V_{dc}$	97%@500W
ABNPC [111]	11	4	3	10	9/NA	$2/V_{dc}(2),0.5V_{dc}(2)$	5	3	$10/2V_{dc}$	98%@400W
ABNPC [112]	8	2	4	7	7/NA	$1.5/V_{dc}(2),0.5V_{dc}(2)$	5	3	$4.66/V_{dc}$	97.8%@400W
ABNPC [113]	10	2	2	9	9/4.1%	$2/0.5V_{dc}(2)$	5	2	$5/V_{dc}$	97.1%@400W
ABNPC [117]	8	1	3	7	7/NA	$1.5/V_{dc}(1),0.5V_{dc}(2)$	4	3	$5.33/V_{dc}$	NA
ABNPC [118]	10	0	4	9	5/NA	$1/0.5V_{dc}(4)$	5	4	$7/1.5V_{dc}$	NA%@160W
ABNPC [119]	8	2	4	7	5/NA	$1/0.5V_{dc}(4)$	5	4	$6/1.5V_{dc}$	97.1%@1kW
ABNPC [120]	6	4	5	6	6/20.2%	$2.5/0.5V_{dc}(2),V_{dc}(3)$	3	4	$4.4/3V_{dc}$	95.8%@450W

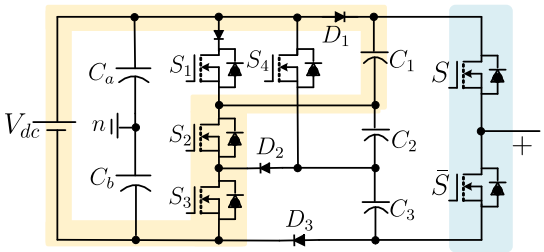

Fig. 38. 6L mid-point-clamped SC-based inverter [120].

stages are charged to the main dc-link voltage, $0.5V_{\rm dc}$, using the well-known series–parallel operation. Hence, considering "n" as the number of SPSC units, the maximum value of the inverter output voltage is $0.5(n+1)V_{\rm dc}$, which can perfectly reflect the voltage-boosting feature of the converter. The number of required power switches in this generalized structure is $6n+4$, while the maximum number of output voltage levels is $2n+3$ with $2n+2$ capacitors.

Taking the recent advances of these mid-point-clamped SC-MLIs into account, another six-level (6L) SC-based topology with 2.5 times static voltage conversion gain and using only six power switches has been proposed in [120]. This structure is shown in Fig. 38, and apart from power switches, it is comprised of five dc-link capacitors with four extra power diodes. Herein, capacitors C_1, C_2, and C_3 are inside the SC network, and they are clamped at $V_{\rm dc}$ with a parallel connection to the input dc source. The charging path of one of these dc-link capacitors has been highlighted with a yellow color in Fig. 38, while to convert the boosted voltage of the SC network to the output, a standard HB leg shown with blue color is used. The reduced number of required semiconductor devices with an improved TSV index is the main circuitry feature of this topology. Although it cannot produce the zero-level output voltage, its maximum number of ON-state power switches at each switching instant is only three, while four out of six switches placed in the SC network must tolerate the largest current stress caused by the parallel charging operation of the capacitors. Table IV has compared all the aforementioned mid-point-clamped SC-MLIs with each other in various previously introduced aspects. Considering this, the presented 6L mid-point-clamped SC-based inverter in [120] has the best circuit characteristics in terms of voltage conversion gain and overall TSV index. Conversely, Liu *et al.* [93] can create the largest number of output voltage levels with a reduced ratio between the number of required power switches and the number of output voltage levels, but at the cost of the largest number of capacitive charging loop switches. From the latter aspect, the 7L mid-point-clamped inverter in [103] has the optimum condition since only two switches are involved in the charging path of the capacitors. Except the structures presented in [93] and [118], all the highlighted topologies suffer from the lack of generalization capability to realize a larger number of inverter output voltage levels.

D. CGSC-Based MLIs

The mid-point-clamped MLIs can considerably reduce the unwanted value of the leakage current for transformerless grid-tied PV applications. HF-CMV in the mid-point-clamped MLIs is given by the voltage of dc-link capacitors. To mitigate the CMV completely, CGSC-based MLIs have recently been proposed, where the ground of the input dc source and neutral point of the grid or the load are directly connected to each other. Hence, no leakage current can be propagated through the system since the parasitic capacitance appearing between the negative terminal of the input dc source such as PV panels and the ground can see a grounded potential rather than a variable HF-CMV [170]–[172]. This type of converter is also named as three-port single-dc-source inverter or doubly grounded transformerless inverter,

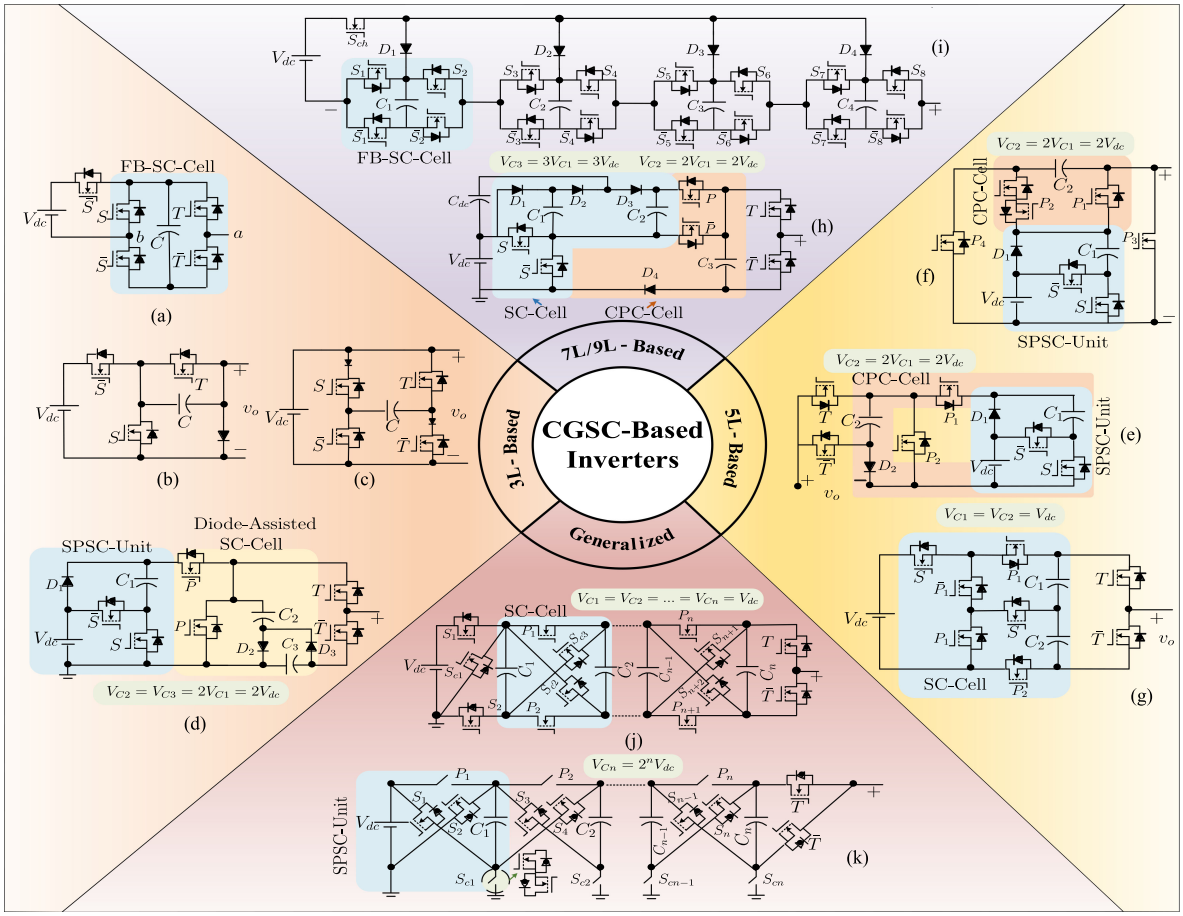

Fig. 39. CGSC-based inverters. (a)–(d) 3L inverters [121], [122], [124]. (e)–(g) 5L inverters [127]–[129]. (h) 7L inverter [136]. (i) 9L inverter [139]. (j) and (k) Generalized symmetric and asymmetric inverters [140], [141].

where the utilization of SC technique/charged-pumped circuit (CPC) cell is an imperative choice since the negative output voltage levels of the inverter must be generated indirectly through a virtual dc-link capacitor.

Well-known CGSC-based inverters that have been recently rehearsed are shown in Fig. 39. Considering Fig. 39(a), a 3L CGSC-based inverter using five power switches and a virtual dc-link capacitor are proposed in [121], where the capacitor, C, is charged to the input dc source, $V_{\rm dc}$, during the positive and zero levels of the output voltage, and in turn, it would be discharged during the negative output voltage generation. The number of switching devices for this type of 3L CGSC-based inverter is reduced through the presented $Siwakoti$-H inverters in [122], as shown in Fig. 39(b) and (c), while an extra diode has been used in Type-I of this converter and two RB-IGBTs are used in its Type-II variant. Another 3L four-switch-based CGSC-based inverter is proposed in [123], while the virtual dc-link capacitor is charged indirectly to $V_{\rm dc}$ through a diode-assisted CPC cell. The common feature among all these mentioned 3L CGSC-based inverters is their unity voltage conversion gain. Having taken Fig. 39(d) into account, a double-voltage-conversion-gain 3L CGSC-based inverter is proposed in [124], while six power switches, a diode-assisted CPC cell, and SPSC Unit-I are employed. Here, C_2 and C_3 are charged to $2V_{\rm dc}$, which is the boosted voltage value of frond-end SPSC Unit-I. In this context, two other similar boost-based topologies of 3L CGSC-based inverters are also proposed in [125] and [126] with more number of power switches and elevated switch voltage stress.

Consequently, Fig. 39(e)–(g) shows three different CGSC-based inverter configurations, which are able to generate 5L double voltage conversion gain output using six power switches [127]–[129], seven power switches [132], [144], and eight power switches [135], respectively. Ardashir *et al.* [145] have recently introduced a 5L CGSC-based inverter, which comprises six power switches. Although it has used a similar virtual dc-link SC technique to create the negative output voltage levels, its overall voltage conversion gain is unity. As for the presented topologies in [127]–[129], [132], and [144], capacitor C_2 acts as a virtual dc-link source, which is required to be charged to the peak voltage of the inverter, $2V_{\rm dc}$, through the series connection of the input dc source and the capacitor, C_1. This charging operation can be realized during the zero and top positive output voltage level generation, which might be troublesome in terms of voltage ripple attenuation of C_2 during the switching process. In these cases, the circuit feature of the inverter structure presented in [135] is slightly different than others. It offers a generalized concept to realize a larger number of output voltage levels, it does not use any power diodes, and both of its involved capacitors

TABLE V
COMPARATIVE STUDY OF DIFFERENT CGSC-BASED MLIS

Type of SCMLI	No. of Components				No. of Levels/ THD	Overall Voltage Gain/ Caps Voltage	Max No. of ON-Switches	Max No. of Switches in Charging Path	TSV (pu)/ MVS	Reported Rated Efficiency
	S	D	C	G						
Ref [127]–[129]	6	2	2	6	5/NA	$2/V_{dc}(1),2V_{dc}(1)$	3	2	$4.5/2V_{dc}$	98.1%@600W
Ref [130]	7	2	2	7	5/NA	$2/V_{dc}(1),2V_{dc}(1)$	4	3	$6/2V_{dc}$	96%@40W
Ref [131]	8	1	2	6	5/35.4%	$2/V_{dc}(2)$	5	5	$5/2V_{dc}$	98%@600W
Ref [132], [144]	7	2	2	6	5/NA	$2/V_{dc}(1),2V_{dc}(1)$	5	4	$5/2V_{dc}$	98%@600W
Ref [133]	8	0	3	7	5/NA	$1/V_{dc}(1),0.5V_{dc}(2)$	5	5	$6.5/V_{dc}$	97.1%NA
Ref [134]	8	1	2	7	5/NA	$2/V_{dc}(1),2V_{dc}(1)$	5	5	$6.5/2V_{dc}$	97.5%600W
Ref [135]	8	0	2	8	5/NA	$2/V_{dc}(2)$	4	6	$5.5/2V_{dc}$	98.3%600W
Ref [23]	9	1	3	7	5/NA	$2/V_{dc}(2),2V_{dc}(1)$	6	6	$5.5/2V_{dc}$	96%@600W
Ref [24]	9	1	2	8	5/NA	$2/V_{dc}(2),2V_{dc}(1)$	6	6	$6/2V_{dc}$	98.5%@1kW
Ref [140]	8	1	2	6	5/36.4%	$2/V_{dc}(1),2V_{dc}(1)$	5	5	$6.5/2V_{dc}$	97.5%600W
Ref [143]	9	0	2	9	5/NA	$2/V_{dc}(2)$	5	4	$6/2V_{dc}$	96.7%1kW
Ref [145]	6	1	2	5	5/NA	$1/0.5V_{dc}(2)$	3	1	$6/V_{dc}$	97%500W
Ref [135]	11	0	2	11	7/NA	$3/V_{dc}(3)$	6	9	$6/3V_{dc}$	98.3%600W
Ref [136]	6	4	4	6	7/NA	$3/V_{dc}(2),2V_{dc}(1),3V_{dc}(1)$	3	3	$6/3V_{dc}$	98%800W
Ref [138]	8	4	3	8	7/NA	$3/V_{dc}(1),2V_{dc}(2)$	3	4	$5.33/3V_{dc}$	NA%1kW
Ref [139]	17	4	4	17	9/NA	$4/V_{dc}(4)$	9	8	$6/4V_{dc}$	NA%275W
Ref [143]	17	0	4	17	9/NA	$4/V_{dc}(4)$	9	8	$6/4V_{dc}$	NA%1kW

need to be charged to a voltage equal to the input dc source. Accordingly, the presented 5L CGSC-based inverters in [130], [131], [133], [134], and [143] are other available topologies in this context, which use more or less the same concept but with a larger number of required power switches. Using SPSC Unit-II with four-quadrant [23] or normal power MOSFETs [24], two similar 5L CGSC-based inverters are developed, in which they can work within two independent modes, i.e., with unity gain (buck mode) and double voltage gain (boost mode) with the same circuit architecture.

Taking Fig. 39(h) into account, another reduced switch-count 7L CGSC-based inverter is presented in [136]. Similar to the aforementioned 5L CGSC-based inverters, this structure is also based on the virtual dc-link concept, where capacitors C_1, C_2, and C_3 are charged to $V_{\rm dc}$, $2V_{\rm dc}$, and $3V_{\rm dc}$, respectively, to synthesize all the 7L inverter output voltages with a triple voltage gain. Although the number of required power switches is only six, it requires four additional power diodes. In this case, the charging path of C_3 is through the series connection of the input dc source and capacitor C_2. Similar to the presented 5L CGSC-based inverters in [127]–[132], this charging operation is possible during the zero and the top positive output voltage level, $+3V_{\rm dc}$, generations. Moreover, the dc-link capacitor $C_{\rm dc}$ is charged and discharged by the load current direction in positive and negative half-cycles of the output voltage. Therefore, these long discharging cycles may demand a larger capacitance for both $C_{\rm dc}$ and C_3 to alleviate the voltage ripple across the capacitors. Considering the advantages of this reduced switch-count CGSC-based inverter, Chen *et al.* [137] have developed a 9L mid-point-clamped inverter with nine power switches, as well. In this case, the front-end SC-based part of the inverter in [136] is combined with the idea used in [92], while a four times voltage conversion gain is achieved. As a counterpart, another 7L CGSC-based inverter with triple voltage conversion gain, eight switches, and four power diodes is proposed in [138], which is based on the series connection of front-end SPSC Unit-I and the SC voltage doubler unit. Although the number of switching devices in this topology is larger than that in [136], i.e., eight versus six, its number of required capacitors is three, while the maximum balanced voltage across them is $2V_{\rm dc}$, which leads to the reduced MVS and TSV indexes of the converter. Alternatively, Jahan *et al.* [139] presented a 9L quadruple-voltage-gain CGSC-based inverter shown in Fig. 39(i), with the SC-integrated FB cells that can even be generalized. Although the number of switching devices in this topology is large, the uniform MVSs across all the FB-cell switches and reduced balanced voltage value of the involved capacitors make it an interesting topology in this regard. Having a long discharging cycle for the capacitors might be a prime shortcoming of this converter since larger values of the capacitance are needed in the case of higher power injection demand.

Concerning Fig. 39(j) and (k), two other generalized CGSC-based MLIs have been proposed in [140] and [141]. Herein, the proposed topology in [140] is based on cross-connected switches, where the voltage across all the involved capacitors is equal to the input dc source in spite of having a voltage-boosting feature. Therefore, this topology is performed based on symmetrical voltage balancing operation of the capacitors. In this case, to achieve n-level output voltage, $(2n-1)$ number of switches are needed. As earlier stated, the presented topology in [135] and shown in Fig. 39(g) can also be generalized with the same symmetrical voltage balancing operation of the capacitors. However, its number of switching devices is much smaller than in [140], i.e., to achieve $(2n+5)$-level output voltage, the number of required power switches is $(3n+8)$, where n is the number of added SC networks inserted in the shown structure of Fig. 39(g). In this regard, Khenari *et al.* [142] presented another version of symmetric generalized CGSC-based MLI, while the solution of cross-connected switching devices with T/NPP-interconnected cells has been merged in each other. To realize $(2n+1)$-level output voltage, Khenari *et al.* [142] need $3n+5$ power switches, where n is the number of capacitors.

TABLE VI
COMPARATIVE STUDY OF DIFFERENT HYBRID MLIS

Type of SCMLI	No. of Components				No. of Levels/ THD	Overall Voltage Gain/ Caps Voltage	Max No. of ON-Switches	Max No. of Switches in Charging Path	TSV (pu)/ MVS	Reported Rated Efficiency
	S	D	C	G						
CGSC-based [146]	6	1	2	6	5/NA	$1/V_{dc}(1),0.5V_{dc}(1)$	3	2	$4/V_{dc}$	95.8%@1.2kW
ABNPC-based [147]	8	2	4	8	7/NA	$1/0.5V_{dc}(2),V_{dc}(1),0.25V_{dc}(1)$	4	3	$5/V_{dc}$	98%@2.2kW
ABNPC-based [148]	10	0	4	8	7/NA	$1/0.5V_{dc}(2),V_{dc}(1),0.25V_{dc}(1)$	5	4	$5.5/V_{dc}$	NA
ABNPC-based [154]	11	0	4	11	7/NA	$0.5/0.5V_{dc}(2),0.33V_{dc}(2)$	5	2	$6/0.5V_{dc}$	NA
HB-based [149]	8	2	3	8	9/NA	$2/V_{dc}(2),0.5V_{dc}(1)$	4	2	$6/2V_{dc}$	96.4%@500W
HBSC-based [150]	11	0	2	11	9/13.5%	$2/V_{dc}(1),0.5V_{dc}(1)$	7	4	$6/V_{dc}$	97.3%@330W
HBSC-based [151]	8	1	2	8	9/NA	$2/V_{dc}(1),0.5V_{dc}(1)$	4	2	$5/2V_{dc}$	96.5%@330W
HBSC-based [152]	8	1	2	8	9/NA	$2/V_{dc}(1),0.5V_{dc}(1)$	4	2	$5.5/2V_{dc}$	96.6%@600W
HBSC-based [153]	12	2	3	12	17/2.7%	$4/V_{dc}(1),2V_{dc}(1),\ 0.5V_{dc}(1)$	6	4	$6.25/4V_{dc}$	95%@800W
HBSC-based [156]	10	0	2	10	9/9.4%	$2/V_{dc}(1),0.5V_{dc}(1)$	6	3	$5.5/V_{dc}$	96.5%@800W
CGSC-based [157]	9	1	3	9	9/NA	$2/V_{dc}(2),0.5V_{dc}(1)$	6	5	$5/2V_{dc}$	97.5%@1.2kW
CGSB-based [158]	9	2	4	9	9/NA	$\frac{2}{1-d}/\frac{V_{dc}}{1-d}(3),\frac{0.5V_{dc}}{1-d}(1)$	5	2	$6.5/\frac{2V_{dc}}{1-d}$	96%700W
CGSB-based [159]	7	2	2	6	5/NA	$2/V_{dc}(1),2V_{dc}(1)$	3	1	$6/2V_{dc}$	97.5%@700W

To asymmetrically charge the voltage of the capacitors with generalized CGSC-based MLIs, Samizadeh *et al.* [141] have proposed another topology shown in Fig. 39(k). This asymmetric topology helps to generate $(2^{n+1}-1)$-level output voltage with $6n$ number of required power switches, where n implies the number of required capacitors. Herein, the binary charging operation of the capacitors leads to generating a larger number of output voltage levels with a larger value of the voltage conversion gain and a reduced number of switching devices. Although the concept is interesting, asymmetrical charging operation of the capacitors in CGSC-based MLIs may be deleterious since the number of RSSs to generate the same levels of the output voltage is reduced, while the voltage ripple performance of the capacitors might be adverse.

A quantitative summary of the aforementioned CGSC-based MLIs has been enlisted in Table VI. Herein, from the number of required power switches and the reduced value of the overall TSV across the switches' viewpoint, the presented CGSC-based MLIs in [74] and [127]–[129] are the best in spite of their unsuitability in delivering high output power ratio due to the long discharging period of the virtual dc-link capacitor. Nonetheless, in terms of the ratio of the balanced voltage value across the capacitors and generalization ability, the CGSC-based MLIs of [135] and [139] possess better condition.

E. Hybrid MLIs

The incorporation of SC-based basic units in different types of MLIs brings some specific merits such as voltage-boosting property in HB-based SC-MLIs, full dc-link utilization in mid-point-clamped-based MLIs, and provision of a virtual dc link in CG-based MLIs. However, their major shortcomings that will be discussed in the next section is related to the large voltage ripple across the capacitors, which leads to large current stress for the capacitive charging loop switches. Moreover, the overall voltage gain of SC-MLIs is static, which can further restrict their applications. Integrating other well-known techniques like FC and/or SB-based concepts into the SC-MLIs can further improve their performances. A few types of hybrid MLIs have recently been introduced so far, in which their details are discussed in following.

In this regard, Grigoletto [146] has merged the virtual dc-link concept of a conventional four-switch based FC leg to realize a 5L inverter with a CG circuit feature, as shown in Fig. 40. In this case, the charging/discharging operation of C_1 is realized in a fully soft fashion using the load current path similar to the FC-based MLIs. However, like other virtual dc-link-based CGSC-based MLIs, C_2 must be charged to peak voltage value of the inverter output voltage, which is equal to $V_{\rm dc}$. Even though using only six power switches, the proposed topology does not provide voltage-boosting feature. Herein, a relay S_P with a parallel resistor, R_P, is used in the charging path of C_2 to attenuate the large charging current at the start-up moment of the operation. The same FC- and SC-based integration concept is developed in [147], which is a 7L mid-point-clamped-based MLI, as shown in Fig. 41. As can be seen from the highlighted current flowing path, capacitor C_3 is charged to $V_{\rm dc}$, while the charging/discharging operation of C_4 is realized in a soft fashion. Generating 7L output voltage with full dc-link utilization and using eight power switches are two main merits of this topology. Having taken the same technique into account, Mhiesan *et al.* [148] have proposed another version of 7L mid-point-clamped inverter, as well, while additional four-quadrant power switches are used in its structure. Alternatively, Wu *et al.* [154] integrated SPSC Unit-II into the conventional ANPC-based MLIs. Owing to this series–parallel operation of SPSC Unit-II, a 7L hybrid topology is introduced. As opposed to the hybrid SC-based MLIs presented in [146] and [147], this structure does not have any skipped output voltage level, which can further improve the inverter output waveform THD.

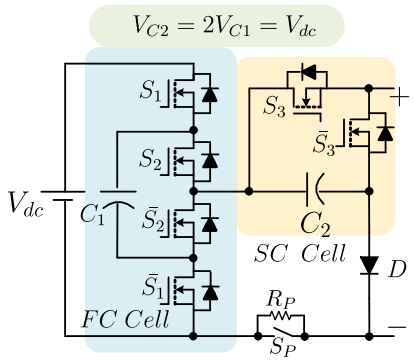

Fig. 40. 5L CGFC/SC-based inverter [146].

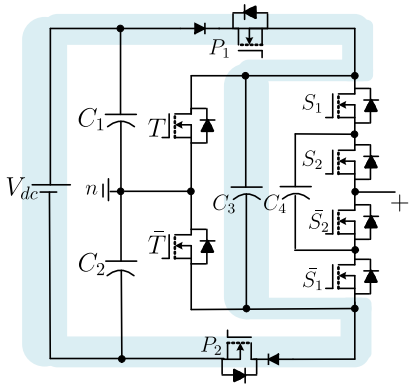

Fig. 41. 7L FC/SC-based mid-point clamped inverter [147].

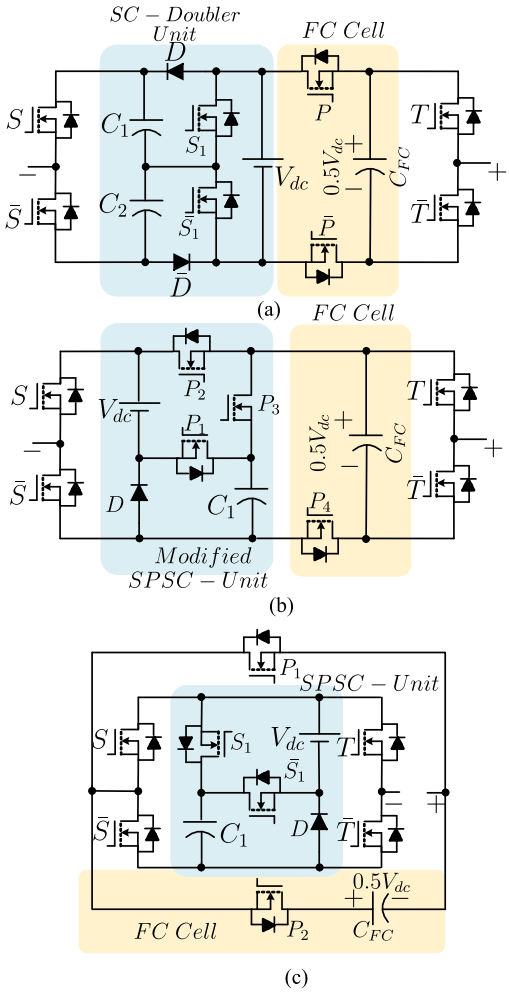

Fig. 42. 9L FC/SC HB-based inverters: (a) [149], (b) [151], and (c) [152].

Hybrid MLIs can also be constructed based on two HB legs, while the static output voltage gain of the converter is enhanced. Fig. 42(a)–(c) shows three different 9L hybrid inverters, which have been presented in [149], [151], and [152], respectively. As can be discerned from Fig. 42(a), an SC voltage doubler unit is used in [149]. This unit with two HB legs can generate up to 5L of the output voltage with double voltage conversion gain.

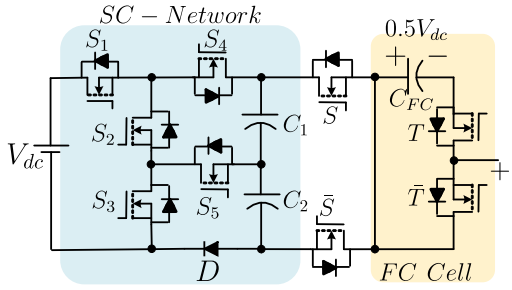

Fig. 43. 9L CGSC/FC-based inverter [157].

Inserting a series FC cell with two complementary switches, P and $\bar{P}$, can create two additional middle output voltage levels of $\pm 0.5V_{\rm dc}$ and $\pm 1.5V_{\rm dc}$. In this case, capacitor $C_{\rm FC}$ is softly charged to $0.5V_{\rm dc}$ through the load current flowing path during the output voltage level generation of $0.5V_{\rm dc}$ and $1.5V_{\rm dc}$, while it is discharged by the reverse direction of the load current in $-0.5V_{\rm dc}$ and $-1.5V_{\rm dc}$ output voltage levels. In this regard, the p.u. scale of TSV for the switches is six, while only two switches shown in the FC cell must tolerate a voltage stress equal to peak of the inverter output voltage, $2V_{\rm dc}$.

Following the same procedure, Naik *et al.* [150] have used the π-type SC network instead of the SC voltage doubler unit. Hence, another 9L hybrid-based inverter is derived using 11 power switches. Concerning Fig. 42(b), the front-end SC network is changed in [151] to a modified version of SPSC-based basic unit with one additional RB-IGBT switch, P_4, while only one switch is used in the FC cell. The working principle of this topology is the same as in [149] and [150], while the TSV index of the switches is reduced to 4.5 with one less power diode. By replacing the power switch P_3 and the power diode D with normal power MOSFETs and using the FC cell of Fig. 42(a), another similar 9L hybrid SC-based inverter with ten power switches and bidirectional power capability has also been introduced in [156]. The same concept has also been developed in [152]. In this case, SPSC Unit-I is used, as can be seen in Fig. 42(c), to generate 9L output voltage with a double voltage conversion gain. Although its number of switches is the same as presented in [151], its p.u. TSV index value is larger than that in [151], i.e., 5.5 with respect to 5. Having taken these SC/FC-based hybrid techniques into account, the front-end SC unit, which is in charge of delivering a multiple-dc-link boosted voltage to the output, can be replaced with any of the generalized SCCs described earlier to develop more number of inverter output voltage levels with a single input dc-source design. Regarding this and considering the binary asymmetrical charging operation of the capacitors described in [45]–[47], a 17L hybrid inverter with quadruple voltage gain and 12 power switches is introduced in [153].

Following this, the inverter in [157] is a newly developed 9L hybrid-based inverter, which has combined the concept of SC network and FC cell with a CG-based circuit architecture. This structure is illustrated in Fig. 43 and is comprised of nine power switches, one power diode, and three self-balanced capacitors. The front-end cell of this hybrid-based inverter is an improved version of the SC network presented in [135], which can promote

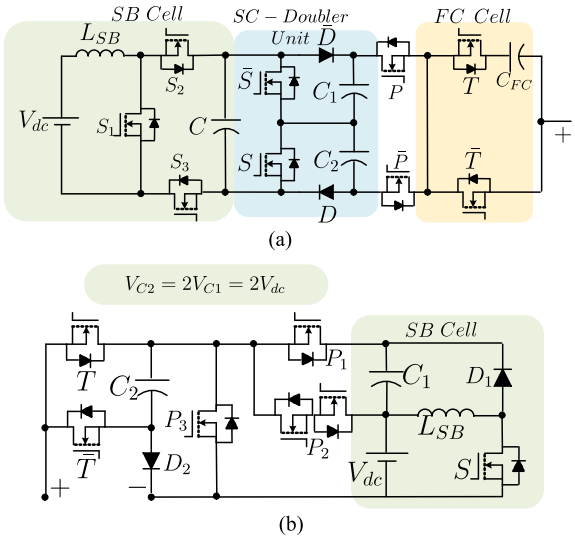

Fig. 44. CGSB-based inverters with the SC technique. (a) 9L topology [158]. (b) 5L topology [159].

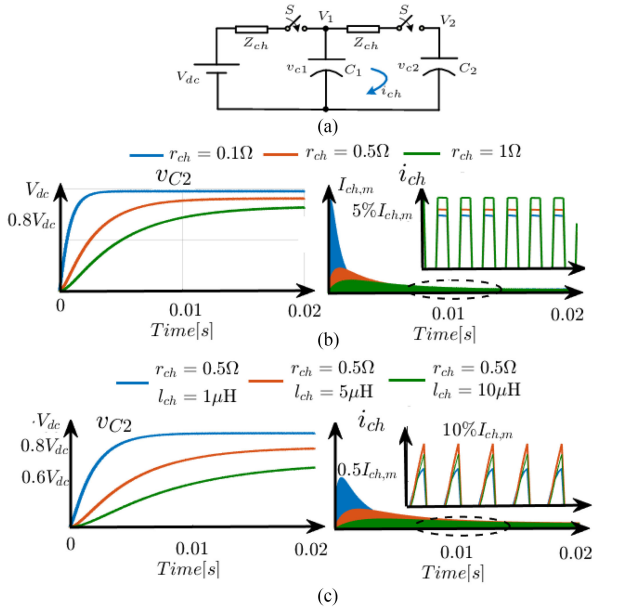

Fig. 45. (a) Typical capacitive charging path circuit for SC-based converters. (b) Voltage of the capacitor and the charging current of the loop for a pure SC-based converter. (c) Voltage of the capacitor and the charging current of the loop for the SC-based converter with QSC operation.

double voltage conversion gain to the output, whereas five power switches are involved there. Hence, a CG-based concept is provided for this inverter, while the p.u. TSV index of the switches is only five.

Finally, the integration of the SB technique with the SC concept can make another family of hybrid-based MLIs. Fig. 44(a) and (b) shows two different CGSB-based inverters presented in [158] and [159] with the capability of 9L and 5L output voltage generations, respectively. Considering Fig. 44(a), the role of the SB cell is to give a dynamic voltage-boosting operation to the capacitor, C, with a fixed boost dc duty cycle of d, while both the SC voltage doubler unit and FC cells can generate additional output voltage levels as discussed earlier. In this regard, the 5L CG-based inverter shown in Fig. 44(b) is an extended topology of [126], while the SPSC unit has been replaced with an SB cell. Hence, the performance of the converter from the input inrush current viewpoint is improved, whereas the voltage gain of the converter is doubled.

A quantitative summary of the aforementioned hybrid-based SC-MLIs from the previously discussed aspects has been provided in Table VI. Excluding the topologies presented in [158] and [159], all the discussed hybrid SC-MLIs are inductorless. Hence, the number of required inductor (L) has not been included in Table VI. In addition, all the discussed hybrid SC-MLIs are operated in 50-Hz fundamental frequency, while the reported rated efficiency of the 9L hybrid CGSC inverter presented in [157] is at 400 Hz. From Table VI, it can be taken that the SC-based hybrid inverter in [151]–[153] with HB legs require the least number of power switches per output voltage levels, whereas from the maximum number of SC charging path switch aspect, the 5L CGSB-based inverter in [159] has better option than others. Obviously, the 9L SB-based hybrid inverter in [158] can offer the largest output voltage gain since it has a dynamic (flexible) voltage-boosting feature.

V. Challenges and Opportunities

The charging operation of the capacitors in the pure SC-based basic units causes a sort of challenges/limitations for almost all the discussed SC-MLIs. Large pulsating current during charging operation increases the current stress profile of the switches involved in the charging path that deteriorates the overall efficiency of the converter. In addition, significant capacitor voltage ripple not only aggravates the pulsating current issue, but also causes distortions in the output ac voltage. These issues might be more severe when multiple SC-based basic units are cascaded to each other to realize larger voltage conversion gain in the SC-MLIs since the top positive/negative output voltage levels are made by the discharging operation of all the capacitors in series. To minimize switch count, the majority of the existing SC-MLIs are lacking RSSs that could be useful for reducing the longest discharging period (LDP) of the capacitor voltage via hybrid PWM. Hence, the optimization of these converters to achieve high power conversion with an improved overall efficiency is an imperative task.

To elaborate this capacitor voltage ripple and pulsating charging current issues, a simplified equivalent circuit considering parasitic ON-state impedance of this capacitive charging loop, Z_{ch}, for any SC-based basic unit is shown in Fig. 45(a). Considering different voltage levels for C_1 and C_2 during the switching operation and assuming V_1 and V_2 as the initial stored voltages of the capacitors while $C_1 \gg C_2$, a power loss caused by this hard charging operation occurs as given in the following [173], [174]:

$$P_{\text{loss}} = \frac{1}{4}C_2(V_1 - V_2)^2 f_{\text{sw}} = \frac{1}{4}C_2 \Delta V^2 f_{\text{sw}} \qquad (1)$$

where f_{sw} is the PWM switching frequency of the switch S, which represents the role of charging path switches in the SC-based circuits. This type of power loss refers to as the ripple loss of capacitors in the SC-MLIs and is dissipated in the parasitic impedance of the SC charging path. This ripple loss is not dependent on the value of this parasitic impedance, and instead, it hinges on the initial voltage difference of the capacitors, which comes at the cost of the charge transfer between the capacitors. Hence, the ripple loss of capacitors is proportional to the charge drawn by the load and inversely proportional to the capacitor values [173]. Moreover, the change of charge in the capacitor is proportional to the duration of the charge/discharge and, thus, is inversely proportional to the switching frequency as [173]

$$\Delta V \propto \frac{1}{f_{sw}}, \frac{1}{C_{eq}} \tag{2}$$

where C_{eq} is the equivalent capacitance of the charging path. Hence, with respect to (1) and (2), we can say P_{loss} is inversely proportional to f_{sw} and C_{eq}. This is the reason why to reach higher portion of the output power, larger capacitance of the capacitors is needed. In addition, it can be discerned that why the performance of SC-MLIs in high-frequency applications is much better than their counterpart in 50-Hz application [160]. As for a pure SC-based basic circuit, the parasitic inductance of the path caused by the layout design of the converter is negligible. Therefore, only an equivalent charging resistance r_{ch} related to the parasitic ON-state resistance of the charging path switch(es) and ESR of the capacitor(s) is predominant. Depending on the values of r_{ch} and f_{sw}, a very large discontinuous charging current i_{ch} is seen when the switch S is ON, which not only is deleterious for the lifetime of the switches and the capacitors but also can propagate EMI concern with a false turned-ON operation for even those switches that are not involved in this SC charging path. Herein, a complete charging process within a so-called fast switching limit (FSL) occurs as long as f_{sw} is to be larger than the critical frequency of this pure SC-based circuit, e.g., $f_{sw} > \frac{1}{2\pi r_{ch} C_{eq}}$. Else, the charging operation of the SC-based converter would not be completed, and it works within a slow switching limit performance, which is not desired and can even cause a larger value of the charging current spike/inrush current [173]. Having considered the FSL region and a constant 50% high-frequency duty cycle for switch S, the effects of different usual values of r_{ch} on the voltage stress across C_2 and on i_{ch} can be seen in Fig. 45(b). As can be realized, the smaller value of r_{ch} cannot reduce the P_{loss} mentioned in (1) since the total power loss in each switching cycle remains the same. In contrast, it can only shorten the capacitor voltage settling time with a larger peak value of i_{ch} ($I_{ch,m}$). It must be noted that this problem in actual case study of SC-MLIs is more significant since the duty cycle of charging path switches is not constant, and it follows a sinusoidal trend.

A solution for this concern is to optimize the SC-based converters from hard charging to soft charging [173]–[175] or quasi-soft charging (QSC) operation [21], [23], [65], [118], [176]–[182]. As for the SC-based dc–dc converters, where the duty cycle of high-frequency switches is constant, inserting a very small value of the charging inductor, l_{ch}, in series with the charging loop of the SC converter is useful in realizing fully soft charging operation. The importance of different values of l_{ch} on both the capacitor voltage and i_{ch} can be observed in Fig. 45(c). Although it can considerably reduce $I_{ch,m}$, it may affect the dynamic response of the capacitor voltage, and even in the case of larger value of l_{ch}, it can cause a voltage drop problem across the capacitor. As for a proper FSL operation, the condition of $f_{sw} > \frac{1}{2\pi\sqrt{l_{ch} C_{eq}}}$ must be fulfilled [173]. Although this concept might be propitious for the SC-based dc–dc converters [183], achieving a fully soft charging operation in SC-MLIs is still challenging owing to the variable ac duty cycle of charging path switches. In this case, the equivalent RLC circuit for the charging loop of most of the SC-MLIs operates within an overdamped oscillation region since the ratio of $\frac{r_{ch}}{2}\sqrt{\frac{C_{eq}}{l_{ch}}}$ is always greater than 1 in practice. Hence, $i_{ch}(t)$ is given as follows [23], [118]:

$$i_{ch}(t) = \frac{C_{eq}}{2}(\delta_1 \rho_1 e^{\delta_1 t} + \delta_2 \rho_2 e^{\delta_2 t}) \tag{3}$$

$$\delta_{1,2} = \frac{r_{ch}}{l_{ch}} \pm \sqrt{\left(\frac{r_{ch}}{2l_{ch}}\right)^2 - \frac{2}{l_{ch} C_{eq}}} \tag{4}$$

$$\rho_{1,2} = \frac{\delta_{1,2}}{\delta_1 - \delta_2}\Delta V. \tag{5}$$

Regarding this, the maximum charging current of the involved switches in the SC network for an QSC operation can be obtained as follows:

$$I_{ch,m} = \frac{C_{eq}\Delta V}{2}\left(\frac{\delta_1 \delta_2}{\delta_1 - \delta_2}\right)(e^{\delta_1 t_r} + e^{\delta_2 t_r}) \tag{6}$$

$$t_r = \frac{1}{\delta_1 - \delta_2} \ln \frac{\delta_1}{\delta_2}. \tag{7}$$

Although in most of the cases, adding this small parasitic inductance in the charging path of switches is workable to mitigate the current stress, it cannot still address the LDP problem of the capacitors in many SC-MLI case studies. In this regard, the type of modulation strategy and the importance of having RSSs are important. As opposed to the other well-known types of MLIs, such as modular multilevel converters (MMCs) or ANPC/FC-based MLIs, the switches of the SC-MLIs must be driven using the well-known level-shifted-sinusoidal pulsewidth modulation (LS-SPWM) technique. This comes at the cost of imperative parallel charging operation of SCs during the output-voltage-level generation. The LDP of the capacitors in the LS-SPWM technique can be controlled by decreasing the maximum value of the modulation index, M. In this regard, it is more preferable to have a structure, which is able to charge/discharge C_{FC} in every switching cycle. As given in the 5L ABNPC-based structure presented in [95] or [96] (see Fig. 31), the maximum value of the charging current is reduced using the following expression:

$$I_{ch,m} \approx \frac{M}{1 - M}\frac{1 + \delta}{1 + 2\delta} I_m \tag{8}$$

where I_m is the maximum value of the load/output current and δ is a constant ratio as $\frac{C_{FC}}{C_1}$.

Although this approach is helpful to realize a highly efficient converter in higher ratio of the output power, it limits the modulation index [117]. An alternative solution is to add one-sixth of the third-harmonic order in the reference signal of LS-SPWM [184] for a three-phase system. Using this technique, the LDP is reduced, while only the fundamental harmonic content can be seen in the line output current/inverter output voltage. Reduction in the maximum value of the modulation index to decrease the current stress of the capacitive charging loop switches/voltage drop across the capacitors can be more effective as long as SC-MLIs offer enough RSSs. In this case, a hybrid modulation method that is a combination between the phase-shifted (PS) and LS-SPWM techniques can be adopted [67], [185]–[187]. The 7L single-input dc-source inverters presented in [20], [25], [39], and [67], the 11L double-port SC inverter presented in [186], the 7L double-port SC inverter with the cascaded connection of two symmetric SC-based inverters proposed in [88], and the 13L and 17L single-input-dc-source inverters reported in [29], [35], [37], and [38] are a few types of SC-MLI topologies that have RSS capability to be applied for this type of hybrid PS/LS-SPWM technique. The concept of this technique is based on the number of RSSs available per each output voltage level. Hence, depending on the number of these RSSs, some PS carriers that have the same amplitude but different phases with respect to each other are used in the modulation. Each of these PS carriers can be assigned to one of the available RSSs. Hence, the capacitors integrated in these RSSs can be alternatively charged/discharged. Therefore, instead of being discharged for a long duration in the normal LS-SPWM technique, the LDP of the capacitors can significantly be optimized, while due to high switching frequency of this hybrid approach, much smaller values of the capacitances can be employed for the involved capacitors [67]. Since the output harmonic profile of the inverter is the same as the conventional LS-SPWM technique, it cannot induce larger switching losses for the charging path switches available in the RSSs.

To further show the importance of this type of modulation, two simulations using MATLAB have been conducted for two different tripler-gain 7L and six-times-gain 13L single-input-dc-source SC-MLIs presented in [39] and [35], respectively. These two topologies are based on SC voltage tripler Unit-I (see Fig. 8) and a series connection of SC voltage tripler Unit-I and the SC voltage doubler unit (see Fig. 17), respectively. The power level for the 7L inverter is 2 kW, while for the 13L inverter, it is 1 kW. $R_{\mathrm{DS,ON}}$ of all the switches has been set at 30 mΩ, which is a standard range for recently commercialized SiC devices. The switching frequency for both the cases is supposed to be the same as 100 kHz. As for the 7L inverter presented in [39], two RSSs are provided when $\pm 2V_{\mathrm{dc}}$ are generated. The details of the hybrid modulation for this topology are shown in Fig. 46(a). An absolute function of a sinusoidal reference signal, $|u_{\mathrm{ref}}|$, with a maximum amplitude of A_{ref} is used. Two out of three carries have been level-shifted between the amplitudes of A_c and $3A_c$, while they have 180° PS with respect to each other. The third carrier, u_3, is just used to create the gate switching pulses of switches involved in the path of $\pm V_{\mathrm{dc}}$ output voltage levels, where both the capacitors of SC voltage tripler Unit-I are charged

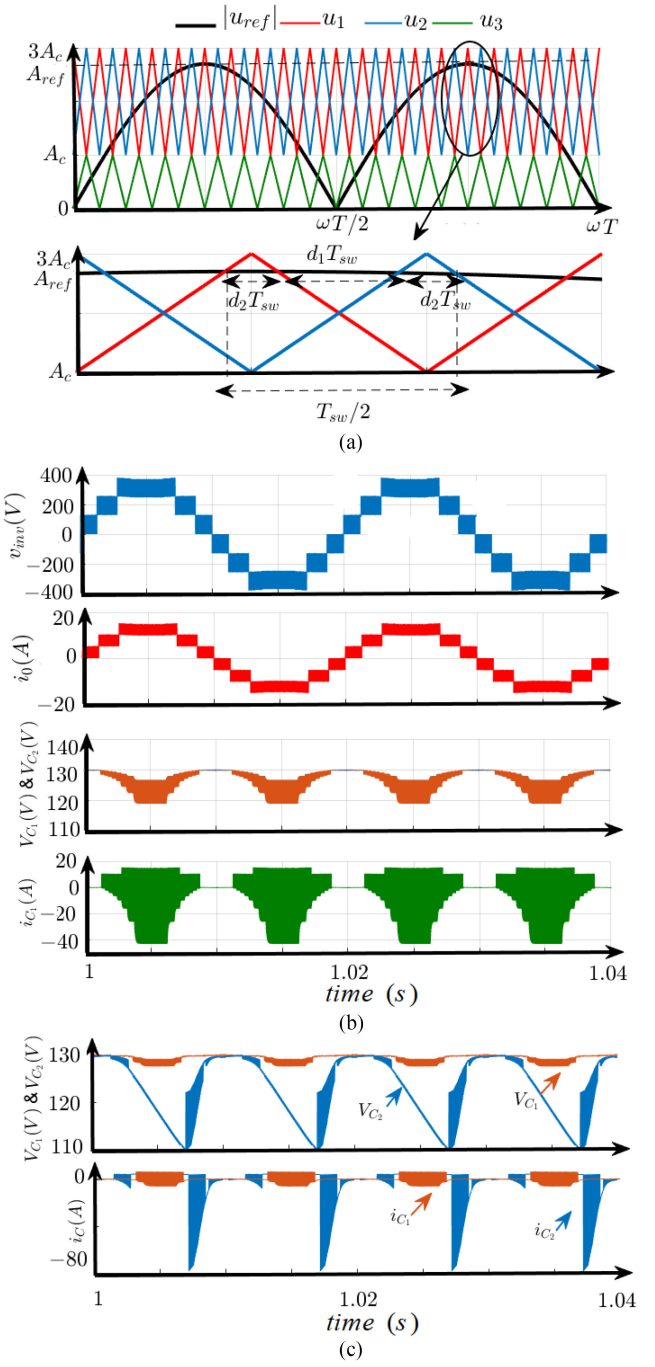

Fig. 46. (a) Principle of a hybrid PWM technique for the single-dc-source 7L SC-based inverters [25], [39], [67]. (b) Simulation result showing from the top to bottom: the inverter output voltage, the load current, the capacitor voltages, and the capacitor currents at 2-kW output power. (c) Capacitor ripple voltage and current stress when the conventional LS-SPWM technique is used.

in parallel to V_{dc} during this switching time interval. Here, the modulation index can be defined as $M = \frac{A_{\mathrm{ref}}}{3A_c}$, and the relevant gate switching pulses of two RSS paths at $\pm 2V_{\mathrm{dc}}$ are obtained by comparing $|u_{\mathrm{ref}}|$ with u_1 and u_2 [67]. In this case, two involved capacitors of this SC voltage tripler unit are alternatively charged and discharged. Taking Fig. 46(a) into account, the ac duty cycles

of d_1 and d_2 offer the following relation:

$$\begin{cases} d_2 + 2d_1 = 0.5 \\ d_1 = \frac{3A_c - u_{\text{ref}}}{3A_c} \\ d_2 = \frac{u_{\text{ref}}}{2A_c} \end{cases} \tag{9}$$

where considering T_{sw} as the switching time interval of the modulation and $d_1 T_{\text{sw}}$ implies the duration when one of the capacitors is connected in series to the input dc source to discharge to the load. Considering these observations and regarding a pure resistive load, R, for the converter, the ripple voltage of the capacitors is obtained as follows [67]:

$$\Delta V = \frac{2u_{\text{ref}} - 3A_c}{A_c f_{\text{sw}} RC} V_{\text{dc}} \tag{10}$$

where the maximum voltage ripple of the capacitors is [67]

$$\Delta V = \frac{2A_{\text{ref}} - 3A_c}{A_c f_{\text{sw}} RC} V_{\text{dc}} = \frac{6M - 3}{f_{\text{sw}} RC} V_{\text{dc}}. \tag{11}$$

Using this hybrid modulation technique, two small values of identical capacitors $C = 100$ μF are required. Considering $V_{\text{dc}} = 130$ V and $R = 25$ Ω, the simulation results of the inverter output voltage, the load current, the capacitor voltage, and capacitor currents are shown in Fig. 46(b). In this case, to keep the maximum ripple voltage of the capacitors under a standard 10% variation, the maximum value of the modulation is set at 0.85, while the maximum value of the current passing through the capacitors at 2-kW power is around 35 A. The literature review shows that to keep the same result for this type of SC-MLIs with a conventional LS-SPWM technique and without using RSSs in the middle output voltage levels, two very large capacitors are needed [20]. To show the performance differences of the inverter, another simulation with the conventional LS-SPWM technique is adopted when the power rating is 1 kW, and the capacitances of the capacitors in front-end SC voltage tripler Unit-I are chosen large enough. As can be seen from Fig. 46(c), through the conventional LS-SPWM technique, only one RSS for the generation of the middle output voltage level is used. Therefore, the ripple voltage of the capacitor that is in charge of feeding the load/grid in both the middle and top positive or negative output voltage levels is larger than the other one. This causes a high current stress even when a half power ratio of the previous hybrid modulation case study is targeted.

The aforementioned hybrid modulation principle has been applied to the presented 13L SC inverter in [35]. In this case, four capacitors are required, in which two of them are used at front-end SC voltage tripler Unit-I, and the remaining two are in the SC voltage doubler unit. There are two RSSs per each of the output voltage levels in $\pm V_{\text{dc}}$ and $\pm 5V_{\text{dc}}$. Hence, as shown in Fig. 47, the PS carriers of u_6 and u_5 are level-shifted between the amplitudes of $4A_c$ and $6A_c$. The same observation is seen for two PS carriers of u_1 and u_2, in which their amplitude is between zero and A_c. Using these PS carriers leads to alternatively charging/discharging operation of the capacitors in front-end SC voltage tripler Unit-I. Owing to the six times voltage conversion gain of the converter, a dc voltage of 75 V with a pure resistive load of 50 Ω is considered for the simulation, and the results

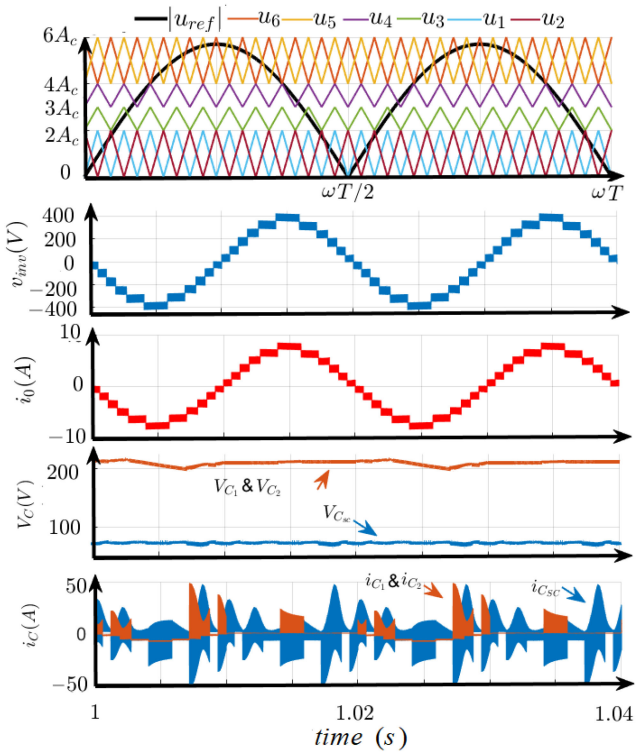

Fig. 47. Simulation result using the hybrid-PWM technique for the presented 13L SC-based topology in [35] showing from the top to bottom: the principle of the modulation, the inverter output voltage, the load current, the capacitor voltages, and the capacitor currents at 1-kW output power.

are shown in Fig. 47. In this case, the maximum modulation index is equal to 0.85, and the capacitance of all the capacitors is the same as $C = 470$ μF. Implementing such modulation technique, all the 13L output voltages with a voltage gain of six are generated, while the voltage ripple of the capacitors is within an acceptable range. Here, the maximum value of the current passing through the capacitors for such a 1-kW model is less than 40 A. Considering $M = \frac{A_{\text{ref}}}{6A_c}$ and applying the same procedure as described for the 7L SC-based inverter, the capacitor ripple voltage of SC voltage tripler Unit-I is then taken as follows [35]:

$$\Delta V = \frac{21M - 15}{f_{\text{sw}} RC} V_{\text{dc}}. \tag{12}$$

In this regard, it is recommended to incorporate an LC input filter for the SC-MLIs since it can help the input dc source to draw a semicontinuous input current free from large pulsating inrush spike [23], [135]. It is worth mentioning that soft start is also another challenge associated with SC-MLIs. This comes from the fact that the capacitors are supposed to be empty of charge at the beginning of the operation. Hence, without taking any procedure, a large inrush current is prone to be induced. Soft-start techniques are usually considered using a relay associated with a resistor that can smoothly charge the capacitors at the beginning of the operation and then can be bypassed in normal operation [117], [146]. Khan *et al.* [182] have also introduced another scheme of soft-start operation based on changing the modulation process. Hence, instead of

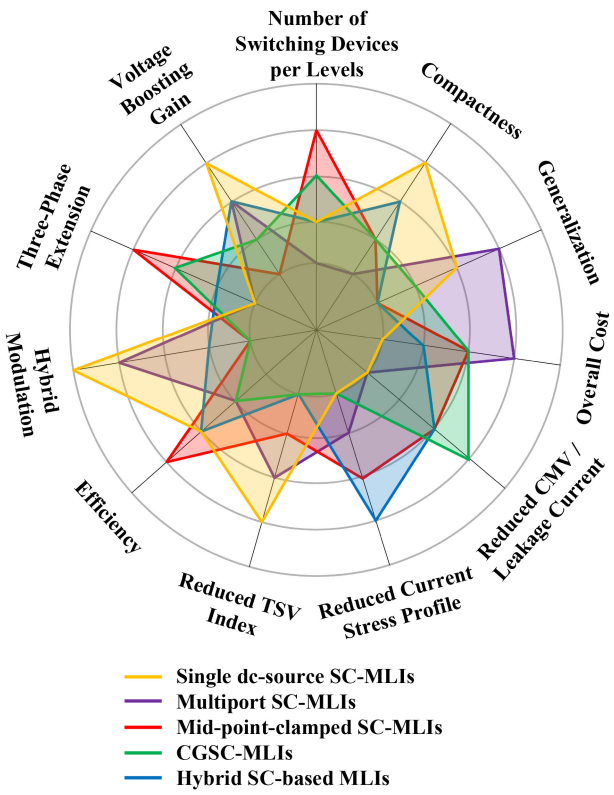

Fig. 48. Qualitative summary of different SC-MLIs in various aspects.

using any relay, the soft-start modulation will not allow the capacitors to be charged at the start-up moment, and after a while, depending on the time constant of the circuit, the main modulation process starts operating.

VI. Qualitative Summary, Application, and Future Roadmap of SC-MLIs

Regarding the outlined review conducted on the recent advances of SC-MLIs, some further discussions related to a qualitative summary of different branches of SC-MLIs, potential applications, and also future roadmap of the research are presented in the following subsections.

A. Qualitative Circuit Features of Different SC-MLIs

To provide a detailed qualitative review over the circuit features of different already-discussed SC-MLIs, 11 different parameters are considered, as shown in Fig. 48. These qualitative parameters are listed as follows: 1) number of switching devices versus output voltage levels; 2) compactness/power density; 3) generalization ability to realize higher number of output voltage levels with a modular design; 4) overall manufacturing cost; 5) possible potentiality of reducing the CMV/leakage current; 6) having a reduced current stress profile of the switches; 7) reduction in the overall value of the TSV index; 8) overall efficiency; 9) possibility of applying hybrid PS/LS modulation technique; 10) three-phase circuit extension capability; and 11) overall voltage conversion gain. The evaluation of different categories of SC-MLIs from the aforementioned aspects is conducted based on the quantitative comparative studies summarized in Tables II–VI.

For mass production, the ease of implementation using the standard HB or T/NPP modules available in market has been considered. Using standard HB, FB, or T-type semiconductor modules, the cost of production considering the gate drive design and auxiliary components is greatly reduced [165]. The reduced rate of balanced voltage across the capacitors with respect to the maximum voltage conversion gain of the converters can also be helpful to employ capacitors with smaller footprint size. Hence, this factor can also affect the overall power density of the converters. As can be seen from Fig. 48, the single- and multiple-input-dc-source SC-MLIs have a better condition from this point of view than others. The factor of generalization is also a merit for the developed topologies of SC-MLIs, in which a larger number of output voltage levels with a modular design can be achieved. From this feature, multiport SC-MLIs offer better rooms since symmetric and asymmetric designs of the input dc-source magnitudes can be considered for them to achieve a large number of output voltage levels. From the overall manufacturing cost viewpoint, many subitems, including the cost of driving board circuits, heatsink with cooling system, the type of printed circuit board from the number of layers and the type of copper points of view, the number of required power switches/passive elements, voltage and current rating stresses of the semiconductors, targeted output power, and so on, must be considered. Using the cost function equation in some literature such as [19], [29], [32], [162], and [163], it can be concluded that multiport SC-MLIs require the highest overall cost than others due to incorporated input dc sources with different varieties/magnitudes, while owing to lower number of semiconductors involved in the charging path of capacitor(s), hybrid MLIs can possess better option than others. The CGSC-based MLIs and mid-point-clamped SC-based MLIs are both suitable case studies from the reduced CMV/leakage current concern viewpoint, although from the reduction in the value of the TSV index and generalization ability, they may not have a suitable condition compared to others. Considering lower voltage conversion gain of the mid-point-clamped SC-MLIs, the SC charging path switches have the possibility to handle smaller discontinuous current rating stress. Hence, it is expected to get higher overall efficiency than others. Hybrid MLIs are also counted as efficient converters in this context, but owing to the incorporation of the inductors and their associated copper losses, achieving high efficiencies is still a challenge.

As earlier stated, applying hybrid modulation is a key option for SC-MLIs to incorporate smaller capacitors with reduced LDP and current stress. So far, a few types of single-input-dc-source SC-MLIs have offered this option, while there is no reported hybrid modulation for the other types of SC-MLIs. The possibility of three-phase circuit extension is also a key merit of the mid-point-clamped SC-MLIs, as can be observed in Fig. 48, while this option for single- and multiple-input-dc-source SC-MLIs is achieved at the cost of stacking (implementing) three single-phase identical topologies.

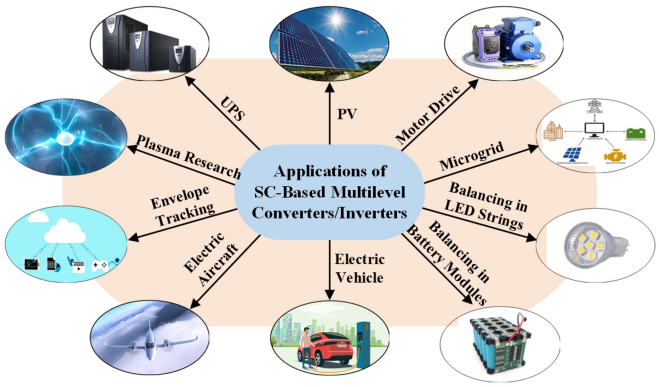

Fig. 49. Illustration of various applications of the SC-MLIs.

B. Reported Applications of SC-Based Converters/Inverters

Different applications of the SC-based dc–dc converters have already been discussed in [9], where SC networks are used to step-up the fixed dc-link voltage with a static voltage conversion gain without using any interfaced transformer [8], [188], [189]. Fig. 49 illustrates some of these applications for SC-based converters. The idea of the generation of multiple boosted dc-link voltages through the SCCs in the HF repetitive pulsed generator has originated from the Marx converters [16]. Plasma, Ozone making, sterilization, food processing, water treatment, and military applications have been the target through these types of converters [190]. In envelope tracking (ET), it is needed to track the envelope of the signal in the radio frequency range to optimize the efficiency of the power amplifier. In this case, to obtain a high tracking bandwidth, the switching frequency is often required to be five to ten times higher than the fundamental frequency [191]. The utilization of multilevel SCCs as the switched-mode converter for the purpose of increasing the equivalent switching frequency and achieving a higher bandwidth with the same switching frequency can help the whole system to offer a reduced THD with a concise configuration. The usual range of power for ET applications is less than 100 W, and their fundamental frequency is around 1–10 MHz [191]–[194].

When it comes to SC-MLIs, their applications can be more broaden. Even though having a pulsating input current, single-stage voltage step-up feature makes SC-MLIs an attractive option of the grid-tied PV-based low-power applications [127], [129], [130], [195]–[197]. Owing to the large value of the current stress drawn by the input dc source, the expected power range of these converters in 50-Hz grid-tied application is less than a few kilowatts. Motor drives [198], [199], electric vehicles [200], [201], energy storage systems [202], and balancing in battery strings [175], [203], [204] are other developed applications of SC-MLIs with a limited output power performance.

As earlier discussed, to increase the range of output power, the applicability of these converters must be improved from the LDP of the capacitor's point of view and, in turn, the large pulsating discontinuous inrush spikes. One of the popular ways to address this is to target some HF-based applications, such as microgrid or electric aircraft. The literature in [31], [90], [157], [160], [164], [176], and [205] has already explored the performance of the SC-MLIs in 400-Hz-to-1-kHz applications, while an acceptable overall efficiency with an improved power density of the converters is achieved rather than the interesting inherent features of SC-MLIs in the voltage-boosting ability and self-voltage balancing operation of the capacitors.

C. Additional Remarks and Future Roadmap

Considering the previous contributions, improving the overall performance of SC-MLIs from both the already-discussed quantitative and qualitative prospectives, and broadening their possible new applications are still challenging and crucial tasks. Regarding this, the following remarks can be made for future roadmaps of the research in this area.

1) Generating a larger number of inverter output voltage levels for single-input-dc-source-based SC-MLIs with RSS possibility has been performed so far for a few types of topologies. Nonetheless, this feature, which can help the converter to achieve higher power level with a reliable performance through the hybrid modulation technique, has not been explored on mid-point-clamped, CGSC-based, and hybrid SC-MLIs. Hence, the investigation of new topologies from these categories is highly recommended.
2) Both the single- and multiple-input-dc-source SC-MLIs are constructed based on either FB back-end cell or HB legs for polarity inverting purpose. This generates variable HF-CMV, and leakage current remains still in place. Hence, improved circuit topologies and new modulation technique are worth investigating to reduce this unwanted value of the HF-CMV [119], [206].
3) A few types of single-input-dc-source SCMLIs are able to operate with a fault-ride-through performance. This important feature has already been elaborated for the other variants of MLIs, i.e., MMC- or FC-based MLIs, which can help the whole converter to show a reliable performance against both the open-circuit and short-circuit faults [43], [207]. Hence, establishing new alternate SC-MLIs with the integration of this concept can be an interesting case study.
4) A compact design and the implementation of SC-MLIs using a new generation of wide-bandgap semiconductor devices, e.g., GaN or SiC, have not been explored. As it has already been explained, SC-MLIs face many challenges in terms of the current stress profile of the switches and the LDP concern of capacitors. Hence, the design guidelines of these converters from efficiency, power density, and thermal observations are helpful for their future development.
5) A few types of SC-MLIs with the closed-loop grid-tied performance have been reported in the literature. As for the single-phase application, canceling the double-line frequency from the input current profile, which is the so-called active power decoupling (APD), is a prime focus [208]. However, owing to pulsating input current nature of SC-MLIs, it is still a challenging matter of concern. Governing the converter with APD and riding

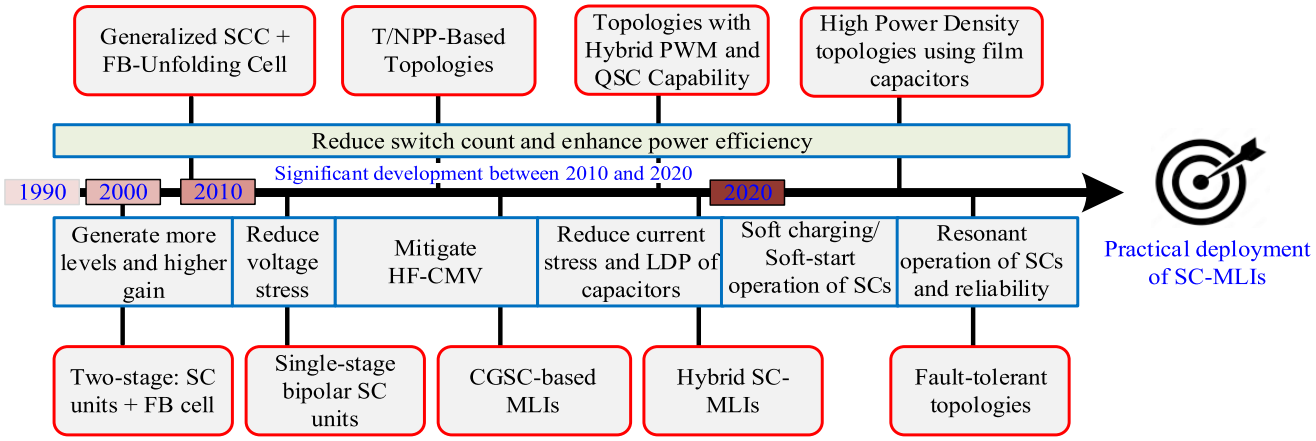

Fig. 50. Perspective evolution and future development of SC-MLIs.

through the active and reactive power injection with hybrid SC-MLIs can be a hot topic for future research in this area.

6) Application of a fully soft switching technique for SC-MLIs to improve the efficiency and reduce the current stress of the switches is still a challenging task that can be interesting for the future research on this topic.

The evolution perspective of SC-MLIs with the aforementioned roadmap is illustrated in Fig. 50, while they are not limited for the future research topic of SC-MLIs. However, these items can be considered besides the investigation of new topologies with larger voltage conversion gain, reduced number of switching devices, reduced value of the MVS and TSV index across the switches, alleviated performance of large pulsating inrush current, and lower overall cost for future generation of SC-MLIs.

VII. Conclusion

After more than a decade of rapid development, a large number of SC-MLIs have been presented. Owing to the diversity and complexity of so many SC-MLI topologies in the literature and lack of having a systematic review, a first attempt to define the current status and future research of this new family of MLIs is presented in this article. The concept of integrating SC-based basic units into different circuit configurations of MLIs is critically reviewed, and almost all the existing topologies are comprehensively categorized. Their advantages and drawbacks are identified through quantitative and qualitative comparative studies.

The review shows that the voltage conversion gain of converters in single-input-dc-source SC-MLIs can be enhanced by adopting some developed SC-based basic units with a reduced overall TSV index and low number of required power switches. Having enough RSSs for different paths of the same output voltage level can further improve their performance from the current stress and capacitor ripple voltage viewpoints. Multiport SC-MLIs can also be driven using symmetric and asymmetric magnitude adjustments of the input dc sources. A large number of output voltage levels with a reduced number of required semiconductor devices can be achieved through these converters. Nonetheless, their overall cost, TSV index, and current stress performance are still challenging. Full dc-link utilization with an appropriate CMV per output voltage level can be achieved through the mid-point-clamped SC-MLIs. The lack of generalization ability in most of the reported topologies and lower range of overall voltage conversion gain are two important setbacks of these converters. Alternatively, CGSC-MLIs with a virtual dc-link concept can nullify the concern of leakage current in many sensitive applications such as grid-tied PV systems. However, poor performance of these converters from the LDP and the current stress profile of the capacitor viewpoint can be a prime focus for future development. Hybrid SC-MLIs can also be propitious if a dynamic voltage gain and the reduced current stress profile of the switches are of priority. Yet, lack of having a generalized topology in this context can imbibe more attention to rehearse new topologies with a larger number of output voltage levels.

Finally, the challenges associated with the state-of-the-art SC-MLIs, such as large pulsating current stress and large voltage ripple across the capacitors, are identified and analyzed. These challenges and their possible solutions, such as the incorporation of the hybrid PWM techniques or the QSC operation of the SC charging loops, are elaborated. The review work is summarized with future research outlooks and technological roadmap for practical applications to inspire further improvements toward a more efficient, high-power-density, reliable, and low-overall-cost power converter for existing and emerging applications.

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