A Temperature-Dependent dVCE/dt and dIC/dt Model for Field-Stop IGBT at Turn-on Transient

Xue, Peng; Davari, Pooya

Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2023.3256439

Publication date:
2023

Document Version
Accepted author manuscript, peer reviewed version

A Temperature-Dependent dV_{CE}/dt and dI_C/dt Model for Field-Stop IGBT at Turn-on Transient

Peng Xue, *Member, IEEE* and Pooya Davari, *Senior Member, IEEE*

***Abstract*—In this paper, a complete expression for dV_{CE}/dt and dI_C/dt at turn-on transient of field-stop (FS) insulated gate bipolar transistor (IGBT) is proposed. With numerical simulation utilized, the critical stray elements and internal physics which have a significant impact on turn-on behaviour of FS IGBT are identified. Based on the improved understanding on the turn-on behaviour, the turn-on transient is divided into two phases and the equivalent circuits of each phase are obtained. The analytical expressions of dV_{CE}/dt and dI_C/dt during the turn-on transient are thereby derived based on the equivalent circuits. The temperature dependency on the turn-on characteristics of FS IGBT is identified by the experimental data. The temperature-dependent models of various device parameters are proposed to describe the temperature dependency. In the end, the double-pulse test is performed on a 650V FS IGBT and a 1200V FS IGBT. The good agreement between the test and analytically derived results validates that the proposed FS IGBT model can accurately predict the dV_{CE}/dt and dI_C/dt during the turn-on transient.**

***Index Terms*—field-stop (FS) IGBT, collector-emitter voltage falling rate, collector current rising rate, IGBT modeling, turn-on.**

I. Introduction

THE high-efficiency power conversion application requires the power switch to operate with high switching frequency. To meet the requirement, miscellaneous designs [1]–[4] are proposed to improve the performance of the insulated gate bipolar transistor (IGBT). As one of the most popular solutions, the field stop (FS) concept is proposed in [3], [4]. In the FS IGBT, a thin and lightly doped FS layer is introduced, as shown in Fig. 1. The FS IGBT can just stop the electrical field without reducing the emitter efficiently [3]. With the FS layer utilized, the FS IGBT can achieve a better trade-off relationship between the on-state voltage and switching losses than the punch-through (PT) IGBT and non-punch-through (NPT) IGBT [3]. Due to its merits, the FS IGBT quickly becomes a mainstay among the mass IGBT market in recent years.

With the FS layer utilized, the fast switching of the FS IGBT generates a high collector-emitter voltage falling slope (dV_{CE}/dt) and collector current rising slope (dI_C/dt) on the device. Recently, the dV_{CE}/dt and dI_C/dt of the FS IGBT arise great concern in industry and academia due to the following reasons. Firstly, the high dV_{CE}/dt and dI_C/dt give rise to high levels of electromagnetic interference (EMI) for power converters. The dV_{CE}/dt is the major source of common mode EMI, whereas the dI_C/dt is the main source of differential-mode EMI [5]. The EMI noise induces electromagnetic compatibility (EMC) problems for the power converters [5]–[7] and can disrupt the converter operation in the worst-case scenario. Secondly, the turn-on losses of the device is a function of dV_{CE}/dt and dI_C/dt. The dV_{CE}/dt and dI_C/dt are thereby very critical for the turn-on losses estimation. Last but not least, the dV_{CE}/dt and dI_C/dt are also found to be good thermo-sensitive electrical parameters which reflect junction temperature of the IGBT [8]–[10]. The dV_{CE}/dt and dI_C/dt are thereby the key for the junction temperature measurement of IGBT [8]–[10].

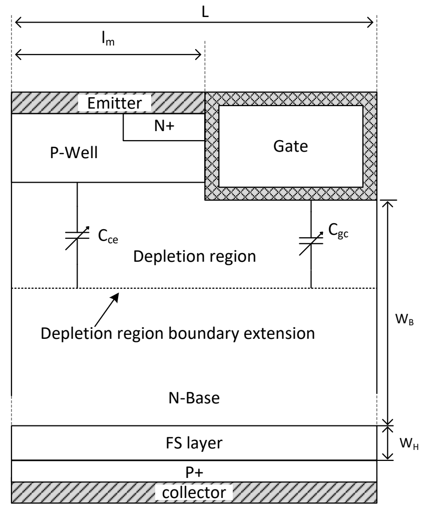


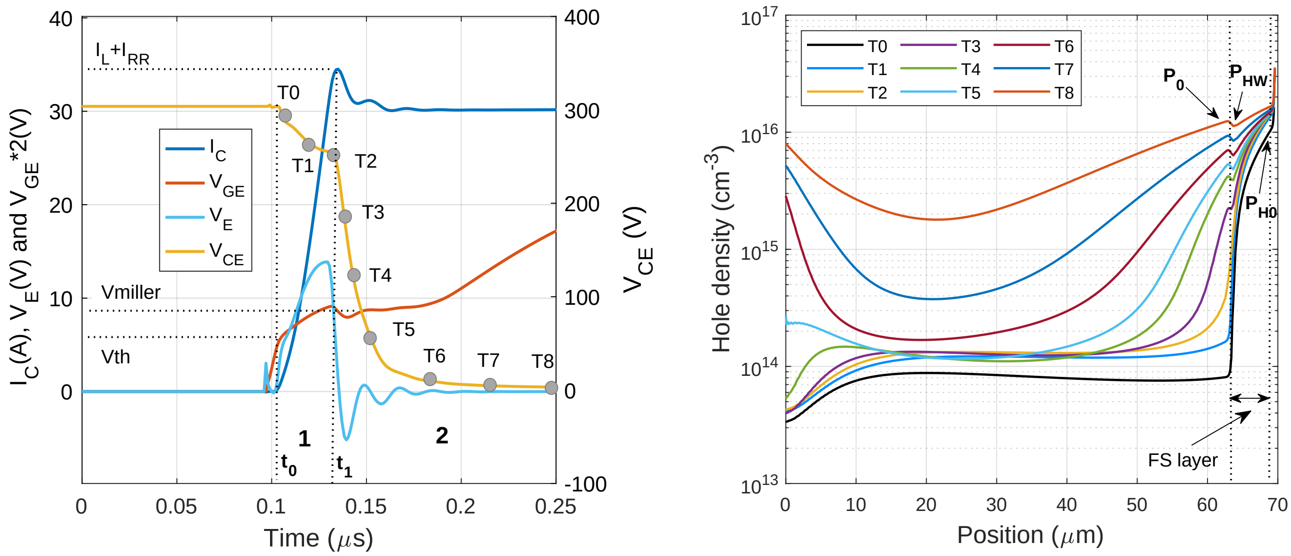
Fig. 1. Schematic structure of FS IGBT

Looking into the previous research on dV_{CE}/dt and dI_C/dt modeling, most studies focus on the turn-off transient [9]–[13]. Only a few research investigate the dV_{CE}/dt and dI_C/dt during turn-on transient. The [14] proposed dV_{CE}/dt and dI_C/dt models for IGBT during the turn-on transient. The model is widely used for turn-on losses calculation [15] and EMI modeling [5] for FS IGBT. In [16], a dV_{CE}/dt and dI_C/dt model is also proposed for the turn-on transient of IGBT. The model is used in [17]–[19] to calculate the switching losses of IGBT.

The current dV_{CE}/dt models proposed in [5], [14]–[19] have a major drawback. In the models, the IGBT is considered as a unipolar device during the turn-on transient. The impact of excess carrier dynamics in the N-base on the dV_{CE}/dt are

The authors are with the Department of Energy, Aalborg University, Aalborg East 9220, Denmark. (E-mail: pexu@energy.aau.dk).

This work was supported by the CLEAN-Power (Compatibility and Low electromagnetic Emission Advancements for Next generation Power electronic systems) project at the Department of Energy, Aalborg University, Aalborg, Denmark, funded by Independent Research Fund Denmark (DFF).



(a)

(b)

Fig. 2. TCAD simulation during clamped inductive turn-on transient of FS IGBT: (a) Simulated turn-on waveforms with the definition of time $T_0 - T_8$ and phases 1-3; (b) Simulated hole density profiles in the N-base at time $T_0 - T_8$.

not included. During the turn-on transient, the excess carrier starts to build up in the N-base, which has a strong impact on the voltage-falling process of IGBT [20], [21]. To accurately predict the dV_{CE}/dt during the turn-on transient, the excess carrier dynamics must be included.

For the dI_C/dt modeling, the current models [5], [14]–[19] neglect a lot of circuit stray elements to simplify the model. This can induce significant errors in the prediction since some circuit stray elements can have a huge impact on the turn-on behaviour. To derive accurate dI_C/dt model, all the circuit stray elements which have a significant impact on the dI_C/dt should be identified and included.

The goal of this paper is to derive a complete expression for dV_{CE}/dt and dI_C/dt during the turn-on transient of FS IGBT. The remainder of this paper is given as follows. In section I, the turn-on behaviour of FS IGBT is analysed. The analysis reveals the equivalent circuit of the two phases during the turn-on transient. Based on the equivalent circuit, the analytical dV_{CE}/dt and dI_C/dt model of FS IGBT is derived in section III. In section IV, the temperature dependence on the turn-on characteristics is identified. Various temperature-dependent device parameters are used to model the temperature dependency. In section V, the parameter extraction methods of the proposed model are presented. In section VI, the double-pulse test is performed to validate the proposed model.

II. Clamped Inductive Turn-on Behaviour of FS IGBT

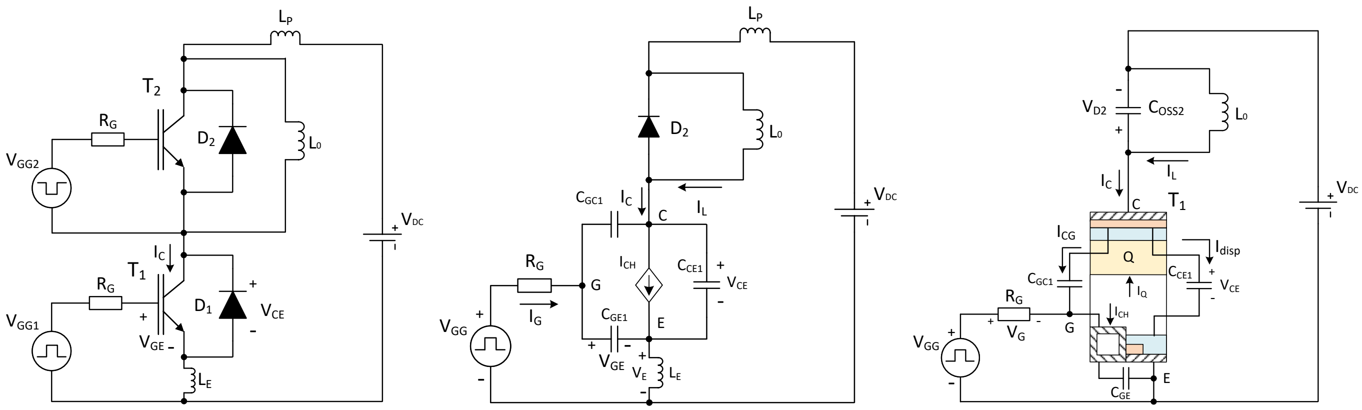
To derive the FS IGBT turn-on model, the internal and external device operation during the turn-on transient should be investigated. To achieve this, technology computer-aided design (TCAD) numerical simulation is performed. Fig. 1 shows the structure of FS IGBT utilized, which defines the cell width L, intercell width l_m, N-base width W_B and FS layer width W_H. In the TCAD model, $L = 18\mu m$, $l_m = 12\mu m$, $W_B = 63\mu m$ and $W_H = 6\mu m$. The doping concentration of N-base and FS layer is $9 \times 10^{13} cm^{-3}$ and $5 \times 10^{15} cm^{-3}$, respectively.

Fig. 2a shows TCAD simulated clamped inductive turn-on waveforms of gate-emitter voltage V_{GE}, collector-emitter voltage V_{CE} and collector current I_C. In the simulated waveforms, the time $T_0 - T_8$ are selected to investigate the excess carrier dynamics. The excess carrier density in N-base and FS layer at $T_0 - T_8$ is presented in Fig. 2b. In Fig. 2a, the turn-on transient is divided into phase 1 (starts at t_1) and phase 2 (starts at t_2). The two phases are described as follows.

Phase 1) When V_{GE} surpasses the V_{th} at t_0, the phase 1 intimates. In this phase, the IGBT operates in the unipolar mode since the excess carrier in the N-base is still depleted, as shown in the excess carrier profile at T_0, T_1 and T_2 in Fig. 2b. The increase of collector current I_C is mainly supported by the MOS channel electron current I_{CH}. The IGBT can thereby be modelled as a unipolar device in this phase. The impact of excess carrier dynamics in the N-base on the turn-on behaviour can be neglected.

Phase 2) The phase 2 starts at t_1 when I_C reaches to its peak value $I_L + I_{rr}$, as shown in Fig. 2a. I_L is the load current. I_{rr} is the peak reverse current of the high-side freewheeling diode. In phase 2, the freewheeling diode starts to support reverse voltage, which gives rise to the abrupt reduction of V_{ce}. In this phase, the excess carrier starts to build up in the undepleted N-base, and the excess carrier profile at T_3-T_8 is shown in Fig. 2b. The IGBT operate in the bipolar mode and the excess carrier dynamics in the N-base should be considered in the model.

Fig. 3a shows the typical half-bridge test circuit. In the circuit, T_1 and D_1 are active IGBT and freewheeling diode. T_2 and D_2 are synchronous IGBT and freewheeling diode. R_G is the gate resistance. L_P is the power loop stray inductance. L_E is the common emitter stray inductance. The equivalent



(a) (b) (c)

Fig. 3. Typical half-bridge test circuit. (a) Half-bridge test circuit with stray inductances. (b) Equivalent circuit during phase 1. (c) Equivalent circuit during phase 2.

circuits in phase 1 and phase 2 are derived and are given as follows.

In phase 1, the IGBT T_1 operates in unipolar mode and is thereby modelled as a unipolar transistor. Fig. 3b shows the equivalent circuit in phase 1. The capacitances C_{CE1}, C_{GC1} and C_{GE1} are collector-emitter, gate-collector and gate-emitter stray capacitances of T_1. The collector-emitter C_{CE} and gate-collector C_{GC} are modelled by (1) and (2), respectively.

$$C_{CE}(V_{CE}) = \frac{\epsilon_{si} A(1-a_i)}{\sqrt{\dfrac{2\epsilon_{si} V_{CE}}{qN_B}}} \tag{1}$$

$$C_{GC}(V_{CE}) = \frac{\epsilon_{si} A a_i}{\sqrt{\dfrac{2\epsilon_{si} V_{CE}}{qN_B}}} \tag{2}$$

where ϵ_{si} is the dielectric coefficient of silicon. A is the active die area. N_B is the doping concentration in the N-base. q is the electron charge. a_i is the area factor. With cell width L and intercell width l_m defined in Fig. 1, a_i is expressed as:

$$a_i = \frac{(L - l_m)}{L} \tag{3}$$

In Fig. 3b, the MOS channel electron current I_{CH} is modelled as a voltage-controlled current source. In this phase, the MOS channel has to support high voltage and thereby operates in the saturation region. I_{CH} can thereby be expressed as [22]:

$$I_{CH} = G_m(V_{GE} - V_{th}) \tag{4}$$

Where G_m is the MOS transconductance and V_{th} is the threshold voltage.

In phase 2, the dI_C/dt generates a very high voltage V_E on the common emitter stray inductance L_E, as shown in Fig. 3b. The V_E counteract a part of gate drive voltage V_{gg}, which in return slows down the dI_C/dt. As a result, a negative feedback process is achieved. To include the negative feedback action, L_E is included in the model. The dI_C/dt also creates a voltage on the power loop inductance L_P, which give rise to the V_{CE} reduction in this phase. To model the dV_{CE}/dt, L_P should also be considered.

Fig. 3c shows the equivalent circuit in phase 2. In this phase, the excess carrier starts to build up in the undepleted N-base and the IGBT is considered as the bipolar device. As shown in Fig. 3c, the abrupt reduction of V_{CE} generates the displacement current I_{CG} and I_{disp} on C_{GC} and C_{CE}, respectively. Due to excess carrier built-up, excess charge Q in the undepleted N-base and FS layer increases. A capacitive current I_Q is thereby generated to support excess charge Q to increase. The current components I_{CG}, I_{disp} and I_Q are very critical and should be included in the model.

In phase 2, high dV_{CE}/dt couples on the capacitance C_{CG} induce the displacement current I_{CG} flowing through the gate circuit, as shown in Fig. 3c. The I_{CG} generates a voltage V_G on the gate resistor R_G, which counteracts the gate driving voltage V_{GG}. This slows down the gate turn-on process, which in return gives rise to a lower dV_{CE}/dt. As a result, a negative feedback process is achieved. The negative feedback action has a huge impact on dV_{CE}/dt and should be included in the model.

In this model, the gate inductance is neglected. This is because the gate loop inductance mainly affects the delay time of the switching process [23]. The impact of gate loop inductance on the dI_C/dt and dV_{CE}/dt is very minor [24].

Based on the equivalent circuits presented in Figs. 3b and 3c, the dV_{CE}/dt and dI_C/dt in phases 1 and 2 can be obtained, which are presented in section III.

III. Turn-on Modeling

A. Phases 1

Based on the equivalent circuit presented in Fig. 3b. the circuit equations of phase 1 can be derived. According to Kirchhoff's voltage law (KVL), (5) can be derived for power loop.

$$V_{DC} = V_{CE} + (L_E + L_P)\frac{dI_C}{dt} \tag{5}$$

In this phase, I_C is mainly supported by the MOS channel current I_{CH}, then:

$$I_C = I_{CH} = G_m(V_{GE} - V_{th}) \tag{6}$$

The gate current is supported by the displacement current on the stray capacitances C_{GE} and C_{GC}, thereby:

$$I_G = C_{GE1}\frac{dV_{GE}}{dt} + C_{GC1}\frac{d(V_{GE}-V_{CE})}{dt} \tag{7}$$

According to the KVL, (8) can be obtained for gate loop.

$$V_{GG} = R_G I_G + V_{GE} + L_E\frac{dI_C}{dt} \tag{8}$$

Where R_G is the gate resistor.

Combining the equations (5)-(8), the following equations can be obtained:

$$\alpha\frac{d^2 I_C}{dt^2} + \beta\frac{dI_C}{dt} + I_C = G_m(V_{GG}-V_{th}) \tag{9}$$

With $\alpha = (L_E + L_P)R_G C_{GC} G_m$, $\beta = R_G(C_{GC}+C_{GE}) + L_E G_m$.

To solve the (9), following initial conditions are needed.

$$I_C(t=t_0) = 0 \tag{10}$$

$$\left.\frac{dI_C}{dt}\right|_{t=t_0} = 0 \tag{11}$$

where t_0 is the time in the beginning of phase 1, as shown Fig. 2a.

With (10) and (11) utilized, (9) can be solved. The solution of (9) depends on the relationship between L_E and a threshold value $L_{E(th)}$ given by:

$$L_{E(th)} = \frac{R_G(C_{GC}-C_{GE})+2\sqrt{R_G C_{GC}(G_m L_P - R_G C_{GE})}}{G_m} \tag{12}$$

When $L_E > L_{E(th)}$, the solutions of I_C is given by:

$$I_C = (V_{GG}-V_{th})\left(\frac{G_m\tau_2}{\tau_1-\tau_2}e^{\tau_1(t-t_0)} + \frac{G_m\tau_1}{\tau_2-\tau_1}e^{\tau_2(t-t_0)}\right) + G_m(V_{GG}-V_{th}) \tag{13}$$

Where the coefficient $\tau_1 = (-\beta+\sqrt{\beta^2-4\alpha})/2\alpha$. The coefficient $\tau_2 = (-\beta-\sqrt{\beta^2-4\alpha})/2\alpha$.

The dI_C/dt is thereby given by:

$$\frac{dI_C}{dt} = (V_{gg}-V_{th})\left(\frac{G_m\tau_1\tau_2}{\tau_1-\tau_2}e^{\tau_1(t-t_0)} + \frac{G_m\tau_1\tau_2}{\tau_2-\tau_1}e^{\tau_2(t-t_0)}\right) \tag{14}$$

When $L_E < L_{E(th)}$, the solutions of I_C is:

$$I_C = e^{\tau_a t}G_m(V_{GG}-V_{th})\left(\frac{\tau_a}{\omega}sin(\omega(t-t_0)) - cos(\omega(t-t_0))\right) + G_m(V_{GG}-V_{th}) \tag{15}$$

where $\tau_a = -\beta/2\alpha$, and $\omega = \sqrt{4\alpha-\beta^2}/2\alpha$.

The dI_C/dt is expressed as:

$$\frac{dI_C}{dt} = e^{\tau_a t}G_m(V_{GG}-V_{th})sin(\omega(t-t_0))\left(\omega+\frac{\tau_a^2}{\omega}\right) \tag{16}$$

When $L_E = L_{E(th)}$, the solutions of I_C is:

$$I_C = e^{\tau_a t}G_m(V_{gg}-V_{th})(\tau_a(t-t_0)-1) + G_m(V_{GG}-V_{th}) \tag{17}$$

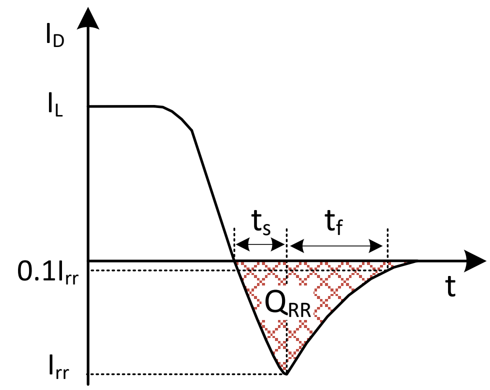


Fig. 4. Reverse recovery current waveform.

The dI_C/dt is given by:

$$\frac{dI_C}{dt} = \tau_a^2 G_m(V_{GG}-V_{th})te^{\tau_a(t-t_0)} \tag{18}$$

In this phase, the dI_C/dt generates a voltage on the stray inductances $L_E + L_P$, which give rise to the V_{CE} reduction. The V_{CE} and dV_{CE}/dt can thereby be obtained by:

$$V_{CE} = V_{DC} - (L_E+L_P)\frac{dI_C}{dt} \tag{19}$$

$$\frac{dV_{CE}}{dt} = -(L_E+L_P)\frac{d^2 I_C}{dt^2} \tag{20}$$

The phase 1 ends when I_C reaches its peak value $I_L + I_{rr}$, as shown in Fig. 2a. The peak reverse recovery current I_{rr} can be expressed by:

$$I_{rr} = \sqrt{\frac{2Q_{rr}dI_C/dt|_{I_C=I_L}}{1+S}} \tag{21}$$

Q_{rr} is the reverse recovery charge. $S = t_f/t_s$ is the softness factor. Q_{rr}, t_f and t_s are defined in Fig. 4.

B. Phase 2

In phase 2, the collector current I_C of the low-side IGBT is mainly determined by the reverse recovery behaviour of the high-side freewheeling diode. Since the FS IGBT often use a silicon p-i-n diode as its freewheeling diode, I_C can thereby be express by [25]:

$$I_C = I_L + I_{RR}\exp\left(-\frac{t-t_1}{T_R}\right) \tag{22}$$

Where T_R is the reverse recovery time constant [25].

The dI_C/dt can thereby be obtained by:

$$\frac{dI_C}{dt} = -\frac{I_{RR}}{T_R}\exp\left(-\frac{t-t_1}{T_R}\right) \tag{23}$$

As shown in Fig. 3c, the load current I_L is supported by I_C and the displacement current on the output capacitance of high-side IGBT C_{OSS2}. I_L can thereby be expressed as:

$$I_L = I_C + C_{OSS2}\frac{dV_{D2}}{dt}$$

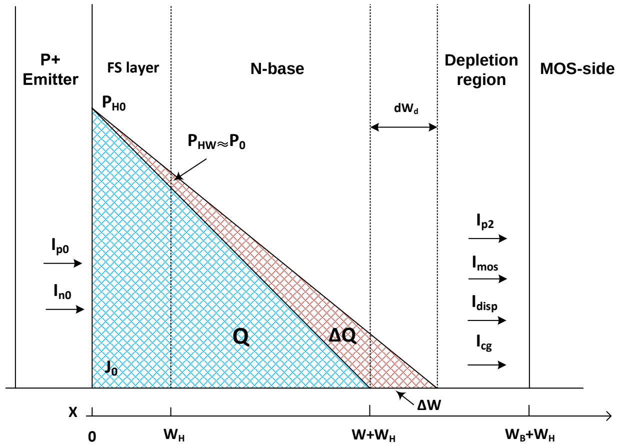


Fig. 5. Coordinate diagram of FS IGBT at phase 2 with boundary condition definition.

$$\approx I_C + C_{OSS2}\frac{dV_{CE}}{dt} \tag{24}$$

The output capacitance $C_{OSS2} = C_{CE2} + C_{GC2}$. The C_{CE2} and C_{GC2} can be obtained by (1) and (2), respectively.

In (24), $dV_{D2}/dt \approx dV_{CE}/dt$ is assumed. In phase 2, the freewheeling diode starts to support reverse voltage, its voltage V_{D2} thereby increases reversely, which causes the reduction of V_{CE}. Therefore, $dV_{CE}/dt \approx dV_{D2}/dt$ can be assumed.

As shown in Fig. 3c, the collector current I_C can be expressed as:

$$I_C = I_{CH} + (C_{CE1} + C_{GC1})\frac{dV_{CE}}{dt} - I_Q \tag{25}$$

Where I_Q is the capacitive current due to the increase of excess charge Q in the N-base and FS layer.

To calculate the I_Q, the excess carrier dynamic in the N-base and FS layer should be obtained. In phase 2, the excess carrier flood in the undepleted N-base and FS layer. As shown in Fig. 2b, the excess carrier density in the FS layer at T_3-T_8 in phase 2 is $2\times10^{15} - 2\times10^{16}\ cm^{-3}$, which is in the same order or surpasses FS layer doping concentration ($10^{15} - 10^{16}\ cm^{-3}$) [3], [4]. Therefore, high-level injection assumption should be adopted for the FS layer in the FS IGBT modeling [10], [20], [26]–[28]. Fig. 5 defines the excess carrier density P_0 at $x = W_H$ in the N-base and excess carrier density P_{HW} at $x = W_H$ in the FS layer. Due to the high-level injection condition, the P_0 becomes very close to P_{HW}, as shown in Fig. 2b. $P_{HW} \approx P_0$ can be assumed to simplify the model [10].

During the turn-on transient, the excess carrier in the N-base and FS layer can be assumed to be linearly distributed [29], as shown in Fig. 5. With $P_{HW} \approx P_0$, the excess carrier $p(x,t)$ in the N-base and FS layer can be expressed as:

$$p(x,t) = P_{H0}(1 - \frac{x}{W + W_H}) \tag{26}$$

Where P_{H0} is the excess carrier density at $x = 0$. $W = W_B - W_d$ is the undepleted N-base width. W_B is the N-base width. W_d is the depletion region width, which can be calculated by [30]:

$$W_d = \sqrt{\frac{2\epsilon_{si}V_{CE}}{qN_B}} \tag{27}$$

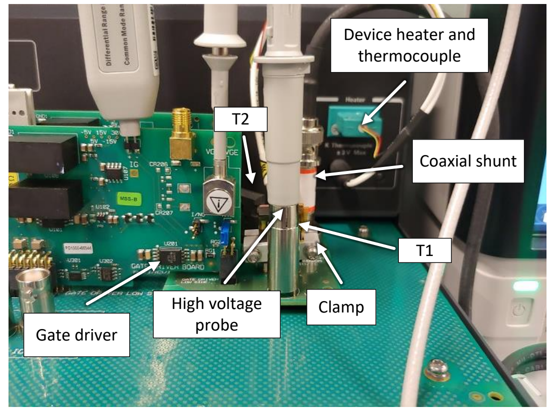


Fig. 6. Double-pulse test fixture.

As shown in Fig. 5, the excess charge Q in the N-base and FS layer can be derived:

$$Q = qA\int_0^{W+W_H} p(x,t)dx = \frac{qA(W+W_H)P_{H0}}{2} \tag{28}$$

The capacitive current I_Q can thereby be calculated by (27) and (28):

$$\begin{aligned} I_Q =& \frac{dQ}{dt} = \frac{qAP_{H0}}{2}\frac{dW}{dt} \\ =& -\frac{A\epsilon_{si}P_{H0}}{2W_dN_B}\frac{dV_{CE}}{dt} \\ =& -C_Q\frac{dV_{CE}}{dt} \end{aligned} \tag{29}$$

Where the C_Q is the equivalent capacitance due to the excess charge build up, which can be expressed as:

$$C_Q = \frac{A\epsilon_{si}P_{H0}}{2W_dN_B} \tag{30}$$

To obtain the capacitance C_Q, the P_{H0} should be obtained. Due to the hole injection at FS layer/P+ emitter junction, the P_{H0} achieves its static-state level and approximately maintains constant in phase 2, as shown in Fig. 2b at T_2-T_8. The static-state value of P_{H0} can thereby be used in (30) to model the C_Q. The solution of P_{H0} is presented in the Appendix.

To include the I_{CG} induced negative feedback action, the (31) is utilized.

$$V_{GE} = V_{GG} + R_GC_{GC1}\frac{V_{CE}}{dt} \tag{31}$$

Combing the (24), (25), (29) and (31), then dV_{CE}/dt can be obtained by:

$$\frac{dV_{CE}}{dt} = \frac{I_L - G_m(V_{GG} - V_{th})}{C_{CE1} + C_Q + C_{OSS2} + C_{GC1}(1 + G_mR_G)} \tag{32}$$

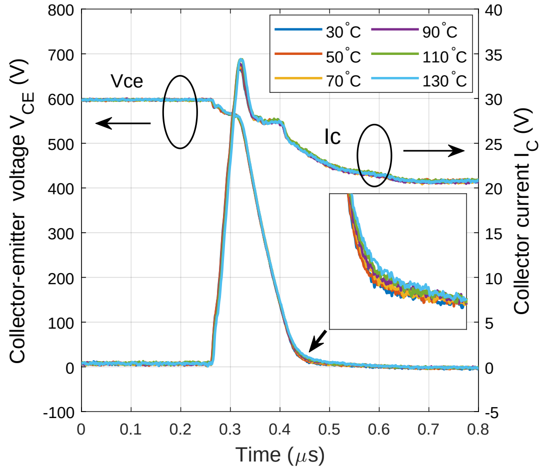


Fig. 7. Experimental turn-on waveforms of IKW40N120CS6 when the T_{J1} varies from 30°C to 130°C while $T_{J2} = 30°C$.

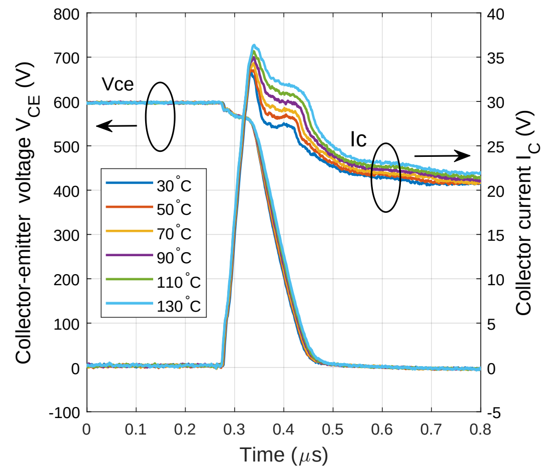


Fig. 9. Experimental turn-on waveforms of IKW40N120CS6 when the T_{J2} varies from 30°C to 130°C while $T_{J1} = 30°C$

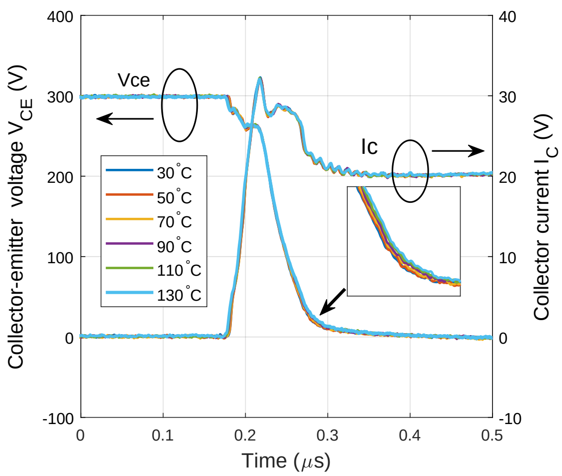


Fig. 8. Experimental turn-on waveforms of IKW40N65ET7 when the T_{J1} varies from 30°C to 130°C while $T_{J2} = 30°C$

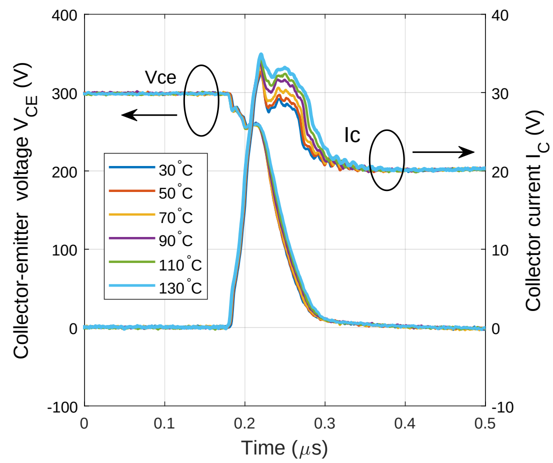


Fig. 10. Experimental turn-on waveforms of IKW40N65ET7 when the T_{J2} varies from 30°C to 130°C while $T_{J1} = 30°C$

IV. Temperature Dependency on the turn-on behaviour

To identify the impact of temperature on the IGBT, the double-pulse test is performed on a 1200V FS IGBT IKW40N120CS6 and a 650V FS IGBT IKW40N65ET7. Fig. 6 shows the double-pulse test fixture. The corresponding circuit schematic is given in Fig. 3a. In the test, a clamp is used to attach the device to a heater, which is used to heat up the junction temperature T_{J1} of low-side IGBT T_1 and the junction temperature T_{J2} of high-side IGBT T_2. The heater is integrated with a thermocouple, which can monitor the junction temperature of the devices.

The double-pulse test is first performed to identify the impact of junction temperature T_{J1} on the turn-on behaviour of FS IGBT. In the test, the T_{J2} of the high-side IGBT is kept at 30°C, while the T_{J1} of low-side IGBT is heated to various temperatures (30°C, 50°C, 70°C, 90°C, 110°C and 130°C). Figs. 7 and 8 show the experimental turn-on waveforms of IKW40N120CS6 and IKW40N65ET7, respectively. It can be noticed that T_{J1} does not have a significant impact on the dI_C/dt. With the increase in T_{J1}, dV_{CE}/dt also does not significantly change except for the stage when V_{CE} drops to tens of volts. This is because the excess carrier cannot fully build up in the entire N-Base until V_{CE} drops to tens of volts, as shown in the excess carrier density profile in Fig. 2b at T_5 - T_8. In the stage when excess carrier built-up is achieved, the T_{J1} can affect the dV_{CE}/dt since excess carrier lifetime is temperature dependent. However, the impact is still relatively minor and the impact of T_{J1} on the turn-on behaviour is neglected in this research.

The double-pulse test is also performed to identify the impact of junction temperature T_{J2} on the turn-on behaviour of FS IGBT. In the test, T_{J1} is set to 30°C, while the T_{J2} is heated to various temperatures range from 30°C to 130°. Figs. 9 and 10 show the test results of IKW40N120CS6 and IKW40N65ET7, respectively. With the increase of T_{J2}, the excess charge in the N-base of the anti-paralleled pin diode increases, which affects the reverse recovery behaviour of the diode. As a result, the dI_C/dt strongly depends on the T_{J2} in phase 2 when I_C recovers from its peak value to I_L. The temperature dependency of dI_C/dt on T_{J2} should be considered. It should be noticed that T_{J2} also has an insignificant impact on dV_{CE}/dt. As shown in Figs. 9 and 10, the dV_{CE}/dt slightly reduces with the increase of T_{J2}. However, since the reduction is relatively tiny, the temperature dependency of dV_{CE}/dt on T_{J2} is thereby neglected.

To include the temperature dependency of dI_C/dt on T_{J2} in phase 2, the temperature-dependent model of reverse recovery charge Qrr and softness factor S are utilized. The Qrr increase with the increase of junction temperature and can be described by (33) [31].

$$Q_{rr}(T_J) = Q_{rr0}(\frac{T_J}{T_0})^{\alpha} \tag{33}$$

Where α is the temperature-dependent coefficient. Q_{rr0} is reverse recovery charge at T_0.

With the increase of junction temperature, the softness factor also increases. In this study, the softness factor S is described by:

$$S(T_J) = S_0(\frac{T_J}{T_0})^{\beta} \tag{34}$$

Where β is the temperature-dependent coefficient. S_0 is the softness factor at T_0.

V. Parameter Extraction

In order to use the proposed model, the model parameters should be extracted. Table I shows the parameter extraction methods. In this study, the die area A is obtained by direct measurement. The IGBT parameters h_p, W_H, V_{th}, G_m, a_i, W_B, N_B and τ, are extracted based on the method presented in [32]–[34]. The diode parameters T_R, Q_{rr0}, S_0, α and β are extracted from the reverse recovery waveforms of the antiparallel diode [25], [35], [36]. The stray inductances L_E and L_P are extracted based on the methods proposed in [32], [37], [38].

TABLE I
PARAMETER EXTRACTION

Parameters	Extraction method
A	Open the package and measure.
V_{th}, G_m	From I-V characteristic curves [32].
a_i	From the reverse transfer capacitance C_{res} and output capacitance C_{oss} [32].
h_p	The empirical range of h_{p0} is $10^{-14} - 10^{-12} cm^4 s^{-1}$ [33]. Accurate values can be extracted by tail current [32]
W_B and N_B	From breakdown voltage [32].
N_H	W_H is about $4 - 10\mu s$ [3], [4]. Accurate values can be extracted by tail current [32]
τ	From decay rate of tail current [32], [34].
T_R, Q_{rr0}, S_0, α and β	From the reverse recovery waveforms [25], [35], [36].
L_E	Typical value of L_E is presented in [37]. Accurate values can be extracted by the methods proposed in [32], [38].
L_P	From dI_C/dt and overshoot voltage at turn-off transient [32].

VI. Experimental validation

In this section, the double-pulse test is performed on a 1200V/40A FS IGBT IKW40N120CS6 and a 650V/40A FS IGBT IKW40N65ET7. The double-pulse test fixture and equivalent schematic circuit utilized are presented in Figs. 6 and 3a, respectively. The low-side gate drives V_{gg1} switches with 15V/0, whereas the high-side gate drives V_{gg2} is set to 0V. A 500 MHz high voltage probe 10076C is used to measure the collector-emitter voltage V_{CE}. The collector current I_C is measured by a 400 MHz coaxial shunt resistor SSDN-414-01. In the test, various values of DC-bus voltage, load current and junction temperature are utilized to obtain the experimental waveforms of V_{CE} and I_C . Based on the proposed model, the V_{CE}, I_C, dV_{CE}/dt and dI_C/dt are also analytically derived and compared with the experimental data.

A. Comparison on Turn-on Transient Characteristics at 30 °C

At first, the double-pulse test is performed on the FS IGBT IKW40N120CS6 at 30°C. In the test, the gate resistor $R_G = 10\Omega$, the DC-bus voltage $V_{DC} = 600V$ and the load current I_L is set to 20A, 30A and 40A. Based on the proposed FS IGBT turn-on model, the turn-on waveforms of IKW40N120CS6 at 600V/20A, 600V/30A and 600V/40A at 30°C are obtained. Fig. 11 compares the experimental and analytical derived waveforms and good agreement is obtained.

At 30°C, the double-pulse test is also performed on the FS IGBT IKW40N65ET7 with $V_{DC} = 300V$ and I_L set to 20A, 30A and 40A. The experimental and analytical derived waveforms of IKW40N65ET7 are compared in Fig. 12 and good agreement is obtained. In Figs. 11 and 12, the good match between analytically derived results and test data proves that the proposed FS IGBT model can provide reasonable prediction on the turn-on behaviour of FS IGBT.

B. Comparison on Turn-on Transient Characteristics at Various Temperatures

To validate the temperature dependency of the proposed model, the double-pulse test is also performed with the various junction temperatures utilized. Fig. 13 compare the analytical derived and experimental waveforms of IKW40N120CS6 when T_{J2} is set to 80 °C and 130°C. The analytical derived results agree with the experimental turn-on waveforms of IKW40N120CS6.

Fig. 14 shows the experimental and analytical derived turn-on waveforms of IKW40N65ET7 with various T_{J2} utilized. The experimental data of IKW40N65ET7 agree with the analytical derived results. The good agreements of the analytical and test results validate the proposed FS IGBT model can capture the temperature dependency on the turn-on behaviour of FS IGBT.

In Figs. 11-14, an oscillation occur when the I_C snaps back from its peak value to I_L. The oscillation is related to the

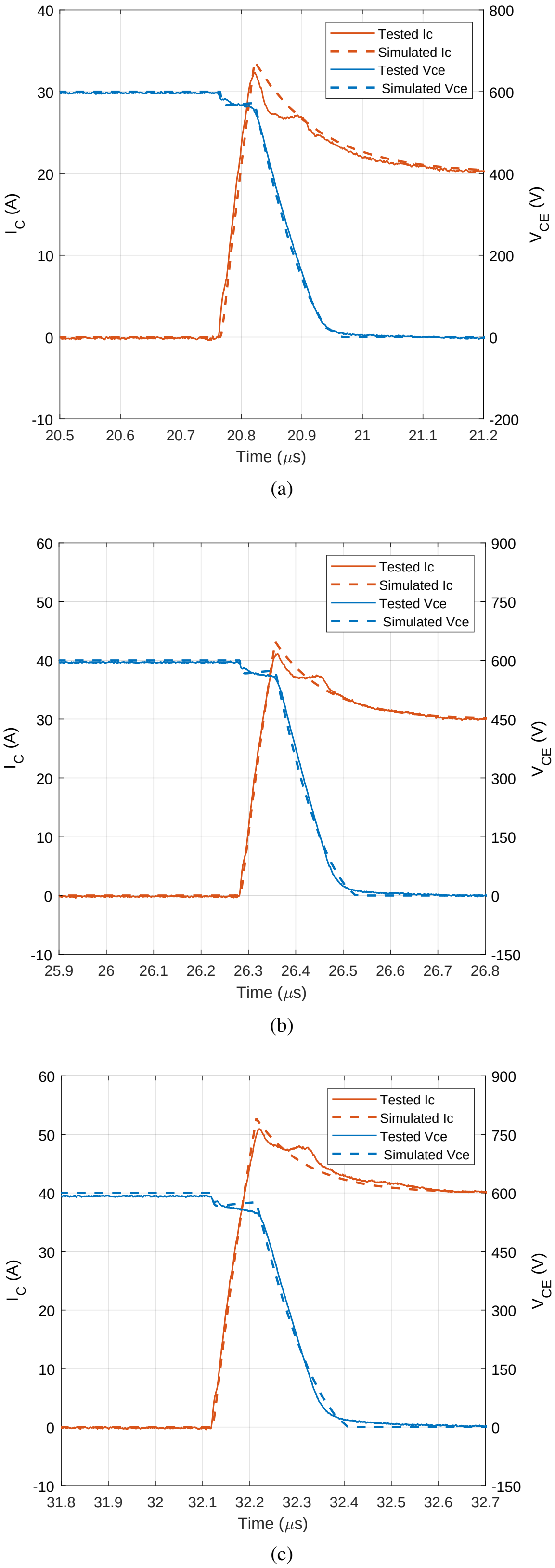


Fig. 11. The experimental and analytical derived waveforms of IKW40N120CS6 with $R_G = 10\Omega$ at (a) 600V/20A. (b) 600V/30A. (c) 600V/40A.

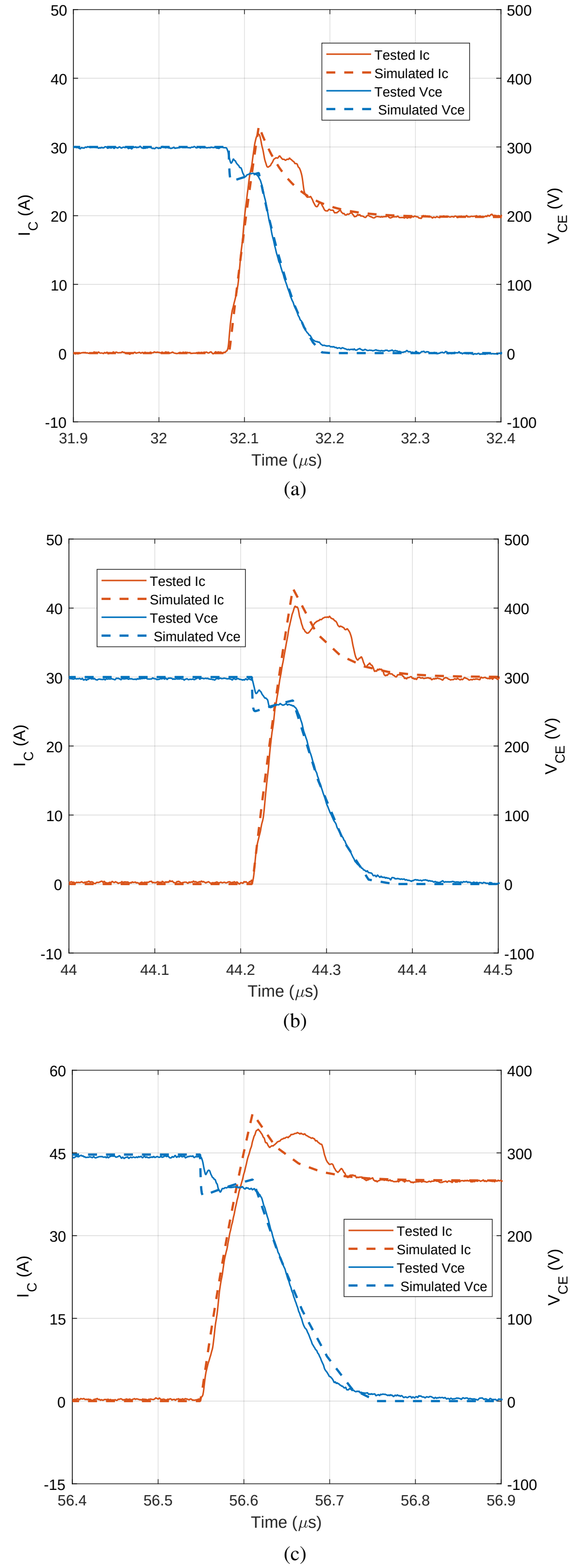
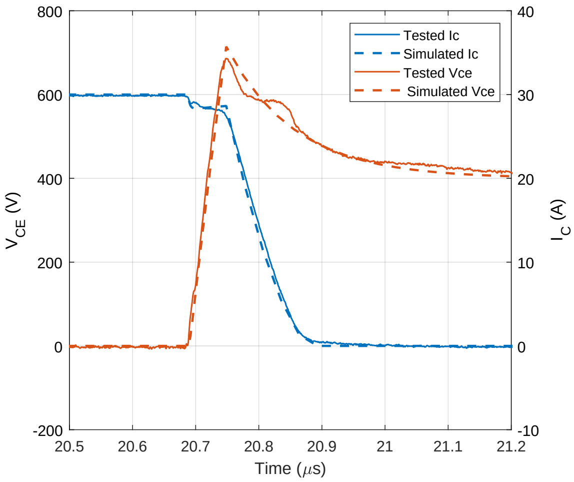
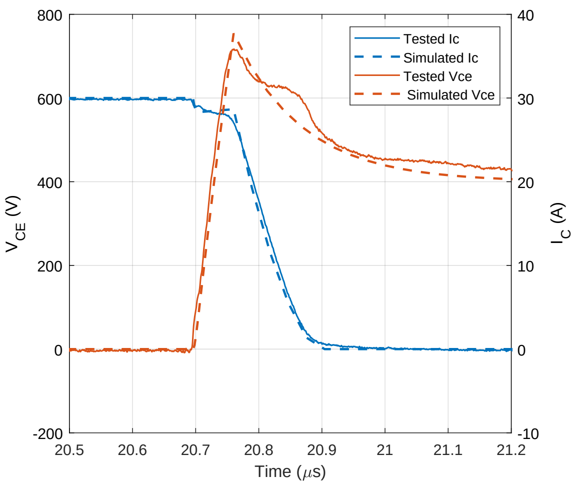


Fig. 12. Comparison of experimental and analytical derived waveforms of IKW40N65ET7 with $R_G = 10\Omega$ at (a) 300V/20A. (b) 300V/30A. (c) 300V/40A.

resonance of circuit stray elements and residual excess charge redistribution in the N-base of the freewheeling diode. During the turn-on transient, the high-side freewheeling diode has to support reverse voltage and its depletion region in the N-

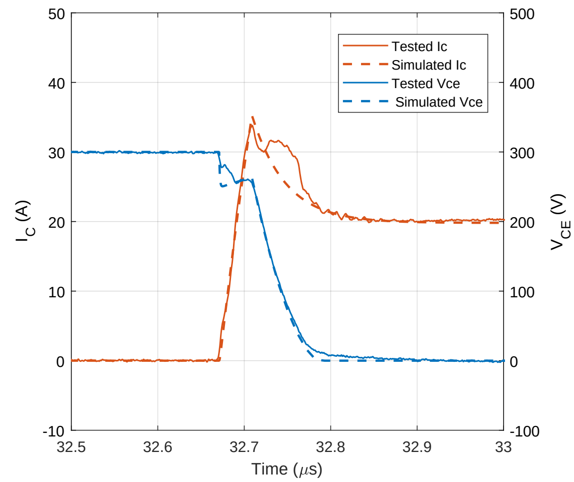


(a)

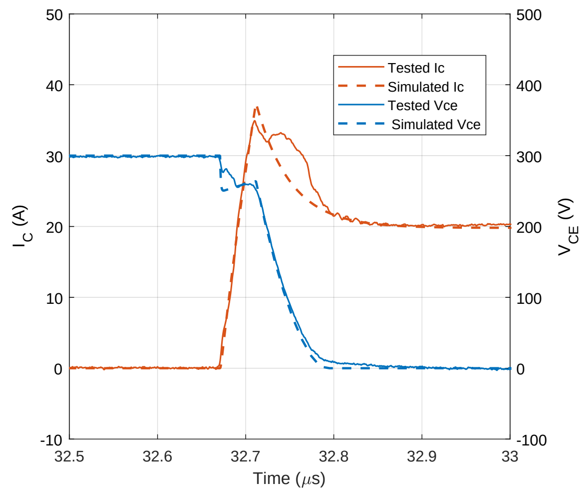


(b)

Fig. 13. The experimental and analytical derived 600V/20A turn-on waveforms of IKW40N120CS6 with $R_G = 10\Omega$ when T_{J2} sets to (a) 80°C. (b) 130°C.



(a)



(b)

Fig. 14. The experimental and analytical derived 300V/20A turn-on waveforms of IKW40N65ET7 with $R_G = 10\Omega$ when T_{J2} sets to (a) 80°C. (b) 130°C.

base extends. The residual excess charge in the N-base has to redistribute, which generates strong effective damping on the oscillation. Due to the damping effect, the oscillation quickly attenuates and thereby has a relatively minor impact on the switching behaviour. As a result, the oscillation is neglected in this research.

C. Comparison on dV_{CE}/dt and dI_C/dt

Figs. 15 and 16 compared the experimental and calculated dV_{CE}/dt of IKW40N120CS6 and IKW40N65ET7. In Fig. 15, the dV_{CE}/dt is extracted from the test waveforms of IKW40N120CS6 presented in Figs. 11 when V_{CE} equals 100V, 200V, 300V and 400V. With the test waveforms of IKW40N65ET7 presented in Fig. 12 utilized, the dV_{CE}/dt is extracted when V_{CE} equals 50V, 100V, 150V and 200V, as shown in Fig. 16. At each V_{CE} level, the dV_{CE}/dt is also calculated based on the proposed model. The error of the proposed model can be obtained by (35).

$$\text{Error} = \frac{\text{Proposed model} - \text{Experimental data}}{\text{Experimental data}} \tag{35}$$

As shown in Figs. 15 and 16, the errors of calculated dV_{CE}/dt are within 9% for IKW40N120CS6 and 14% for IKW40N65ET7. The test results agree with the calculated values of dV_{CE}/dt.

Figs. 17 and 18 compares the experimental and analytical calculated dI_C/dt of IKW40N120CS6 and IKW40N65ET7. The dI_C/dt is extracted at different I_C levels depending on the load current I_L. When $I_L = 20A$, the dI_C/dt is extracted at 5A, 10A, 15A and 20A. When $I_L = 30A$, the dI_C/dt is extracted at 7A, 14A, 21A and 28A. When $I_L = 40A$, the dI_C/dt is extracted at 10A, 20A, 30A and 40A. At each I_C level, the dI_C/dt is also calculated based on the proposed model. The comparison shows the errors of calculated dI_C/dt are within 5% for IKW40N120CS6 and 9% for IKW40N65ET7. The calculated values of dI_C/dt agree with the test data.

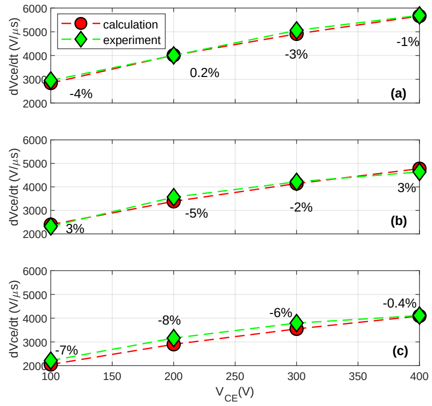


Fig. 15. Comparison of experimental and analytical calculated dV_{CE}/dt of IKW40N120CS6 on various V_{CE} levels for the test performed at (a) 600V/20A. (b) 600V/30A. (c) 600V/40A.

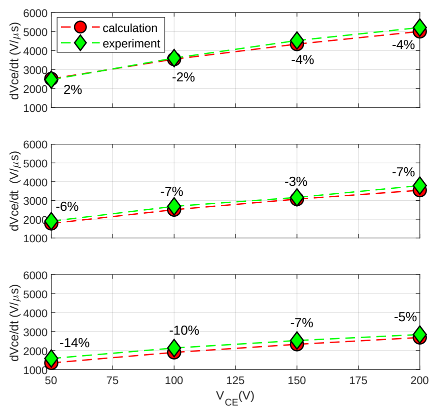


Fig. 16. Comparison of experimental and analytical calculated dV_{CE}/dt of IKW40N65ET7 on various V_{CE} levels for the test performed at (a) 300V/20A. (b) 300V/30A. (c) 300V/40A.

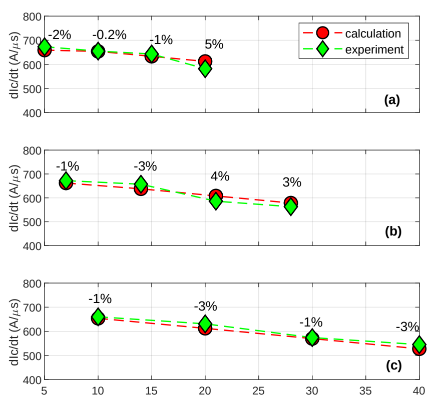


Fig. 17. Comparison of experimental and analytical calculated dI_C/dt of IKW40N120CS6 on various I_C levels for the test performed at (a) 600V/20A. (b) 600V/30A. (c) 600V/40A.

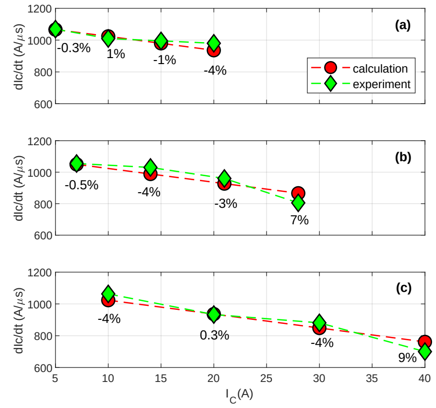


Fig. 18. Comparison of experimental and analytical calculated dI_C/dt of IKW40N65ET7 on various I_C levels for the test performed at (a) 300V/20A. (b) 300V/30A. (c) 300V/40A.

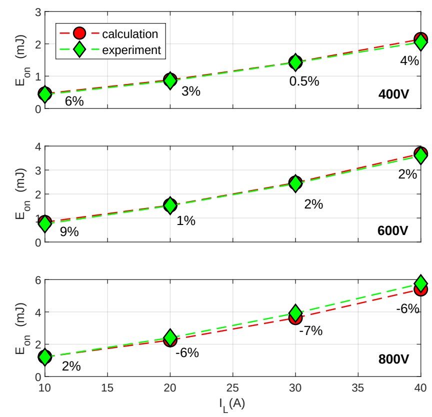


Fig. 19. Comparison of experimental and analytical calculated turn-on losses of IKW40N120CS6 at 400V, 600V and 800V with $R_G = 10\Omega$.

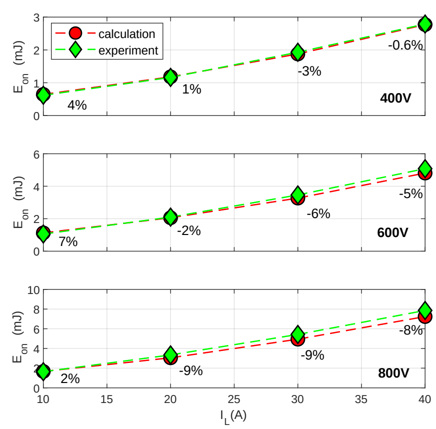


Fig. 20. Comparison of experimental and analytical calculated turn-on losses of IKW40N120CS6 at 400V, 600V and 800V with $R_G = 20\Omega$.

D. Comparison on Turn-on losses

Based on the experimental and analytical derived turn-on waveforms, turn-on losses E_{on} are calculated by the time integration on the products of V_{CE} and I_C. The error of the calculated results are also obtained.

Figs. 19 and 20 show the experimental and analytical calculated turn-on losses of IKW40N120CS6 utilizing various V_{DC} (400V, 600V and 800V) and R_G (10Ω and 20Ω). It can be noticed that the calculated E_{on} is very close to the experimental data. The difference between the experimental and calculated E_{on} is within 9%.

Figs. 21 and 22 show the experimental and analytical calculated turn-on losses of IKW40N65ET7 utilizing various

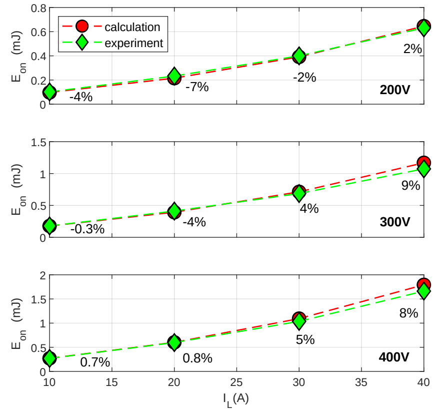


Fig. 21. Comparison of experimental and analytical calculated turn-on losses of IKW40N65ET7 at 200V, 300V and 400V with $R_G = 10\Omega$.

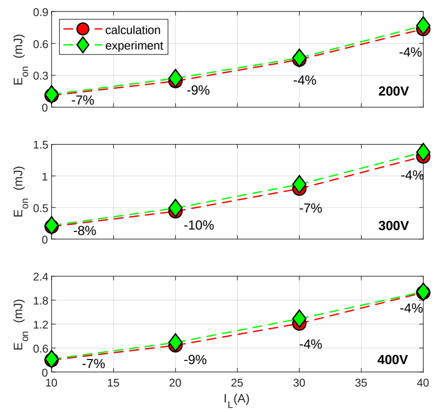


Fig. 22. Comparison of experimental and analytical calculated turn-on losses of IKW40N65ET7 at 200V, 300V and 400V with $R_G = 20\Omega$.

V_{DC} (200V, 300V and 400V) and R_G (10Ω and 20Ω).The difference between the experimental and calculated E_{on} is within 10%.

Fig. 23 compares experimental and analytical calculated turn-on losses of IKW40N120CS6 when T_{J2} is 30°C, 80°C and 130°C with $V_{DC} = 600V$ and $R_G = 10\Omega$. In Fig. 24, the experimental and analytical calculated turn-on losses of IKW40N65ET7 when T_{J2} is 30°C, 80°C and 130°C with $V_{DC} = 300V$ and $R_G = 10\Omega$ are presented. The difference between the experimental and calculated E_{on} is within 9%. The turn-on losses comparison shown in Figs. 19 - 24 validate that the proposed model can make an accurate prediction on the turn-on losses of FS IGBT.

In Fig. 21, the calculated turn-on losses of IKW40N65ET7 has maximum error (9%) at 300V/20A. To show the origin of the error, the related power waveform ($I_C \times V_{CE}$) is plotted, as shown in Fig. 25. In the power waveform, errors occur in the regions A1, A2 and A3. The error in region A1 is due to the discrepancy between the calculated and experimental dI_C/dt and I_{rr} in the region. The oscillation of I_C in the experimental waveforms gives rise to the error in region A2. In region A3, the error is induced by the discrepancy between the calculated and experimental dV_{CE}/dt. Despite the errors, the calculated power waveform agrees with the test result in

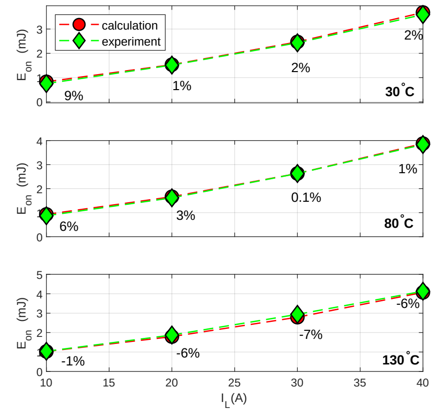


Fig. 23. Comparison of experimental and analytical calculated turn-on losses of IKW40N120CS6 when T_{J2} is 30°C, 80°C and 130°C with $V_{DC} = 600V$ and $R_G = 10\Omega$.

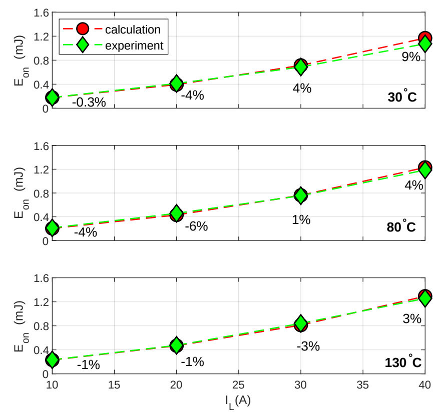


Fig. 24. Comparison of experimental and analytical calculated turn-on losses of IKW40N65ET7 when T_{J2} is 30°C, 80°C and 130°C with $V_{DC} = 300V$ and $R_G = 10\Omega$.

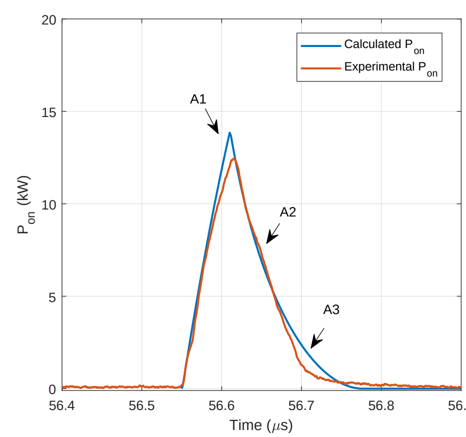


Fig. 25. Comparison of experimental and analytical calculated power waveform of IKW40N65ET7 at 300V/20A with $R_G = 10\Omega$.

the other phases of the turn-on transient.

E. Comparison of the proposed and previous IGBT models

With various critical internal and external device physics included, the proposed model should have better accuracy

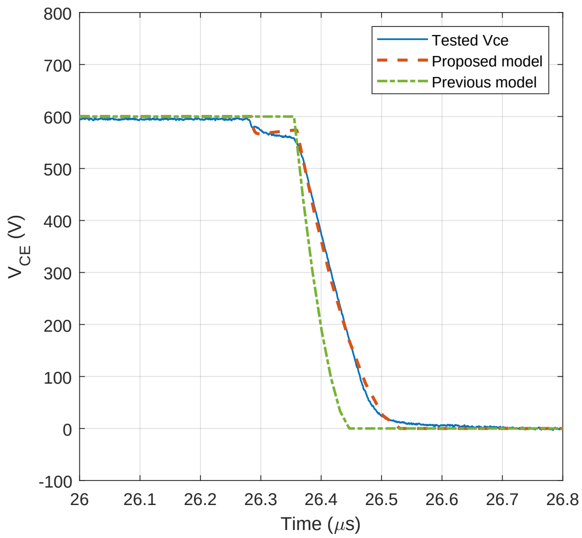


Fig. 26. Comparison between previous and proposed dV_{CE}/dt model at turn-on transient.

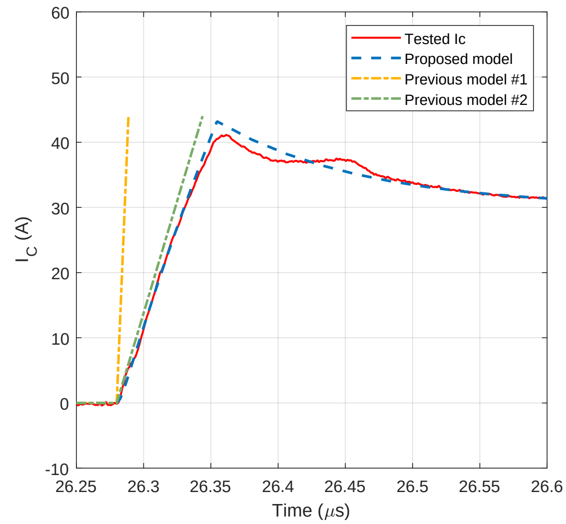


Fig. 27. Comparison between previous and proposed dI_C/dt model at turn-on transient.

compared to the previously proposed IGBT models. To validate this, the proposed model is compared with the previous IGBT models. In the previous research [5], [14]–[19], (36) is widely utilized to model the dV_{CE}/dt at turn-on transient.

$$\frac{dV_{CE}}{dt} = -\frac{V_{gg} - V_{th} - I_L/G_m}{C_{GC}R_G} \tag{36}$$

Fig. 26 compares this dV_{CE}/dt model with the proposed model. It can be noticed that the proposed model is much more accurate than the previous model. The dV_{CE}/dt derived by (36) is much steeper than the test data. This is mainly because the previous model does not include capacitive current I_Q generated by the excess carrier built-up in the N-base and FS layer. The lack of considering the displacement current on the C_{OSS2} and C_{CE1} also contribute to the error.

In the previous research, two dI_C/dt models are widely utilized for IGBT turn-on modeling. The model #1 proposed in [16]–[19] is expressed as:

$$\frac{dI_C}{dt} = G_m\frac{V_{gg} - V_{th} - I_P/2G_m}{(C_{GC} + C_{GE})R_G} \tag{37}$$

The model #2 proposed in [5], [14], [15] is given by:

$$\frac{dI_C}{dt} = G_m\frac{V_{gg} - V_{th}}{(C_{GC} + C_{GE})R_G + G_mL_E} \tag{38}$$

Fig. 27 compares the proposed model, model #1 and model #2. It can be noticed that model #1 is very inaccurate. This is because the model #1 does not consider the negative feedback action induced by the L_E. With L_E included, the model #2 can provide a much more accurate result than that of the model #1. However, compared with the proposed model, the model #2 still has a significant error. This is because the proposed model includes all the stray elements which have a significant impact on the dI_C/dt.

VII. Conclusion

The contribution of this paper is the introduction of a complete expression of dV_{CE}/dt and dI_C/dt at the turn-on transient of FS IGBT. The proposed FS IGBT model considers the internal device physics like the excess carrier built-up in the N-base and FS layer. All the critical external stray elements are also considered in the model. Based on the double-pulse test, the reverse recovery charges Qrr and softness factor S are identified to be pivotal temperate-dependent parameters. The temperature-dependent model of Qrr and S are thereby proposed to include the temperature-dependent effect.

In the end, the proposed model is validated by the double-pulse test performed under a wide range of test conditions. The comparison of the analytical derived and experimental results verifies the accuracy of the proposed model. The proposed model is also compared with the currently available IGBT model, which demonstrates the proposed model can provide a much more accurate prediction than the previous models.

Appendix
FS Layer Excess Carrier Density P_{H0}

Under static state, the excess carrier $p(x,t)$ in the N-base and FS layer can be expressed as [10]:

$$p(x,t) = P_{H0}\frac{sinh[(W_B + W_H - x)/L]}{sinh((W_B + W_H)/L)} \tag{39}$$

Where $L = \sqrt{D\tau}$. τ is the carrier lifetime in the N-base. D is the ambipolar diffusion coefficient. The electron current I_{n0} is expressed as:

$$\begin{aligned} I_{n0} &= \frac{bI_L}{1+b} + qAD\frac{\partial p(x,t)}{\partial x}\bigg|_{x=0} \\ &= \frac{bI_L}{1+b} - \frac{qADP_{H0}}{L}coth(\frac{W_B + W_H}{L}) \end{aligned} \tag{40}$$

Where $b = \mu_n/\mu_p$. μ_n and μ_p are the election and hole mobilities of silicon.

The electron current I_{n0} is generated due to the minority carriers recombination and can also be expressed as [39]:

$$I_{n0} = qAh_pP_{H0}^2 \tag{41}$$

Where h_p is the recombination parameter at the P+ emitter.

Combining equations (40) and (41), the P_{H0} can be solved as:

$$P_{H0} = \frac{K}{2h_p}(\sqrt{1 + \frac{4bh_pI_L}{(1+b)qAK^2}} - 1) \tag{42}$$

Where

$$K = \frac{D}{L}coth(\frac{W_B + W_H}{L}) \tag{43}$$

References

[1] M. Ishiko, S. Kawaji, K. Nishiwaki, and T. Ohnishi, "A PT-IGBT with a p-/n+ buffer layer," in *ISPSD'03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs, 2003. Proceedings.*, 2003, pp. 341–344, DOI: 10.1109/ISPSD.2003.1225297.

[2] K. Nakamura, S. Kusunoki, H. Nakamura, Y. Ishimura, Y. Tomomatsu, and T. Minato, "Advanced wide cell pitch CSTBTs having light punch-through (LPT) structures," in *Proc. ISPSD*, 2002, pp. 277–280, DOI: 10.1109/ISPSD.2002.1016225.

[3] T. Laska, M. Munzer, F. Pfirsch, C. Schaeffer, and T. Schmidt, "The field stop IGBT (FS IGBT)- a new power device concept with a great improvement potential," in *Proc. ISPSD Conf.*, 2000, pp. 355–358, DOI: 10.1109/ISPSD.2000.856842.

[4] J. G. Bauer, F. Auerbach, A. Porst, R. Roth, H. Ruething, and O. Schilling, "6.5 kV-modules using IGBTs with field stop technology," in *Proc. ISPSD Conf.*, 2001, pp. 121–124, DOI: 10.1109/ISPSD.2001.934571.

[5] M. Jin and M. Weiming, "Power converter EMI analysis including IGBT nonlinear switching transient model," *IEEE transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1577–1583, 2006, DOI: 10.1109/TIE.2006.882009.

[6] X. Yang, Y. Yuan, X. Zhang, and P. R. Palmer, "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1669–1677, 2014, DOI: 10.1109/TIA.2014.2347578.

[7] J. Yedinak, J. Gladish, B. Brockway, S. Shekhawat, P. Shenoy, D. Lange, G. Dolny, and M. Rinehimer, "A 600V quick punch through (QPT) IGBT design concept for reducing EMI," in *ISPSD*, 2003, pp. 67–70, DOI: 10.1109/ISPSD.2003.1225232.

[8] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 235–247, 2011, DOI: 10.1109/TPEL.2011.2160988.

[9] A. Bryant, S. Yang, P. Mawby, D. Xiang, L. Ran, P. Tavner, and P. R. Palmer, "Investigation into igbt dv/dt during turn-off and its temperature dependence," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3019–3031, 2011, DOI: 10.1109/TPEL.2011.2125803.

[10] Y. Chen, H. Luo, W. Li, X. He, F. Iannuzzo, and F. Blaabjerg, "Analytical and Experimental Investigation on A Dynamic Thermo-Sensitive Electrical Parameter With Maximum dI_C/dt During Turn-off for High Power Trench Gate/Field-Stop IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6394–6404, 2016.

[11] A. Ramamurthy, S. Sawant, and B. Baliga, "Modeling the [dV/dt] of the IGBT during inductive turn off," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 601–606, 1999, DOI: 10.1109/63.774195.

[12] A. Das, N. Islam, M.-u. Haq, and Z. R. Khan, "Transient anode voltage modeling of IGBT and its carrier lifetime dependence," in *TENCON*. IEEE, 2015, pp. 1–5, DOI: 10.1109/TENCON.2015.7372970.

[13] S.-H. Ryu, H.-K. Lee, H.-K. Ahn, and D.-Y. Han, "Modeling of Anode Voltage Drop for PT-IGBT at Turn-off," *Journal of the Korean Institute of Electrical and Electronic Material Engineers*, vol. 21, no. 1, pp. 23–28, 2008, DOI: jkem.2008.21.1.023.

[14] S. Park and T. M. Jahns, "Flexible dv/dt and di/dt control method for insulated gate power switches," in *36th IAS Annual Meeting*, vol. 2, 2001, pp. 1038–1045, DOI: 10.1109/IAS.2001.955592.

[15] G. Zou and Z. Zhao, "Research on impacts of different parameters on transient power loss of IGBT," in *ICEMS*. IEEE, 2013, pp. 490–495, DOI: 10.1109/ICEMS.2013.6713115.

[16] F. Blaabjerg, J. K. Pedersen, P. O. Lauritzen, and C. L. Ma, "Optimum design and test of a snubberless IGBT PWM-VSI inverterbridge," in *Proceedings of 1994 IEEE Industry Applications Society Annual Meeting*, vol. 2, 1994, pp. 795–804, DOI: 10.1109/IAS.1994.377509.

[17] H. Liu, J. Ma, H. Ma, and Z. Bai, "Improved switching loss calculation in neutral point clamped inverter via waveforms linearization," in *2013 IEEE International Symposium on Industrial Electronics*, 2013, pp. 1–6, DOI: 10.1109/ISIE.2013.6563632.

[18] F. Blaabjerg and J. K. Pedersen, "Optimized design of a complete three-phase pwm-vs inverter," *IEEE Transactions on Power Electronics*, vol. 12, no. 3, pp. 567–577, 1997, DOI: 10.1109/63.575684.

[19] A. I. Maswood, "A switching loss study in spwm igbt inverter," in *2008 IEEE 2nd International Power and Energy Conference*, 2008, pp. 609–613, DOI: 10.1109/PECON.2008.4762548.

[20] P. Xue, G. Fu, and D. Zhang, "Modeling inductive switching characteristics of high-speed buffer layer IGBT," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3075–3087, 2016, DOI: 10.1109/TPEL.2016.2570838.

[21] A. T. Bryant, L. Lu, E. Santi, J. L. Hudgins, and P. R. Palmer, "Modeling of IGBT resistive and inductive turn-on behavior," *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 904–914, 2008.

[22] M. Rodríguez, A. Rodríguez, P. F. Miaja, D. G. Lamar, and J. S. Zúniga, "An insight into the switching process of power mosfets: An improved analytical losses model," *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1626–1640, 2010, DOI: 10.1109/TPEL.2010.2040852.

[23] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on mosfet switching characteristics," in *The 2010 International Power Electronics Conference-ECCE ASIA-*. IEEE, 2010, pp. 164–169.

[24] J. Wang, H. S.-h. Chung, and R. T.-h. Li, "Characterization and experimental assessment of the effects of parasitic elements on the mosfet switching performance," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 573–590, 2012.

[25] P. Lauritzen and C. Ma, "A simple diode model with reverse recovery," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 188–191, 1991, DOI: 10.1109/63.76804.

[26] Y. Tang, B. Wang, M. Chen, and B. Liu, "Simulation model and parameter extraction of Field-Stop (FS) IGBT," *Microelectronics Reliability*, vol. 52, no. 12, pp. 2920–2931, 2012, DOI: 10.1016/j.microrel.2012.07.025.

[27] Y. Duan, Y. Kang, F. Iannuzzo, I. Trintis, and F. Blaabjerg, "A temperature dependent lumped-charge model for trench FS-IGBT," in *IEEE APEC*, 2018, pp. 249–254, DOI: 10.1109/APEC.2018.8341018.

[28] G. Fu and P. Xue, "Physics-based model of LPT CSTBT including MOS-side two-dimensional effects," *IET Power Electronics*, vol. 9, no. 5, pp. 1019–1028, 2016, DOI: 10.1049/iet-pel.2015.0479.

[29] A. R. Hefner and D. L. Blackburn, "A performance trade-off for the insulated gate bipolar transistor: Buffer layer versus base lifetime reduction," *IEEE transactions on power electronics*, no. 3, pp. 194–207, 1987, DOI: 10.1109/TPEL.1987.4766360.

[30] P. Xue, G. Fu, and D. Zhang, "Comprehensive physics-based compact model for fast pin diode using MATLAB and Simulink," *Solid-State Electronics*, vol. 121, pp. 1–11, 2016.

[31] H. Luo, Y. Chen, W. Li, and X. He, "Online high-power pin diode junction temperature extraction with reverse recovery fall storage charge," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2558–2567, 2016, DOI: 10.1109/TPEL.2016.2580618.

[32] A. T. Bryant, X. Kang, E. Santi, P. R. Palmer, and J. L. Hudgins, "Two-step parameter extraction procedure with formal optimization for physics-based circuit simulator IGBT and p-i-n diode models," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 295–309, 2006, DOI: 10.1109/TPEL.2005.869742.

[33] T. K. Gachovska, J. L. Hudgins, E. Santi, A. Bryant, and P. R. Palmer, *Modeling Bipolar Power Semiconductor Devices*, ser. Synthesis Lectures on Power Electronics, 2013, vol. 4.

[34] G. Fu and P. Xue, "An excess carrier lifetime extraction method for physics-based igbt models," *Journal of Power Electronics*, vol. 16, no. 2, 2016.

[35] B. Shi, Z. Zhao, and Y. Zhu, "Piecewise analytical transient model for power switching device commutation unit," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5720–5736, 2018, DOI: 10.1109/TPEL.2018.2867735.

[36] O. Al-Naseem, R. W. Erickson, and P. Carlin, "Prediction of switching loss variations by averaged switch modeling," in *APEC*, vol. 1, 2000, pp. 242–248, DOI: 10.1109/APEC.2000.826111.

[37] K. Aikawa, T. Shiida, R. Matsumoto, K. Umetani, and E. Hiraki, "Measurement of the common source inductance of typical switching device packages," in *IFEEC and ECCE Asia*. IEEE, 2017, pp. 1172–1177.

[38] I. Kovacevic-Badstuebner, R. Stark, U. Grossner, M. Guacci, and J. W. Kolar, "Parasitic extraction procedures for SiC power modules," in *International Conference on Integrated Power Electronics Systems*. VDE, 2018, pp. 1–6.

[39] P. R. Palmer, E. Santi, J. L. Hudgins, X. Kang, J. C. Joyce, and P. Y. Eng, "Circuit simulator models for the diode and IGBT with full temperature dependent features," *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1220–1229, 2003.

Peng Xue received the M.S., and Ph.D. degrees from Beihang University, Beijing, China in 2013 and 2017, respectively.

From 2017 to 2019, he works as a Post-Doctoral Research Fellow at University of Naples Federico II, Italy. He is currently a Post-Doctoral researcher at the Aalborg University, Denmark. His research interests include modeling, simulation, and experimental characterization of power semiconductor devices.

Pooya Davari (S11M13-SM19) received the B.Sc. and M.Sc. degrees in electronic engineering in 2004 and 2008, respectively, and the Ph.D. degree in power electronics from QUT, Australia, in 2013. From 2005 to 2010, he was involved in several electronics and power electronics projects as a Development Engineer. From 2013 to 2014, he was with QUT, as a Lecturer. He joined Aalborg University (AAU), in 2014, as a Postdoc, where he is currently an Associate Professor.

He has been focusing on EMI, power quality and harmonic mitigation analysis and control in power electronic systems. He has published more than 180 technical papers. Dr. Davari served as a Guest Associate Editor of IET journal of Power Electronics, IEEE Access Journal, Journal of Electronics and Journal of Applied Sciences. He is an Associate Editor of Journal of Power Electronics, IET Electronics, Editorial board member of Journal of Applied Sciences and Journal of Magnetics. He is member of the International Scientific Committee (ISC) of EPE (ECCE Europe) and a member of Joint Working Group six and Working Group eight at the IEC standardization TC77A. Dr. Davari is the recipient of Equinor 2022 Prize and 2020 IEEE EMC Society Young Professional Award for his contribution to EMI and Harmonic Mitigation and Modeling in Power Electronic Applications. He is currently Editor-in-Chief of Circuit World Journal. He is founder and chair of IEEE EMC SOCIETY CHAPTER DENMARK and Leader of EMI/EMC in Power Electronics Research Group at AAU Energy.