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RESEARCH ARTICLE

A High Step-Up Interleaved Current-Fed Resonant Converter for High-Voltage Applications

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ABSTRACT A current-fed LLC resonant converter is proposed for high-voltage and high-power applications. Here, a two-phase interleaved structure is used in the input stage under the continuous conduction mode (CCM) to effectively reduce the input current and output voltage ripple values and the input filter and the output capacitors volumes. Due to the expandable structure and high voltage gain, the proposed configuration is suitable for high voltage applications since low voltage stresses are applied across its components. In fact, voltage stresses across the power semiconductors, i.e., MOSFETs and output diodes, along with the output capacitors, are almost one-third of the output voltage in the implemented three-stage configuration of the proposed converter. Here, the switching frequency is chosen close to, but less than, the converter series resonant frequency to reduce its different components' current stresses and perform soft-switching operation for all power devices under wide input voltage and output power variations. Therefore, conduction and switching losses, and EMI noises are effectively reduced. Consequently, efficiency is improved and high-frequency operation is possible, which reduces the volume of passive components to achieve high-power density. The given topology is thoroughly analyzed mathematically. Also, a 1 kW prototype converter has been implemented to validate the given simulations and analyses. Here, wide input voltage (100 V-200 V) and output power (100 W-1000 W) variations are applied, and an asymmetric pulse width modulation (APWM) technique is used at 143 kHz switching frequency to regulate the output voltage at 1 kV. The obtained maximum efficiency value is 95.3%.

INDEX TERMS Asymmetric pulse width modulation (APWM), current-fed converter, interleaved technique, LLC resonant converter, multi-winding transformer.

I. INTRODUCTION

Recently, renewable energy sources have been regarded as a solution to the environmental issues [1], [2]. Since depletable energy sources mostly have low and fluctuating output voltage, using a dc-dc step-up power converter is indispensable to both level up and regulate their output voltages [3], [4]. Till now, various converters such as high step-up, high voltage, interleaved, and resonant converters have been introduced to increase voltage gain, output voltage, and output power of the dc-dc converters. The given converters in [5], [6], [7], and [8] that have been introduced for high voltage applications usually use large transformers turn-ratios to obtain high voltage gains, which in practice increase voltage stresses on some output stage components.

On the other hand, although the transformer turn ratios in most of the high step-up converters [4], [9], [10], [11], [12], [13] are lower than the previously referred ones, they still use large transformer turn ratios to obtain high voltage gains. Consequently, these converters also suffer from similar disadvantages, as mentioned earlier. In some other converters [14], [15], where the transformer turn ratios are small, lower voltage gains are obtained in practice.

Interleaved structures [2], [16], [17], [18], [19], [20], [21] are another large category of converters, which are proposed to increase output power, but they often give small output

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voltages, and they are not suitable for high voltage applications. Some of these converters have been used as PFC converters [22], [23], [24].

On the other hand, among the different isolated and non-isolated dc-dc topologies, the full-bridge converter is preferred in many pieces of literature [18], [25], [26], [27], [28]. The soft switching operation is achievable for this converter by phase-shifting without using auxiliary circuits. But, the soft-switching range in conventional phase-shifted full-bridge (PSFB) converter is limited due to the loss of zero voltage switching (ZVS) for primary switches in worst-case conditions. Also, circulating currents power losses are high [29]. Albeit using additional circuits may widen the soft-switching range [30], [31], [32], [33], it leads to higher components count and cost. Resonant-type full-bridge converters can realize soft-switching operation by using resonant tank on the primary side, which can improve the efficiency by eliminating MOSFET-based [28], [34] and IGBT-based [35] converters' turn-on and turn-off switching losses, respectively.

Another one of the most widely used converters is LLC-based resonant converters, which have received much attention from researchers and industry in recent years due to their good features. These resonant converters have low electromagnetic interference (EMI), and they can provide ZVS condition for primary MOSFETs and zero current switching (ZCS) turn-off condition for output diodes when they operate between series-resonance and parallel-resonance frequencies [36], [37]. Moreover, by paralleling small capacitors to the drain-source of MOSFETs, their turn-off switching losses can be reduced [38], [39]. The LLC resonant converter is widely used in practice in many applications such as renewable energy systems [40], [41], on-board chargers [42], [43], light-emitting diodes (LEDs) [44], [45], and power factor correction (PFC) [46]. To regulate the output voltage of the LLC-based resonant converters, several methods such as Pulse Frequency Modulation (PFM), Phase Shift Modulation (PSM), Pulse Width Modulation (PWM), Asymmetric PWM (APWM), or hybrid modulation strategies like PFM + PWM and PFM + PSM can be utilized [26]. In the PFM strategy that operates based on the resonant tank impedance modification, a wide frequency range is used to regulate the output voltage. So, optimal designs of transformer(s) and inductor(s) are a challenge [47]. Besides, in the PSM strategy, the lagging leg soft commutation may also be lost under the light-load conditions [48].

However, topologies like [22], [23], [49] are only suitable for low voltage applications. Also, the achievable output voltages in [5], [11], [14], [15], [16], [17], [24], [50], [51], and [52], which are roughly twice the abovementioned LLC-based resonant converters due to their half or full bridge output rectifiers, are still low for lots of applications. On the other hand, although using voltage quadrupler rectifier configuration [2], [6], [20], [53], [54] increases the converter voltage gain and output voltage values, these values are still low for some applications and we need more improvements.

Interleaving the primary current fed stages and stacking the output rectifiers stages of series-based [19] or LLC-based [55] resonant topologies is a good approach to increase the converter voltage gain, output voltage, and power values. However, many components must be used in these topologies, which in practice reduce the converters' reliabilities and increase their costs.

Finally, it should be mentioned that [7] is a good configuration for high-voltage high power applications, but its VM rectifier stage needs more capacitors, and lower voltage gain is achieved as compared to the given one here, which has a continuous input current with small ripple value instead of a pulsating current waveform.

Here, a high step-up interleaved current-fed LLC resonant converter, suitable for high-voltage high-power applications, is introduced. Low input current and output voltage ripples values, as well as soft-switching operations, are performed under wide input voltage and output power variations by using the well-known asymmetric PWM (APWM) technique to control the output voltage. So, low EMI, high efficiency, high frequency operation, and high power density are practically achievable.

The proposed converter is introduced in Sec. II and its key waveforms and different operational states are given in Sec. III. Then, its steady-state and dead-time analyses are given in Sec. IV and V, respectively. Next, the resonant tank components are calculated in Sec. VI. Also, output stage capacitors values are derived in Sec. VII. Finally, experimental results and conclusions are respectively given in VIII and IX.

II. PROPOSED CONVERTER

The proposed converter with full-bridge topology, suitable for high-power applications, is shown in Fig. 1. This converter current-fed interleaved structure reduces the input current ripple, as well as the input filter volume. The LLC resonant circuit is employed, among existing resonant topologies, due to its excellent features such as soft switching operation of all primary stage switches and output stage diodes even under the wide input voltage and output load variations, low EMI, high efficiency, high power density, low circulating currents, and so forth. A full-wave rectifier is used for each output stage to reduce each diode voltage and current stress. Also, the output-stage diodes and capacitors voltages stresses can be reduced by adding more stages. So, the proposed converter can be used for high-voltage applications. Here, two small capacitors are connected in parallel to M_{a_1} and M_{b_1} MOSFETs to reduce all power MOSFETs' turn-off switching losses. Furthermore, the output voltage is regulated by the APWM technique at a desired fixed switching frequency. As a result, unlike pulse frequency modulation (PFM), magnetic components can be designed more efficiently.

III. PROPOSED CONVERTER KEY WAVEFORMS AND ITS DIFFERENT OPERATIONAL STATES

The fundamental waveforms of the proposed converter are plotted in Fig. 2. Based on these waveforms, the proposed

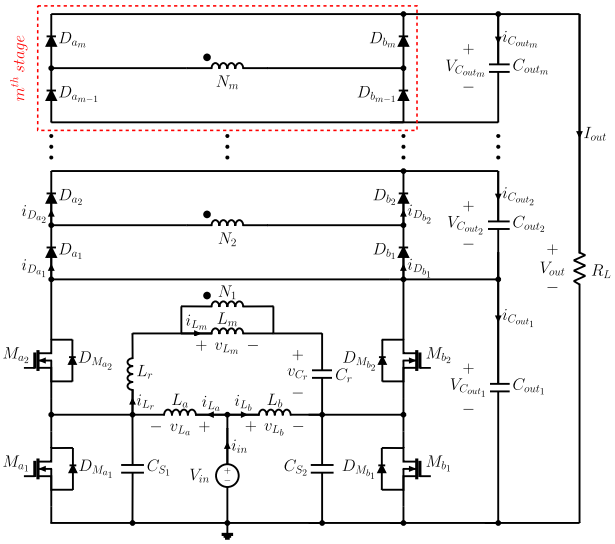


FIGURE 1. General configuration of the proposed step-up converter.

converter has eight different operational states during a switching period for a three-stage configuration, as depicted in Fig. 3. These states are summarized as follows:

State I [$t_0 - t_1$]: at the beginning of this interval, the body diode of M_{a_2} begins conducting. Therefore, this power switch can be turned on under ZVS condition, as shown in Fig. 2. Diodes $D_{a_{2,4}}$ and $D_{b_{1,3}}$ also start conducting current from zero by increasing their currents sinusoidally. Here, $D_{a_{2,4}}$ and $D_{b_{1,3}}$ are conducting and delivering power to the load during this interval, M_{b_1} is also conducting current and M_{a_1}, M_{b_2}, $D_{a_{1,3}}$, and $D_{b_{2,4}}$ are all off, as shown in Fig. 3(a). This state ends after M_{a_2} is turned off. The resonant tank capacitor voltage and inductors current waveforms are respectively given as follows:

$$\begin{aligned} v_{C_r}(t) &= Z_0 i_{L_r}(0)\sin(\omega_0 t) \\ &\quad + \left(v_{C_r}(0) - V_{C_{out_1}} + \frac{1}{n}V_{C_{out_2}}\right)\cos(\omega_0 t) \\ &\quad + V_{C_{out_1}} - \frac{1}{n}V_{C_{out_2}} \end{aligned} \tag{1}$$

$$\begin{aligned} i_{L_r}(t) &= i_{L_r}(0)\cos(\omega_0 t) \\ &\quad - \frac{1}{Z_0}\left(v_{C_r}(0) - V_{C_{out_1}} + \frac{1}{n}V_{C_{out_2}}\right)\sin(\omega_0 t) \end{aligned} \tag{2}$$

$$i_{L_m}(t) = \frac{V_{C_{out_2}}}{nL_m}t + i_{L_m}(0) \tag{3}$$

where,

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}}, \quad Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{4}$$

State II [$t_1 - t_2$]: during this interval, M_{b_1} continues to conduct current, but M_{a_2} is turned off with small switching losses due to the presence of its drain-source equivalent parasitic capacitance, its fast gate drive signal, and a properly selected dead-time value. In addition, the output stage diodes are switched off under ZCS condition. Therefore, the reverse recovery issue is simply overcome. The conducting states of the different components of the converter are shown in Fig. 3(b).

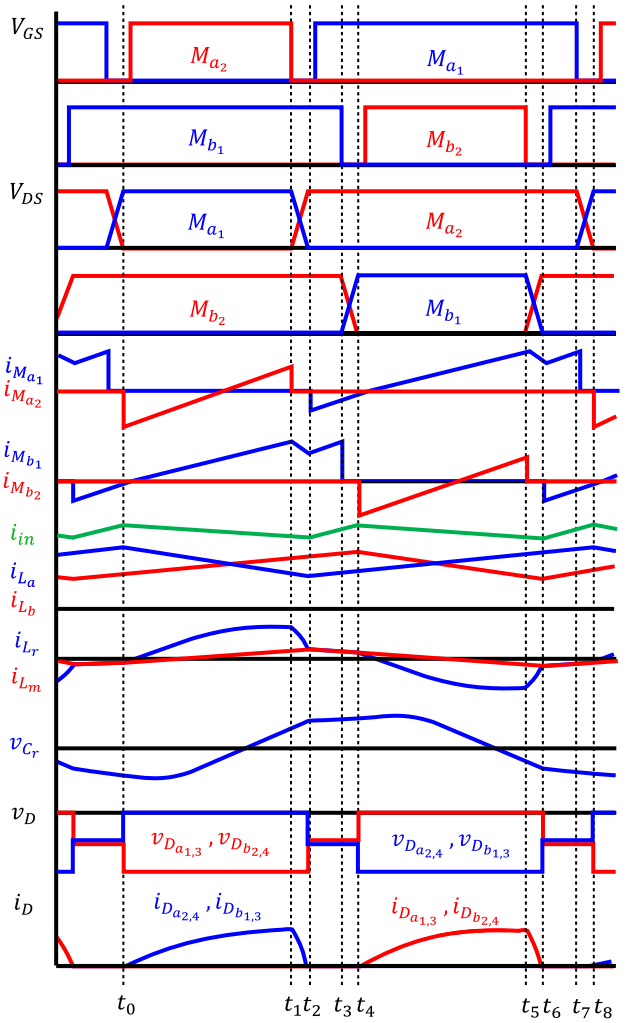


FIGURE 2. The fundamental waveforms of the proposed converter.

State III [$t_2 - t_3$]: at the beginning of this interval, the body diode of M_{a_1} starts conducting current after discharging its drain-source capacitance at the end of the previous state. Therefore, M_{a_1} can be switched on under ZVS condition. M_{b_1} is still conducting, but M_{a_2} and M_{b_2} are off. Since, the transformer magnetizing current reaches the resonant inductor current, no current passes from the primary side winding to the secondary and third windings. As a result, the output diodes are off and the output load is fully powered by the output capacitors. The conducting states of the converter components are shown in Fig.3(c). The resonant tank capacitor voltage and inductors currents can be given as follows:

$$\begin{aligned} v_{C_r}(t) &= Z_1 i_{L_r}(t_2)\sin(\omega_1(t - t_2)) \\ &\quad + v_{C_r}(t_2)\cos(\omega_1(t - t_2)) \end{aligned} \tag{5}$$

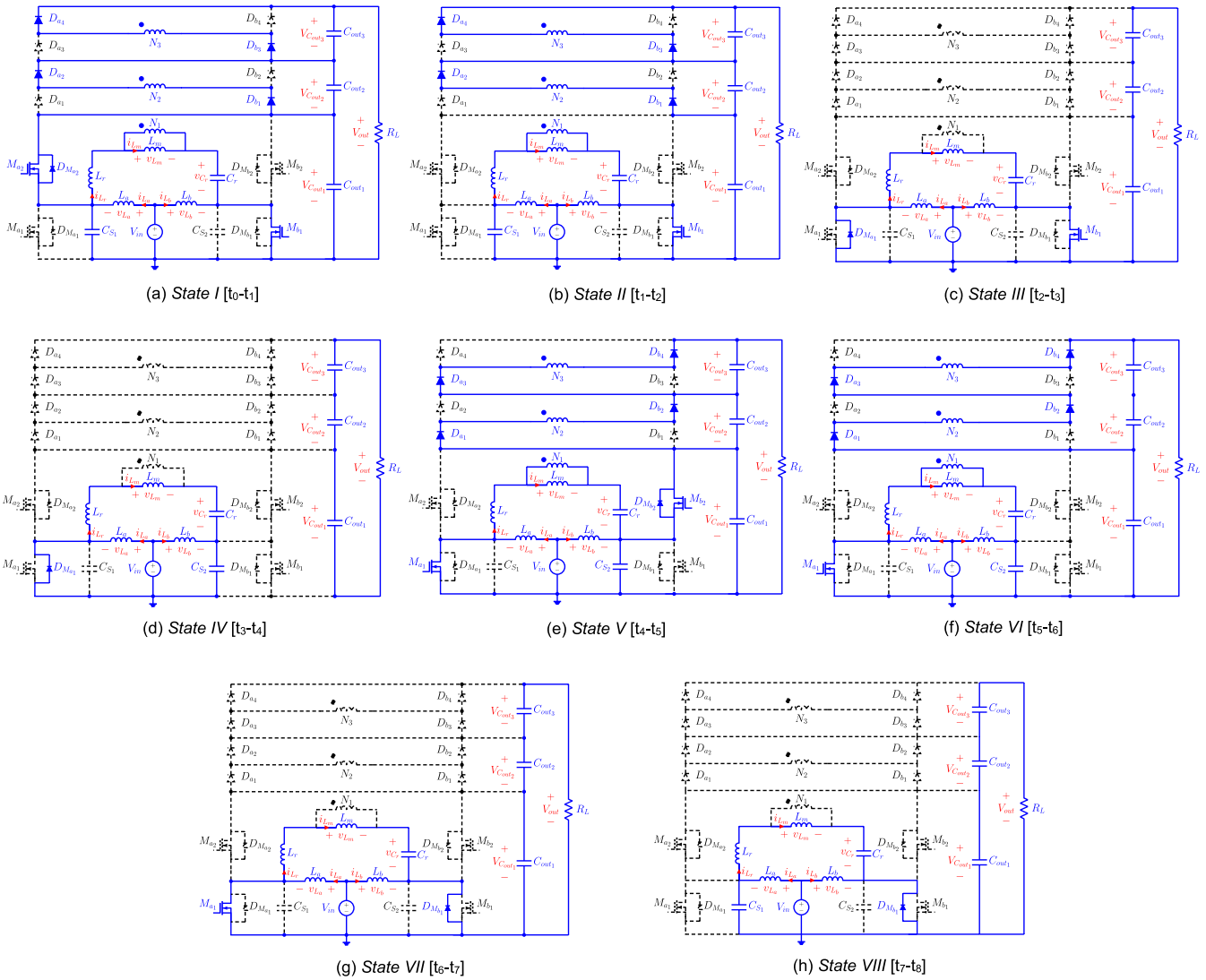


FIGURE 3. Different operational states of the proposed converter for $D > 0.5$.

$$i_{L_r}(t) = i_{L_m}(t) = i_{L_r}(t_2)\cos(\omega_1(t - t_2)) - \frac{v_{C_r}(t_2)}{Z_1}\sin(\omega_1(t - t_2)) \quad (6)$$

where,

$$\omega_1 = \frac{1}{\sqrt{(L_r + L_m)C_r}}, \quad Z_1 = \sqrt{\frac{L_r + L_m}{C_r}} \quad (7)$$

State IV [t_3– t_4]: during this state, the body diode of M_{a_1} continues to conduct current, but M_{b_1} is turned off with small switching losses, as previously explained for M_{a_2} during operational *State II*. All output diodes are still off, and the load is still powered by the output capacitors, as shown in Fig. 3(d). During the next half-switching period, the different operating states of the converter are the same as previously described for *States I-IV*, but in the opposite direction. Also, the operating states for D < 0.5 are the same as described for D > 0.5, but there are two simple differences. For D < 0.5, M_{a_2} and M_{b_2} gate-source signals overlap, in contrast to D > 0.5, where the gate-source signals of the lower switches, i.e., M_{a_1} and M_{b_1} overlap. *States III* and *IV* are depicted in Fig. 4 for D < 0.5. *States VII* and *VIII* are similar to *States III* and *IV*, but in opposite directions.

IV. STEADY-STATE ANALYSIS OF THE CONVERTER

To simplify the analysis of the steady-state behavior of the converter, following assumptions are considered: 1) During a switching period, voltage ripples of the output capacitors (i.e., $C_{out_1} - C_{out_m}$) are ignored. 2) The primary stage switches and the output stage diodes are considered ideal. 3) Both input inductors are the same ($L_a = L_b = L$). 4) Two non-dominant *operational States* of *II* and *IV* are ignored first, but the converter behavior during the dead-time is separately analyzed in more details later. 5) Different turns ratios of the transformer are considering being the same, i.e., $N_2/N_1 = \cdots = N_m/N_1 = n$.

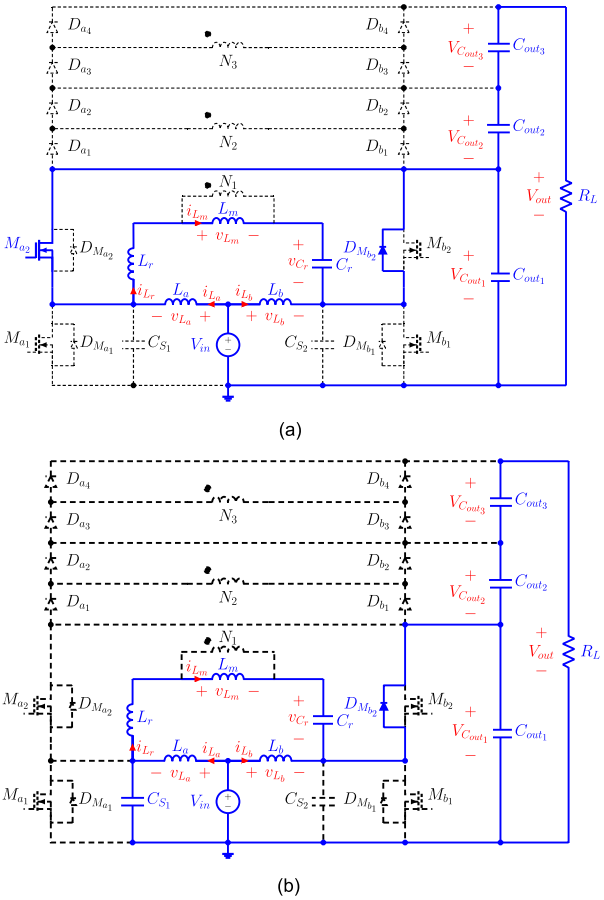


FIGURE 4. Operational States of the proposed converter for $D < 0.5$ (a) State III (b) State IV.

1) VOLTAGE STRESSES OF THE OUTPUT CAPACITORS

By applying the volt-second balance principle to one of the input inductors, voltage across C_{out_1} is derived.

$$V_{C_{out_1}} = \frac{V_{in}}{1-D} \tag{8}$$

Thus, voltages of the other capacitors can be identified.

$$V_{C_{out_2}} = \cdots = V_{C_{out_m}} = \frac{V_{out}}{m-1} - \frac{V_{in}}{(m-1)(1-D)} \tag{9}$$

where, m is the number of the stages of the converter.

2) INITIAL RESONANT INDUCTOR CURRENT AND RESONANT CAPACITOR VOLTAGE

By ignoring the non-dominant operational *States*, i.e., *II* and *IV*, the following equations set can be derived during a half switching period:

$$\begin{cases} i_{L_r}(0) &= -i_{L_r}(t_4) \\ i_{L_r}(0) &= i_{L_m}(0) \\ i_{L_r}(t_4) &= i_{L_m}(t_4) \\ v_{C_r}(0) &= -v_{C_r}(t_4) \end{cases} \tag{10}$$

Furthermore, since non-dominant operational states are ignored, the following expressions can then be derived:

$$i_{L_{m_1}}(t_2) = i_{L_{m_3}}(t_2) \tag{11}$$

$$v_{C_{r_1}}(t_2) = v_{C_{r_3}}(t_2) \tag{12}$$

where, $i_{L_{m_1}}$, $v_{C_{r_1}}$ and $i_{L_{m_3}}$, $v_{C_{r_3}}$ are the magnetizing inductor current and resonant capacitor voltage during operational *States I* and *III,* respectively. By using (10)-(12), the resonant inductor current and capacitor voltage initial values, i.e., $i_{L_r}(0)$ and $v_{C_r}(0)$, are derived as:

$$i_{L_r}(0) = -a_2 V_{out} - b_2 V_{in} \tag{13}$$

$$v_{C_r}(0) = -c_2 V_{out} - d_2 V_{in} \tag{14}$$

where the given coefficients are calculated as follows:

$$\begin{cases} a_1 &= Z_1 \sin\theta_y - Z_0 \sin\theta_x \\ b_1 &= (1-\cos\theta_x)(1+\cos\theta_y) \\ c_1 &= (1+\cos\theta_y)\cos\theta_x \\ d_1 &= 1+\cos\theta_y - \frac{Z_0}{Z_1}\sin\theta_x \sin\theta_y \end{cases} \tag{15}$$

$$a_2 = \frac{\theta_x \cos\theta_y}{n(m-1)L_m\omega_0 d_1} + \frac{\sin\theta_y}{z_1 d_1}\left[\left(c_2 - \frac{1}{n(m-1)}\right)\cos\theta_y + \frac{1}{n(m-1)}\right] \tag{16}$$

$$b_2 = \frac{-\theta_x \cos\theta_y}{n(m-1)L_m\omega_0(1-D)d_1} + \frac{sin\theta_y}{Z_1 d_1}\left[\left(d_2 + \frac{n(m-1)+1}{n(m-1)(1-D)}\right)\cos\theta_x - \frac{n(m-1)+1}{n(m-1)(1-D)}\right] \tag{17}$$

$$c_2 = \frac{1}{c_1+d_1}\left(\frac{\theta_x a_1}{n(m-1)L_m\omega_0} - \frac{b_1}{n(m-1)}\right) \tag{18}$$

$$d_2 = \frac{-1}{(c_1+d_1)(1-D)}\left(\frac{\theta_x a_1}{n(m-1)L_m\omega_0} - \frac{n(m-1)+1}{n(m-1)}b_1\right) \tag{19}$$

Here θ_x, θ_y, λ, and F parameters are given as follows:

$$\theta_x = \begin{cases} \frac{2\pi D}{F} & D \le 0.5 \\ \frac{2\pi(1-D)}{F} & D > 0.5 \end{cases} \tag{20}$$

$$\theta_y = \begin{cases} \frac{2\pi(0.5-D)}{F}\sqrt{\frac{\lambda}{1+\lambda}} & D \le 0.5 \\ \frac{2\pi(D-0.5)}{F}\sqrt{\frac{\lambda}{1+\lambda}} & D > 0.5 \end{cases} \tag{21}$$

$$\lambda = \frac{L_r}{L_m}, F = \frac{f_s}{f_r} \tag{22}$$

A. CONVERTER VOLTAGE GAIN

Voltage gain of the proposed converter can be derived by calculating the average output current value as follows:

$$I_{out} = \frac{V_{out}}{R_L} = \frac{1}{nT_s}\int_0^{T_s/2}\left(i_{L_r}(t) - i_{L_m}(t)\right)dt \tag{23}$$

By substituting (2), (3), (8), (9), (13), and (14) into (23) and doing some straightforward algebraic calculations, the converter voltage gain is derived, given by as in (24), shown at the bottom of the page. Here, $R_N = R_L/Z_0$ is the normalized output load resistance value. (24) clearly shows that the converter voltage gain depends on the converter duty cycle, normalized output load, and normalized switching frequency.

Since the output voltage regulation by varying switching frequency can cause some problems such as inefficient design of magnetic components and also efficient usage of parasitic components of the transformer is a challenge by employing this approach [4], [56]; therefore, the APWM approach is used here to regulate the output voltage.

To identify the necessary duty cycle variations for regulating the output voltage at a desired switching frequency when both input voltage and load variations are applied to the converter, the normalized output voltage is defined as follows:

$$V_{out\ N} = \frac{V_{out}}{V_b} = \frac{V_{out}}{V_{in}}\frac{V_{in}}{V_b} = MV_{in\ N} \tag{25}$$

Here, $V_{in\ N}$ is the normalized input voltage and V_b is defined as:

$$V_b = \frac{V_{in\ min} + V_{in\ max}}{2} \tag{26}$$

Using (25), the converter normalized output voltage has been plotted in Fig. 5 under the two worst-case conditions, i.e., (a) minimum input voltage and minimum output load resistance and (b) maximum input voltage and maximum output load resistance. Fig. 5(a) depicts three-dimensional normalized circuit voltage gain versus normalized load resistance, R_N and duty cycle. The intersections of the desired normalized output voltage value with the two other normalized output voltage curves under the worst-case conditions, shown in dashed lines, specify the duty cycle variations to regulate the output voltage when wide input voltage and output power variations are applied to the converter. Here, the duty cycle should theoretically vary from 0.3 to 0.75 to regulate the output voltage, as it is depicted in Fig. 5(b).

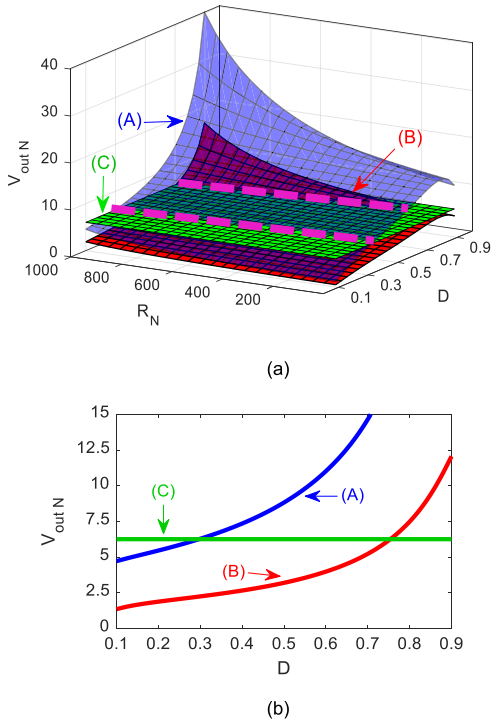


FIGURE 5. Converter normalized output voltage versus different parameters (a) R_N and D, and (b) D (A: $V_{in\ max}$, $R_{N\ max}$, B: $V_{in\ min}$, $R_{N\ min}$, and C: desired constant value).

B. MINIMUM AND MAXIMUM VALUES OF THE INPUT INDUCTORS CURRENT AND THE CONVERTER INPUT CURRENT RIPPLE VALUE

The input inductors current for $D > 0.5$ are shown in Fig. 6. Considering these waveforms, the L_a inductor current during a switching period can be expressed as follows:

$$i_{L_a}(t) = \begin{cases} \frac{V_{in}}{L_a}t + I_{L_{min}} & 0 < t < DT_S \\ \frac{V_{in} - V_{C_{out1}}}{L_a}(t - DT_S) + I_{L_{max}} & DT_S < t < T_S \end{cases} \tag{27}$$

By substituting (8) into (27), using average value of $i_{in} = V_{out}I_{out}/\eta V_{in}$ and $i_{in} = i_{L_a} + i_{L_b}$, and doing some algebraic calculations, the minimum and maximum values of the input current are derived as follows:

$$\begin{cases} I_{L_{min}} = \left[\frac{M}{\eta R_L} - \frac{DT_S}{2L_aM}\right]V_{out} \\ I_{L_{max}} = \left[\frac{M}{\eta R_L} + \frac{DT_S}{2L_aM}\right]V_{out} \end{cases} \tag{28}$$

where η and M are the efficiency and voltage gain of the converter, respectively. Since a two-phase interleaved structure is used at the primary side of the proposed converter, the input current ripple is minimized because the inductors currents are the same, but 180 degrees out of phase, as shown in Fig. 6. It should be noted that when D = 0.5, the inductors currents cancel out each other ripples; thus, the converter has a ripple-free input current under this condition. In addition, when the proposed converter operates under the CCM conditions, the inductors current ripple values as well as the converter input current ripple are further reduced. Therefore, a smaller input filter can be used. Both inductors current

$$M(D, R_N, F) = \frac{V_{out}}{V_{in}} = \frac{\frac{\theta_x^2}{2n(m-1)(1-D)L_m\omega_0} - \frac{\cos\theta_x - 1}{Z_0}\left(d_2 + \frac{n(m-1)+1}{n(m-1)(1-D)}\right) - b_2(\sin\theta_x - \theta_x)}{\frac{\theta_x^2}{2n(m-1)L_m\omega_0} + \frac{\cos\theta_x - 1}{Z_0}\left(c_2 - \frac{1}{n(m-1)}\right) + \frac{n\pi}{Z_0FR_N} + a_2(\sin\theta_x - \theta_x)} \tag{24}$$

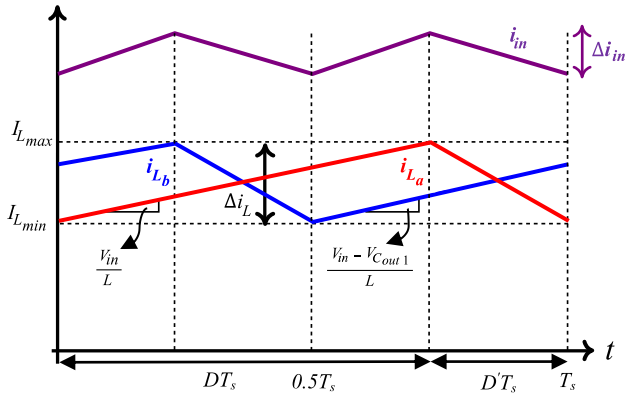


FIGURE 6. Input inductors current and input current waveforms D > 0.5.

ripple values are the same and can be calculated as follows:

$$\Delta i_L = \frac{DT_s V_{in}}{L} \tag{29}$$

Calculating the ratio of the converter input current ripple value to each of its input inductor current ripple values, i.e., Δi_{in} to Δi_L, it can be shown that how much the input current ripple value decreases with respect to the values of the inductors currents ripples values in the given interleaved structure.

$$\frac{\Delta i_{in}}{\Delta i_L} = \begin{cases} \frac{1-2D}{1-D} & D \le 0.5 \\ \frac{2D-1}{D} & D > 0.5 \end{cases} \tag{30}$$

By substituting (29) into (30), the normalized input current ripple of the interleaved two-phase structure can be derived as:

$$\Delta i_{inN} = \frac{\Delta i_{in}}{T_s V_{out}/L} = \begin{cases} \frac{D(1-2D)}{(1-D)M} & D \le 0.5 \\ \frac{2D-1}{M} & D > 0.5 \end{cases} \tag{31}$$

Based on (31), some curves are plotted in Fig. 7, where Fig. 7(a) illustrates the normalized input current ripple versus different duty cycles and normalized output resistance load values. This figure clearly shows that the input current ripple value increases by increasing the output power value. In addition, when the duty cycle deviates from $D = 0.5$, then the input current ripple increases. Therefore, to minimize the input current ripple, the converter should operate around $D = 0.5$ under full load conditions. Fig. 7(b) shows the normalized input current ripple versus λ. Because λ has a little effect on the normalized input current ripple value, as shown in Fig. 7(b), using large magnetizing inductor value is preferred to minimize the circulating currents and conduction losses.

V. DEAD-TIME ANALYSIS

Although turn-on switching losses of the MOSFETs of the proposed converter are almost eliminated due to their ZVS

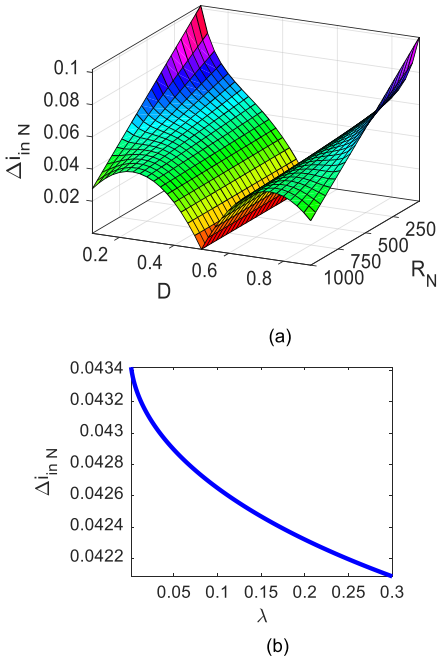


FIGURE 7. Normalized input current ripple versus different parameters (a) D and R_N and (b) $\lambda = L_r/L_m$.

operation, their turn-off switching losses are still remaining. To decrease these switching losses, small capacitors may be connected in parallel with the MOSFETs' drain-source [39], [57], [58], in addition to their parasitic capacitances, by turning them off fast and properly considering dead-time subintervals. These switching losses are effectively reduced by increasing the abovementioned capacitances, even when the minimum input voltage is applied to the converter and maximum power is delivered to the load, which is the worst-case condition for turn-off switching losses of the MOSFETs. However, using higher capacitances lead to a narrower ZVS operation range because larger currents are required to fully charge/discharge these capacitors to provide the ZVS condition. Thus, ZVS operation may not be fulfilled under the light load conditions, especially when the maximum input voltage is applied to the converter. This is also a worst-case condition to fully charge/discharge the MOSFETs parallel connected capacitors during the dead-time subintervals to realize the ZVS operation. Consequently, a proper trade-off between reducing the turn-off switching losses and providing the ZVS condition for reducing the turn-on switching losses must be addressed here for the abovementioned worst-case conditions to overcome this issue in practice. Fig. 8 shows the *operational State II*, occurring due to the considered dead-time subinterval. Therefore, maximum capacitance value, C_S, can be identified as follows:

$$C_S \frac{dv_{C_S}}{dt} = i_{C_S\,min} = \left(I_{L_a} - i_{L_r(t_2)}\right)_{min} \approx C_{S\,max} \frac{V_{in\,max}}{\Delta T} \tag{32}$$

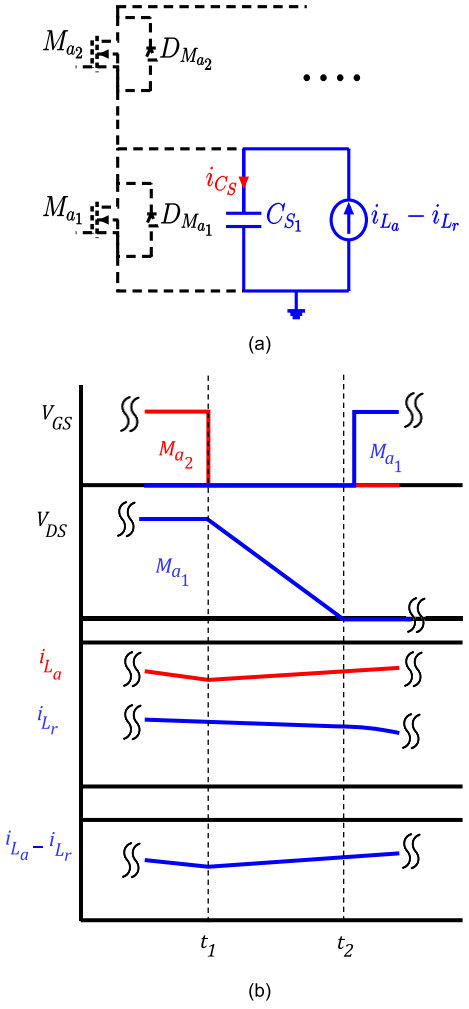


FIGURE 8. Dead-time subinterval $[t_1 - t_2]$ at $V_{in\ max}$, $R_{N\ max}$ (a) Simplified equivalent circuit and (b) some key waveforms.

By keeping in mind that $i_{L_r}(t_2) = i_{L_m}(t_2)$ and using (3), (9), (16), (28), and (32), the maximum capacitance value of C_S can be calculated as follows:

$$C_{S_{max}} \leq \frac{(1 - D_{min})\,\Delta T}{V_{in_{max}}} \times \left[\left(\frac{M(D_{min}, R_{L_{max}})}{2\eta R_{L_{max}}} - \frac{(1-D_{min})T_S}{n(m-1)L_m} + a_2 \right) V_{out} - \left(\frac{D_{min} T_S}{2L} - \frac{T_S}{n\,(m-1)\,L_m} - b_2 \right) V_{in_{max}} \right] \quad (33)$$

Here, ΔT is the dead-time value which can be obtained from the datasheet of the used power MOSFET by considering some parameters such as rise and fall times, turn on and off delay times, and body-diode reverse recovery duration time [59].

VI. CALCULATING THE RESONANT TANK COMPONENTS VALUES

Here, a simple approach is used to calculate the converter components values. $V_{C_{out_1}}$ is approximately applied to the transformer primary winding because the converter operates near its series resonant frequency. Therefore, the transformer turns ratios can be approximated as follows:

$$n = \frac{V_{C_{out_{2,\cdots,m}}}}{V_{C_{out_1}}} \quad (34)$$

So, the transformer turns ratios can easily be identified. Since the output stage capacitors with the same voltages stresses are preferred in practice, the transformer unity turns ratios are considered here. Considering Fig. 9, voltage of C_r changes from minimum to maximum value during t_x to t_z time duration and these values are respectively occurring-when $i_{D_{b_1}}(t_x) = i_{D_{a_1}}(t_z) = I_{out}$ during *States I* and *IV*. Therefore,

$$\frac{1}{2n}\left(i_{L_r}(t) - i_{L_m}(t)\right) = \frac{V_{out}}{R_L} \quad (35)$$

Substituting (2), (3), (13), and (14) into (35), t_x and t_z can be obtained numerically. Consequently, peak-to-peak voltage variation of C_r is obtained as follows:

$$\Delta V_{C_r} = \frac{1}{C_r}\int_{t_x}^{t_z} i_{L_r}(t)\,dt = \frac{1}{C_r}\left(\int_{t_x}^{D'T_s} i_{L_r}(t)dt + \int_{D'T_s}^{t_4} i_{L_r}(t)dt + \int_{t_4}^{t_z} i_{L_r}(t)dt\right) \quad (36)$$

Doing some algebraic calculations, ΔV_{C_r} can be calculated as expressed in (37), shown at the bottom of the next page.

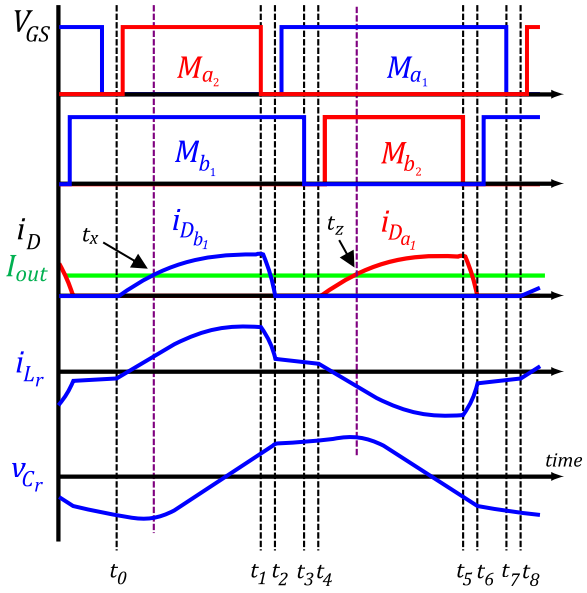


FIGURE 9. Resonant capacitor voltage and inductor current waveforms.

Here, different parameters are given as follows:

$$\begin{cases} \kappa_1 = \chi_1 d_2 - n\,(m-1) + 1 \\ \kappa_2 = T_s + \chi_2 b_2 \\ \kappa_3 = Z_1^{-1} \sin\left(\omega_0 D' T_s\right) \\ \kappa_4 = Z_1^{-1} \cos\left(\omega_0 D' T_s\right) \\ \kappa_5 = \chi_1 d_2 + n\,(m-1) + 1 \\ \kappa_6 = (1-D)\,T_s - \chi_2 a_2 \\ \chi_1 = n\,(m-1)\,(1-D) \\ \chi_2 = n\,(m-1)\,L_m \\ \tau_1 = \sin\left(\omega_0 D' T_s\right) - \sin\left(\omega_0 t_x\right) \\ \tau_2 = \sin\left(\omega_0 t_z\right) - \sin\left(0.5\omega_0 T_s\right) \\ \tau_3 = \cos\left(\omega_0 D' T_s\right) - \cos\left(\omega_0 t_x\right) \\ \tau_4 = \cos\left(\omega_0 t_z\right) - \cos\left(0.5\omega_0 T_s\right) \end{cases} \tag{38}$$

Considering (38), and substituting (4) and (7) into (37), C_r can be identified numerically from (37) for given voltage ripple value under the worst-case condition. Then, for given resonant frequency, L_r is also simply identified from (4).

VII. CALCULATING THE OUTPUT STAGE CAPACITORS VALUES

To limit the output voltage ripple value, the output stage capacitors values must be chosen properly. Fig. 10 shows the different output capacitors voltages ripples and currents waveforms for $D > 0.5$ during a switching period. Considering these waveforms, the capacitors voltages ripples are calculated. As illustrated in Fig. 10, $V_{C_{out1max}}$ is occurred at t_y, which can be identified as follows:

$$t_y = \frac{(1-D)\,T_S}{2} \tag{39}$$

Therefore, peak-to-peak voltage variations of C_{out_1} is identified.

$$\begin{aligned} \Delta V_{C_{out_1}} &= \frac{1}{C_{out_1}} \int_0^{t_y} i_{C_{out_1}}(t)\,dt \\ &= \frac{1}{C_{out_1}} \int_0^{t_y} \left[\frac{1}{n}\left(i_{L_a}(t) - i_{L_r}(t)\right) - I_{out}\right] dt \\ &= \frac{1}{C_{out_1}} \left[\left(\frac{\kappa_7}{\chi_3} + \frac{(1-D)\,b_2\kappa_8 + \kappa_9}{(1-D)\,\chi_4}\right) V_{in} \right. \\ &\quad \left. + \left(\frac{\kappa_{10}}{\chi_5} + \frac{a_2\kappa_8 + \kappa_{11}}{\chi_4}\right) V_{out}\right] \end{aligned} \tag{40}$$

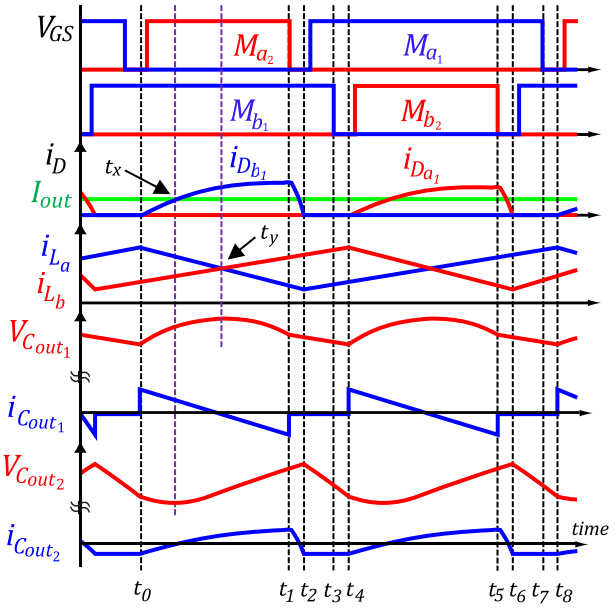


FIGURE 10. Output capacitors voltages ripples and currents waveforms for $D > 0.5$.

where,

$$\begin{cases} \kappa_7 = -Dty^2 - nD(1-D)t_y T_s \\ \kappa_8 = n(m-1)\sin(\omega_0 t_y) \\ \kappa_9 = [\chi_1 d_2 + n(m-1) - 1]\tau_5 \\ \kappa_{10} = (M - 2\eta)t_y \\ \kappa_{11} = [n(m-1)c_2 - 1]\tau_5 \\ \chi_3 = 2nL(1-D) \\ \chi_4 = n^2\omega_0(m-1) \\ \chi_5 = 2\eta R_L \\ \tau_5 = C_r\omega_0(\cos(\omega_0 t_y) - 1) \end{cases} \tag{41}$$

Moreover, $V_{C_{out_{2,\cdots,m}}}$ varies from its minimum to maximum value during t_x to t_p. Therefore, peak-to-peak voltage variations of $V_{C_{out_{2,\cdots,m}}}$ is obtained as follows:

$$\begin{aligned} \Delta V_{C_{out_{2,\cdots,m}}} &= \frac{1}{C_{out_{2,\cdots,m}}} \int_{t_x}^{t_p} i_{C_{out_{2,\cdots,m}}}(t)\,dt \\ &= \frac{1}{C_{out_{2,\cdots,m}}} \times \left[\left(-\kappa_{12} b_2 \tau_6 + \frac{\kappa_{12}\kappa_{13}\tau_7}{Z_0} \right.\right. \\ &\quad \left. + \frac{\tau_8}{(1-D)} + \frac{b_2\tau_9}{2n}\right) V_{in} \\ &\quad \left. - \left(\kappa_{12} a_2 \tau_6 + \frac{\kappa_{12}\kappa_{14}\tau_7}{Z_0} + \tau_8 - \kappa_{15}\tau_9\right) V_{out}\right] \end{aligned} \tag{42}$$

$$\begin{aligned} \Delta V_{C_r} = \frac{1}{C_r} &\left[\left(\frac{b_2\,(\tau_2 - \tau_1)}{\omega_0} + \frac{C_r\kappa_1\,(\tau_4 - \tau_3)}{\chi_1} - \frac{\kappa_2}{\omega_1\chi_2}\sin\left(\omega_1\,(D-0.5)\,T_s\right) + \frac{Z_0\chi_1\kappa_3 b_2 + \kappa_4\kappa_5}{\chi_1}(D-0.5)\,T_s\right) V_{in} \right. \\ &+ \left(\frac{a_2\,(\tau_2 - \tau_1)}{\omega_0} + \frac{C_r\,(\chi_1 c_2 - (1-D))\,(\tau_4 - \tau_3)}{\chi_1} + \left(Z_0\kappa_3 a_2 + \frac{(\chi_1 c_2 - (1-D))\,\kappa_4}{\chi_1}\right)(D-0.5)\,T_s \right. \\ &\left. \left. + \frac{\kappa_6}{\omega_1\chi_2}\sin\left(\omega_1\,(D-0.5)\,T_s\right)\right) V_{out}\right] \end{aligned} \tag{37}$$

where,

$$\begin{cases} \kappa_{12} = \frac{1}{2n\omega_0} \\ \kappa_{13} = d_2 + \frac{1}{1+D} + \frac{1}{n(m-1)Z_0(1-D)} \\ \kappa_{14} = c_2 - \frac{1}{n(m-1)} \\ \kappa_{15} = \frac{a_2}{2n} - \frac{1}{R_L} \\ \tau_6 = sin\left(\omega_0 t_p\right) - \sin\left(\omega_0 t_x\right) \\ \tau_7 = cos\left(\omega_0 t_p\right) - \cos\left(\omega_0 t_x\right) \\ \tau_8 = \frac{t_p^2 - t_x^2}{4n^2(m-1)L_m} \\ \tau_9 = t_p - t_x \end{cases} \tag{43}$$

Also, t_p can be approximated as follows:

$$t_p \approx \begin{cases} (1-D)\, T_s & D > 0.5 \\ t_0 = 0 & D \le 0.5 \end{cases} \tag{44}$$

Now, for the given voltages ripples values, the output stage capacitors can be identified by considering (40) and (VII). Finally, it must be mentioned that voltage stresses of all power MOSFETs are equal to $V_{C_{out_1}}$. Also, each stage output capacitor and diodes voltage stresses are the same. Since all output capacitors voltages are almost equal, consequently, all power diodes voltage stresses are also the same. Therefore, each MOSFET, diode, and capacitor voltage stress can be identified.

$$\begin{cases} V_{DS} = \frac{V_{out}}{mn} \\ V_D = V_{C_{out}} = \frac{V_{out}}{m} \end{cases} \tag{45}$$

The converter stages number can be identified easily by considering the available devices volt-ratings and the desired output voltage values properly. Because the converter devices entirely operate under the soft switching conditions over wide input voltage and output power variation ranges, the conduction losses are dominant components of the converter losses. Thus, to reduce the converter conduction losses and to improve its efficiency, low volt-rating devices are preferred. Therefore, a trade-off between efficiency, cost, and complexity of the converter must be done to properly identify the converter stage number in practice.

VIII. EXPERIMENTAL RESULTS

To confirm the theoretical analyses of the proposed converter, a 1 kW prototype converter has been implemented, as shown in Fig. 11. The implemented converter can step up wide input voltage variation ranges (100-200 V) to be regulated to 1000 V at the output port. Also, its output power varies in a wide range (100 W- 1 kW). Here, unlike the conventional LLC resonant converter, where the minimum switching frequency determines the sizes of the converter's magnetic devices, the switching frequency is fixed at $f_s = 143\ kHz$, and the output voltage is regulated by the APWM method, as mentioned before. Therefore, the converter's magnetic components used in the input filter, resonant inductor, and multi-winding transformer can be designed more appropriately. The specifications of the main parameters of the prototype converter are given in Table 1. Here, the gate driver

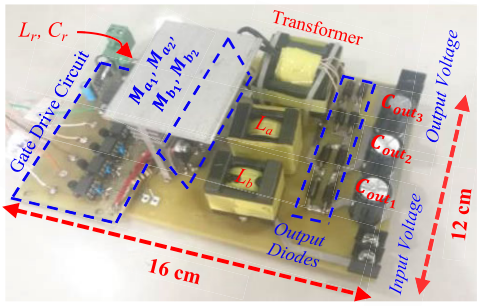


FIGURE 11. A photograph of the 1 kW prototype step-up converter.

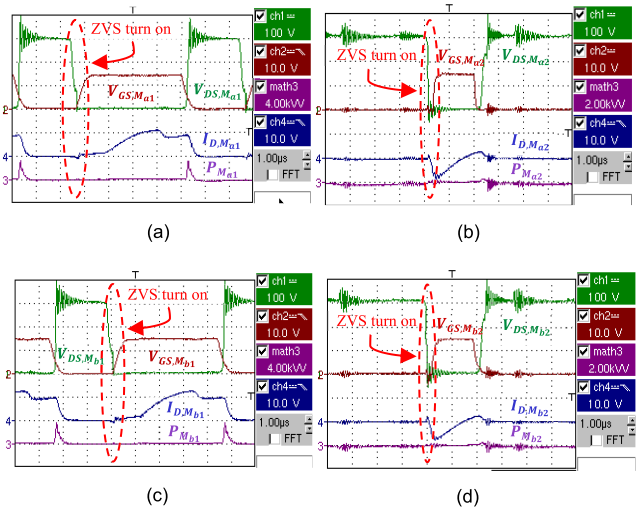


FIGURE 12. ZVS operation of the power MOSFETs when $V_{in} = 100\ V$, $V_{out} = 1\ kV$, and $P_{out} = 1\ kW$, (a) switch M_{a_1}, (b) switch M_{a_2}, (c) switch M_{b_1}, and (d) switch M_{b_2}.

signals are generated by a STM32F334R8 board. The steady-state experimental waveforms for two worst-case conditions, i.e., $V_{in} = 100\ V$, $P_{out} = 1\ kW$ and $V_{in} = 200\ V$, $P_{out} = 100\ W$ are given. Figs. 12 and 13 show the ZVS operation of the primary stage MOSFETs for the two worst-case conditions, respectively. Like the other resonant converters, to realize ZVS operation, the resonant tank network input current waveform must be lagged properly compared to the output voltage of the switching network [60]. Consequently, by turning on M_{a_1} MOSFET, for instance, the converter current fully discharges the parallel connected C_{S_1} capacitor during the dead-time. Then, anti-parallel body-diode $D_{M_{a_1}}$ is forward-biased and starts conducting the current. So, M_{a_1} power MOSFET can be turned on a short time later under the zero-voltage condition without having switching losses. To realize the ZVS operation, each power MOSFET anti-parallel body-diode must first conduct the current. This means that each power MOSFET current waveform must have a negative part before turning it on by the control circuit, which passes through the anti-parallel body-diode of the MOSFET in the reverse direction, as clearly marked with a dashed curve in Figs. 12 and 13. As shown in Figs. 12 and 13, all MOSFETs' drain-source voltages reach zero before applying their gate-source signals under the given two worst-case

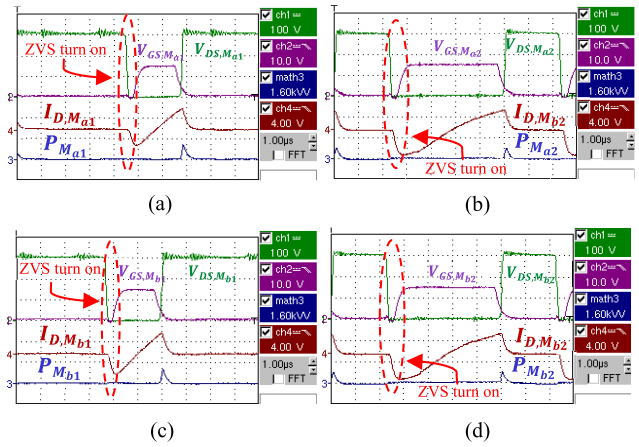


FIGURE 13. ZVS operation of the power MOSFETs when $V_{in} = 200V$, $V_{out} = 1\ kV$, and $P_{out} = 100\ W$, (*a*) switch M_{a_1}, (*b*) switch M_{a_2}, (*c*) switch M_{b_1}, and (*d*) switch M_{b_2}.

conditions. So, all MOSFETs turn-on switching losses are effectively eliminated due to their ZVS operation. Switching losses of the MOSFETs are illustrated by the bottommost waveforms of the different parts of Figs. 12 and 13, too.

Also, the bottommost waveforms of Figs. 14 and 15 clearly show that the output stage diodes turn-off switching losses are effectively eliminated due to their ZCS operations that significantly alleviate their reverse recovery problem. Therefore, the soft-switching operation is guaranteed for all power switches of the proposed converter in all input voltage and output power variations ranges. It means that high efficiency, low EMI noises, and high switching frequency operation are achievable. Consequently, high power densities can be realized in practice.

Fig. 16 shows the input inductors currents and the converter input current waveforms under the abovementioned two worst-case conditions. Due to the converter interleaved structure, its input current ripple value is effectively lower than both input inductors current ripple values, as clearly illustrated in Fig. 16. Also, the input current frequency is twice the frequency of both input inductors current waveforms, which is effectively reducing the input filter volume. Fig. 17 shows the resonant tank inductor current and capacitor voltage waveforms under the abovementioned two worst-case conditions when the output oltage is 1 kV. Also, Fig. 18 shows the different output stage capacitors voltages as well as the converter output voltage waveforms under the two worst-case conditions. This clearly illustrates that the output voltage is almost equally divided between the output capacitors. Thus, these capacitors, as well as the output stage diodes, experience the same voltage stresses, even when more stages are used to employ either lower volt-rating devices or to achieve higher output voltage values in practice. Also, Fig. 19(a) shows the converter's different efficiency curves versus output power for different input voltages. Besides, Fig. 19(b) depicts the loss distribution of the proposed converter. Based on Fig. 19(b), although the dominant switching losses of the MOSFETs are eliminated due to soft-switching, most of the

TABLE 1. Main parameters of the prototype converter.

Parameter or device	Symbol	Value
Input DC voltage	V_{in}	$100\ V - 200\ V$
Output DC voltage	V_{out}	$1\ kV$
Output power	P_{out}	$100\ W - 1\ kW$
Input inductors	L_a, L_b	PQ 32/20 core $50\ \mu H$
Transformer	$N_1/N_2/N_3$	ETD 34/17/11 core 15/15/15
Resonant inductor	L_r	RM8 core $11.8\ \mu H$
Resonant Capacitor	C_r	$100\ nF$
Output capacitors	$C_{out_{1,2,3}}$	$47\ \mu F$
Capacitors connected in parallel with lower MOSFETs	C_{S_1}, C_{S_2}	$1\ nF$
Switching frequency	f_s	$143\ kHz$
Power MOSFETs	M_{a_1}, M_{a_2} M_{b_1}, M_{b_2}	IPP50R140CP
Rectifier diodes	$D_{a_1} - D_{a_4}$ $D_{b_1} - D_{b_4}$	MUR450

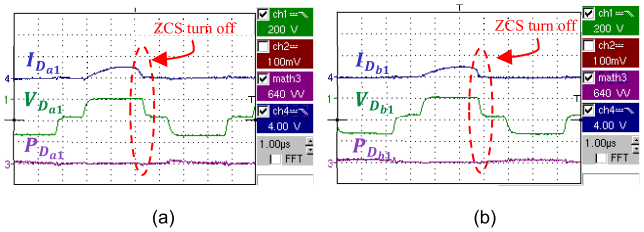


FIGURE 14. ZCS operation of the output stage diodes when $V_{in} = 100\ V$, $V_{out} = 1\ kV$, and $P_{out} = 1\ kW$ **(a)** $D_{a_1}, D_{a_3}, D_{b_2}$, and D_{b_4}, and **(b)** $D_{a_2}, D_{a_4}, D_{b_1}$, and D_{b_3}.

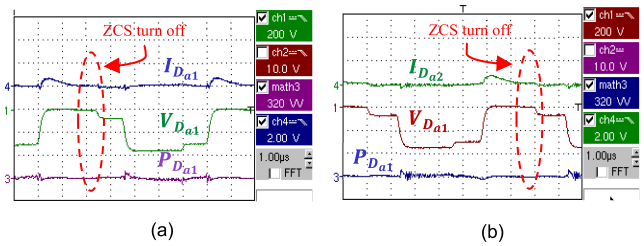


FIGURE 15. ZCS operation of the output stage diodes when $V_{in} = 200\ V$, $V_{out} = 1\ kV$, and $P_{out} = 100\ W$ (*a*) $D_{a_1}, D_{a_3}, D_{b_2}$, and D_{b_4}, and (*b*) $D_{a_2}, D_{a_4}, D_{b_1}$, and D_{b_3}.

losses are related to the conduction losses of the MOSFETs. Thus, by selecting switches with a lower $r_{ds\ on}$ higher efficiencies can be achieved. To gain a deeper insight about this issue, the proposed converter is compared with the most similar converters in Table 2. Although some better efficiencies have been reported in the literature, this is mainly due to their used components with lower conduction losses and switches

TABLE 2. Comparison of the proposed converter with the most similar converters.

Ref. \ Parameter	Components Specifications												Efficiency (%)	Suitable for high power	Suitable for high voltage
	Switches			Diodes				Inductors		Capacitors		Transformers				
	No.	I (A)	$R_{ds\,on}$ (mΩ)	No.	V (V)	I (A)	V_F (V)	No.	L (μH)	No.	C (μF)	No.	n			
[18]	6	120, 36.5	5.1, 45	-	-	-	-	3	35.6, 2×60	4	2×0.141, 2×20	1	1.85	97.3	NO	NO
[2]	4	57	23	4	1000	3	1.7	3	15, 2×68	5	2×2, 22, 2×220	1	1	96.8	YES	NO
[24]	4	36	80	6	800	30	2.4	3	37, 2×1000	3	0.068, 17, 1500	1	1	96.2	NO	NO
[19]	4	69	49	4	200	8	0.975	4	2×4, 2×50,	5	2×10, 3×20	-	-	94.7	YES	NO
[52]	4	38	75	4	-	-	-	3	17.715, 107.54, 108.64	3	0.133, 10, 100	1	2	NM	YES	NO
[20]	4	31	82	4	1000	1	1.1	3	10, 2×150	6	0.32, 4×10, 270	1	1.5	NM	YES	YES
[55]	8	56	40	4	600	6	1.6	6	2×14.5, 4×70	5	2×0.356, 110, 2×440	2	1.3	NM	YES	YES
Proposed	**4**	**23**	**140**	**8**	**500**	**4**	**1.28**	**3**	**11.8, 2×50**	**4**	**0.1, 3×47**	**1**	**1**	**95.3**	**YES**	**YES**

NM: Not Mentioned

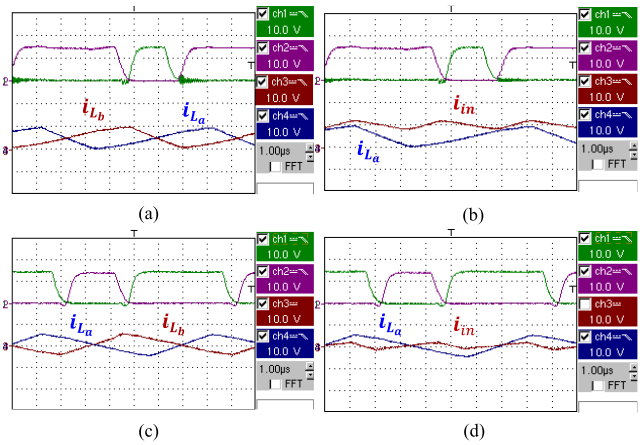


FIGURE 16. Converter input current and its input inductors currents waveforms under different conditions: (a) and (b) $V_{in} = 100\ V$, $V_{out} = 1\ kV$, and $P_{out} = 1\ kW$, and (c) and (d) $V_{in} = 200\ V$, $V_{out} = 1\ kV$, and $P_{out} = 100\ W$.

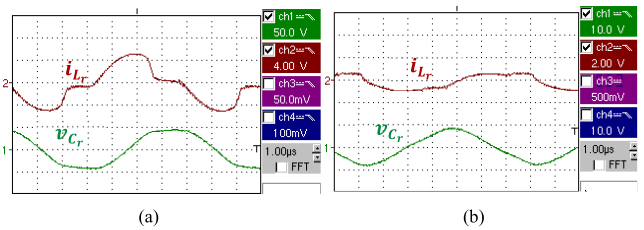


FIGURE 17. Resonant tank inductor current and capacitor voltage waveforms under different conditions (a) $V_{in} = 100\ V$ and $P_{out} = 1\ kW$ and (b) $V_{in} = 200\ V$ and $P_{out} = 100\ W$.

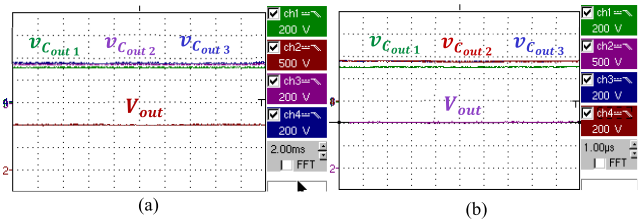


FIGURE 18. Output capacitors and regulated output voltages waveforms under different conditions (a) $V_{in} = 100\ V$, $V_{out} = 1\ kV$, and $P_{out} = 1\ kW$ and (b) $V_{in} = 200\ V$, $V_{out} = 1\ kV$, and $P_{out} = 100\ W$.

with lower on-state resistances, as clearly given in Table 2. Based on Figs. 12-15, the dominant switching losses of the MOSFETs and diodes are eliminated due to the converter's soft-switching operation in wide input voltage and output power variation ranges. Effects of the power MOSFETs and diodes conduction losses on the converter efficiency curves have been simulated, as given in Fig. 19(c). These simulation results clearly show that to improve the converter efficiency, different components with low conduction losses can be used. In practice, a trade-off between the converter efficiency and its cost can be done to improve the converter efficiency

Parameters / References		V_{out} (V)	V_{in} (V)	P_{out} (W)	Switching operation		Switching Freq. (kHz)	Number of:		Input Inductors (μH)	Capacitors Capacitances (μF)	Resonant Inductance (μH)	Transformer turns ratio (n)	Peak efficiency (%)	Modulation Strategy
					MOSFETs	Diodes		Switches	Diodes						
High step-up	[4]	200	40-80	200	†	**	100	5	6	-	0.1795, C	NM	4.8	97	PWM
	[9]	210	25-100	250	NM	NM	80-140	6	8	-	0.408, 200	3.16	16.2, 5.64	97.7	PFM
	[10]	300	12-24	600	**	-	50	5	6	500	0.36, C	0.3, 0.9	12	94	PWM
	[11]	380	20-40	300	†	NM	90-180	4	4	-	0.99, 20, 4×0.001	1.1	13	96	PFM + PWM
	[13]	400	36-57	1000	†	NM	60	5	4	54	4.4, 220, 2×330, 2×560	0.4, 2.92	2, 2.75	95.84	PWM
	[14]	400	80-200	1000	†	**	80-160	4	4	-	2×0.141	2×9.2	0.5	97.5	PFM
	[15]	600	100	1000	†	**	200	4	2	-	0.22, 4×100	2.86	1.5	97	NM
High voltage	[5]	1000	24	600	**	**	90-100	4	4	NM	1.2	0.25	30	92	PFM
	[6]	2500 (per module)	240-440	5000 (per module)	Aux: *, †† Main: †	*, **	37.5	10	8	-	2×0.1, 4×1	2×211	3	98.8	PSM
	[7]	8000-10000	100	325-550	†	**	32-48	4	16	-	0.2, 13×C	78.5	20	96	PFM
	[8]	15000	424-636	5000	$S_{1,2,3,4}$: *, ** $S_{a1,2}$: †, ††	$D_{2,3}$: ** $D_{1,4}$: *	20	6	10	NM	0.022, 0.2	3.6	20	93	PWM
Interleaved	[16]	100	30-50, 64-80	600	†	**	100	6	2	2×100	C	5	0.75	97	PWM + PSM
	[2]	200	25	400	†, ††	**	50	4	4	2×68	2×2, 22, 2×220	0.9	1	96.8	PWM
	[17]	360	65-115, 165-200	500	†	**	74-100	4	4	2×150	0.0735, C	34.4	1.8	96	PFM + PWM
	[18]	380	35-45	600	$S_{3,4,5,6}$: †, $S_{1,2}$: HS	-	50	6	0	2×60	2×0.141, 2×20	35.6	1.85	97.3	PWM
	[19]	380	40	1500	†	*, **	70	4	4	2×50	2×10, 3×20	2×4	-	94.7	PWM
	[20]	400	40-60	500	†	**	60-80	4	4	2×150	0.32, 4×10, 270	10	1.2	NM	PFM
	[21]	400	20	500	-	-	100	3	6	3×100	3×8.2, 2×22, 2×120	-	-	94.6	PWM
	[52]	60	10-20	18	†	-	NM	4	4	108.64, 107.54	0.133, 10, 100	17.715	2	NM	PFM
	[22]	48	120 RMS	350	†	**	140	4	2	2×110	0.0099, 0.0164, 400	70	0.125	92.3	NM
	[24]	400	110-220 (PFC)	1000	†	**	100	4	6	2×1000	0.068, 17, 1500	37	1	96.2	PWM
	[23]	48	85-265 (PFC)	300	†	**	50-119	4	4	2×195	0.0133, 120, 660	177	7.1	92.7	PFM/IAPWM
	[49]	20-160	12	48	†	**	100	4	2	2×2000	0.053, 100, 200	50	4.7	NM	NM
LLC-based converters	[51]	400	44-52	1000	†	**	78-135	4	4	2×24.2	2×856, 2×220, 1000	2×3	3.75	93.3	PFM
	[55]	400	40-76	1200	†	**	NM	8	4	4×70	2×0.356, 2×440, 110	2×14.5	1.3	NM	PWM, PFM
	[53]	500-840	390	1300	†	**	100	6	8	-	0.044, 6×150, 2×C	57	2.6	95.5	PFM
	[54]	760	25-50	300	†	**	75-110	6	8	-	0.62, 6×C	4.1	4	96.1	PFM
Proposed Converter		1000	100-200	1000	†	**	143	4	8	2×50	0.1, 3×47	11.8	1	95.3	APWM

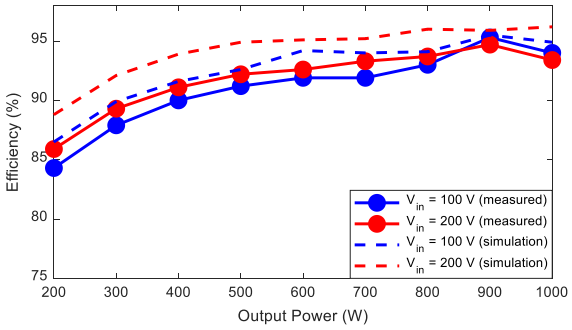
† ZVS turn on, †† ZVS turn off, * ZCS turn on, ** ZCS turn off, C: Unknown, and NM: Not Mentioned

TABLE 3. Comparison of the proposed converter with some different existing topologies.

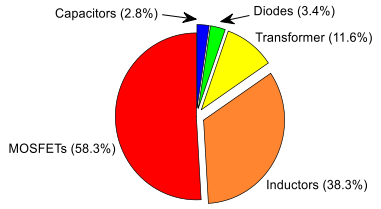
and pay a reasonable cost by choosing low-loss inductors and transformer, low-ESR capacitors, and low voltage drop MOSFETs and diodes.

By considering Table 2, some conclusions are given as follows:

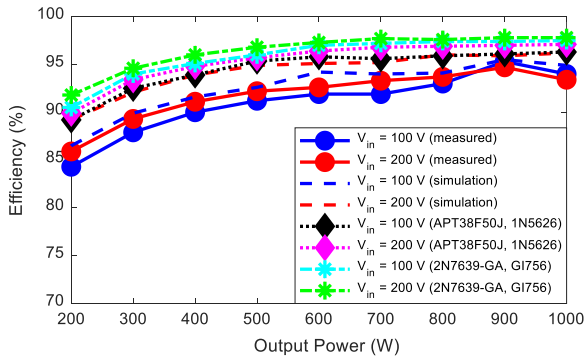
a) Generally, transformers and inductors are massive components that strongly affect the converter's power densities and prices. However, Table 2 clearly shows that this is a common issue in many dc-dc converters. The soft-switching operation of the converters, which is



(a)



(b)



(c)

FIGURE 19. (a) different simulated and experimental efficiency curves of the proposed converter under the different conditions, (b) loss distribution, (c) simulated efficiency curves of the proposed converter with different MOSFETs and diodes.

also achieved here, is an efficient approach to overcome this problem and improve the power density and reduce the cost.

b) Number of the active switches and their driver and control circuits are other issues. But, Table 2 clearly shows that the proposed converter is one of the best solutions from this point of view.

c) Input filter and output capacitors are also reduced here due to the given symmetrical configuration.

d) Although more diodes have been used here, as tabulated in Table 2, this is not a significant issue because lower current and voltage stresses are applied to these components, and this issue cannot very much affect the price and power density of the proposed converter in practice.

Fig. 20 shows the dynamic response of the proposed converter when the load changes between 90% and 10%. To have a

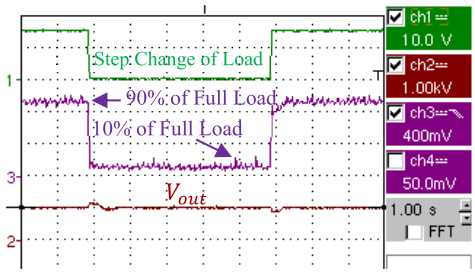


FIGURE 20. Dynamic response of the proposed converter when load changes between %90 and %10.

better clarification, an implemented 3-stage configuration of the proposed converter has been compared in more details in Table 3 with some other existing high step-up, high-voltage, interleaved, and LLC-based converters.

Finally, it must be mentioned that some unavoidable manufacturing mismatches may lead to improper operation of this proposed converter in practice, like many well-known power electronics converters, including interleaved-based topologies. For instance, any mismatches between the input inductors, the power switches of the different legs, their gate-drive circuits, their gate-source generated pulses, and so forth can affect the ideal operation of the proposed converter. This is a well-known issue in the power electronics field, and there are some solutions to overcome this problem. For instance, the average or peak current control approach can easily be used here to overcome this issue. However, the small signal modeling and closed-loop control approach of the proposed converter are ignored and not addressed here in detail to shorten the subject.

IX. CONCLUSION

In this paper, a new expandable high step-up LLC-based converter is proposed. The experimental results clearly show that all its primary stage MOSFETs and output stage diodes are operating under the soft-switching conditions in the entire wide input voltage and output power variation ranges. Therefore, high efficiency and low EMI noises are achievable, and high frequency operation is possible to reduce its passive components volume and thereby increase its power density. Also, integrating a two-phase interleaved current-fed structure with a LLC resonant converter makes it possible to achieve high voltage gain, as well as low input current ripple value. Besides, the input current frequency is twice the switching frequency that effectively reduces the input filter volume in practice. To regulate the output voltage, an asymmetric PWM technique at a fixed switching frequency is used to design the converter magnetic components, including input filter, resonant inductor, and multi-winding transformer, more effectively. A 1 kW prototype converter has also been implemented to verify the given analyses results. Wide input voltage 100-200 V, and output power 100-1000 W variations are applied to the converter. The APWM technique at 143 kHz switching frequency is used to regulate the output voltage at 1 kV.

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