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Wideband Dissipativity Enhancement for Grid-Following VSC Utilizing Capacitor Voltage Feedforward

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***Abstract*—Frequency-domain dissipativity of the converter admittance provides an intuitive approach to analyze wideband resonances due to the interactions with the grid. Although the reasons for high- and low-frequency resonances are different, it is found that the proportional capacitor voltage feedforward (CVF) can affect and reshape the converter admittance in a wide frequency range. To enhance wideband dissipativity under a weak/capacitive grid, a proportional-integral-derivative CVF is proposed in this paper. Specifically, high-frequency dissipativity can be guaranteed through the multi-sampling control with proportional-derivative CVF. The low-frequency non-dissipative region caused by the phase-locked loop and proportional CVF can be compensated through multi-order integrations. In light of grid frequency disturbances, modified integrators are further proposed for the multi-order integrations. The proposed method also applies to the conventional double-sampling control with regard to the low-frequency dissipativity enhancement. Finally, experiments validate the proposed control method.**

***Index Terms*—Grid-connected converter, wideband resonance, dissipativity, capacitor voltage feedforward.**

NOMENCLATURE

VSC	Voltage source converter
PLL	Phase-looked loop
CCF	Capacitor current feedback
CVF	Capacitor voltage feedforward
DSC	Double-sampling control
MSC	Multi-sampling control
ACC	Alternating-current control
SCR	Short circuit ratio
DEC	Dissipativity enhancement control
PWM	Pulse-width modulation
MRF	Modified repetitive filter
CMAF	Compromised moving average filter

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I. INTRODUCTION

WITH rapid penetration of renewable generations, the modern power grid is shifting its paradigm towards a power-electronic-based structure [1]. As a bridge between the renewables and the power grid, the grid-following voltage source converters (VSCs) are of importance to guarantee stable and reliable power conversions [2]. However, wideband resonance may occur due to undesired interactions between VSCs and the grid [3]. The poorly damped resonance can destabilize systems, which threatens grid security [4].

To reveal the occurrence and risk of resonances, the dissipativity theory provides an intuitive approach by analyzing the frequency-domain property of the converter output admittance [5]. If the real part of the admittance is positive, sufficient damping can be provided by the converter naturally, so that resonances at corresponding frequencies can dissipate and the system stability is guaranteed [6]. However, non-dissipative region, is observed over a wide frequency range for grid-following VSCs. If the converter admittance intersects with the grid admittance in the non-dissipative region, VSC system will become unstable.

Generally, the reasons for the non-dissipative region can be categorized into two types. The high-frequency non-dissipative region is induced by the control delay, which is located between the critical frequency and Nyquist frequency [7]. The low-frequency non-dissipative region is caused by various control loops. Specifically, investigated with the *dq*-frame admittance models, the phase-locked loop (PLL) induces non-dissipative region in *q*-*q* channel, which challenges weak-grid operations [8-9]. The interactions among the PLL and other loops can also induce various resonance modes and destabilize the system [10]. It is also found that the capacitor voltage feedforward (CVF) affects both high- and low-frequency dissipativity [11].

Capacitor current feedback (CCF) is widely used to mitigate the high-frequency non-dissipative region, while its robustness is sensitive to the passive filter parameter deviation and the delay of current controller [12]. Combining the CCF and a proportional CVF, high-frequency dissipativity can be achieved but the parameter design is based on try and error [13]. If the CCF is replaced with a digital derivative CVF to save capacitor current sensors, the conventional double-sampling control (DSC) is not feasible to fully mitigate high-frequency non-dissipative region due to considerable control delay [14]. By reducing the control delay directly, multi-sampling control

(MSC) is a promising solution to enhance high-frequency dissipativity [15]. Utilizing eight-sampling proportional-derivative or sixteen-sampling proportional CVF with a ripple filter, positive dissipation can be realized up to the switching frequency [16]. If the ripple filter is not considered, the dissipative region can even be extended to twice of the switching frequency without CVF [17-18]. With the MSC, not only the resonant frequency of *LCL*-filter can be flexibly designed, but also the robustness against filter parameter deviation is enhanced [19].

To mitigate the low-frequency non-dissipative region induced by the PLL, two types of approaches are considered. The first type focuses on modifying the PLL itself, e.g., either to optimized the control gains of the PLL in accordance with other loops [20-21], or to modify the PLL structure by inserting an additional filter [22]. However, the bandwidth of the PLL is affected, and the tuning of control gains depends on specific cases, requiring additional efforts. The second type focuses on reversely compensating the small-signal disturbances of the PLL utilizing voltage feedforwards. Due to the Park or inverse Park transformation, the PLL induces disturbances in the feedback current, modulating voltage, and the proportional CVF [9]. To reversely compensate the impact of the PLL, compensations with different orders of voltage feedforwards can be inserted at either the current reference [23], or the modulation voltage [24], or both [25], following a model-based approach. Utilizing the concept of virtual elements, a first-order compensation scheme is adopted at the current reference [26]. However, damping gains are tuned by trial and error. Besides, multi-order integrations of the *q*-axis voltage are constructed in [24-26], which can lead to a constant steady-state error of currents or destabilize the system under grid frequency variations. A dual-PLL-based scheme is considered to ensure stability under grid frequency variations [27]. However, the impact of the second PLL is not revealed.

Besides, the above-mentioned methods neglect the impact of the proportional CVF, which is often required during the start-up or grid disturbances [28]. Although the high-frequency dissipative region can be extended with the CVF, low-frequency dissipativity deteriorates due to the interaction of the CVF and alternating-current control (ACC) and PLL [11, 26]. To realize wideband dissipation, low-frequency non-dissipative region caused by the CVF and PLL shall be further enhanced.

As the CVF can affect and also compensate for both high- and low-frequency dissipativity, a control scheme is proposed to realize wideband dissipativity enhancement utilizing the CVF. Since positive dissipation can be easily obtained with the MSC only using the CVF, MSC is considered in this work. Based on that, low-frequency dissipativity is designed considering negative impacts of the CVF and PLL. The main contributions are summarized as follows:

a) Concrete admittance models are derived with *dq*-frame transfer matrices considering multiple sampling rates, and the wideband impact of the CVF is investigated.

b) Based on the high-frequency dissipativity enhancement control structure, a dissipativity enhancement control (DEC) is proposed to mitigate the low-frequency non-dissipative region induced by the CVF and PLL, with a generalized structure.

c) To remain stability under grid frequency deviations, a modified DEC is proposed by replacing high-order integrations with low-pass filters, and the parameter design is investigated.

With the proposed method, wideband dissipation can be realized from several hertz to the switching frequency. The system is capable to operate with a short-circuit ratio (SCR) of 1.1, and remains stabilized under grid frequency deviations.

The rest of this paper is organized as follows. In Section II, a detailed admittance-model-based dissipativity analysis is derived for the grid-following VSC, considering multiple sampling rates. To realize wideband dissipation, a DEC is proposed in Section III to mitigate low-frequency non-dissipative region induced by the CVF and PLL, and the design guideline of damping gains is elaborated. In Section IV, modified integrators are proposed for the DEC, to ensure the tracking capability of the reactive current and remain stability against grid frequency variations, the design criterion of control parameters is investigated. Experimental results are presented in Section V to verify the effectiveness of the proposed control scheme. Conclusions are drawn in Section VI.

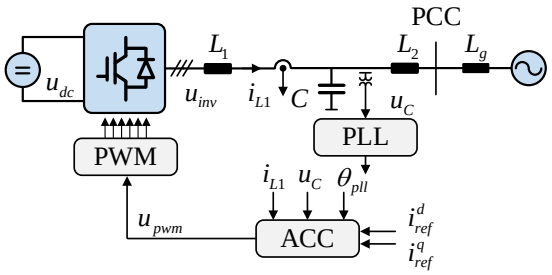


Fig. 1. Control diagram of a three-phase grid-following VSC.

II. Admittance Modeling and Dissipativity Analysis With High-Frequency Dissipativity Enhancement

The investigated three-phase grid-following VSC is depicted in Fig. 1. An *LCL* filter is implemented for switching harmonics suppression, where L_1 is the converter-side inductance, C is the grid-side capacitance, and L_2 is the grid-side inductance. The ACC is implemented to regulate the converter-side currents. The filter capacitor voltages are measured for the grid synchronization with a synchronous-frame-based PLL. To reveal the impact of complete control loops, especially considering the effect of the MSC, CVF, and PLL, *dq*-frame transfer matrices are adopted to model the converter output admittance. For clarity, *dq*-frame variables are represented with real vectors $x^{dq}=[x^d \quad x^q]^T$, small-signal variables are marked with ΔX, while steady-state variables are denoted as X.

A. Alternating-Current Control (ACC)

Since the grid-following VSC is regulated with ACC in *dq*-frame, the transfer matrix of the ACC G_{ACC} is obtained with diagonal proportional-integral (PI) control functions F_{ACC}, which are given as

$$G_{ACC}=\begin{bmatrix} F_{ACC} & 0 \\ 0 & F_{ACC} \end{bmatrix}, \tag{1}$$

$$F_{ACC} = K_p^{ACC} + \frac{K_i^{ACC}}{s}. \tag{2}$$

To compensate for the cross-coupling effect, a decoupling matrix G_{dec} is required, which is

$$G_{dec} = \begin{bmatrix} 0 & \omega_g L_1 \\ -\omega_g L_1 & 0 \end{bmatrix}. \tag{3}$$

For the conventional double-sampling PWM, the control delay $T_{del} = 1.5T_{sp}$ includes a computation delay T_{sp} and a zero-order hold delay $0.5T_{sp}$. It is preferred to adopt a Euler function, i.e., $F_{del} = e^{-sT_{del}}$, to model the delay effect precisely. Since the delay is reflected in the stationary frame, the *dq*-frame correspondence can be obtained by including a grid frequency shift [29]. By separating the real and imaginary parts, the transfer function of control delay is

$$G_{del} = \begin{bmatrix} \mathrm{Re}\{F_{del}(s+j\omega_g)\} & -\mathrm{Im}\{F_{del}(s+j\omega_g)\} \\ \mathrm{Im}\{F_{del}(s+j\omega_g)\} & \mathrm{Re}\{F_{del}(s+j\omega_g)\} \end{bmatrix}. \tag{4}$$

Combining (1)-(4), the converter output voltage u_{inv}^{dq} settled by the ACC is given as

$$u_{inv}^{dq} = G_{del}G_{ACC}i_{ref}^{dq} - G_{del}\left(G_{ACC} + G_{dec}\right)i_{L1}^{dq}. \tag{5}$$

Considering the voltages and currents of the *LCL* filter, the converter output voltage can be also represented as

$$u_{inv}^{dq} = u_C^{dq} + Z_{L1}i_{L1}^{dq} \tag{6}$$

$$Z_{L1} = \begin{bmatrix} sL_1 & -\omega_g L_1 \\ \omega_g L_1 & sL_1 \end{bmatrix} \tag{7}$$

where Z_{L1} is the impedance matrix of the converter-side inductor. Resorting (5)-(7), the converter output admittance considering only the ACC $Y_{inv,1}^{dq}$ is given as

$$Y_{inv,1}^{dq} = \frac{I}{G_{del}\left(G_{ACC} + G_{dec}\right) + Z_{L1}}. \tag{8}$$

B. High-Frequency Dissipativity Enhancement

To enhance high-frequency dissipativity and save capacitor current sensors, proportional-derivative CVF is used in this paper, which is given as

$$G_{CVF} = \begin{bmatrix} K_p^{CVF} + K_d^{CVF}F_{dev} & 0 \\ 0 & K_p^{CVF} + K_d^{CVF}F_{dev} \end{bmatrix}. \tag{9}$$

The proportional term in CVF is adopted to enhance the dynamics during start-up and grid disturbances. Since an ideal derivative does not exist, a digital derivative F_{dev} is considered in practical implementation [30], which is

$$F_{dev} = \frac{1.8}{T_{sp}} \frac{1 - e^{-sT_{sp}}}{1 + 0.8e^{-sT_{sp}}}. \tag{10}$$

The derivative gain depends on the loop delay and the system parameters [7], which is expressed as

$$K_d^{CVF} = \frac{4T_{del}^2 K_p^{ACC}}{\pi^2 L_1}. \tag{11}$$

Since the compensation depends on the control delay, which is determined by the sampling rate, the DSC cannot fully remove the non-dissipative region near the switching frequency [13]. Hence, MSC is considered to enhance high-frequency dissipativity, whose control delay is inversely proportional to the sampling rate [14]. The detailed implementation of multi-sampling pulse width modulation (PWM) is shown in Fig. 2(b), where state variables and the duty cycles are sampled and updated multiple times within one switching period.

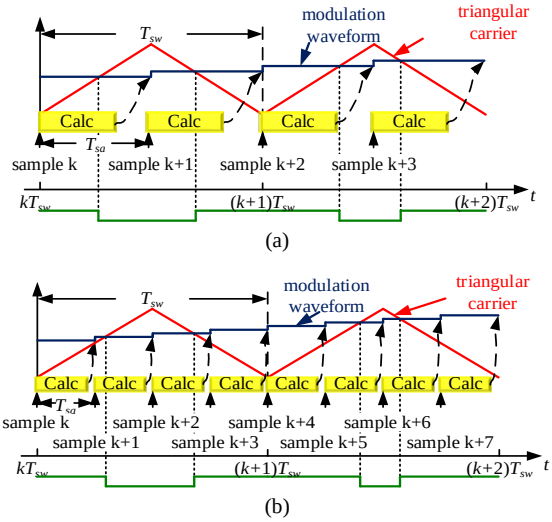


Fig. 2. Diagram of digital PWM. (a) Double-sampling PWM. (b) Multi-sampling PWM.

However, the switching harmonics are introduced to control loops when using the MSC, and the aliased low-frequency harmonics distorts the grid-side current quality [31]. Especially for the eight-sampling control, a ripple filter is required due to severe aliasing effect [31]. When using a high multi-sampling rate, e.g., thirty-two-sampling, the grid-side current quality is comparable to the DSC, so that a ripple filter may not be required [32]. To save computation resources of microprocessors, eight-sampling control with a modified repetitive filter (MRF) is considered in this paper. The MRF contains a compromised moving average filter (CMAF) and a delay compensator [16], which is

$$F_{\mathrm{MRF}} = \underbrace{\frac{2}{N}\frac{1-e^{-NsT_{sp}}}{1-e^{-2sT_{sp}}}}_{\text{CMAF}} \underbrace{\frac{1-r^N}{1-r^2}\frac{1-r^2e^{-2sT_{sp}}}{1-r^Ne^{-NsT_{sp}}}}_{\text{Delay Compensator}} \approx e^{-\frac{sT_{sw}}{4}} \tag{12}$$

where r is the attenuation factor and N represents the sampling rate. Similar to the delay effect modeling, the MRF can be converted to a transfer matrix, which is

$$G_{MRF} = \begin{bmatrix} \mathrm{Re}\{F_{MRF}(s+j\omega_g)\} & -\mathrm{Im}\{F_{MRF}(s+j\omega_g)\} \\ \mathrm{Im}\{F_{MRF}(s+j\omega_g)\} & \mathrm{Re}\{F_{MRF}(s+j\omega_g)\} \end{bmatrix}. \tag{13}$$

Consequently, the equivalent loop delay including both the control delay and the MRF delay is obtained as

$$T_{del,eq} = \underbrace{\frac{1.5}{N}T_{sw}}_{\text{Control delay}} + \underbrace{\frac{1}{4}T_{sw}}_{\text{MRF delay}} = \frac{6+N}{4N}T_{sw}. \tag{14}$$

where T_{sw} is the switching period. The multi-sampling derivative gain can be calculated using (14) and (11). Then the converter output admittance $Y_{inv,2}^{dq}$ is given as

$$Y_{inv,2}^{dq}=\frac{I-G_{del}G_{MRF}G_{CVF}}{G_{del}G_{MRF}\left(G_{ACC}+G_{dec}\right)+Z_{L1}}. \tag{15}$$

C. Phase-Locked Loop (PLL)

To facilitate the analysis, variables are divided into the system and the control frame, which are denoted by the superscript *s* and *c*, respectively [8-9]. The small-signal relationship between the detected phase angle and the *q*-axis capacitor voltage in the system frame is

$$H_{PLL}=\frac{\triangle\theta_{PLL}}{\triangle u_C^{q,s}}=\frac{F_{PLL}}{s+U_C^dF_{PLL}}, \tag{16}$$

$$F_{PLL}=K_p^{PLL}+\frac{K_i^{PLL}}{s}. \tag{17}$$

where F_{PLL} is the PI controller in the PLL. Taking the converter output current i_{L1}^{dq} as an example, the small-signal relationship between two frames is given as

$$\triangle i_{L1}^{dq,c}=\underbrace{\begin{bmatrix}0 & I_{L1}^qH_{PLL}\\ 0 & -I_{L1}^dH_{PLL}\end{bmatrix}}_{G_{PLL}^i}\triangle u_C^{dq,s}+\triangle i_{L1}^{dq,s}. \tag{18}$$

This also applies to the capacitor voltage u_C^{dq} and modulating voltage u_m^{dq}, leading to G_{PLL}^u and G_{PLL}^m, which are expressed as

$$\triangle u_C^{dq,c}=\underbrace{\begin{bmatrix}0 & U_C^qH_{PLL}\\ 0 & -U_C^dH_{PLL}\end{bmatrix}}_{G_{PLL}^u}\triangle u_C^{dq,s}+\triangle u_C^{dq,s}, \tag{19}$$

$$\triangle u_m^{dq,s}=\underbrace{\begin{bmatrix}0 & -U_m^qH_{PLL}\\ 0 & U_m^dH_{PLL}\end{bmatrix}}_{G_{PLL}^m}\triangle u_C^{dq,s}+\triangle u_m^{dq,c}. \tag{20}$$

By further including (16)-(20), the converter output admittance including the PLL $Y_{inv,3}^{dq}$ is obtained as

$$\begin{aligned}Y_{inv,3}^{dq}=&\frac{I-G_{PLL}^m}{G_{del}G_{MRF}\left(G_{ACC}+G_{dec}\right)+Z_{L1}}\\&-\frac{G_{del}G_{MRF}\left(G_{CVF}\left(I+G_{PLL}^u\right)-\left(G_{ACC}+G_{dec}\right)G_{PLL}^i\right)}{G_{del}G_{MRF}\left(G_{ACC}+G_{dec}\right)+Z_{L1}}.\end{aligned} \tag{21}$$

Note that (21) is equal to (15) if the PLL impacts are neglected.

D. Dissipativity analysis

To investigate the dissipativity of the two-dimensional converter output admittances, the frequency-domain real-part values are depicted in Fig. 3 for both DSC and MSC. System specifications of the analyzed VSC are given in Table I. Wideband non-dissipative regions are observed in the diagonal elements, if the CVF is not implemented. The off-diagonal dissipativity are negligible comparing to the diagonal ones, as the decoupling term is implemented and the converter is operated with a unity power factor.

Affected by the control delay, non-dissipative region is inevitable in the high-frequency area above the critical frequency ($1/4T_{del}$). Besides, low-frequency non-dissipative region is also observed in Y_{qq} due to the impact of the PLL. With the proportional-derivative CVF, high-frequency non-dissipative region can be completely mitigated with the MSC. However, non-dissipative region still exists with the DSC.

It is also found that the CVF deteriorates the low-frequency dissipation in both diagonal admittances for both DSC and MSC. The impact of the derivative gain of the CVF is investigated in Fig. 4, which shows no impact on the low-frequency dissipativity. Hence, the low-frequency non-dissipative regions are caused by the proportional gain of the CVF and the PLL. Extra compensations should be considered to achieve wideband dissipativity.

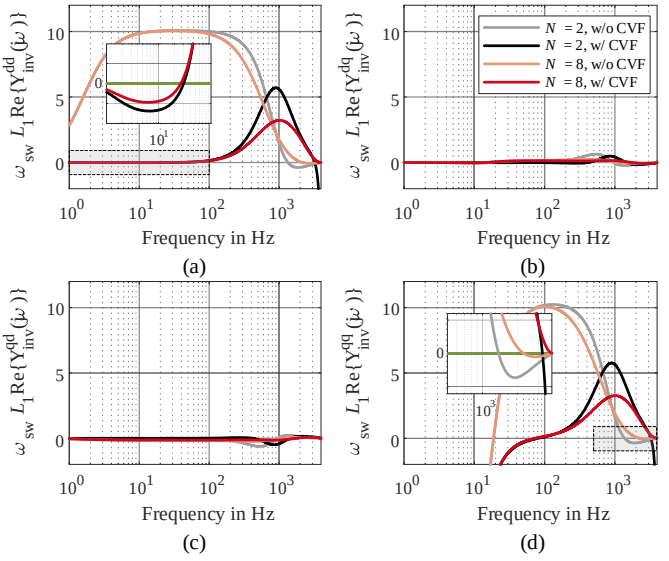


Fig. 3. $\mathrm{Re}\{Y_{inv}(j\omega)\}$ influenced by the CVF, sampling rate *N*, and PLL. (a) $\mathrm{Re}\{Y_{inv}^{dd}(j\omega)\}$. (b) $\mathrm{Re}\{Y_{inv}^{dq}(j\omega)\}$. (c) $\mathrm{Re}\{Y_{inv}^{qd}(j\omega)\}$. (d) $\mathrm{Re}\{Y_{inv}^{qq}(j\omega)\}$.

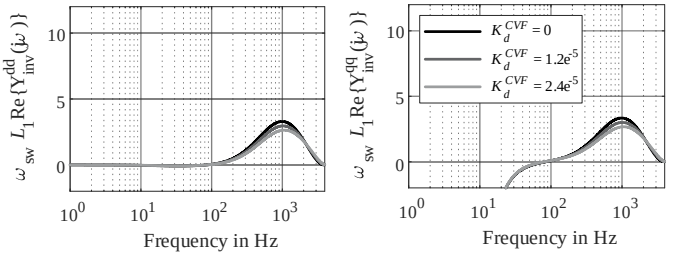


Fig. 4. $\mathrm{Re}\{Y_{inv}(j\omega)\}$ affected by the derivative gain. (a) $\mathrm{Re}\{Y_{inv}^{dd}(j\omega)\}$. (b) $\mathrm{Re}\{Y_{inv}^{qq}(j\omega)\}$.

TABLE I
SYSTEM SPECIFICATIONS OF THE GRID-FOLLOWING VSC

Symbol	Description	Value	Symbol	Description	Value
P_n	Nominal Power	3.5 kW	U_g	Grid phase rms voltage	110 V
U_{dc}	DC-link voltage	350 V	L_1	Converter-side inductor	2 mH
C	Filter capacitor	6 μF	L_2	Converter-side inductor	1 mH
f_{sw}	Switching frequency	4 kHz	r	Attenuation factor for MSC	0.6
$f_{sp,2}$	Sampling frequency	8 kHz	$f_{sp,8}$	Sampling frequency	32kHz
K_p^{ACC}	Proportional gain of ACC	5	K_i^{ACC}	Integral gain of ACC	500
K_p^{PLL}	Proportional gain of PLL	0.8	K_i^{PLL}	Integral gain of PLL	50
K_p^{CVF}	Proportional gain of CVF	1	K_d^{CVF}	Derivative gain of CVF	$1.2e^{-5}$

III. Low-Frequency Disturbance Compensation with Dissipativity Enhancement Control

To enhance VSC stability for weak-grid operations, control schemes are proposed to mitigate asymmetric low-frequency non-dissipative regions in diagonal elements considering the impact of the proportional CVF and PLL. Based on that, a DEC scheme is proposed to unify the low-frequency dissipativity enhancement with a generalized structure utilizing the CVF. The control structure and the parameter design, are elaborated in this section. To realize wideband dissipativity enhancement, the model with MSC is considered for the following analyses. The results also apply to the conventional DSC.

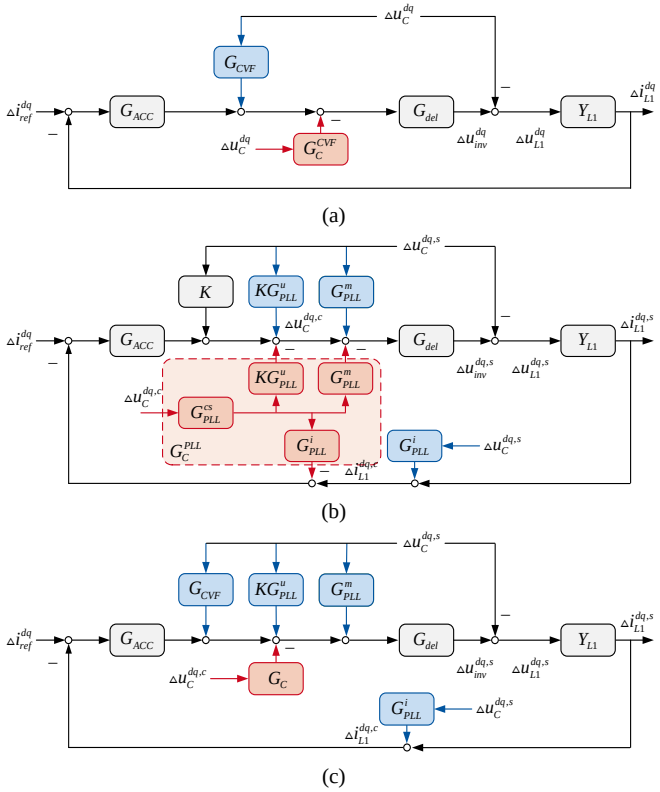


Fig. 5. Control diagram for low-frequency disturbance compensation. (a) Small-signal impact of proportional CVF and its compensation. (b) Small-signal impact of PLL and its compensation. (c) Small-signal impact of both CVF and PLL and complete compensation.

A. Proportional CVF Impact Compensation

According to Fig. 3, the CVF with a unity proportional gain induces low-frequency non-dissipative region. Thus, it is reasonable to enhance dissipativity by partly compensating for the CVF impact. Thereby, a diagonal matrix G_C^{CVF} is subtracted from the G_{CVF}, as illustrated in Fig. 5(a), which is

$$G_C^{CVF} = \begin{bmatrix} D_0 & 0 \\ 0 & D_0 \end{bmatrix}, \tag{22}$$

where D_0 is a constant damping gain between zero and one. Consequently, the proportional gain of CVF is modified to a new equivalent gain K, which is

$$K = K_p^{CVF} - D_0. \tag{23}$$

The compensation performance of G_C^{CVF} is depicted in Fig. 6. An increased value of D_0 can effectively improve the low-frequency dissipativity, which however, deteriorates the high-frequency dissipativity and reduces the dynamic performance against grid disturbances. As a tradeoff between the dissipativity enhancement and dynamic performance, $D_0 = 0.1$ is considered in this work, which has also been discussed in [13, 15]. It is found that D_0 has no impact on the non-dissipative region induced by the PLL (see Fig. 3(d) and Fig. 6(b)).

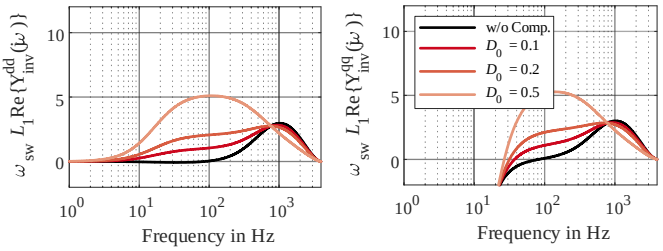


Fig. 6. $\mathrm{Re}\{Y_{inv}(j\omega)\}$ with the CVF impact compensation. (a) $\mathrm{Re}\{Y_{inv}^{dd}(j\omega)\}$. (b) $\mathrm{Re}\{Y_{inv}^{qq}(j\omega)\}$.

B. PLL Impact Compensation

According to (18)-(20), the PLL disturbance on Y_{qq} is induced by the capacitor voltage in the system frame $u_C^{s,q}$, while the reverse compensation can only utilize the capacitor voltage in the control frame $u_C^{c,q}$. Thus, a conversion from the control to the system frame is required. According to (16) and (19), the conversion is derived as follows

$$G_{PLL}^{cs,q} = \frac{\Delta u_C^{q,s}}{\Delta u_C^{q,c}} = \frac{s + F_{PLL} U_C^d}{s}. \tag{24}$$

The small-signal diagram of the PLL impact and the compensation scheme are shown in Fig. 5(b). The compensation of the current disturbance at the current reference is obtained as

$$G_{PLL}^{cs,q} G_{PLL}^{i,q} = \frac{-I_{L1}^d}{s}\left(K_p^{PLL} + \frac{K_i^{PLL}}{s}\right). \tag{25}$$

To explore a generalized control structure, the compensation can also be moved to the modulating voltage by including the ACC, which is

$$-F_{ACC} G_{PLL}^{cs,q} G_{PLL}^{i,q} = \frac{I_{L1}^d}{s}\left(K_p^{PLL} + \frac{K_i^{PLL}}{s}\right)\left(K_p^{ACC} + \frac{K_i^{ACC}}{s}\right). \tag{26}$$

Since the voltage drop on the converter-side inductor is negligible, the impact of the Park transformation on the CVF and the inverse Park transformation on the modulating voltage is counteracted, i.e., $G_{PLL}^{m,q} \approx -G_{PLL}^{u,q}$. Thus, the compensation considering the CVF with a variable gain K is obtained as

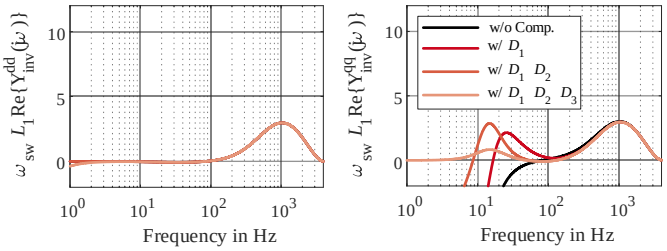
$$G_{PLL}^{cs,q} G_{PLL}^{u,q} (1-K) = \frac{U_C^d}{s}\left(K_p^{PLL} + \frac{K_i^{PLL}}{s}\right)(1-K). \tag{27}$$

Consequently, the PLL disturbance can be compensated with a single matrix G_C^{PLL} at the modulating voltage. Resorting (26) and (27), the compensation including multiple integrators is

$$G_C^{PLL}=\begin{bmatrix}0 & 0\\ 0 & \dfrac{D_1}{s}+\dfrac{D_2}{s^2}+\dfrac{D_3}{s^3}\end{bmatrix}, \tag{28}$$

$$\begin{cases} D_1=\left(K_p^{ACC}I_{L1}^d+(1-K)U_C^d\right)K_p^{PLL}\\ D_2=\left(K_p^{ACC}I_{L1}^d+(1-K)U_C^d\right)K_i^{PLL}+K_i^{ACC}K_p^{PLL}I_{L1}^d\\ D_3=K_i^{ACC}K_i^{PLL}I_{L1}^d \end{cases}. \tag{29}$$

where D_1, D_2, and D_3 are the damping gains of integrators. It is recommended to design the damping gains using the rated current and voltage, in order to achieve better dissipativity. Besides, computational resources can also be saved without updating the damping gains. The compensation performance of G_C^{PLL} is depicted in Fig. 7, and low-frequency non-dissipative region induced by the PLL can be completely mitigated.



(a) (b)

Fig. 7. Re{$Y_{inv}(j\omega)$} with the PLL impact compensation. (a) Re{$Y_{inv}^{dd}(j\omega)$}. (b) Re{$Y_{inv}^{qq}(j\omega)$}.

C. Dissipativity Enhancement Control

Combining the compensation scheme for the CVF and PLL, a DEC strategy is proposed, which unifies the dissipativity enhancement to an asymmetric diagonal matrix G_C, which is

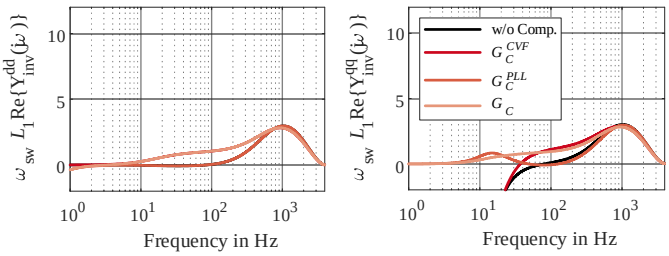
$$G_C=G_C^{CVF}+G_C^{PLL}=\begin{bmatrix}D_0 & 0\\ 0 & D_0+\dfrac{D_1}{s}+\dfrac{D_2}{s^2}+\dfrac{D_3}{s^3}\end{bmatrix}. \tag{30}$$

According to Figs. 6 and 7, damping gains with different orders can improve dissipativity at different frequency regions. Thus, (30) provides a generalized structure to design low-frequency dissipativity flexibly. Note that (29) only provides a guideline for the control design. Since the compensation is inserted at the modulating voltage, the damping gains can be tuned individually according to the compensation requirements, which are decoupled with the ACC.

The control diagram with the proposed DEC is presented in Fig. 5(c).and the converter output admittance $Y_{inv,4}^{dq}$ is

$$Y_{inv,4}^{dq}=\frac{I-G_{PLL}^m}{G_{del}G_{MRF}\left(G_{ACC}+G_{dec}\right)+Z_{L1}}- \frac{G_{del}G_{MRF}\left(\left(G_{CVF}-G_C\right)\left(I+G_{PLL}^u\right)-\left(G_{ACC}+G_{dec}\right)G_{PLL}^i\right)}{G_{del}G_{MRF}\left(G_{ACC}+G_{dec}\right)+Z_{L1}}. \tag{31}$$

The compensation performance of the proposed DEC is illustrated in Fig. 8. With the DEC, low-frequency dissipativity can be significantly lifted, and the dissipativity can be realized in both low- and high-frequency regions.



(a) (b)

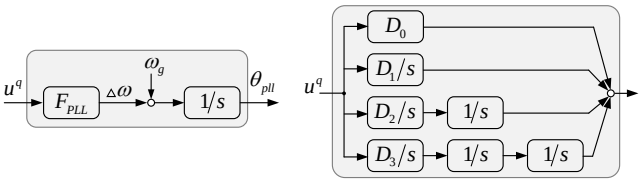
Fig. 8. Re{$Y_{inv}(j\omega)$} with the complete compensation. (a) Re{$Y_{inv}^{dd}(j\omega)$}. (b) Re{$Y_{inv}^{qq}(j\omega)$}.

IV. Modified Integrators Against Grid Frequency Variations

The DEC contains high-order integrations, which affect the current tracking capability and can destabilize system under grid frequency deviations. To cope with the challenge, a modified DEC is proposed by replacing the high-order integrators with low-pass filters (LPFs). The current tracking capability with modified integrators, the design of the LPF bandwidths, and the control robustness are elaborated.

A. Modified Integrators

As compared in Fig. 9, the control structure of the PLL and the complete compensation in *q*-axis both utilize the capacitor voltage as an input. With the PI controller and an integrator, the PLL contains a 2nd-order integration of the *q*-axis voltage. The dynamics of the PLL influences the detected grid phase angle, which does not directly affect the ACC. Different from the PLL, as depicted in Fig. 9(b). the *q*-axis compensation is directly fed at the modulation voltage with 3rd-order integrators. Hence, the impact of pure integrations requires further inspections.



(a) (b)

Fig. 9. Control diagram comparison. (a) Phase-locked loop. (b) Dissipativity enhancement control (*q*-axis).

The reference tracking capability can be analytically exanimated by dividing the G_C with the ACC, and the complete compensation provides indeed an additional current reference Δi_{refC}^q, whose transfer function is

$$\begin{aligned} M_C&=\frac{\Delta i_{refC}^q}{\Delta u_C^q}=-\frac{D_0+\dfrac{D_1}{s}+\dfrac{D_2}{s^2}+\dfrac{D_3}{s^3}}{F_{ACC}}\\ &=-\frac{sD_0}{sK_p^{ACC}+K_i^{ACC}}-\frac{D_1}{sK_p^{ACC}+K_i^{ACC}}\\ &\quad\underbrace{-\frac{D_2}{s\left(sK_p^{ACC}+K_i^{ACC}\right)}}_{\text{Frequency Disturbance}}\underbrace{-\frac{D_3}{s^2\left(sK_p^{ACC}+K_i^{ACC}\right)}}_{\text{Angle Disturbance}}. \end{aligned} \tag{32}$$

Similar to the dynamics of the PLL, a 1st-order integration of the *q*-axis voltage disturbance leads to a frequency disturbance,

and a 2nd-order integration results in an angle disturbance. Since the grid phase angle disturbance is usually not zero, a non-zero constant is added in the *q*-axis reference current, which leads to undesired reactive power. Under grid frequency deviations, the 1st-order integration is a non-zero value and the 2nd-order integration is infinite, which destabilizes the system.

To eliminate the steady-state error of the reactive current for cases without the grid frequency deviation, one of integrators of the 3rd-order term is modified to a LPF with a cutoff frequency $\omega_{c1} = 2\pi f_{c1}$, and type-I DEC is

$$G_{Cm1} = \begin{bmatrix} D_0 & 0 \\ 0 & D_0 + \dfrac{D_1}{s} + \dfrac{D_2}{s^2} + \dfrac{D_3}{s^2(s+\omega_{c1})} \end{bmatrix}. \quad (33)$$

By dividing the *q*-axis transfer function of G_{cm1} with the ACC, the additional current reference Δi^q_{refCm1} is

$$\begin{aligned} M_{Cm1} &= \frac{\Delta i^q_{refCm1}}{\Delta u^q_C} = -\frac{D_0 + \dfrac{D_1}{s} + \dfrac{D_2}{s^2} + \dfrac{D_3}{s^2(s+\omega_{c1})}}{F_{ACC}} \\ &= -\frac{sD_0}{sK_p^{ACC} + K_i^{ACC}} - \frac{D_1}{sK_p^{ACC} + K_i^{ACC}} \\ &\quad -\frac{D_2}{s\left(sK_p^{ACC} + K_i^{ACC}\right)} - \frac{D_3}{s(s+\omega_{c1})\left(sK_p^{ACC} + K_i^{ACC}\right)}. \end{aligned} \quad (34)$$

Note that (34) contains only 1st-order integrations, which is zero without grid frequency deviations. Hence, no additional current reference is introduced by the complete compensation. However, considering grid frequency deviation, it is required to further modify one of integrators of the 2nd-order term to a LPF with a cut-off frequency $\omega_{c2} = 2\pi f_{c2}$, and type-II DEC is

$$G_{Cm2} = \begin{bmatrix} D_0 & 0 \\ 0 & D_0 + \dfrac{D_1}{s} + \dfrac{D_2}{s(s+\omega_{c2})} + \dfrac{D_3}{s(s+\omega_{c2})(s+\omega_{c1})} \end{bmatrix}. \quad (35)$$

In this case, the additional current reference Δi^q_{refCm2} is

$$\begin{aligned} M_{Cm2} &= \frac{\Delta i^q_{refCm2}}{\Delta u^q_C} = -\frac{D_0 + \dfrac{D_1}{s} + \dfrac{D_2}{s(s+\omega_{c2})} + \dfrac{D_3}{s(s+\omega_{c2})(s+\omega_{c1})}}{F_{ACC}} \\ &= -\frac{sD_0}{sK_p^{ACC} + K_i^{ACC}} - \frac{D_1}{sK_p^{ACC} + K_i^{ACC}} \\ &\quad -\frac{D_2}{(s+\omega_{c2})\left(sK_p^{ACC} + K_i^{ACC}\right)} \\ &\quad -\frac{D_3}{(s+\omega_{c2})(s+\omega_{c1})\left(sK_p^{ACC} + K_i^{ACC}\right)}. \end{aligned} \quad (36)$$

Note that (36) contains no pure integrations, and both the reference tracking capability and stability can be guaranteed.

B. Low-Pass Filter Bandwidth Design

The bandwidths of LPFs in the modified integrators affect both the frequency response of the DEC and the frequency-domain dissipation of the converter output admittance. Hence, the selection of LPF bandwidths requires further investigations.

The frequency responses of the pure integrator and LPFs with different bandwidths are compared in Fig. 10. The pure integrator has an infinite dc gain and shows poor attenuation in the low-frequency area, which challenges both the reference tracking capability and dynamics of the *q*-axis current, according to (32). To eliminate undesired reactive current in the steady-state, a finite dc gain should be designed, which can be realized by a LPF with any bandwidth. To improve the response dynamics, a higher bandwidth of the LPF is desired. The LPF with a higher bandwidth provides more attenuation for a wider low-frequency area, which can effectively suppress the slow-dynamic components in transients. As a result, the *q*-axis current dynamics can be improved. From the perspective of control dynamics, a higher LPF bandwidth is preferred.

However, the LPFs also affect the dissipation of the converter output admittance. As indicated in Fig. 8, the DEC with pure integrations can fully mitigate low-frequency non-dissipative region. Nevertheless, the dissipative area reduces with increased LPF bandwidths. Fig. 11 illustrates the lower frequency boundaries with positive dissipation affected by the

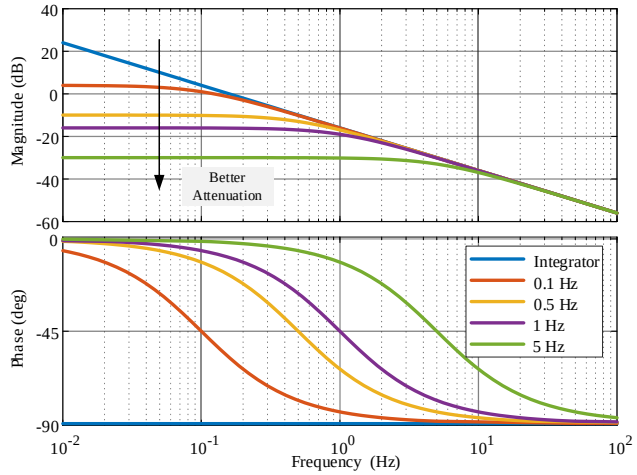


Fig. 10. Frequency response of the pure integrator and the LPF $1/(s+2\pi f_c)$ with different bandwidths.

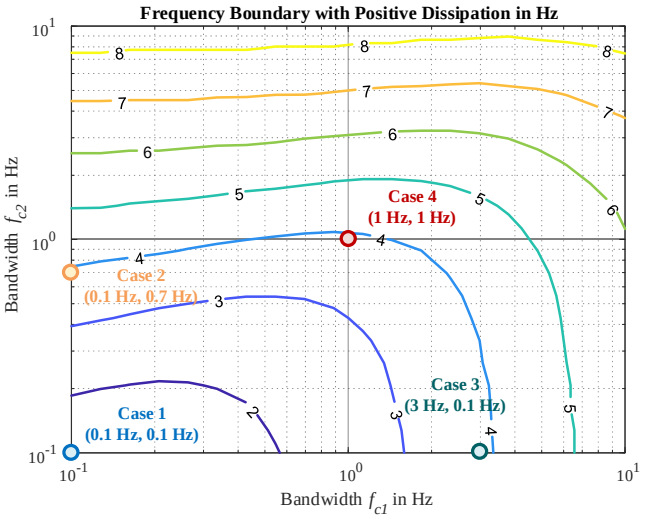


Fig. 11. The lower frequency boundary contour with positive dissipation affected by f_{c1} and f_{c2}, and investigated cases.

bandwidths f_{c1} and f_{c2}, simultaneously. It is found that the dissipation boundary is more sensitive to the bandwidth f_{c2}. This is reasonable, as f_{c2} modifies both the 2nd- and 3rd-order integrations of the DEC. Depending on the desired dissipation boundary, the upper limit of f_{c1} and f_{c2} can be determined quantitatively.

Taking the control dynamics and the dissipativity of converter admittance both into account, it is suggested to select all bandwidths as high as possible within the desired dissipativity boundary, so that the control dynamics can be improved without affecting the target dissipation boundary.

To validate the design criterion, four cases with different combinations of LPF bandwidths are considered within the desired dissipation boundary, as depicted in Fig. 11. It is found that the admittances of the converter and grid intersect at about 8 Hz under a very weak grid (SCR = 1.1). Thus, the desired lower boundary with positive dissipation is considered as 4 Hz, to leave a certain margin. Case 1 extends the positive dissipation to 1.5 Hz with rather low bandwidths, while Cases 2-4 realize the target dissipation boundary with different combinations of bandwidths. The dissipativity properties with the modified DEC are depicted in Fig. 12. Though with different LPF bandwidths, the lower boundaries with positive dissipation are almost same for Cases 2-4, which presents similar dissipation feature. The proposed DEC also applies to the conventional DSC. With the same parameters of DEC, identified low-frequency dissipation can be realized comparing to the MSC. However, high-frequency dissipation cannot be secured with the DSC, as explained in Fig. 3.

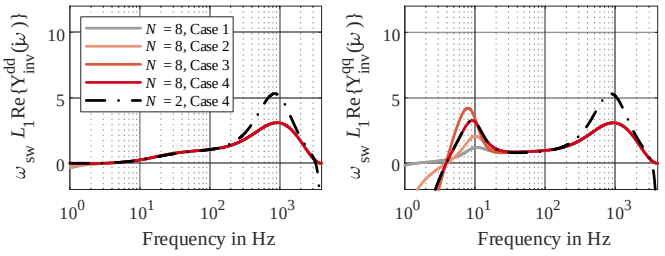


Fig. 12. Re{$Y_{inv}(j\omega)$} of the DEC with modified integrators considering various LPF bandwidths and sampling rates N. (a) Re{$Y_{inv}^{dd}(j\omega)$}. (b) Re{$Y_{inv}^{qq}(j\omega)$}.

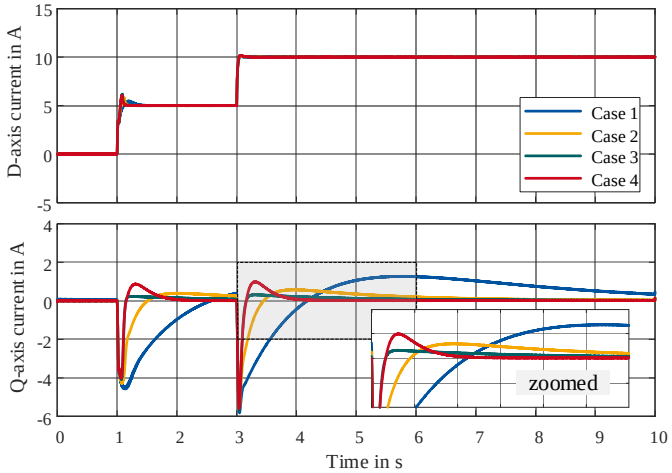


Fig. 13. Dynamic performance of currents with different LPF bandwidths (f_g = 51 Hz, SCR = 1.1).

The dynamic performance of currents for four different cases are compared in Fig. 13, considering a current step change. Although the dissipation boundary can be extended with smaller LPF bandwidths, the q-axis current dynamics becomes quite slow, as explained with Fig. 10. Among the selected cases, the fastest transient is achieved if both bandwidths are considered as 1 Hz, which proves the proposed design criterion. Hence, 1 Hz is considered for both bandwidths in this work for the following analyses.

C. Robustness Analysis

Since the damping gains of the DEC are designed considering the rated current and voltage according to (29), it is necessary to investigate the robustness of the control scheme against a wide variation of operating points.

The control robustness against variable SCR is illustrated in Fig. 14(a) from a normal grid to a very weak grid operation. It is found that a decreased SCR does not enlarge the existing non-dissipative region.

The control robustness against d-axis current variation is investigated in Fig. 14(b). The low-frequency non-dissipative region extends with a higher current. The designed dissipative boundary is reached, when the d-axis current increases to the rated value (15 A).

Besides, the control robustness is validated considering ±20% variation of the converter-side filter inductance. Various filter inductance affects the high-frequency dissipativity, while it has no impact on the low-frequency dissipativity.

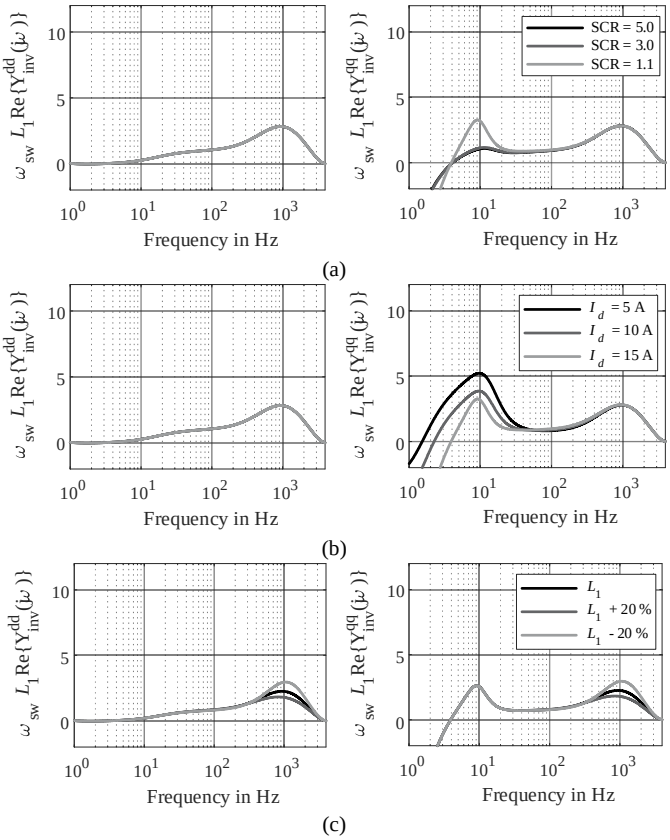


Fig. 14. Robustness analyses of the proposed DEC. (a) Re{$Y_{inv}(j\omega)$} with variable SCR (I_d = 15 A). (b) Re{$Y_{inv}(j\omega)$} with variable current (SCR = 1.1). (c) Re{$Y_{inv}(j\omega)$} with variable filter inductance (I_d = 15 A and SCR = 1.1).

TABLE II
COMPARISONS WITH STATE-OF-ART METHODS

Ref	Method	High-freq. Dissipation	High-freq. Robustness	Low-freq. Dissipation	Low-freq. Robustness
[12]	DSC and CCF	+	-	N/A	N/A
[13]	DSC, CCF, and CVF	+	+	N/A	N/A
[14]	DSC and CVF	-	+	N/A	N/A
[16][19]	MSC and CVF	+	+	N/A	N/A
[20-21]	PLL gain design	N/A	N/A	+	+
[22]	Lead-leg comp. in PLL	N/A	N/A	+	+
[5][11]	Reduce CVF gain	N/A	N/A	+	+
[23-25]	Reverse comp. of PLL	N/A	N/A	+	-
[27]	Dual PLL	N/A	N/A	+	+
Proposed	MSC and CVF	+	+	+	+

The proposed method is also compared to other state-of-the-art methods for high- or low-frequency dissipativity design, as summarized in TABLE II. Combining the MSC and CVF, robust high-frequency dissipation can be obtained up to the switching frequency. Utilizing multi-order integrations, asymmetric low-frequency non-dissipative regions induced by CVF and PLL can be reversely compensated, so that wideband dissipativity enhancement can be realized. By further modifying high-order integrations, the system is capable to operate with very weak grid even under frequency variations. The proposed DEC control also applies to the conventional DSC with regard to the low-frequency dissipation enhancement.

V. EXPERIMENTAL VALIDATION

To further verify the theoretical analyses, experiments are carried out on a down-scaled three-phase grid-connected VSC with an *LCL* filter, as shown in Fig. 15. The grid is emulated with a high-fidelity linear amplifier APS 15000. The applied half-bridge module and the control platform are a PEB-SiC-8024 module and a B-BOX RCP control platform from Imperix, respectively. Discretization time of the digital controller is considered the same as the sampling time. The parameters of used three-phase grid-connected VSC are presented in Table I. To prove the breadth of applicability of the proposed DEC, experiments are conducted considering both the MSC and DSC.

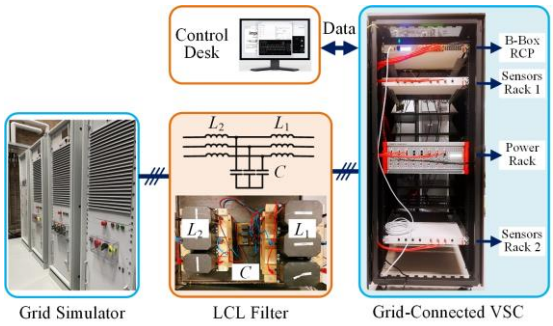


Fig. 15. A down-scaled three-phase grid-connected VSC with an *LCL* filter.

A. Weak Grid

To investigate the low-frequency dissipativity performance of the proposed DEC, two weak-grid cases are considered for an eight-sampling controlled VSC, with and without the DEC. Based on the system specifications in Table I, the base grid impedance is 33 mH, and the grid impedance is set to 30 mH to emulate a weak-grid scenario of SCR = 1.1.

The system stability can be judged through the intersection between the diagonal admittances of the inverter seen from the filter capacitor $Y_{inv}(s)$ and the equivalent grid admittance $Y_{g,eq}(s)$. Herein, L_2, L_g, and C are regarded as an equivalent grid admittance $Y_{g,eq}(s) = 1/s(L_2+L_g)+sC$.

The frequency-domain properties of the *q*-axis diagonal admittances are depicted in Fig. 16, considering SCR=1.1 and $i_{ref}^{d} = 15$ A. The low-frequency admittances are identified for both MSC and DSC. It is observed that $Y_{inv}(s)$ intersects with $Y_{g,eq}(s)$ in its low-frequency negative-real-part region, which leads to a -28° phase margin (PM) and destabilizes the system. After implementing the proposed DEC, the system becomes stabilized due to the reshaped dissipativity, which applies to both MSC and DSC. Note that the high-frequency (>1kHz) characteristic of $Y_{inv}(s)$ remains almost the same as the case without using the DEC.

Experimental results of the eight-sampling control are carried to validate the analysis. The *q*-axis reference current is set to zero for a unity power factor operation, while the *d*-axis reference current varies from 0 A to 15 A (rated current) step by step to validate the robustness against the operation point variation. It can be seen from Fig. 17 that the VSC system becomes unstable when $i_{ref}^{d} = 15$ A without using the DEC.

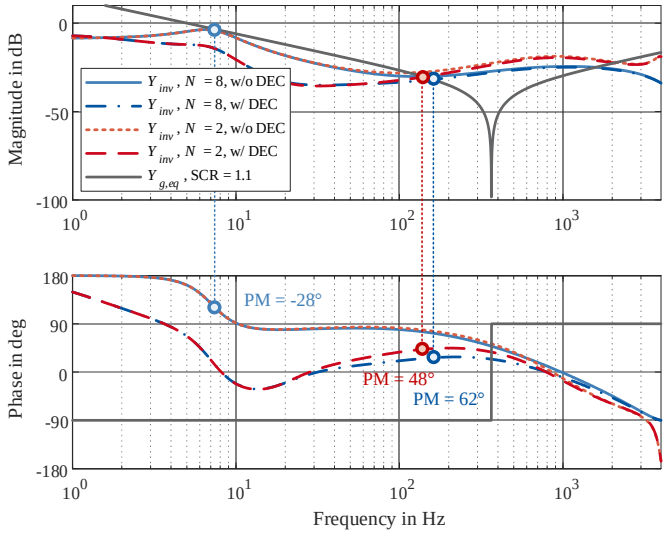


Fig. 16. VSC output admittance using the eight-sampling and double-sampling control seen from the filter capacitor $Y_{inv}(s)$ and the equivalent grid admittance $Y_{g,eq}(s)$, both are *q*-axis diagonal admittances.

After implementing the type-II modified DEC, the system stability is guaranteed under a weak-grid scenario, even for full-power operation, as presented in Fig. 18. It is also validated with experiments that the proposed type-II DEC also applies to the DSC, as observed in Fig. 19.

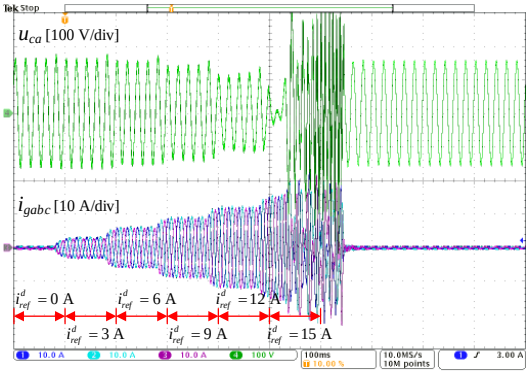


Fig. 17. Experimental result using the eight-sampling without the dissipativity enhancement control (f_g = 50 Hz, SCR = 1.1).

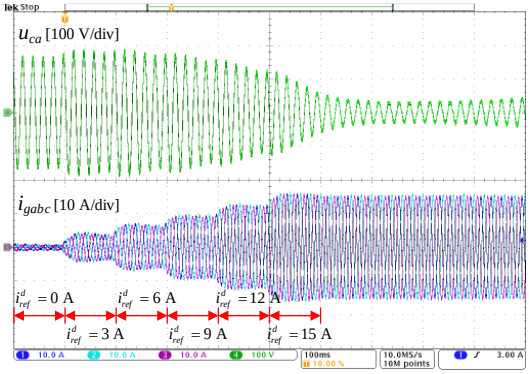


Fig. 18. Experimental result using the eight-sampling and the dissipativity enhancement control (f_g=50 Hz, SCR = 1.1, modified integrators).

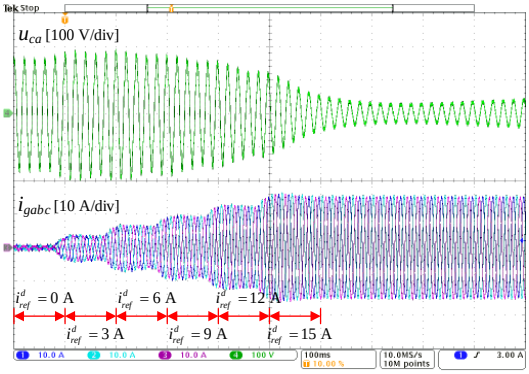


Fig. 19. Experimental result using the double-sampling and the dissipativity enhancement control (f_g=50 Hz, SCR = 1.1, modified integrators).

B. Grid Frequency Deviation

To verify the effectiveness of the proposed DEC with modified integrators, experiments are further conducted considering the scenario with both weak grid and grid frequency deviations, i.e., with SCR = 1.1 and f_g = 51 Hz.

If the DEC is implemented without modified integrators, the *q*-axis reference current change towards infinite due to the pure integrations in the DEC, as explained in (32). As a result, the *q*-axis current continually increases, which eventually triggers the over-current protection, as depicted in Fig. 20. Note that the *d*-axis reference current is set as zero in this case.

After implementing the type-II DEC with the modified integrators, the system can remain stable even under a frequency deviation f_g = 51 Hz, as illustrated in Fig. 21. No extra reactive current is introduced, which is consistent with the analysis in (36). With the proposed DEC and modified integrators, the system stability can be guaranteed for weak-grid operations even under grid frequency deviations. It is also validated with experiments that the proposed type-II DEC also applies to the DSC, as observed in Fig. 22.

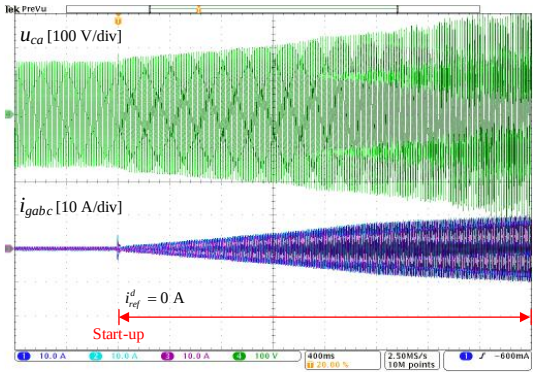


Fig. 20. Experimental result using the eight-sampling with the dissipativity enhancement control and grid frequency deviation (f_g = 51 Hz, SCR = 1.1, pure integrations).

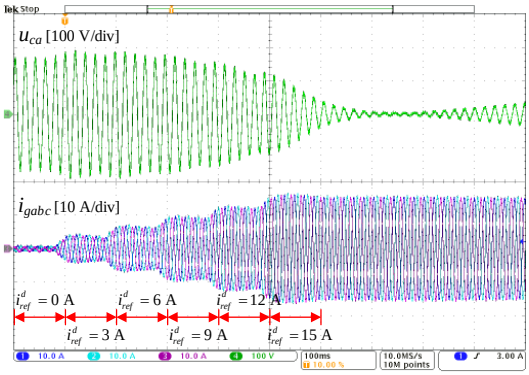


Fig. 21. Experimental result using the eight-sampling with the dissipativity enhancement control and grid frequency deviation (f_g = 51 Hz, SCR = 1.1, modified integrators).

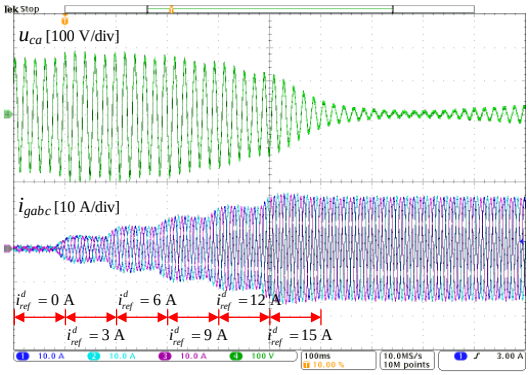


Fig. 22. Experimental result using the double-sampling with the dissipativity enhancement control and grid frequency deviation (f_g = 51 Hz, SCR = 1.1, modified integrators).

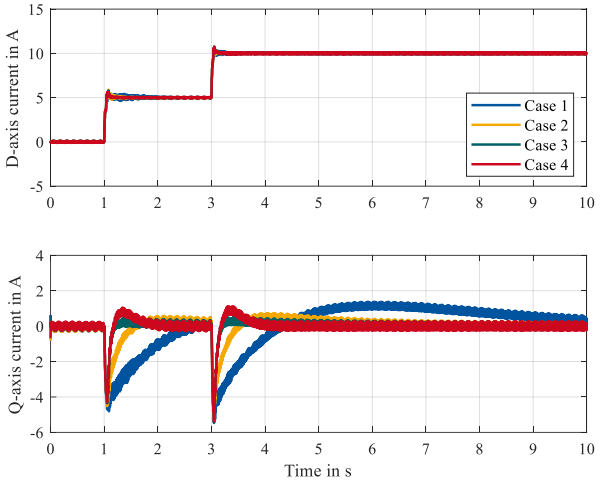


Fig. 23. Experimental result of current dynamic performance with different LPF bandwidths (f_g = 51 Hz, SCR = 1.1).

In addition, the dynamic performances of LPFs with different bandwidths are compared in Fig. 23, considering four cases selected in Fig. 11. Note that Case 4 achieves the fastest transient, while Case 1 shows the slowest transient, which is consistent with the simulation results depicted in Fig. 13. Hence, it can be validated that higher bandwidths are preferred within the desired dissipation boundary to improve control dynamics.

C. Strong Grid

To validate the high-frequency dissipativity of the proposed method, experiments for strong-grid cases are also considered. Herein, the grid impedance is set as zero, L_2 and C are regarded as the equivalent grid admittance $Y_{g,eq}(s) = 1/sL_2+sC$.

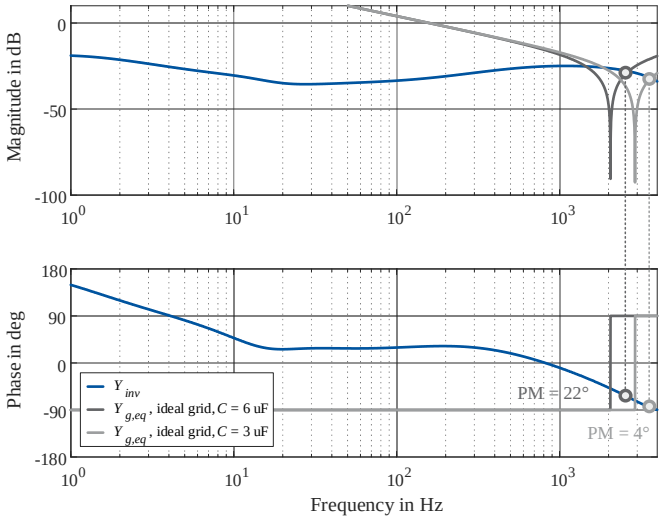


Fig. 24. VSC output admittance using the eight-sampling seen from the filter capacitor $Y_{inv}(s)$ and the equivalent grid admittance $Y_{g,eq}(s)$, both are q-axis diagonal admittances and grid impedance is zero.

In the first case, the *LCL* resonance frequency is f_r = 2517 Hz with C = 6 μF. Due to the MSC, the high frequency dissipativity is realized up to the switching frequency. As a result, the system shows a stability margin of PM=22°, as depicted in Fig. 24. For a more severe case, i.e., with C = 3 μF and the *LCL* resonance frequency f_r=3559 Hz, the system still remains a positive PM. However, a non-dissipative region would occur around the switching frequency with the conventional DSC, which has been validated in [15] and is not discussed in this work.

Experimental results for strong-grid operations are shown in Figs. 25-26. The q-axis reference current is set as zero for the unity power factor operation, while the d-axis reference current varies from 0 A to 15 A (rated current) step by step. As presented in Fig. 25, the system can remain stable for full-power operation with the proposed method, as the high-frequency non-dissipative region is eliminated through the MSC. For the worse case with C = 3 μF, the *LCL* resonance frequency is 3559 Hz, which is close to the switching frequency of 4 kHz. As depicted in Fig. 26, the *LCL* filter almost loses the switching harmonic filtering capability in this case due to a too small grid-side capacitor, so that the grid-side current quality is not satisfied. However, the system can still remain stabilized.

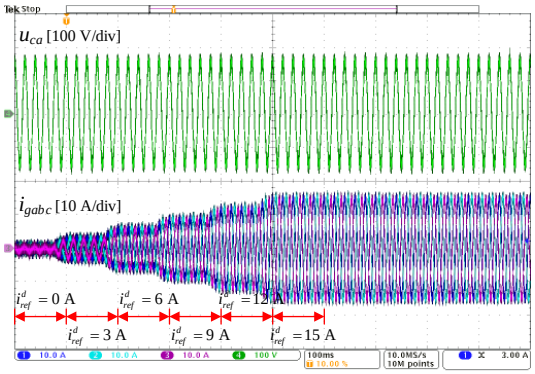


Fig. 25. Experimental result using the eight-sampling with the dissipativity enhancement (f_g = 50 Hz, strong grid, C = 6 μF).

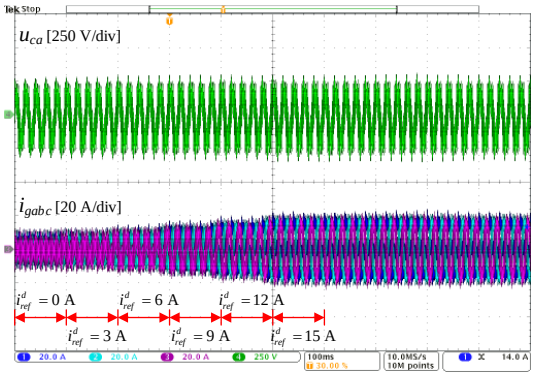


Fig. 26. Experimental result using the eight-sampling with the dissipativity enhancement control (f_g = 50 Hz, strong grid, and C = 3 μF).

As a summary, wideband dissipativity enhancement is realized utilizing the MSC and the proposed DEC, so that both low-frequency and high-frequency resonances can be prevented. The system can remain stabilized with the proposed DEC and the modified integrator for strong-grid operations, weak-grid operations, and grid frequency disturbances.

VI. Conclusion

This paper analyzes the frequency-domain dissipation of grid-following VSCs, considering different sampling rates. It is found that the CVF can reshape the converter admittance in a wide frequency range. With the MSC and proportional-

derivative CVF, robust high-frequency dissipation can be realized up to the switching frequency. To further improve the low-frequency dissipativity, a DEC scheme is proposed to compensate for the negative impact of the proportional CVF and PLL. The compensation utilizes the CVF with a generalized structure and multiple-order integrations. However, high-order integrations can lead to undesired reactive current or even destabilize system under grid frequency deviations. Thus, modified integrators are proposed to further optimize the DEC against grid frequency variations. With the proposed DEC and modified integrators, wideband dissipativity can be realized from several hertz to the switching frequency. The system can remain stabilized under very weak grid even with frequency deviation. The proposed method applies to both the MSC and conventional DSC, which is also verified through experiments.

REFERENCES

[1] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B. Hodge, and B. Hannegan "Achieving a 100% renewable grid: operating electric power systems with extremely high levels of variable renewable energy," *IEEE Power Energy Mag*., vol. 15, no. 2, pp. 61–73, Mar. 2017.

[2] X. Wang and F. Blaabjerg, "Harmonic stability in power electronic-based power systems: concept, modeling, and analysis," *IEEE Trans. Smart Grid*, vol. 10, no. 3, pp. 2858-2870, May 2019.

[3] C. Li, "Unstable operation of photovoltaic inverter from field experiences," *IEEE Trans. Power Deliv*., vol. 33, no. 2, pp. 1013-1015, April 2018.

[4] J. Sun, G. Wang, X. Du, and H. Wang, "A theory for harmonics created by resonance in converter-grid systems," *IEEE Trans. Power Electron*., vol. 34, no. 4, pp. 3025-3029, April 2019.

[5] L. Harnefors, M. Bongiorno, and S. Lundberg, "Input-admittance calculation and shaping for controlled voltage-source converters," *IEEE Trans. Ind. Electron*., vol. 54, no. 6, pp. 3323-3334, Dec. 2007.

[6] L. Harnefors, X. Wang, A. Yepes, and F. Blaabjerg, "Passivity-based stability assessment of grid-connected VSCs-An overview," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 4, no. 1, pp. 116–125, Mar. 2016.

[7] L. Harnefors, A. Yepes, A. Vidal, and J. Gandoy, "Passivity-based controller design of grid-connected VSCs for prevention of electrical resonance instability," *IEEE Trans. Ind. Electron*., vol. 62, no. 2, pp. 702-710, Feb. 2015.

[8] B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters," *IEEE Trans. Power Electron., vol*. 31, no. 1, pp. 26-38, Jan. 2016.

[9] Z. Yang, C. Shah, T. Chen, L. Yu, P. Joebges, and R. De Doncker, "Stability investigation of three-phase grid-tied PV inverter systems using impedance models," *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 10, no. 3, pp. 2672-2684, June 2022.

[10] D. Wang, L. Liang, L. Shi, J. Hu, and Y. Hou, "Analysis of modal resonance between PLL and DC-link voltage control in weak-grid tied VSCs," *IEEE Trans. Power Syst*., vol. 34, no. 2, pp. 1127-1138, March 2019.

[11] H. Gong, X. Wang, and L. Harnefors, "Rethinking current controller design for PLL-synchronized VSCs in weak grids," *IEEE Trans. Power Electron*., vol. 37, no. 2, pp. 1369-1381, Feb. 2022.

[12] X. Wang, Y. He, D. Pan, H. Zhang, Y. Ma, and X. Ruan, "Passivity enhancement for LCL-filtered inverter with grid current control and capacitor current active damping," *IEEE Trans. Power Electron*., vol. 37, no. 4, pp. 3801-3812, April 2022.

[13] C. Xie, K. Li, J. Zou, and J. Guerrero, "Passivity-based stabilization of LCL-type grid-connected inverters via a general admittance model," *IEEE Trans. Power Electron*., vol. 35, no. 6, pp. 6636-6648, 2020.

[14] C. Wang, X. Wang, Y. He, and X. Ruan, "A passivity-based weighted proportional-derivative feedforward scheme for grid-connected inverters with enhanced harmonic rejection ability," *IEEE J. Emerg. Sel. Top. Power Electron., early access*, 2023.

[15] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "A review of multi-sampling techniques in power electronics applications," *IEEE Trans. Power Electron*., vol. 37, no. 9, pp. 10514-10533, Sept. 2022.

[16] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Passivity-based multisampled converter-side current control of LCL-filtered VSCs," *IEEE Trans. Power Electron*., vol. 37, no. 11, pp. 13848-13860, Nov. 2022.

[17] I. Z. Petric, P. Mattavelli, and S. Buso, "Multi-sampled grid-connected VSCs: a path toward inherent admittance passivity," *IEEE Trans. Power Electron*, vol. 37, no. 7, pp. 7675-7687, July 2022.

[18] I. Z. Petric, P. Mattavelli, and S. Buso, "Passivation of grid-following VSCs: A comparison between active damping and multi-sampled PWM," *IEEE Trans. Power Electron*., vol. 37, no. 11, pp. 13205–13216, Nov. 2022.

[19] S. He, Z. Yang, D. Zhou, X. Wang, R. W. De Doncker and F. Blaabjerg, "Dissipativity robustness enhancement for LCL-filtered grid-connected VSCs with multisampled grid-side current control," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3992-4004, March 2023.

[20] D. Zhu, S. Zhou, X. Zou, and Y. Kang, "Improved design of PLL controller for LCL-type grid-connected converter in weak grid," *IEEE Trans. Power Electron*., vol. 35, no. 5, pp. 4715-4727, May 2020.

[21] X. Li and H. Lin, "A design method of phase-locked loop for grid-connected converters considering the influence of current loops in weak grid," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 3, pp. 2420-2429, Sept. 2020.

[22] L. Huang, H. Xin, Z. Li, P. Ju, H. Yuan, Z. Lan, and Z. Wang "Grid-synchronization stability analysis and loop shaping for PLL-based power converters with different reactive power control," *IEEE Trans. Smart Grid*, vol. 11, no. 1, pp. 501-516, Jan. 2020.

[23] J. Fang, X. Li, H. Li, and Y. Tang, "Stability improvement for three-Phase grid-connected converters through impedance reshaping in quadrature-axis," *IEEE Trans. Power Electron*., vol. 33, no. 10, pp. 8365-8375, Oct. 2018.

[24] X. Zhang, D. Xia, Z. Fu, G. Wang, and D. Xu, "An improved feedforward control method considering PLL dynamics to improve weak grid stability of grid-connected inverters," *IEEE Trans. Ind. Appl*., vol. 54, no. 5, pp. 5143-5151, Sept. 2018.

[25] D. Zhu, S. Zhou, X. Zou, Y. Kang, and K. Zou, "Small-signal disturbance compensation control for LCL-type grid-connected converter in weak grid," *IEEE Trans. Ind. Appl*., vol. 56, no. 3, pp. 2852-2861, May-June 2020.

[26] Z. Yang, C. Shah, T. Chen, J. Teichrib, and R. W. De Doncker, "Virtual damping control design of three-phase grid-tied PV inverters for passivity enhancement," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6251-6264, June 2021.

[27] L. Huang, C. Wu, D. Zhou, and F. Blaabjerg, "A double-PLLs-based impedance reshaping method for extending stability range of grid-following inverter under weak grid," *IEEE Trans. Power Electron*., vol. 37, no. 4, pp. 4091-4104, April 2022.

[28] S. Zhou, X. Zou, D. Zhu, L. Tong, and Y. Kang, "Improved capacitor voltage feedforward for three-phase LCL-type grid-connected converter to suppress start-up inrush current," *Energies*, vol. 10, no. 5, May 2017.

[29] L. Harnefors, "Modeling of three-phase dynamic systems using complex transfer functions and transfer matrices," *IEEE Trans. Ind. Electron*., vol. 54, no. 4, pp. 2239-2248, Aug. 2007.

[30] D. Pan, X. Ruan, and X. Wang, "Direct realization of digital differentiators in discrete domain for active damping of LCL-type grid-connected inverter," IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8461–8473, Oct. 2018.

[31] S. He, D. Zhou, X. Wang, and F. Blaabjerg, "Aliasing suppression of multisampled current-controlled LCL-filtered inverters," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 10, no. 2, pp. 2411–2423, Apr. 2022.

[32] I. Z. Petric, P. Mattavelli, and S. Buso, "Investigation of nonlinearities introduced by multi-sampled pulsewidth modulators," *IEEE Trans. Power Electron*, vol. 37, no. 3, pp. 2538-2550, March 2022.