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Parasitic Capacitive Couplings in Medium Voltage Power Electronic Systems - an Overview

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***Abstract*—Recent development within the field of medium voltage wide-bandgap semiconductor devices are drawing the attention from both researchers and industries, due to the demanding requirements for more efficient high-power energy conversion. The rapid development has entailed an increased awareness of the negative impact of increased rate of change in voltage, dv/dt, and its derived issues caused by the inevitable parasitic capacitive couplings. This paper is dedicated to present an overview of the parasitic capacitive couplings in high-power medium voltage power electronic converter systems, using an example reference system enabled by medium voltage SiC MOSFETs. The definitions of capacitive couplings are presented and the impacts raised by parasitic capacitive couplings are reviewed. In addition, the similarities of different capacitive couplings introduced by components in practical medium voltage systems are presented and summarized. Lastly, the challenges and future work with respect to parasitic capacitive couplings in medium voltage power electronics converter systems are shared from the authors' perspective.**

***Index Terms*—Capacitive couplings, power electronic systems, medium voltage applications, wide-bandgap devices, electromagnetic interference, reliability, semiconductor losses, grounding.**

I. Introduction

CAPACITIVE couplings are attracting more attention by both research and industry due to the exponential growth of Power Electronic Converters (PEC)s enabled by Wide-Bandgap (WBG) semiconductors [1]–[6]. Differing from conventional PECs enabled by Silicon (Si), the converters enabled by WBG semiconductors, including Silicon Carbide (SiC) and Gallium Nitride, can switch faster at higher frequencies, voltages, and temperatures from which the PEC system benefits in more efficient and compatible designs [7]–[16]. However, the fast switching behaviours and high voltage characteristics of WBG-based PEC systems also pose several new challenges. In prevalent Si-based PEC systems, minimizing parasitic inductance has been of main concern due to the high rate of change in current (di/dt) [17]–[20], while, in comparison, the slow switching speeds results in low rate of change in voltage (dv/dt). However, with the high dv/dt of the WBG semiconductor devices, the design regime of PECs are moving towards reducing the parasitic capacitive couplings as they can introduce high-frequency capacitive currents within the system, which further results in conducted/radiated noise issues and additional losses in the power semiconductor devices [21]–[23].

In $10\,\mathrm{kV}$ medium voltage (MV) SiC MOSFET applications, the highest dv/dt recorded has been as high as $250\,\mathrm{kV/\mu s}$, which is around 100 times larger than its prevalent Si IGBT counterparts [24]. Since the WBG devices help PECs to achieve higher efficiency and switching frequency, the power density of the PECs can be significantly increased [25], [26]. As the physical dimensions of the PECs are reduced, the electric fields strengths within the PECs will be increased which will further amplify the magnitude of the internal parasitic capacitive couplings. During the switching transition with high dv/dt, the capacitive couplings in the PEC system can generate high-frequency displacement currents, which can circulate in the system and consequentially result in two main issues [27]–[30]:

1) *Electromagnetic Interference (EMI)* where parasitic capacitive couplings can cause high-frequency common-mode (CM) or differential-mode (DM) currents which may result in conducted and radiated EMI.
2) *Thermal Stresses* where the charging and discharging of the parasitic capacitive couplings in the PEC system will induce displacement currents through the semiconductor device, which incurs additional losses. Furthermore, the charging and discharging will effectively reduce the switching speed and thus further increase the switching losses in the semiconductor devices. This surplus joule heating can cause additional non-predicted thermal stressing to the power semiconductor devices, which can negatively impact the reliability of the PEC and in worst case will result in premature failures of the power semiconductor devices.

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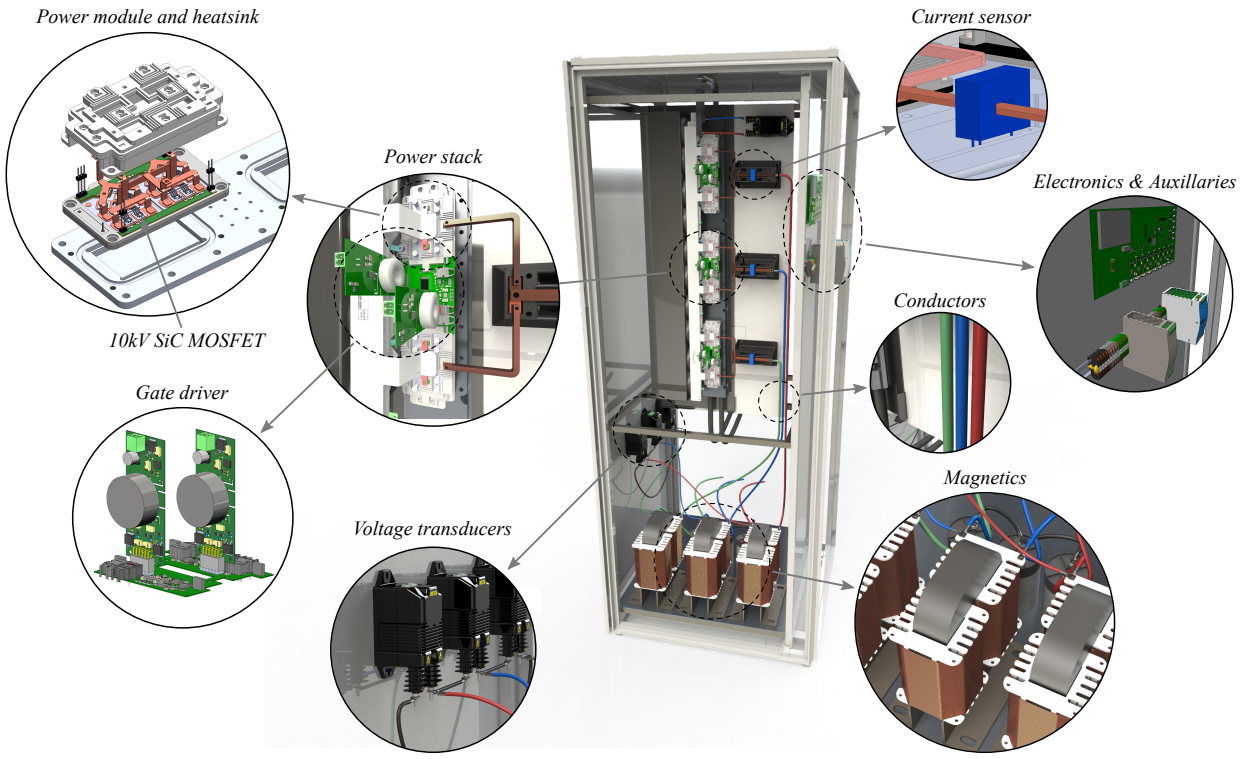

Fig. 1. Illustration of a typical high power medium voltage PEC system enclosed within a cabinet.

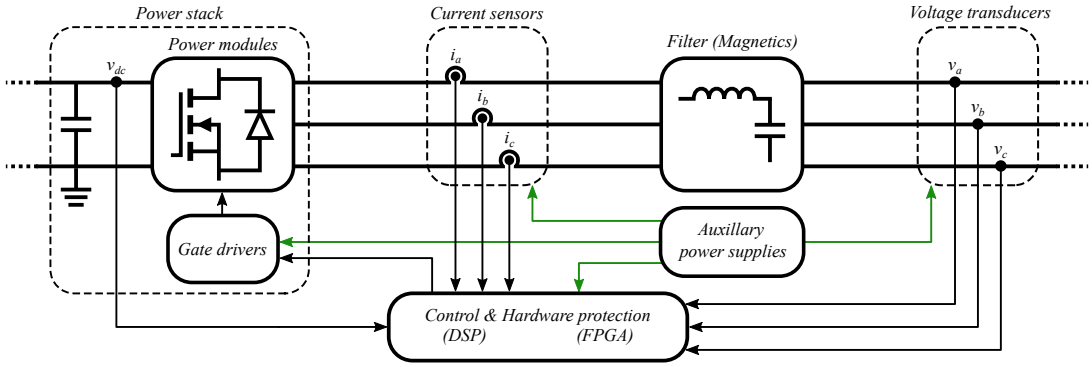

Fig. 2. Circuit schematic of the chosen PEC architecture.

To tackle these issues, the capacitive currents can be reduced by either reducing the dv/dt of the power semiconductor devices or by reducing the internal capacitive couplings in the PEC system. With the fast switching behaviours of WBG semiconductor devices being considered as the most promising feature to enable higher switching frequency operation and reduced semiconductor switching energy dissipation [31], [32], in most designs, it is undesirable to sacrifice the switching speed for reducing the capacitive high-frequency currents. As another solution, the parasitic capacitive couplings can be reduced by improving the geometrical structures or using dielectric material with lower relative permittivity [33]–[35]. Others options involve different grounding schemes, where high impedance CM current paths are introduced, by eg. having no earthing return path [36], however this poses other risks in terms of safety [37]. These considerations are relevant to all PEC systems enabled by WBG semiconductor devices, which emphasises the need for any PEC systems designer to have a basic understanding of the inevitable parasitic capacitive couplings in the PEC system.

In general, both passive and active devices of a PEC system introduce parasitic capacitive couplings due to their physical structures. In this paper, a typical high power, MV PEC system enabled by 10 kV SiC MOSFETs is used as an example to illustrate the parasitic capacitive couplings of individual components as shown in Fig. 1. Relevant components of the PEC system are highlighted, i.e., power modules, gate drivers, conductors, magnetics, sensors, and grounded cabinets.

Consequently, this paper addresses four main questions relevant to researchers and engineers:

1) *How to define parasitic capacitive couplings?*
2) *Why is it necessary to carefully consider the parasitic*

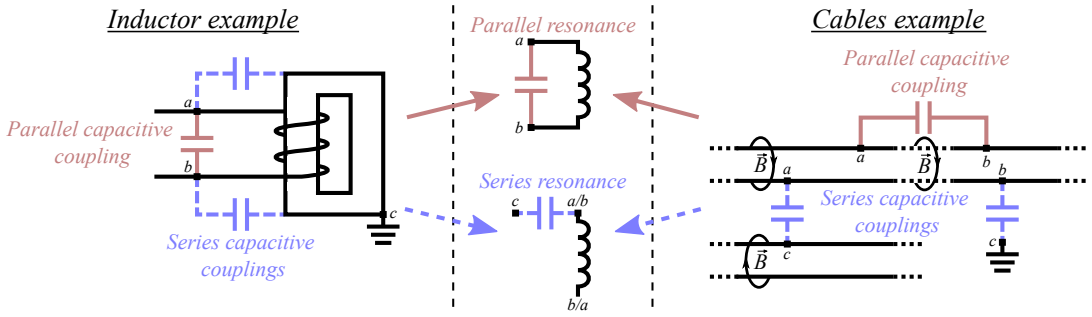

Fig. 3. Definitions of series and parallel capacitive couplings by equivalent circuit representations.

capacitive couplings?

3) *Where in the PEC system can the parasitic capacitive couplings be identified?*
4) *What are the remaining challenges and perspectives?*

To systematically answer these four questions, this paper is organized as follows; The definitions of capacitive couplings are introduced in Section II, where the physical concepts and engineering insights are provided. Then, the issues raised by capacitive couplings are addressed in Section III. This is followed by the comprehensive review on different capacitive couplings in power electronic systems in Section IV. Section V and VI concludes the paper with the remaining perspectives on capacitive couplings and the prospects for future research.

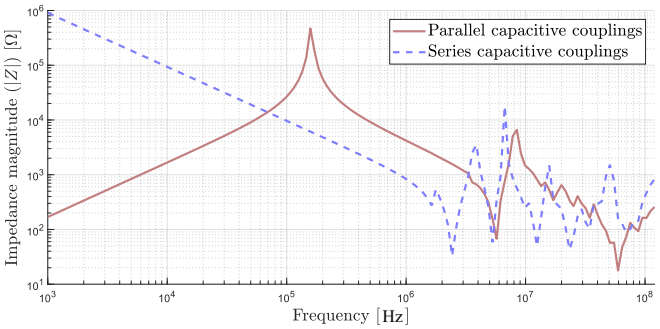

Fig. 4. Experimental impedance magnitude curve of an inductor modelled using both parallel and series capacitive coupling models.

II. Definitions of Capacitive Couplings

In a PEC system electric field energy is stored within and around the electrical components. In this paper, the stored electrical energy is defined as capacitance and the electrical coupling between nodes is defined as a capacitive coupling. The parasitic capacitive coupling is defined as the unintended electrical coupling between nodes. However, the characteristics of capacitive couplings, e.g. time-domain and frequency-domain response, are also governed by other parameters of components, e.g. voltage dependent capacitances, temperature dependent dielectric properties, and the LC resonance frequency being likewise governed by the parasitic inductance [38]–[40].

The capacitive couplings can be divided into two types; a) parallel capacitive couplings and b) series capacitive couplings. The definitions of the two types of capacitive couplings are supported by the equivalent circuit representations in Fig. 3.

The two types of capacitive couplings will result in significantly different behaviours in the frequency-domain as each of the two types of capacitive couplings governs a unique LC resonant circuit; a) the parallel capacitive coupling corresponds to a parallel resonance, which acts inductive and turns capacitive after the resonance frequency. The parallel capacitive coupling model is well known from the literature of inductor modelling as the equivalent circuit model up to and around the first resonance frequency [41], [42], and b) the series capacitive coupling corresponds to a series resonance, which acts capacitive and turns inductive after the resonance frequency. The series capacitive coupling model is known from the literature on the modelling of CM or ground capacitances [43], [44].

As a simplification, and for illustration purposes, it is preferable to use a single capacitance in parallel to the inductance to represent the parasitic parallel capacitive coupling as shown in Fig. 3. However, in reality, the equivalent single capacitance consists of multiple parallel capacitive couplings, e.g. winding-to-winding capacitances in the example of the inductor.

An RLC laboratory measurement of the parallel capacitive couplings of an inductor is shown in Fig. 4, illustrating multiple resonance peaks after the first resonance frequency, implying multiple parallel capacitive couplings. Therefore, using a parallel RLC circuit (the resonant method) [45], the single equivalent capacitor of the illustrated parasitic capacitive coupling can only be identified with a valid frequency range up to and around its first resonance frequency and the equivalent capacitance should not be mistaken for a physical capacitance in the circuit.

The series capacitive couplings can similarly be modelled as a single equivalent capacitive coupling with a valid frequency range up to and around its first series resonance frequency. Figure 4 likewise depicts the RLC measurements of the series capacitive couplings, illustrating multiple resonance peaks after the first resonance peak, implying multiple series capacitive couplings.

To summarize, Fig. 3 showcases how the individual capacitive couplings can be portrayed as 1st order resonant circuits. Generally, researchers and engineers prefer to use simplified equivalent circuits (1st- or 2nd order resonant circuits) to represent the parasitic capacitive couplings as this presenta-

tion is straightforward and convenient, however, it should be emphasised that this is not accurate and rigorous. This view is a simplification of parasitic capacitive couplings since it can only represent the practical behaviours up to and around the first resonance frequency. In reality, a combination of multiple parallel and series capacitive couplings are present as shown in Fig. 4 where both parallel and series resonance peaks are observed after the first resonance peak, thus emphasizing the need for higher order resonant circuit models. By introducing equivalent capacitances, the capacitive couplings are reduced to low order resonant circuit models, thus significantly lowering the modelling complexity. However, such simplification neglects the higher order resonance peaks and can thus result in inaccurate simulations and analyses. In reality, the actual response (waveforms) during the switching transition will be affected by the higher order resonances when the switching frequency is close to or above the first parallel/series resonance frequency. In order to tackle this issue, the idea of using high-order equivalent circuits can be applied to represent the behaviours of capacitive couplings after the first parallel/series resonance frequency, and therefore, provide a more precise solution to quantify the high-frequency capacitive displacement currents and EMI performance [46]–[49].

In conclusion, both parallel and series capacitive couplings can be utilized to model the behaviour of a PEC system, however, in all PEC systems both types of capacitive couplings will be present. Thus, to extensively model the behaviour of the PEC system covering the full frequency spectrum operation range, a combination of series and parallel high-order capacitive couplings should be included in the model. With the capacitive couplings being defined, the issues raised by these capacitive couplings will be addressed in the next Section.

III. Issues raised by Parasitic Capacitive Couplings

As was briefly mentioned in Section I, the main underlying issue with parasitic capacitive couplings in a PEC system is the capacitive displacement currents. The claim of this paper is that with the push towards higher switching frequency, higher switching speeds, and higher voltage levels from the emerging WBG semiconductor switching devices, the impact of the induced capacitive displacement currents will significantly increase. The following chapter will address some of the common issues governed by both parallel and series parasitic capacitive couplings in a PEC system. These issues are summarized into four categories; 1) Electromagnetic Compatibility and Interference, 2) Additional Semiconductor Losses, 3) Reliability and Thermal Stresses and 4) Safety and Grounding Issues.

A. EMI/EMC Performance

From an EMI perspective, the parasitic capacitive couplings in the PEC system creates CM and DM current paths, due to high switching speed, switching frequency, and switching oscillations [50]. These CM and DM coupling paths will cause circulating high-frequency displacement currents in the PEC system resulting in both conducted and radiated EMI, which can negatively impact communication, control, switching performance, system efficiency, reliability, and in general, fail to meet the EMC standards [51]–[55].

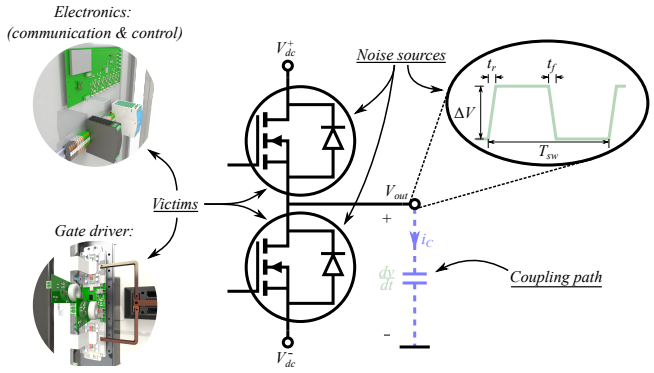

Fig. 5. Definitions of noise sources, coupling path and victims in a PEC system, exemplified with a series capacitive coupling of a VSC.

To clarify and further elaborate on this, the noise source for the induced displacement currents will be defined. In a switch mode PEC system, the noise source will be the Pulse Width Modulated (PWM) output voltage of the converter. With the PWM voltage generating large dv/dt, the parasitic capacitive couplings, C_{para}, experiencing this dv/dt will oppose this change in voltage by inducing a capacitive displacement current, i_{C}, as shown in (1).

$$i_{\text{C}} = C_{\text{para}} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \tag{1}$$

These currents will circulate in the PEC system as exemplified in Fig. 5. In Fig. 6, the PWM voltage is dissected into three different case studies governed by the transition from a LV system based on IGBTs to a MV system based on WBG semiconductor devices by increasing: a) voltage, b) switching frequency, and c) switching speed. Each case study is exemplified with ideal trapezoidal output voltage waveforms allowing for analytical spectral analysis of the frequency envelopes [56]. A Fourier frequency spectra of shown PWM voltages defines the frequency envelope of the generated noise from the different case studies as illustrated in Fig. 6. As can be observed, an increase in DC voltage level by 10x will entail a magnitude increase of approx. 20 dBµV. A switching frequency increase of 3x will shift the first corner frequency 3x and similarly a rise time decrease of 4x will increase the second corner frequency by 4x [57]. This is valid under the assumption that the rise- and fall times are equal, else a third corner frequency should be introduced for the fall time. In general, it can be concluded that all three case studies will increase the emissions generated by the noise source, which will impact the EMC of the PEC system. It should be clarified that the frequency envelopes in Fig. 6 are created only to illustrate the frequency content of the noise source for the different case studies and thus is not equivalent to the expected conducted and radiated EMI emission magnitude levels. However, the relative difference between noise source magnitudes for different case studies is expected to be reflected

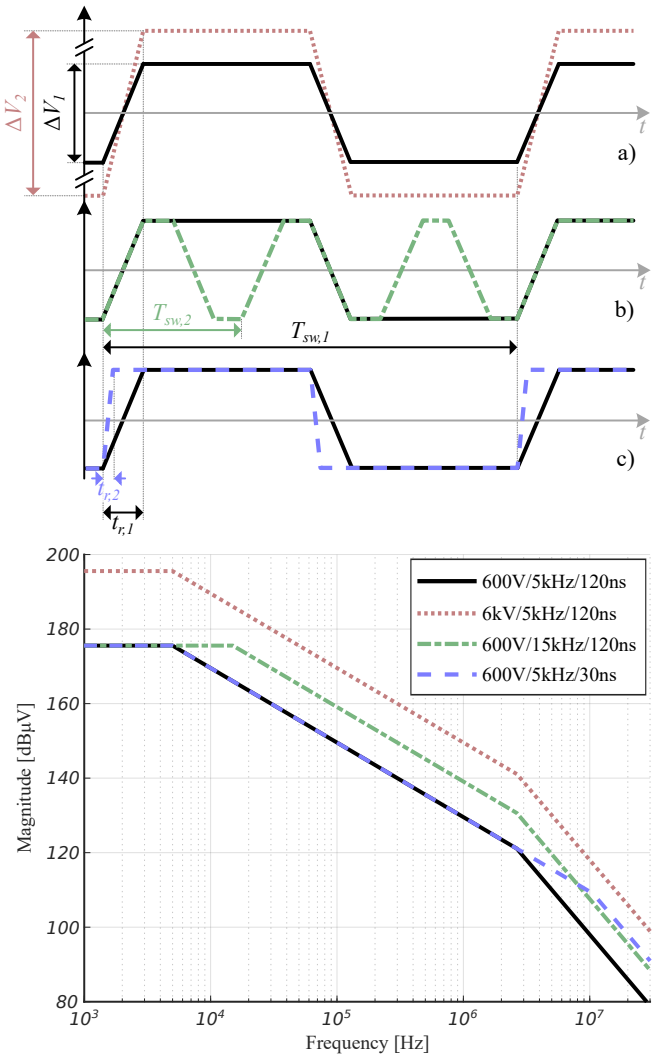

Fig. 6. Dissection of PWM voltage using the three case studies; a) voltage increase, b) switching frequency increase, and c) switching speed increase. The legend shows the nominal operating voltage level, operating frequency and nominal rise time respectively for the case studies.

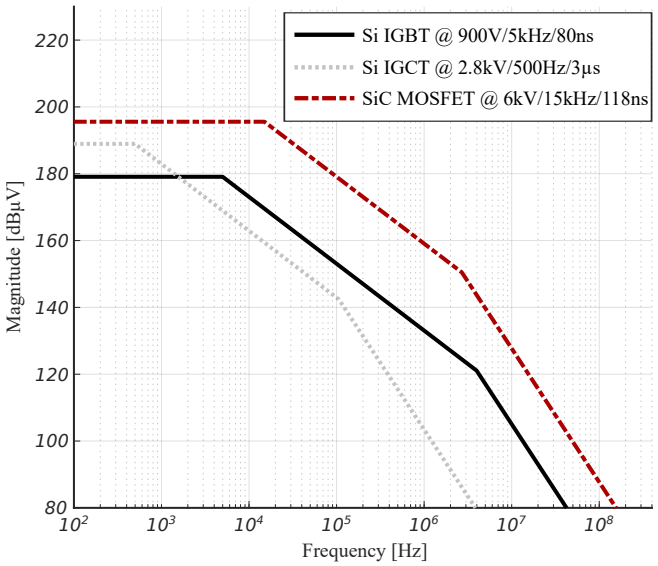

Fig. 7. Noise source frequency envelopes for Si IGBT [58], Si IGCT [59], [60], and SiC MOSFET [21]. The legends shows the nominal operating voltage level, nominal operating frequency and nominal rise time respectively for three compared devices.

onto the measured conducted and radiated emission magnitude levels.

The frequency envelopes in Fig. 6 has illustrated the one-by-one impact of the chosen case studies; a) voltage increase, b) switching frequency increase, and c) switching speed increase (rise/fall time). However, when employed in an actual PEC system, the noise source frequency envelope will be defined by a combination of these parameters. For comparative evaluation of the noise source frequency content of actual power semiconductor switching devices, the frequency envelopes in Fig. 7 are shown. When evaluating the noise level for SiC MOSFETs compared to Si based power semiconductor devices, Fig. 7 clearly depicts how both the frequency content and magnitude levels has been extended for the SiC MOSFET device when considering the noise source frequency envelopes. Similar trends from experimental measurements has been documented in [57], [61]–[63]. As can be seen from the trends in Fig. 6 and 7, the promising features of the WBG semiconductor devices entails a shift in the EMI spectra towards higher frequencies and magnitudes. In a modelling context, this emphasizes the need for multi-stage parallel and series capacitive coupling models, which was discussed in Section II, as the resonances being triggered by the noise source extends to higher frequency levels as illustrated in Fig. 4.

In dealing with these issues and achieving electromagnetic compatibility when compliance testing the PEC systems enabled by WBG semiconductor devices, the typical practices has been to; (1) reduce switching speed to lower the EMI emissions which comes with the penalty of increased switching losses [62], [64], or (2) introduce EMI filters which lowers the power density and adds to the total cost of the PEC system [65]–[67]. Unfortunately, both practices suffers from the drawback of being in discrepancy with the advantages gained by introducing the WBG semiconductor devices. In addition, it is demonstrated in [68] that the parasitic capacitive couplings of the grounding paths in the EMI filter can be detrimental to the intended functionality of the EMI filter, highlighting the need to consider the capacitive couplings. Instead, in [69], it is proposed to identify the critical coupling paths raised by the parasitic capacitive couplings in the PEC system during the design phase, thus giving the designer a tool to minimize/circumvent the EMI issues during the design phase of the component/product which in turn is expected to help meeting the EMC standards without compromising the advantages gained from the WBG semiconductor devices. Additionally, the early stage of identifying the EMI issues can increase the total revenue of the product [70].

B. Additional Semiconductor Losses

The power dissipation of an arbitrary power semiconductor device can be described as shown in (2) [71].

$$P_{\text{loss}} \approx \sum_{n=1}^{t_{\text{sum}}/T_{\text{sw}}} \left(\frac{E_{\text{sw}}(T_{\text{j}}, C_{\text{para}}, \ldots)^{(n)}}{t_{\text{sum}}} + \left(\langle i_{\text{on}} \rangle_{T_{\text{sw}}}^{(n)} \right)^2 R_{\text{on}}(T_{\text{j}}) \right) \tag{2}$$

Where P_{loss} is the total semiconductor switching and conduction power loss, n is the n^{th} switching period from 1 to $t_{\text{sum}}/T_{\text{sw}}$, where T_{sw} is the switching period and t_{sum} is the summation time interval, E_{sw} is the combined switching energy dissipation per switching period, $\langle i_{\text{on}} \rangle_{T_{\text{sw}}}$ is the average conducted current through the device per switching period, R_{on} is the on-state resistance, and T_{j} is the mean junction temperature per switching period. In the case where $t_{\text{sum}} = 1\,\text{s}$ in (2), the summation interval will be from 1 to f_{sw}. For a typical hard switched controllable power semiconductor device, the switching losses are dependent on the switching speed and loading profile of the device. The switching speed is governed by the charging and discharging dynamics of the intrinsic capacitances of the semiconductor device [72]. During the switching transition, the parasitic capacitive couplings present in the switching loop of the power semiconductor device needs to be charged and discharged which results in two main issues; a) an effective reduction in device switching speed which will result in higher switching loss energy dissipation (E_{sw}) due to the increase of the Volt-Ampere integral [73], [74], and b) induced capacitive displacement currents through the channel of the semiconductor devices, which with the push towards systems design using WBG semiconductor devices with higher switching speeds, will effectively increases the switched current magnitude as is showcased from (1), thus incurring additional switching losses during the dynamic switching transition period [21].

As shown in (2), the switching power loss will increase linearly with the increase in switching frequency [75], expected to be enabled by the WBG semiconductor devices.

Additionally, the higher voltage levels enabled by WBG semiconductor devices significantly increases the amount of capacitive energy being transferred through the semiconductor device channel during each switching transition [21], as is illustrated from (3).

$$E_{\text{C}} = \frac{1}{2} \cdot C_{\text{para}} \cdot v^2 \tag{3}$$

To further quantify the differences between a Si IGBT enabled LV system and a SiC MOSFET enabled MV system, the energy stored between passive parasitic inductive and capacitive elements, L_{para} and C_{para} respectively, can be evaluated as depicted in Fig. 8, which shows the ratio of stored parasitic energy as a function of the ratio of parasitic capacitance and inductance, S_{para}, as given from (4).

$$\frac{E_{\text{C}}}{E_{\text{L}}} = \frac{C_{\text{para}} \cdot v^2}{L_{\text{para}} \cdot i^2} = S_{\text{para}} \left(\frac{v}{i} \right)^2 \tag{4}$$

Where the red (dashed) and black (solid) lines in Fig. 8 indicates the two voltage class transistor types comparable in power rating; the MV SiC MOSFET power module [21] and the LV IGBT power module [58] respectively. By assuming the typical quantity of C_{para} in the nF range and the typical quantity of L_{para} in the µH range, the typical power module parasitic ratio (hatched area) is defined as $1\,\text{m} \pm 1$ order of magnitude. From the MV SiC MOSFET power module it can thus be observed that the capacitive energy is dominant in the majority of the typical parasitics ratio hatched area, dependent of the ratio S_{para}. This emphasizes the need to consider the parasitic capacitive couplings of the MV PEC system in terms of additional energy being dissipated in the semiconductor devices during each switching transition.

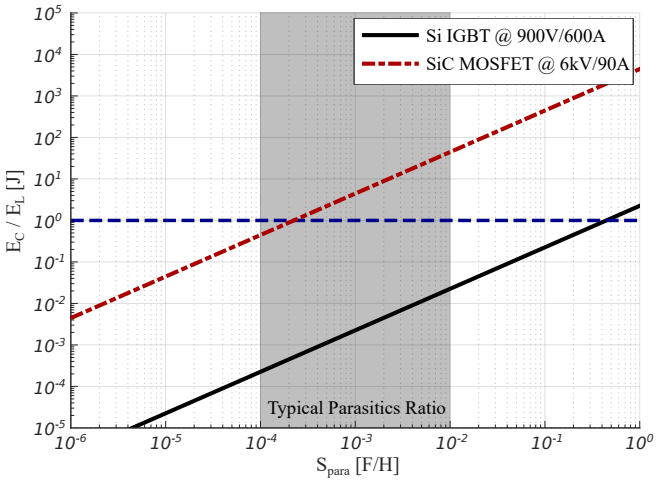

Fig. 8. Stored energy ratio of parasitics as a function of S_{para} for a LV Si IGBT power module [58] and a MV SiC MOSFET power module [21].

TABLE I
QUANTIFICATION OF CAPACITIVE COUPLINGS IMPACT ON SEMICONDUCTOR SWITCHING ENERGY DISSIPATION [76].

C_{para} [pF]	$E_{\text{sw @ 8 A}}$ [mJ]			
	@ 3 kV	@ 4 kV	@ 5 kV	@ 6 kV
54.2	9.50	13.6	18.7	23.8
227.3	10.7	15.7	21.6	27.9

In [76] the increase in switching energy dissipation is quantified by evaluating the impact of intra-component capacitive couplings between power module B, from [52] populated with 10 kV 3rd generation Cree dies, and the load inductor, using different grounding configurations of inductor core and frame with different equivalent capacitive coupling magnitudes, and testing at different voltage levels. The results are summarized in Table I where it is shown how an increase in parasitic capacitance has a direct impact on the semiconductor switching energy dissipation. Additionally, it is observed how the increase in DC-link voltage increases the switching energy dissipation, as expected from (3). These results are demonstrated for the specific 10 kV power module first presented in [33], however it assessed that these trends will be valid also for other devices under test.

Thus, it is evident, that the total increase in power semiconductor switching energy dissipation caused by the capacitive couplings in the WBG enabled MV PEC system will

impact the system efficiency. However, the advantages gained by the WBG devices, such as increased thermal performance and higher switching frequencies will likewise benefit the total efficiency and power density of the PEC system [77], [78], thus significantly increasing the complexity of evaluating the impact of capacitive couplings on the efficiency of the WBG enabled PEC system. In the literature different device figures of merits are proposed as a method of quantitatively evaluating the impact of the semiconductor parasitic capacitive couplings on the overall device performance parameters [79]–[81]. However, to the authors information no such figures of merit exists on a PEC system level, which includes the impact of the intra-component capacitive couplings between semiconductors, heatsinks, magnetics etc., and thus further research are needed on this topic.

C. Reliability and Thermal Stresses

The following section will address how the reliability of the MV PEC system is both directly and indirectly affected by the capacitive couplings.

The reliability of a PEC system or sub-component can be assessed from the number of cycles to failure determined from empirical data analysis. For power semiconductor devices different analytical models at increasing complexity is proposed in the literature from Coffin-Manson [82] to the Semikron Model [83]. However, none of these include the loss mechanism dependencies of the parasitic capacitive couplings. To quantify the impact of the capacitive couplings on the power semiconductor reliability, the power dissipation and thermal stresses of the components are often considered as informative quantities as the mean temperature and temperature swing of a device are directly correlated to the power dissipation of the device [84], [85], as depicted by (2) and (5).

$$T_{\mathrm{j}} = P_{\mathrm{loss}} \cdot R_{\mathrm{th}} + T_{\mathrm{a}} \tag{5}$$

Where T_{j} and T_{a} are the mean junction- and ambient temperatures respectively and R_{th} is the total thermal resistance of the device from junction-to-ambient. Thus, by assuming an approximately constant thermal resistance from junction-to-ambient it is evident that the semiconductor switching and conduction losses are proportional to the mean junction temperature which is directly correlated to the device degradation and thus the number of cycles to failure [86]–[88]. Additionally, the device will be subject to a switching frequency temperature swing caused by the surplus energy dissipation during each switching transitions, which can impact the lifetime of the device due to bondwire failure mechanisms [89], [90].

As the parasitic capacitive couplings for WBG enabled MV PEC systems will add significantly to the energy dissipation of the power semiconductor devices, as described in Sec. III-B, the reliability and stability of the devices will be further stressed, which will often result in derating of the power semiconductor devices [91].

Additional failure mechanisms related to the parasitic capacitive couplings of MV PEC systems are the degradation of the dielectric materials within the PEC system. During each switching commutation, these dielectric materials are subjected to high electric fields stresses causing conducted leakage current through the insulation material due to the capacitive couplings, over time this can degrade the insulation properties of the dielectric materials [92]. In [93] a correlation between gate oxide degradation and the MOSFET intrinsic capacitive couplings are reported, where it is proposed to use the MOSFET change in capacitance as a precursor to the gate oxide degradation, however the mechanisms behind the proposed correlation are unclear. Another phenomenon related to the insulation degradation in PEC systems is the partial discharge phenomenon, which in various studies have been documented to cause long term degradation of dielectric material insulation properties [94]–[96]. Particularly in WBG enabled MV PECs the partial discharge inception voltage will decrease with higher dv/dt posing an increased threat in terms of reliability [97]–[101]. Another failure mechanism related to the parasitic capacitive couplings is the cross-talk induced MOSFET self turn on, which poses the risk of a phase-leg short circuit [102]–[105]. During a phase-leg short circuit the device will enter the saturation region causing the energy dissipation of the device to increase significantly and the risk of non-recoverable device degradation will be substantial [106]–[109]. However, as limited publications exists on the direct impact of capacitive couplings on failure mechanisms and reliability of MV SiC MOSFETs, the authors would like to encourage researchers to investigate more on this.

D. Safety and Grounding Issues

To ensure personnel safety in a PEC system generally safety grounding of any bare conducting surface is ensured and for the high-power and medium to high voltage applications safety grounding is a requirement [37]. Likewise grounding of heatsinks, magnetic frames and supporting structures, magnetic cores, and cabinets are recommended as a safety precaution [110]–[112]. Additionally grounded shielding of cables is often employed to reduce radiated EMI [113]. As two conductors coupled by an electrical field can be represented by a parasitic capacitive coupling, these safety and shielding groundings can introduce a series capacitive coupling path to ground [70]. As explained previously in Sec. III-A the high dv/dt during switching transitions can thus induce CM displacement currents in the PEC system due to the parasitic capacitive couplings providing a CM coupling path [43], [114]. In commercial low voltage (LV) applications, the earthing system is often applied with TNS, TNC, TNCS, TT, IT, etc. according to IEC-60364 [115], which has been an industry standard for many years. The TN derived earthing systems (TNS, TNC and TNCS) have a well defined low impedance path to earth, thus providing excellent personnel safety during normal operation, however at the cost of a low impedance path for the CM currents to circulate in the PEC system [116], [117]. Generally, the same applies for the TT earthing system, under the assumption of a well defined low impedance earthing path between the locally Terra connected equipment. The IT earthing system provides a high impedance CM return path thus providing excellent features in terms of minimizing the impact of capacitive couplings and the circulating CM currents

[36]. However, in terms of both personnel and equipment safety, the IT earthing system can cause increased CM voltages at the intended safety grounded equipment terminals and thus poses a severe safety hazard [118]. As an additional safety feature the Residual Current Device (RCD) or similar relay devices can be employed to protect against dangerously high leakage currents to earth, which might be flowing through a human touching a live part. When using IT systems or in the case of line-to-earth/neutral faults in TN and TT systems, the RCD will measure the zero sequence current as the sum of the phase currents, and trip if the imbalance reaches a set threshold [119], [120]. Due to the increased magnitude of the CM currents in WBG enabled MV PEC systems, false nuisance tripping of the RCDs can occur, however the threshold current level of the RCD is also frequency dependent which can impact when and if the RCD is falsely tripped [121]–[123].

However, regarding impact of earthing and protection solutions in WBG enabled MV PEC systems, very limited amount of publications exists concerning high frequency CM voltage/current in different grounding configurations caused by the parasitic capacitive couplings of the system, thus further studying of the grounding issues in MV PEC systems would be attractive both in academia and industry.

E. Summary

The increased switching speed and switching frequency of the WBG semiconductor devices puts more focus on the parasitic capacitive couplings as they introduce high-frequency capacitive displacement currents to the circuit, negatively impacting the EMC of the system and incurring additional losses in the semiconductor devices. A special issue related to the MV WBG semiconductor devices is the increased voltage levels, e.g. in applications above $6\,\mathrm{kV}$, where the issues raised by parasitic capacitive couplings will be more challenging as the stored energy in the electric field capacitance increases with squared of the voltage. By comparing the energy stored in parasitic inductive and capacitive element, it becomes evident that the medium voltage systems bring a change in design regime for parasitic circuit elements. Another issue is the increase in the rate of change in voltage which incurs an increase in magnitude of the capacitive displacement currents. This increase in channel current incurs additional semiconductor switching energy dissipation losses. The surplus losses to the semiconductor devices due to capacitive couplings will introduce additional thermal stresses to the device, which, in a long term aspect due to thermo-mechanical wear, can negatively impact the lifetime of the devices. Other failure mechanism related to the capacitive couplings are the dielectric materials insulation properties degradation due to high electric fields stresses in the MV applications. In addition to the EMC and reliability of the MV PEC system being impacted by the capacitive displacement currents, another aspect of the surplus losses at the device level, caused by capacitive couplings, is the negative impact on the total converter efficiency. Therefore, it is important and necessary to have a more comprehensive understanding of the capacitive couplings within the PEC system to be able to identify the capacitive couplings and to interpret how they affect the components and system level performance of the MV PEC system.

IV. Overview of Capacitive Couplings in Components

This section is split into 8 subsections. Each subsection addresses the capacitive couplings of one or multiple of the PEC system components highlighted in Fig. 1.

A. Transistors

Transistors are at the heart of PEC systems [124] and the parasitic capacitances associated with these devices are highly important for the operation characteristics of the PEC systems. The most common power semiconductor devices for switch mode power converters in MV applications are power Insulated Gate Bipolar Transistors (IGBTs) and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [125], [126]. Both device types are voltage-controlled, being characterized by an insulated gate structure.

For these types of devices, the most commonly used capacitance modelling is the three-element lumped capacitance network, gate-source capacitance: C_{gs}, gate-drain capacitance: C_{gd}, and drain-source capacitance: C_{ds} (or equivalently for an IGBT with drain/source swapped with collector/emitter) [127] as shown in the lumped circuit model in Fig. 9. These capacitances act as a function of the drain-source voltage v_{ds} and are typically found in the device data sheet expressed as the values which can be easily measured with common impedance analyzers [128], [129], namely output capacitance: $C_{\mathrm{oss}} = C_{\mathrm{ds}} + C_{\mathrm{gd}}$, input capacitance: $C_{\mathrm{iss}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$, and reverse transfer capacitance: $C_{\mathrm{rss}} = C_{\mathrm{gd}}$. It should be noted that the intrinsic die capacitances can vary due to manufacturing processes [130], thus for precise modelling of these capacitances, they should be measured individually from die to die. In addition to the intrinsic capacitances of the controllable power semiconductor device, the anti-parallel freewheeling diode likewise contributes to the stored energy of the output capacitance [131]. Commonly, the body diode pn-junction charge is included in the datasheet values of the output capacitance, however, this depends entirely on the modelling convention of the manufacturer.

The above mentioned capacitances play an important role in determining the transient behaviour of a circuit, and in particular, for the power MOSFET, a majority carrier device, the switching speed is mainly limited by the parasitic capacitances [132]–[134]. The non-linearity and voltage dependency of the intrinsic MOSFET capacitances are modelled using analytical physics-based modelling in [135]–[137] and in [138] the voltage dependency of the capacitances are modelled from piece-wise linear approximations. How the capacitances arise from the physical structure of a MOSFET is shown in Fig. 10.

Of particular importance is the voltage behaviour of the intrinsic capacitances. The gate-source capacitance is almost constant with voltage since it is made up of electrodes with oxides in between [140]. However, both the gate-drain and the drain-source capacitances are highly voltage-dependent

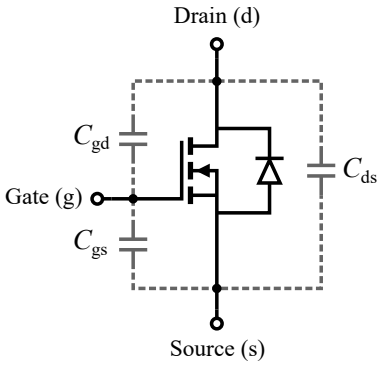

Fig. 9. Circuit representation of the MOSFET parasitic capacitances [127].

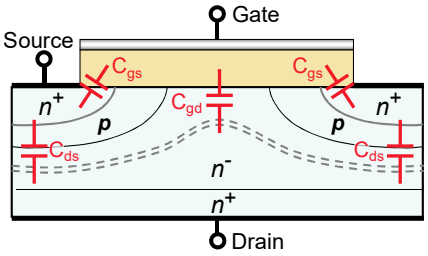

Fig. 10. Vertical power MOSFET structure with parasitic capacitances [139].

since they contain pn-junctions [135], [141]. These are reverse biased in the transistor OFF-state such that the width of the depletion regions expands and dramatically lowers the capacitance [142] as shown in Fig. 11. Engineering of parasitic capacitances is an important topic in semiconductor component design. Detailed physics-based models and process knowledge, as well as simulation tools such as TCAD, are used to investigate the impact of semiconductor materials, cell structure, and doping profiles on the electrical parameters in order to optimize device performance and tailor them with regard to the intended application area [144]–[147].

The switching device capacitances each impact the performance of the PEC systems in various ways. The charging of the gate-drain capacitance, also referred to as reverse transfer or Miller capacitance, can delay the drain current rise [148]. Therefore, reducing the reverse transfer capacitance minimizes turn-on losses by increasing the achievable dv/dt and reducing switching times [149]. The gate-source capacitance needs to be charged or discharged during every switching event. This not only puts demands on having a low output impedance of the gate driver circuit, but also results in increased losses proportional to the switching frequency [150]–[152]. A large output capacitance can slow down the switching transitions as it demands a reactive drain current to charge the capacitance during commutation [153], [154]. Depending on the topology, the energy stored in this capacitance may be lost every switching event [155]–[157].

B. Power Semiconductor Packaging

In a PEC system, the available power semiconductor device packages are the discrete devices, wire-bonded modules, and

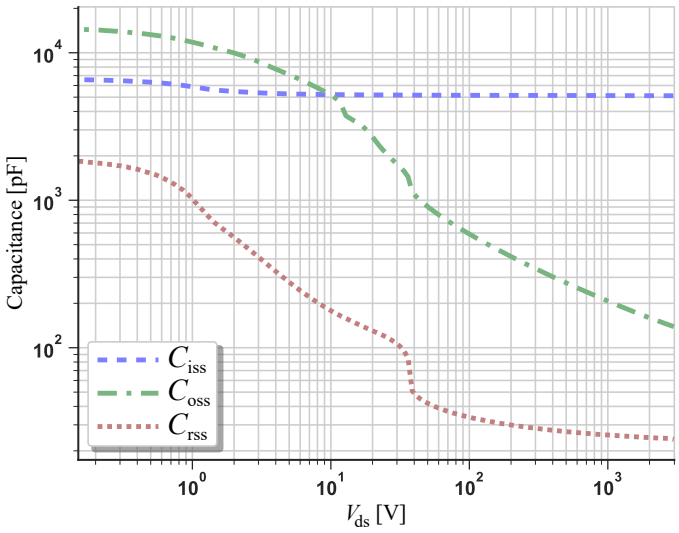

Fig. 11. 10 kV SiC MOSFET intrinsic capacitances depicting the drain-source voltage dependencies and non-linearities [143].

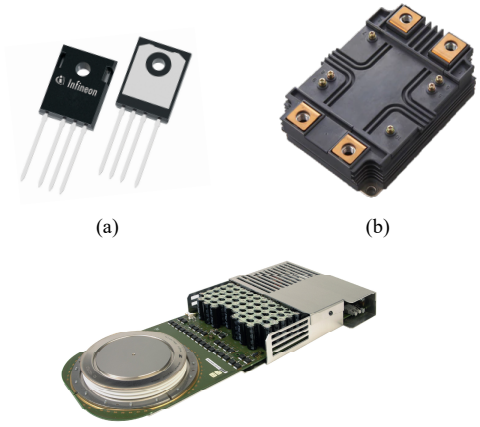

Fig. 12. a) Infineon 2 kV SiC MOSFET TO-247-4 discrete package [160], b) Mitsubishi 6.5 kV SiC MOSFET wire-bonded power module [161], and c) ABB/Hitachi Energy Si IGCT 4 kV press pack type package [162].

press pack type packages [158]. Example medium voltage packaged semiconductor devices are illustrated in Fig. 12. The primary purposes of the power semiconductor packaging are to 1) ensure sufficient electrical insulation between critical electrical potentials, 2) provide convenient electrical interconnections, 3) efficiently transfer the heat generated within the semiconductor devices to the cooling system through a baseplate/heatsink, and 4) ensure mechanical strength supporting the fragile power semiconductor dies [159]. Discrete packaged devices are most commonly used in low-power PEC applications, due to current limitations of the single chip design and cooling limitations of the TO type packages [87]. The discrete devices offer benefits in terms of off-the-shelf accessibility and cost. For high power applications, paralleling of the discrete devices is required, which due to increased layout inductance limits the applications range of the discrete packaged devices [163]. The wire-bonded module package offers benefits in terms of ease of paralleling multiple chips

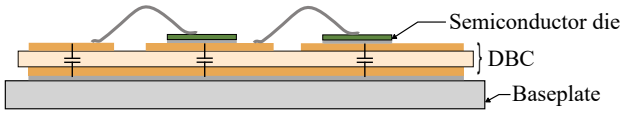

Fig. 13. Cross-section of a typical power module layout illustrating the associated parasitic capacitive couplings [52].

while maintaining low layout inductance. This makes the wire bond module type package widely popular for power levels up to a few MVA and voltage levels below ($\leq 4.5\,\mathrm{kV}$) while offering a large degree of versatility in terms of packaging [164]–[166]. Most commonly the power module packaging types are offered in standard half-bridge or full-bridge circuit configurations which serve as basic building blocks for most PEC systems [167]. The press pack is the most commonly used packaging for PECs utilized in applications starting from tens of MVA and high voltage ($\geq 4.5\,\mathrm{kV}$) i.e., High Voltage Direct Current (HVDC) transmission and motor drives [168]–[172]. The press pack packaging offers benefits in terms of series connection, cost, and power density compared to the wire bond packaging [173]–[176]. However, with the introduction of the WBG semiconductor devices with higher blocking voltage capabilities, the benefits of the press pack type in terms of achieving higher blocking voltages by the ease of series connection can leveraged [163], [177]. However, WBG devices suffer from a relatively lower current rating, which in order to achieve higher power levels, results in the need for paralleling [178]–[180], which can be provided by the power module packaging.

Thus, for high power, medium voltage PEC system as shown in Fig. 1, the wire bonded power module packaging will be used as a case study in the remainder of this paper. However, it should be highlighted, that due to the similarities in physical layering structures and cooling assemblies between different packaging types, the parasitic capacitive couplings identified in the wire-bonded module will be similar for the other packaging types although different in magnitudes. Power modules are typically made by attaching (soldering/sintering) power devices on the etched copper layer pattern on a Direct Bonded Copper (DBC) substrate, along with terminals to provide interconnection to the external electrical system. The DBC is then typically attached to the baseplate, which is further connected to a cooling system. The electrical insulation between the high electrical potential at the top copper layer of the DBC and the mounting baseplate is provided by the isolating ceramic substrate of the DBC. The isolating ceramic substrate introduces capacitive couplings between the top copper layer of the DBC and the mounting baseplate/heatsink [33], [181], as depicted from the cross-sectional view of a power module in Fig. 13. Since these power module planes are directly connected to the switching devices which are the noise source of the high-frequency content, these capacitive couplings are subjected to the full switching frequency spectrum and will thus be charged or discharged during every switching event [39]. Therefore, these are particularly important to consider with respect to ground noise and EMI issues. As explained thoroughly in Sec. III-B, this creates

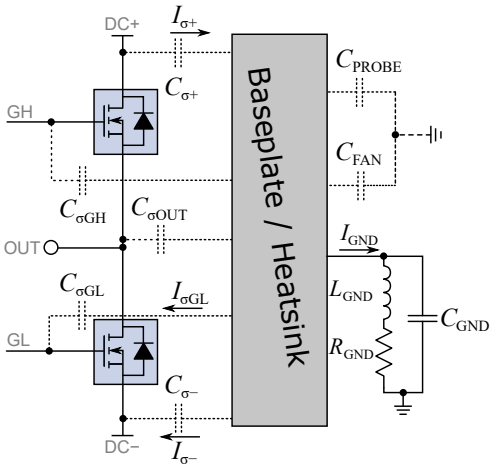

Fig. 14. Power module parasitic capacitances to baseplate [43].

Joule heating in the power semiconductor device as a result of additional switching losses from the charging and discharging of the capacitive coupling [73], and it can also slow down the switching speed of the power semiconductor devices as these power module capacitive couplings can be effective in parallel with e.g. part of the input or output capacitances of the power semiconductor device [52].

In a typical half-bridge power module, these capacitive couplings can be represented as the equivalent circuit schematic shown in Fig. 14. As an example the capacitance $C_{\sigma+}$ refers to the equivalent parasitic capacitance between the copper layer/island associated with the DC+ plane within the power module and the baseplate/heatsink. In the case of a half-bridge power module, the dv/dt at the output terminal of the half-bridge power module results in the charging or discharging of the power module parasitic capacitances through displacement currents. These displacement currents have an adverse impact on the semiconductor switching performance and EMC due to increased conducted noise within the PEC leading to a significant risk of EMI and cross-talk issues [43], [182]–[185] and additional switching energy dissipation within the power module [52]. If the capacitive coupling is strong this can lead to significant contamination of the ground path due to unwanted CM noise [186]. Even symmetry of capacitive couplings can be important [187]. An example is a common two-level half-bridge electrical configuration, in which different capacitive coupling values for DC+ and DC- voltage planes can cause differential-mode EMI.

To mitigate the above issues, there are some established options for the power module designer. For instance, simply reducing the area of the top copper islands can significantly reduce parasitic capacitance [33]. A fast design-change is to increase the thickness of the ceramic used for the DBC, making the distance between the top copper and bottom copper larger. The downside of this approach is an increased thermal resistance [188], however in terms of heat transfer, depending on the rest of the thermal resistance layers between the power device and the cooling system, this may be a very small overall sacrifice. Another approach for minimizing

module parasitic capacitance is to make a double DBC stack [181]. In [21] this approach is used where only the terminal connections of the power module are moved to the top-most DBC. This can be achieved as the terminal connections do not require significant cooling, and can greatly reduce the copper island area required on the top layer of the first DBC that is subjected to a voltage potential. In [189] the stacked direct bonded aluminum (DBA) is shown to reduce module parasitic capacitance by $22\,\%$ without impacting the thermal performance of the power module. Another approach for utilizing the stacked DBC is the embedded chip soldering layout proposed in [190], showing increased thermal performance and $57\,\%$ reduction in switching losses compared to commercial wire bond module, implying a significant reduction in the power module parasitic capacitance. The theoretical limit for common mode capacitance reduction using stacked DBC will be equal to the CM capacitance of a one-layer DBC multiplied by $1/n$, with n being the number of substrate layers [191]. In terms of conducted CM emissions, the midplane in the double DBC/DBA stack can be connected to the midpoint of the local decoupling capacitors in the power module, thus achieving a common-mode screen within the power module [183]. For nearly complete elimination of the output plane and its associated capacitance, more advanced techniques such as flip-chip assembly may be applied [192], [193], although this requires more advanced die processing techniques [28].

As previously explained in Sec. III-C, these incurred displacement current losses within the power module will heat up the semiconductor devices. For efficient thermal management of the heat generated from the power losses incurred within the power module, the high-power PECs typically employ forced air cooling or liquid cooling for the heatsink on which the power module baseplate is mounted. Generally, in a PEC, the heatsink is connected to ground potential due to safety precautions. However, by adopting different connection schemes for the heatsink, a degree of freedom to control the magnitude and frequency response of the power module parasitic capacitance induced displacement currents is available. Additionally, specific applications or multi-level converter typologies require the heatsink to be connected to a fixed potential or even kept floating due to limitations in terms of the isolation voltage rating of the power module ceramic substrate. Except for the case where the heatsink is grounded, the remaining connection schemes for the heatsink will attain voltage potential. This requires additional measures for thermal management system, i.e., insulation coordination between the fan and heatsink in the case of forced air cooling and deionized coolant for a liquid-cooled system.

The magnitude, frequency response, and circulation path for the power module parasitic capacitance, which is dependent on the heatsink connection scheme [194], can be modelled or predicted by utilizing the equivalent circuit presented in Fig. 15 [43], under the assumption that a ground return path to the DC poles exists, e.g. grounded DC- as depicted in Fig. 2. In the equivalent impedance network presented in Fig. 15, impedance Z_1 is modelled as the parallel combination of the parasitic capacitance associated with high-side and output gate plane, and impedance Z_2 is modelled as the parallel

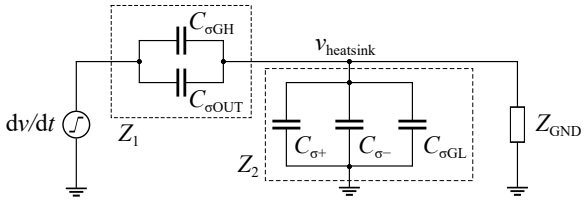

Fig. 15. Equivalent impedance network between the output terminal of the half-bridge power module and baseplate/heatsink [52].

combination of the capacitance associated with the DC planes and low-side gate plane. The impedance Z_{GND} represents the impedance between the heatsink and ground potential. The values of module parasitic capacitance can for example be extracted utilizing the Finite Element Method (FEM)-based simulation tools. Utilizing this impedance network with the known value of module parasitic capacitance the CM current due to module parasitic capacitance can be simulated or predicted with high accuracy by utilizing measured half-bridge output voltage or any arbitrary voltage slew rate signal as a noise voltage excitation to the circuit, respectively [43], [52].

C. Magnetic Components

Magnetic components, mainly including inductors and transformers [195], are essential components in power electronics converters. Due to the voltage drops of windings, and the voltage potential difference between the winding and core, the electric field is also distributed in and around magnetic components, and therefore, electric-field energy is stored [196].

1) Inductors: Compared to transformers, inductors usually have a simpler structure and fewer terminals [197], [198] as shown in Fig. 16. For single-phase inductors with floating cores and frames, they can be considered as a two-terminal network [199], where only a single parallel (differential-mode) equivalent parasitic capacitance needs to be identified [200] as shown in Fig. 17(a) and (c). State-of-the-art has done thoughtful research on predicting and analyzing the parallel capacitance of inductors using physics-based modelling methods [5]. For inductors with a grounded core and frame, two additional common-mode capacitances are introduced which need to be identified [201] as shown in Fig. 17(b) and (d), where the two common-mode capacitances can also be analytically calculated by using the improved modelling methods [5]. The physics-based modelling methods can only quantify the equivalent capacitor before the first resonant/anti-resonant frequency [42]. In order to quantify the characteristics (or capacitive couplings) after the first resonant frequency/anti-resonant frequency, the behavioural-based modelling method can be applied [46], which however, requires manufacturing prototypes first and then measuring the time-domain or frequency-domain response. Chokes and multi-phase inductors are more complex than single-phase inductors [49], [202], where more capacitive couplings should be taken into consideration due to the increased number of terminals.

2) Transformers: The capacitive couplings in transformers are similar but more complex to inductors. For two-winding

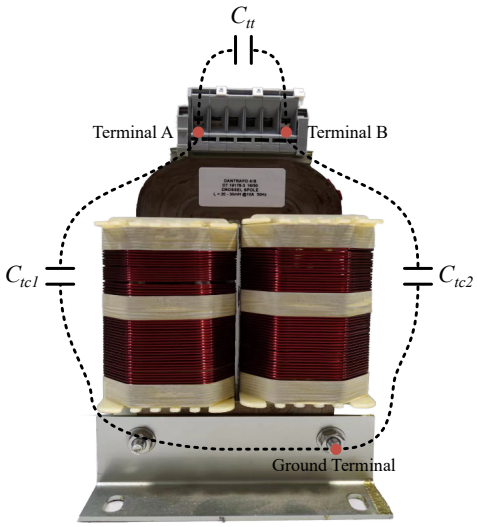

Fig. 16. A picture of a prototype medium voltage inductor with depicted parasitic capacitive couplings [5].

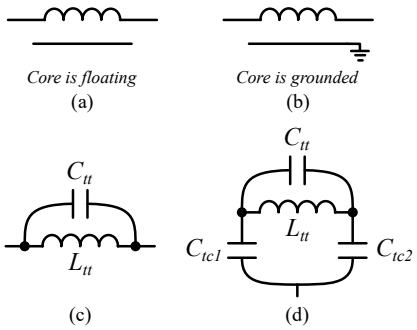

Fig. 17. Equivalent circuit for a) an inductor with floating core and b) and inductor with the grounded core. Equivalent circuits, including indication of capacitances, for c) an inductor with floating core [200] and d) an inductor with grounded core [5], [203].

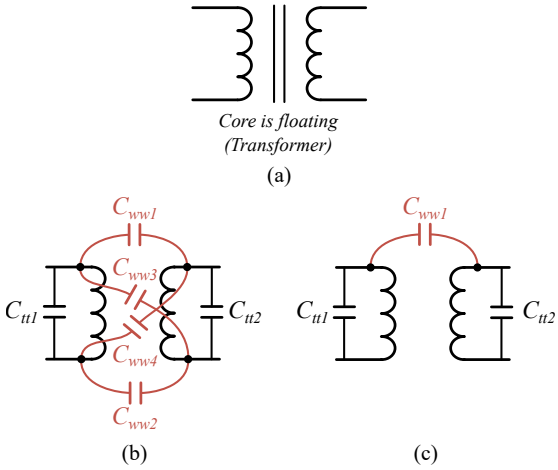

Fig. 18. Equivalent circuit for a) a two-winding transformer with floating core, b) a six-capacitor model of a two-winding transformer with floating core [208], and c) a simplified three-capacitor model of a two-winding transformer with floating core [204].

transformers with floating core and frame shown in Fig. 18(a), they should have two terminal-to-terminal parasitic capacitive couplings on each side, and four winding-to-winding capacitive couplings between the primary and secondary sides, as shown in Fig. 18(b) [204]. According to the definitions of capacitive couplings in Sec. II the terminal-to-terminal couplings can be considered as parallel capacitive couplings and the winding-to-winding couplings are the series capacitive couplings which in the literature are also sometimes considered as CM capacitive couplings [205]–[207].

In most applications, the six parasitic capacitive couplings are simplified to six capacitors [208]. Therefore, the equivalent circuit shown in Fig. 18 should only be valid before the first resonant frequency. The six-capacitor model can also be simplified to the three-capacitor model by considering only one common-mode capacitive coupling between primary and secondary side [209]–[211] as shown in Fig. 18(c). For transformers with grounded core and frame or with more than two windings, the number of terminals will be increased resulting in a similar increase in the actual parasitic capacitive couplings, [212] presents a 10-capacitor model for characterizing the complex capacitive couplings in a two-winding transformer with a grounded core, which leads a two-winding transformer to be a 5-terminal component. Generally, magnetic components can be considered as a N terminal network, and therefore, a total number of $\mathrm{N}\cdot(\mathrm{N}-1)/2$ individual capacitors should be quantified for the model [210].

3) Electrical Machines: Motors and generators are other typical magnetic components in power electronics applications. The parasitic capacitive couplings in machines are coupled between terminals and frame, stators and frame, and rotors and frame [213]. Since the frame of the machine is required to be grounded in practice due to safety precautions, it will provide a common-mode path for high-frequency capacitive currents [214]. The situation will be further challenged by machines without filters since the voltage variations at the terminals of the machine can be very high [215]. The high-frequency common-mode noise will add on the bearing current and finally results in a larger magnitude of bearing current [216].

In summary, at high frequency and with fast switching slew rates, the magnetic components in the PEC systems are also challenged by the overshoot transient voltage in the internal windings due to the resonance of parasitic capacitive couplings [217]. The overshoot transient voltage is important for high voltage applications since it increases the electrical stress which can damage the winding insulation and therefore cause winding insulation failures. To reduce the parasitic capacitive couplings, the improved geometrical structure including enlarging the distance between neighboring layers/windings [218], [219] and using more advanced winding layouts has been proposed in [220] with a sacrifice of either less power density or more complex optimization and manufacturing processes. In addition to the intrinsic magnetic component design considerations, the capacitive couplings of the magnetic components can induce capacitive displacements through the channel of the power semiconductor device, incurring additional losses during switching transitions [221]. Thus, emphasizing the need to consider the intra-components

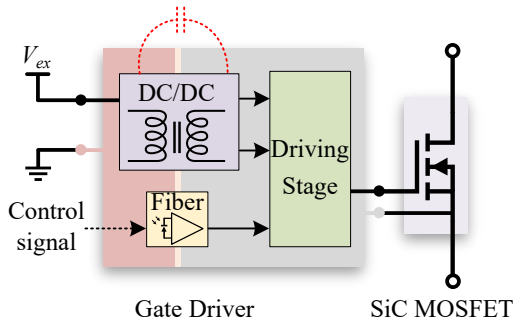

Fig. 19. Gate driver common mode capacitance [226].

effects of capacitive couplings. In terms of modelling and the applicability of different models for the same magnetic components, different models might be valid dependent on the need of the user. In general the higher order models with increased amount of capacitive couplings might be able to reveal more details and provide coverage of a higher frequency spectrum, however, they will significantly increase the complexity. For a specific problem, dependent on the needed level of accuracy, the higher order models can be simplified without sacrificing applicability.

D. Gate Drivers

Series parasitic capacitance exists between the primary side and the secondary side of an isolated gate driver as depicted from Fig. 19. They provide paths for conducting CM noise during switching transients of the driven power device, further resulting in the signal interference on the gate driver [222]. Consequently, to alleviate the negative influence, minimizing the CM parasitic capacitance is much concerned in the gate driver design. Multiple gate driver components contribute to the parasitic capacitance which may affect the CM capacitance, e.g. the gate driver IC barrier capacitance [223] and the desaturation diode for over current protection schemes contributing the junction capacitance [224], as well the PCB layout regarding traces or polygons forming parasitic capacitance [225]. Generally, the challenges of gate driver design are mainly considered in terms of the CM parasitic capacitance of the Gate Driver Power Supply (GDPS), and recent literature has provided significant corresponding analyses and optimizations, which can be classified into four categories from the perspective of GDPS design methods.

1) Isolated DC-DC converter methods: A commonly adopted typology for GDPSs is the isolated DC-DC converters, which are favored for their compact and mature designs with the help of a transformer to transfer the power from the primary powering side to the secondary gate side of power device as well for providing the insulation between primary and secondary sides. Massive successful commercial GDPS products for MV applications are designed on this basis and $4\,\mathrm{pF}$ CM parasitic capacitance is claimed as the state-of-the-art [227]. As introduced in the previous section, the isolated transformers will have several parasitic capacitive couplings. Especially for gate drivers, the common-mode parasitic capacitance between the primary side and secondary side is the most significant due to the large dv/dt variations across the isolation of transformers [228]. Generally, reducing the overlapping area [229] and introducing the larger gap [152] to reduce turn-to-core capacitance as described above are the effective approaches to reduce CM parasitic capacitance. However, both of them result in a larger size of GDPS. In summary, the high compactness of a transformer would always lead to a large CM parasitic capacitance, which makes it necessary to strike a compromise between the two.

2) Wireless power transfer methods: Wireless power transfer is an emerging technique in the design of GDPS, which is reported suitable for some MV applications with high isolation requirements. By using different typologies from the above isolated DC-DC converter methods, it makes the conventional transformer core unnecessary since it utilizes the air gap to transfer the power between the primary and secondary coils, which well satisfies the voltage isolation requirements [230]. Moreover, the CM parasitic capacitance between the transmitter and receiver coils can be decreased by proper arrangement of the coil positions and applying shielding layers [231].

3) Power over fiber methods: Comparatively, transferring power over fiber seems to be an attractive option since the fiber optic cables can provide optic isolation and induce extremely low CM parasitic capacitance. In [232], above $20\,\mathrm{kV}$ insulation voltage and above $200\,\mathrm{kV/\mu s}$ CM transient rejection are declared by considering the characteristic of fiber optic cables. However, the transferred power in the designed gate driver is limited, maximum $0.5\,\mathrm{W}$ at a low conversion efficiency.

4) Self-powering methods: Different from the above methods, the self-powering concept derives the gate driver power from the local DC bus, therefore eliminating the need for an additional external auxiliary power supply. The method is widely adopted in MV cascaded converter design [223], multilevel modular converter design [233], etc., where a local DC bus capacitor is configured that can provide a stable input voltage for various self-powering typologies. The benefit is that the voltage isolation requirement of the gate driver is decreased from the total DC bus voltage to the local one, and the imposed dv/dt across the gate driver during switching transients of the power device is decreased as well, contributing to a lower requirement of CM parasitic capacitance minimizing design. Another type of self-powering method is the bootstrap, which extracts the gate driver power from a bootstrap capacitor or from the snubber circuit of the switching power device directly, and thus no CM path is formed theoretically since the input and output of the gate driver have the same voltage potential [226], [234]. However, these methods bring more complexity to the PEC system.

E. Probes and Sensors

Probes and sensors for voltage and current measurements will introduce additional parasitic capacitive couplings to the PEC system and their influence needs to be analyzed. The authors would like to highlight two important aspects, which need to be considered; a) the purpose of the measurements and b) the physical placement of the measuring equipment within the PEC system.

The purpose of the measurements influences multiple factors, including size, cost, bandwidth, isolation, etc. as the requirements for a feedback measurement used for control purposes differs significantly from a measurement used for characterization of the switching performance of a power module as an example.

The placement of voltage and current probes is highly dependent on the purpose and the required measurements, whereas the placement of voltage and current sensors are generally determined by the desired control structure. The most common placement from an industrial point of view is as shown in Fig. 2, where the current is being measured at the power module output terminals and the voltage is being measured as the grid- or filter voltage [235]–[237]. The physical placement has a large impact on the relevance of the parasitic capacitive coupling between the AC busbar/cable and the measuring equipment as it is only the measuring equipment connected to the output terminal of the power module that experiences the high dv/dt, which needs to be considered.

1) Current measurement: The commercially available high-performance current probes are generally either coaxial shunt resistors, split core current probes, or some type of current transformer. The coaxial shunt resistor in itself does not introduce any additional parasitic capacitive coupling as it is an integrated part of the circuitry being measured, however, the analysis of parasitic capacitive coupling applies to the two remaining current sensing types.

In case the current measurement is to be used for control purposes, current sensors based on Faraday's law of induction, magnetic field sensing, or a combination of both are considered to be the dominant current sensing technologies utilized within the field of isolated current sensors for LV applications [238].

All of the above current sensing types except the coaxial shunt resistor have working principles derived from that of a transformer, with a current in the primary winding to induce a scaled down measurable current in the secondary winding. Thus, from a modelling perspective of the parasitic capacitive coupling, a direct equivalent can be drawn to a transformer with a floating core as was thoroughly explained in Section IV-C.

As a case example, the negative impact of parasitic capacitive couplings is given for a closed loop hall-effect sensor utilized in a MV SiC application. In [239], it was demonstrated that CM noise currents are coupling into the measurement signal of a closed loop hall-effect sensor during a switching event of a 10 kV SiC MOSFET power module. Two critical couplings were identified due to the parasitic capacitive couplings between the primary conductor and its; 1) secondary winding contributing to C_{P2S} and 2) the hall-effect element contributing to C_{P2H} as shown in Fig. 20. The strength of the parasitic capacitive coupling within the sensor depended on a number of factors, e.g. the internal structure of the sensor, the number of primary and secondary windings, and the placement of the primary conductor in the current sensor opening. This emphasizes the need to consider advanced digital filtering, alternative sampling schemes, or other measures such as an alternative placement of the current sensor within the PEC

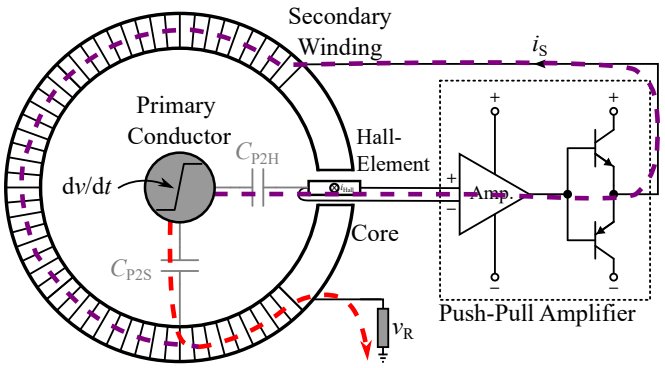

Fig. 20. Schematic of the closed loop hall-effect current sensor with its key parasitic capacitances indicated. The dashed current paths indicate the noise components caused by series capacitive couplings [239].

system to reduce the negative impact of CM noise currents and to achieve reliable signal integrity.

2) Voltage measurement: The commercially available voltage probes for MV applications are most commonly either passive- or differential probes connected to an oscilloscope to achieve measurements with high bandwidth and accuracy. Regardless of the type, the insertion of a voltage probe will introduce a parasitic capacitive coupling to the ground as a CM coupling through the shielded cables, oscilloscope, control board, etc. The CM capacitance (commonly denoted as input capacitance) is most often given as a rated value in the datasheet, which is typically modelled in parallel with a large resistor. When the voltage probe is used to measure at a high dv/dt node, the input capacitance of the probe can introduce high-frequency capacitive CM currents, leading to high requirements in terms CM rejection ratio to avoid the capacitive coupling affecting the desired measurement [240]. In [241], a number of commercially available MV probes have been tested and the CM capacitance of the probe has been found to have a significant impact on the accuracy and reliability of the measurements.

However, in case the voltage measurement is intended for control purposes, the commercially available high-performance voltage probes cannot be used, and therefore, alternative voltage sensors need to be deployed such as the LEM DVM series [242] shown in Fig. 1. However, with their physical placement and their low bandwidth in mind, the voltage sensors are generally being used to measure the near-sinusoidal grid- or filter voltage, hence the high dv/dt is not being experienced by the voltage sensors.

F. Conductors

In typical PEC systems, the connections between potentials are ensured by either busbars or cables, dependent on requirements such as low inductance, connector flexibility, and shielding necessity.

1) Busbar: For conventional high-power applications, both AC and DC laminated busbars have been widely used.

DC busbar made of laminated conductor plates, e.g. steel, aluminum, and copper, normally perform with high current conducting capabilities, low self-inductance due to mutual

inductance cancellation, and high capacitive coupling energy and thus the state-of-the-art research has been to minimize the power loop inductance [243]–[246]. In [247], three different lamination schemes for the laminated MV DC busbars are evaluated in terms of radiated flux density and induced voltage overshoot, demonstrating a minor change in EMF magnitude between the three designs. Additionally, it has been demonstrated in [248] that the extremely low inductance requirements for prevalent DC busbar design have little influence on the MV DC busbar design due to the low d*i*/d*t*, thus emphasizing the shift in design regime. In [249]–[251], the issues regarding Partial Discharge (PD) are addressed as being a design concern for laminated MV DC busbars due to the increased electric field strength, impurities, and air pockets causing PDs within the insulation material. Thus, the insulation materials and curing processes should be carefully examined for MV DC busbar design.

For AC busbars, the self-inductance has traditionally been considered negligible compared to the line-side reactor inductance, thus the main design concern has been to increase ampacity and reduce conduction losses. Limited research on capacitive couplings of AC busbar has been documented in the literature. However, the AC busbar capacitive couplings should not be neglected as they are electrically connected to the output terminal of the power module and thus in a similar manner as the power module output capacitance has a significant impact on the switching performance of the power semiconductor devices. From the authors' perspectives, two series capacitive couplings should be considered for the AC busbars which can be visualized from the cables example in Fig. 3, the DM coupling between busbars and the CM coupling to grounded surfaces, e.g. cabinet, cable trays, or mounting brackets. Both of these capacitive couplings are caused by the alternating output voltage potential creating electric fields between the busbars with the insulating air being the dielectric material of these capacitive couplings. The DM capacitive couplings can create series resonances with the self-inductance of the busbars and the mutual inductive couplings between busbars can create parallel resonances with the DM capacitive couplings. The CM capacitive coupling can create CM return paths to the power semiconductors causing high-frequency circulating CM currents governed by the series resonance of the grounding impedance/busbar self-inductance and the CM capacitive coupling.

2) Cables: For AC cables, the same considerations as for AC busbars are valid. However, for the physics-based modelling of the cable capacitive couplings, the dielectric constant of the insulation material of the cable should be considered.

From an EMI perspective, the shielding of cables has proven beneficial to reduce the radiated EMI emission and magnetic couplings [113]. However, such shielding introduces strong CM capacitive couplings, which is why the shielding of AC cables may need to be avoided for applications with high d*v*/d*t* at the output terminals of the power semiconductor devices. Similar effects can be observed for cables being tied to or laying on grounded surfaces as depicted in Fig. 21.

Another consideration for the parasitic capacitive couplings

Fig. 21. Cable common-mode capacitive couplings for a) a shielded cable and b) a cable in close proximity to a grounded surface.

in the cable is the wave reflection phenomenon. The reflection issue is normally identified in applications with long cable lengths, e.g. transmission lines and machine drives [252]. However, with the high frequency content imposed by the fast switching WBG semiconductor devices, the capacitive couplings also become evident for shorter cables [253]–[255]. The effects of the wave reflection phenomenon can be quantified by the wave propagation delay t_{p}. If t_{p} is in the range of the transmitted signal frequency content then reflected wave oscillations can cause severe distortions in the intended transmitted signal [253] and multiple magnitudes of the input voltage can occur at the cable terminals [256]. The wave reflection phenomenon for shielded vs. unshielded cables is investigated in [257], where it is emphasized that the wave propagation delay for shielded cables will increase compared to unshielded cables due to an increase in wave propagation velocity. In [258], it is demonstrated that the undamped reflected waves negatively impact the power semiconductor switching losses. The wave propagation delay t_p can be derived from [252] and [256] to be proportional to the square root of the cable capacitive coupling as a function of the cable length. The impact of the wave reflection for a cable is thus dependent on the size of the cable parasitic capacitive CM couplings throughout the length of the cable and the rise- and fall times of the PWM voltage of the power semiconductor device.

Mitigation strategies proposed for the reflected wave phenomenon currently involves the introduction of filters to damp the undamped reflected waves [259], however, these strategies introduce additional losses in the filters [260]. This emphasizes the need for more research addressing the reflected wave phenomenon and possible mitigation strategies for short cable lengths.

G. Cabinet

The cabinets are commonly used for practical high-power PEC systems, where most of the components of the PEC systems are placed and installed inside the closed metal enclosures. As a general recommended standard, the cabinets should also be grounded for avoiding floating voltage potential and providing protective earth or bonding paths if faults occur as safety precautions [111], [112]. Generally, the following three aspects will be impacted by the grounding of the cabinets.

1): It will provide a CM path for capacitive couplings to other power electronic components, e.g., the metal base/frame of magnetic components are normally connected to the core. By fixing the metal base to the cabinet, the magnetic core can be electrically connected to the cabinet. Therefore, a CM path

is created for the capacitive couplings in magnetic components via the cabinet.

2): It can contribute to new capacitive couplings in the system due to the electrical field distribution between power electronic components and cabinets as was likewise mentioned in previous section. Normally, the distance between power electronic components and cabinets is large, thus in most situations, such new capacitive couplings are relatively weak. However, the capacitive couplings between non-shielding cables and cabinets might still be strong due to the possible long lengths of cables placed in close proximity to the grounded cabinet.

3): Cabinets with grounding configuration also act as Faraday cages. Therefore, it can decouple the capacitive couplings of the power electronic components inside the cabinet from the outside, which is commonly known as shielding. This emphasizes the need to differentiate between; 1) capacitive couplings within the converter cabinet, which could, from an electrical view-point, be in close proximity to the noise source, thus inducing high-frequency displacement currents within the PEC system and 2) capacitive couplings outside of the converter cabinet which although potentially being very strong capacitive couplings, will not induce capacitive displacement currents due to the Faraday cages effects of the cabinet.

H. Summary

Capacitive couplings are dominant and inevitable in PEC systems as the parasitic couplings are present in nearly all power electronic components. Critical capacitive couplings of key components in MV PEC systems have been identified in this chapter and it is shown that both series and parallel capacitive couplings are contributed from multiple components. These capacitive couplings, if experiencing high $\mathrm{d}v/\mathrm{d}t$, can introduce capacitive currents within the PEC system. State-of-the-art clarifies that the effects of different capacitive couplings are intensified in MV PEC systems. The increase in power density enabled by the WBG semiconductor devices will further magnify the strength of the capacitive couplings.

V. Challenges and Future Work

The challenges regarding parasitic capacitive couplings in MV PEC systems are shared from the authors' perspective. The section is divided into two subsections which addresses 1) the summarized state-of-the-art challenges raised by the parasitic capacitive couplings and 2) the future work needed, from the perspectives of capacitive couplings, to realise the goal of a high power WBG enabled MV PEC system.

A. Summarized Challenges of Existing Work

1) Reduced Semiconductor Switching performance: As the power semiconductor devices are at the heart of the PEC systems the effects of the semiconductor parasitic capacitive couplings are of highest importance as these determines the device switching performance, as described in Section IV-A. In the literature some intra-components effects of capacitive couplings has been identified, where other component parasitic capacitive couplings can be analyzed as being in parallel to the semiconductor intrinsic parasitic capacitance and thus likewise severely impacts the switching performance and switching losses of the power semiconductor devices. The power semiconductor packaging capacitive couplings are generally shown to both slow down the switching speed of the semiconductor devices and increase the magnitude of the capacitive displacement currents through the channel of the device causing increased semiconductor switching losses, as described in Section IV-B. New trends and advanced packaging solutions such as stacked DBC and flip-chip design are emerging with excellent reduction in packaging capacitive couplings, however these solutions suffers from very high manufacturing complexity and reduced technology maturity. Load magnetics (inductors, machines and transformer) also contribute with capacitive couplings which can be analyzed as being in parallel to the semiconductor output capacitance and thus similarly to the power semiconductor packaging capacitance impacts the semiconductor switching performance in terms of increased switching losses from the surplus capacitive currents induced through the channel of the device and increased EMI to the PEC system, dependent on the windings and core configurations, as described in Section IV-C. However, from a high-frequency modelling perspective, the higher order resonance models of the magnetic components are still insufficient for accurate prediction of the capacitive couplings impact. Cables connected between output terminals and load of the power semiconductor package can likewise contribute with additional capacitive couplings which can be analyzed as being in parallel to the semiconductor output capacitance, as described in Section IV-F2.

2) Reduced PEC System Performance: The power semiconductor packaging capacitive couplings have been identified in the literature as posing an increased risk of cross-talk and EMI issues thus threatening robustness and reliability, as described in Section III and IV-A. In the gate drivers the GDPS contributes capacitive CM couplings to the gate which are reported to negatively impact the PEC system EMC and the robust and reliable operation of the semiconductor devices. A variety of existing GDPS methodologies exists, where the more advanced methods such as power over fiber or self-power methods significantly reduces the CM capacitive couplings and thus reduces EMI and noise issues down to a level where it can be considered mitigated, as described in Section IV-D. However, these methods introduce more complexity to the PEC system and gate driver design. When probing/sensing in a PEC system the measurement equipment itself can contribute capacitive couplings to the system which significant impact the accuracy and robustness of the measurements, as described in Section IV-E. Generally, the voltage probes and currents sensors are identified as the components, from an electrical view-point, in closest proximity to the semiconductor switching devices, and thus having the largest impact from the capacitive couplings perspective. The wave reflection phenomenon of cables can impact the system performance, dependent on the length of the cables, as the reflected waves can significantly increase the voltage level at the terminals of the cables, e.g. filter, powermodule, transformer or machine terminals, and

thus impact safe and reliable operation of the PEC system, as described in Section IV-F2. Safety groundings in the PEC system of cabinets, frames, inductor cores etc. will contribute with CM capacitive couplings, which dependent on the earthing system and the reference point of the capacitive coupling can impact EMC and cause intra-component capacitive couplings to incur additional displacement currents through the channel of the semiconductor devices causing extra losses and thus indirectly impacting the PEC system reliability and efficiency, as described in Section III-D and IV-G.

B. Future Work

1) *Modelling methods*: The inevitable capacitive couplings in PEC systems are difficult to predict and estimate. The FEM digital twin approach has been proven to have a great predictability and very high accuracy. Although convenient, the drawbacks of the FEM based approaches are; a) extractions only valid for individual case studies analysing different designs, due to the extractions being numeric solutions, and b) computation power limitations and time-consuming extractions for complex layouts/structures, e.g., PEC system level extractions. These limitations yields a highly case-by-case based design approach. The analytical physics-based approach can provide design oriented insights such as design constraints, however, it suffers from the drawback of being less accurate compared to the FEM digital twin approach. behavioural-based modelling methods can be used for empirical estimations using, e.g., the resonance method, which has been proven useful up to and around the 1st resonance peak, however, for prediction of more complex structures with multiple series and parallel capacitive couplings this method is insufficient. Hence, the need for improved modelling methods at higher accuracy and with increased applicability are highlighted here, with the core requirement being better predictability of the capacitive couplings.

2) *Measurements of high-frequency capacitive current*: This paper has addressed the parasitic capacitance introduced by probes and sensors. In practice this implies that what we measure may not be the actual behaviors of the system, as the measuring equipment itself contributes high-frequency capacitive current signals. This calls for further research on identifying the behaviors and responses of MV PEC systems without the effects of probes, sensors, and scopes.

3) *Effects of capacitive couplings*: This paper has addressed the contributions of capacitive couplings on a system level and from different sub-components of the MV PEC system. However, methods for quantitatively analyzing the impact of the capacitive couplings on the system level are still lacking in literature. This includes reliability assessment and loss estimation methods at both system and component level considering the intra-component effects of parasitic capacitive couplings.

4) *Design trade-offs*: To minimize the parasitic capacitive couplings some design trade-offs/contradictions need to be considered. In general, the minimizing the capacitive couplings could be achieved by increasing the distance between components in the MV PEC system, however, this comes with the sacrifice of decreased power density which is opposing the trend of compact design for modern WBG enabled PEC systems. For optimized thermal management of a given component, the distance from source to sink can be reduced to minimize the thermal resistance, however, this comes with the penalty of increasing the capacitive coupling. Another trade-off is the relation between inductive and capacitive couplings, which is often inversely correlated such that a reduction in parasitic capacitance leads to an increase in parasitic inductance.

5) *Dielectric properties*: The aforementioned trade-offs are related to the increase in distance causing a decrease in capacitive coupling. However, this assumes no change in dielectric materials properties, which emphasizes the need for research into new materials and material properties to reduce capacitive couplings while minimizing the impact on other system design variables.

6) *Cost*: Another perspective related to the optimized design for reducing capacitive couplings is the cost. Often, the methods to reduce capacitance usually increases material cost and manufacturing complexity, which is also highlighted by the previous point on minimizing capacitive couplings by investigating new materials. As the MV WGB devices are already costly, the additional cost of optimized design to minimize capacitive couplings is a major drawback in terms of further maturing of the technologies with both research and industry being more reluctant to invest in such costly technologies.

7) *Inductive couplings*: The case study of this paper is a WBG enabled MV PEC system which is based on the argument that, with the introduction of WBG semiconductor devices, the industry will transition from LV to MV PEC designs, which results in a decrease in current and thus emphasises a shift in design regime considering the capacitive vs. inductive parasitic couplings. However, assuming that the trend of the wind turbine industry continues, and the transition from LV to MV PEC designs are realised, the power envelopes of the wind turbines will be pushed to tens of MVA. Thus, the electrical design engineers needs to consider both inductive and capacitive couplings due to the high di/dt and high dv/dt. Hence, future challenges in the WBG enabled MV PEC design includes optimized design for hybrid inductive and capacitive couplings, emphasizing the need for advanced, precise, and applicable modelling methods of parasitic circuit elements in future MV PEC systems.

VI. Conclusions

This paper shows that the critical capacitive couplings are the ones in close proximity to the high dv/dt caused by the switching of the wide-bandgap power semiconductor devices. The concept of parasitic capacitive couplings in PEC systems is systematically reviewed. The definitions of two different parasitic capacitive couplings in PEC systems are first pointed out as being either series or parallel capacitive couplings. Then the issues raised by parasitic capacitive couplings in PEC systems are presented and identified via three different categories which are significant in practical applications; electromagnetic interference and compatibility, additional semiconductor

losses, reliability and thermal stress, and safety and grounding issues. It is emphasized how the increase of switching speed and operating voltage levels for the PEC system will amplify the severity of these issues. Subsequently, according to a comprehensive literature overview, the contributed parasitic capacitive couplings in typical components of a PEC system are presented. The effects of identified parasitic capacitive couplings are discussed and similarities between effects of parasitic capacitive couplings in different components are revealed. As a general design consideration, identifying the high dv/dt hotspots of the PEC and directing attention towards the capacitive coupling paths from these hotspots are proposed as a suitable mitigation strategy. In the literature, particularly the output terminal of the half-bridge power module is identified as a high dv/dt hotspot. The perspectives to the most significant challenges and mitigation strategies relevant to parasitic capacitive couplings are highlighted and thoroughly addressed and summarized.

Overall, it can be concluded from this overview, that in order to achieve high power, high efficiency, electromagnetic compatible, robust and reliable WBG enabled MV PEC systems, the intra-component effects of parasitic capacitive couplings must be evaluated during the design phase, which calls for new recipes in terms of design, modelling and performance predictions at both component and system level of the MV PEC systems.

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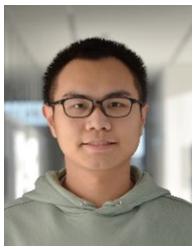

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