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Test Platform for Comparative Evaluation of 690 V – 4160 V Power Electronic Converters

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(Invited Paper)

***Abstract*—This paper presents a 500 kVA DC-fed regenerative power circulation platform to test newly emerging Silicon Carbide (SiC) MOSFETs based medium voltage (MV, 4160 V) Power Electronic Converter (PEC) against commercially available Silicon (Si) IGBT based low voltage (LV, 690 V) PEC allowing for comparative performance evaluation. Each voltage level have AC/DC and DC/AC conversion stages allowing for testing of two MV and two LV simultaneously. The interface between voltage levels is facilitated by a line frequency transformer and two mechanically coupled induction machines. The paper presents the principle functionalities of the designed power circulation test platform with insights into considerations on safety, communication protocols, controllers, hardware protection and system control for a reliable and safe testing of kVA rated LV and MV PEC systems. The designed test platform features calorimetric power loss measurements enabled by high precision coolant temperature and mass flow transducers. Circulating power through multiple converters at once will allow for a comparative analysis of power conversion efficiency, power quality and electromagnetic interference and emissions for Si IGBT and SiC MOSFET enabled high power LV and MV PECs.**

***Index Terms*—Wind turbines, Regenerative power circulation test platform, Electrical efficiency, Si IGBT, SiC MOSFET, Low voltage, Medium voltage, Induction Machines.**

I. Introduction

THE rated power of offshore wind turbines is approaching few tens of Mega Watts in capacity, this has necessitated the need for comparably rated power electronic converters (PECs) that can handle the full power and act as an interface between the wind turbine and power grid. In recent years, offshore wind turbines rated for $14\,\mathrm{MW}$ – $15\,\mathrm{MW}$ have been erected by leading turbine manufacturers [1]–[5]. These $14\,\mathrm{MW}$ – $15\,\mathrm{MW}$ offshore wind turbines will be deployed in future gigawatt capacity wind farms [6]–[8]. If this trend continues, then the larger wind farms of the future will contain even larger wind turbines with higher power ratings. A wind turbine consists of mechanical, electrical, hydraulics and thermal subsystems, wherein the PEC is the key component of the electrical subsystem. Taking a $15\,\mathrm{MW}$ wind turbine into account, 1% of electrical losses translates into $150\,\mathrm{kW}$ of power being lost to heat. This heat has to be cooled resulting in increased cooling requirements and it also negatively impacts the overall energy production and earnings. A standard voltage rating for commercial wind turbines is $690\,\mathrm{V}$ with at least one wind turbine featuring a more non-standard voltage rating of $3.3\,\mathrm{kV}$, a voltage rating designated as medium voltage (MV) [9], [10]. Increasing the voltage from LV to MV will decrease the current proportionally which can decrease the conduction losses. This reduction in conduction losses make it more viable to go for different wind turbine tower topologies, like moving some parts of the electrical subsystem down tower. At present commercially available MV PECs for wind turbines utilize multi-level power converter topologies, such as three-level neutral point clamped converter (3L–NPC) [10], [11]. Such MV PECs boasts roughly 98% efficiency which is 1 % higher compared to approximately 97% for its LV counterpart [12]. Multi-level topologies such as 3L-NPC are more complex and have more switching devices when compared to a two-level (2L) topology used in LV [13], [14]. At present, commercially produced LV or MV PECs utilize Si based power semiconductor devices such as IGBTs or IGCTs with rated maximum blocking voltage of up to $6.5\,\mathrm{kV}$ for IGBT and $10\,\mathrm{kV}$ for IGCT [10], [11], [15]. Emerging power semiconductor devices based on silicon carbide (SiC) can achieve blocking voltages as high as $10\,\mathrm{kV}$ – $15\,\mathrm{kV}$ for SiC MOSFETs and $27.5\,\mathrm{kV}$ for SiC IGBTs [16]. With an increased blocking voltage of semiconductor devices, a simple 2L converter topology can be used for MV power conversion thus eliminating the need of series connection of power semiconductor devices or use of multi-level converter topologies to achieve MV levels. Theoretically, the use of less switching devices made of a superior SiC material should yield higher efficiency than modern Si based switching devices. The intrinsic material advantage of SiC based switching devices is documented in comparative experiments with Si based switching devices at comparative voltages, switching frequency and electromagnetic interference (EMI) levels, even when accounting for electromagnetic compatibility (EMC) [17], [18]. EMC is important because it sets a standard for output waveform quality and this is a problem that fast switching wide bandgap technologies like SiC have to deal with. The prospects of SiC enabled PECs is the simplification of MV PEC topologies with the additional benefit of improved efficiency. SiC based switching devices are still not widely demonstrated in high power applications, why it can be said

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that the technology is still immature. Only through repeated testing at high power in conditions similar to what will be seen in an application like a wind turbines electrical subsystem can SiC based switching devices gain technological maturity.

A. State of The Art - Medium Voltage Demonstrators

The state of the art for a PEC system in a wind turbine is fully rated 2-stage back–to–back (BTB) PEC system as shown in Fig. 1. A BTB PEC system topology decouples the two line sides with a DC-link in the middle, allowing for frequency independent line side and machine side waveform control. Multiple BTB PEC systems can be placed in parallel to increase the total power rating [11], meaning each BTB PEC can be developed separately. The SiC based switching devices that are developed in-house may end up in a PEC system like the one seen in a wind turbine, why it is a goal of the test platform to emulate a wind turbines PEC system as closely as possible. When discussing the efficiency of a wind turbines 2-stage BTB PEC system like the one in Fig. 1 it will include both PECs and ancillaries such as filters. When addressing the efficiency of a single PEC it will be assumed that ancillaries are disregarded as the focus is typically on switching and conduction losses in the PEC itself. For efficiency comparisons multi-stage PECs with specified efficiency will be calculated as a single PECs efficiency by assuming that the efficiency is a product of all the PECs individual efficiency. The actual single PEC efficiency must be higher because this calculation assumes no ancillary losses. MV BTB PEC systems for wind turbines are commercially

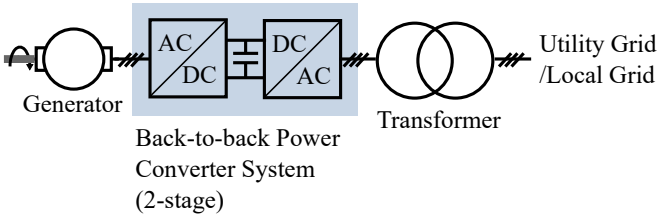

Fig. 1. Example of wind turbine power electronic converter system [11].

available; ABB has deployed a $7\,\mathrm{MW}$–$12\,\mathrm{MW}$ $3.3\,\mathrm{kV}$ 3L-BTB NPC PEC system enabled by $6.5\,\mathrm{kV}$ Si IGCT in one of the latest offshore wind turbines [10]. The efficiency is stated to be 98% for the BTB PEC system, which equates to above 99% per PEC. In the scientific and research society a myriad of MV PECs using different converter topologies have been built for railroad, aviation, power substation or wind turbine applications using Si IGBTs [19]–[24]. Some of these MV PECs utilize SiC elements in their otherwise Si based PECs to achieve higher efficiency [25], [26]. The authors in many of these papers believe that SiC has latent potential, but due to the immaturity and cost of SiC dies or SiC devices they still primarily choose to use Si based devices. A few researchers have also built PECs entirely with SiC devices; in [18] a $855\,\mathrm{kVA}$ 4-stage SiC based MV PEC system was built back in 2011 with a total efficiency of 97% equating to a single converter efficiency of above 99.2%. In [27] a $100\,\mathrm{kW}$ 4-stage PEC system was built utilizing $10\,\mathrm{kV}$ SiC MOSFETs on the MV side, this converter was tested up to $30\,\mathrm{kW}$ of active power with no efficiency specified. An efficiency of 99.1% was reached in a $25\,\mathrm{kW}$ test for a single phase 2L converter switching at $48\,\mathrm{kHz}$ in [28] and in [29] a three phase $100\,\mathrm{kVA}$ multi-level PEC with $15\,\mathrm{kV}$ SiC MOSFETs was built, reaching DC voltage levels of $20\,\mathrm{kV}$ and having an efficiency over 97%, but due to power supply limitations only $14\,\mathrm{kW}$ was circulated per phase. In [30] the PEC test platform preceding the one presented here is described. That test platform is used to test a 2L $10\,\mathrm{kV}$ SiC MOSFETs MV PEC in a DC-fed BTB configuration with a line voltage of $4.16\,\mathrm{kV}$ while circulating $42\,\mathrm{kVA}$ of apparent power through inductors, the estimated efficiency was found to be over 99% per converter. The test platform presented in this paper is designed to be a flexible platform. BTB power circulation in inductors with a high-capacity MV DC-link or power circulation between LV and MV with induction machines in the loop are just two modes of operation. The building blocks to emulate many realistic power conversion scenarios are there and the control system is flexible enough that most of the aforementioned state of the art medium voltage converters can be tested in this test platform.

II. Test platform and facilities

The first test setup built in the test platform is a motor mode test setup, intended for comparative performance evaluation of LV and MV PECs at 500 kVA. Other test setups will be built in the future using many of the same features used in this first test setup.

A. Motor mode test setup

The schematic of the motor mode power circulation test setup is presented in Fig. 2. The test setup consists of LV and MV PECs connected in BTB configurations. These LV and MV BTB PECs at different voltage levels are coupled through a line frequency transformer (LFT) seen in Fig. 3 enabling the required voltage conversion and galvanic isolation at one end. On the other end two induction machines (IM) are mechanically coupled as seen in Fig. 4, effectively acting as a second voltage transformer. The key electrical parameters of the PECs, IMs and LFT is presented in Table I. The power loss incurred during power circulation is resupplied by a LV DC-link. The LV DC-link has a low short-circuit capacity to reduce the damage from a potential destructive fault, this does not account for the short circuit capacity of the DC-link capacitors. This test setup has two primary functionalities, one of which is to provide controlled power circulation with motors in the loop and the other is to have a degree of freedom to evaluate PECs enabled by different topologies. Having motors in the loop makes the PEC system resemble a wind turbines PEC system more and introduces parasitics like common mode currents in the induction machine necessitating the use of carefully designed filters. The rotating machines grant the system a large inertia, but because induction machines are used, then the inertia can be decoupled from the electrical system by removing the flux generated in the stator windings.

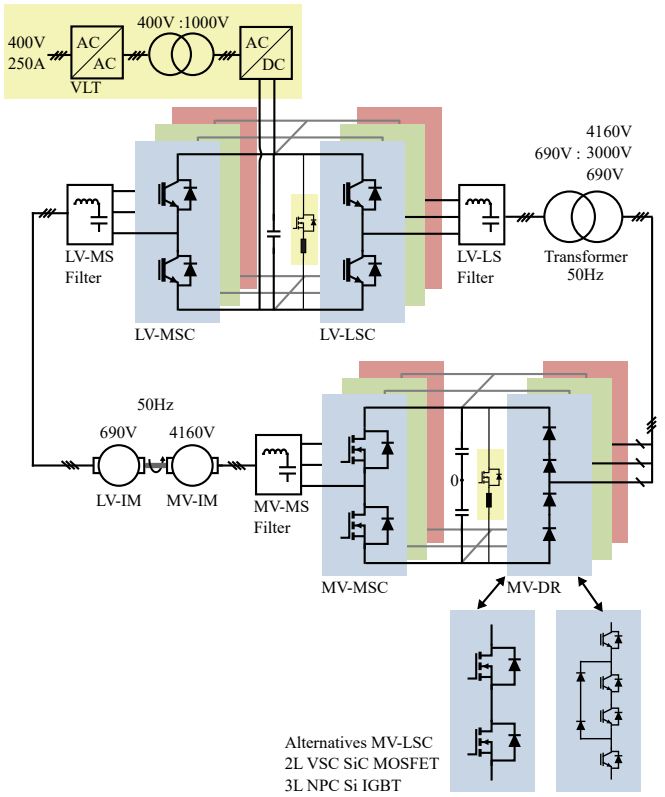

Fig. 2. 500 kVA motor mode regenerative power circulation test setup schematic

B. Motor mode power circulation

Power circulation in the motor mode test setup shown in Fig.2 is a procedural process. The system is DC-fed by a $55\,\mathrm{kW}$ variable frequency drive (VFD or VLT [31]) whose $400\,\mathrm{V}$ 3-phase line output is transformed up to $1000\,\mathrm{V}$ before being rectified at which point it is connected to the LV DC-link. When the LV DC-link is energized then the LV line-side-converter (LV-LSC) can generate a sinusoidal voltage which is transformed to $4.16\,\mathrm{kV}$ or alternatively to $3\,\mathrm{kV}$ or $0.69\,\mathrm{kV}$. The transformed voltage is then rectified with a MV diode-rectifier (MV-DR). To reduce the maximum voltage potential to the protective ground; the MV DC-link makes use of a center tapped neutral point connection. The MV machine-side-converter (MV-MSC) drives the MV induction machine (MV-IM). The LV induction machine (LV-IM) is driven by the LV machine-side-converter (LV-MSC) and can be used to load the MV-IM and facilitate circulation of power within the test system. The BTB connected LV PECs thus control all power circulation in the system. If the LV-LSC is turned off then the MV DC-link discharges which shuts down the MV-MSC, whereas if LV-MSC is turned off then no machine flux will be present and thus the MV-IM will experience no load and only no power will be circulated. In addition to PECs, the test setup also includes the passive filters: line-side sine wave filter on LV side, $\mathrm{d}v/\mathrm{d}t$ filters between MV-MSC and MV-IM as well as LV-MSC and LV-IM. The sine wave filter is used to form a sinusoidal waveform with low harmonic distortion to the LFT. The $\mathrm{d}v/\mathrm{d}t$ filters are designed to limit the voltage slew rate ($\mathrm{d}v/\mathrm{d}t$) appearing across MV-IM and LV-IM terminals to below the permissible levels specified by the IM manufacturers. Both LV and MV PECs have DC-choppers installed parallel to the LV and MV DC-link. The LV DC-chopper is dimensioned to absorb the regenerative braking of the LV-IM, making it well equipped to also handle over voltage events and discharging of the LV DC-link. The MV DC-chopper is only dimensioned to absorb energy from over voltage and the discharging of the MV DC-link.

TABLE I
TEST SYSTEM PARAMETERS

Subsystem	Parameter	Value	Unit
Low voltage powerstack	$V_{\mathrm{LL,rated(rms)}}$	690	V
	$V_{\mathrm{DC,rated}}$	1070	V
	$I_{\mathrm{ph,rated(rms)}}$	407	A
	f_{sw}	1–3	kHz
Medium voltage powerstack	$V_{\mathrm{LL,rated(rms)}}$	4160	V
	$V_{\mathrm{DC,rated}}$	6000	V
	$I_{\mathrm{rated(rms)}}$	70	A
	f_{sw}	5–10	kHz
Medium voltage induction machine	$V_{\mathrm{LL,rated}}$	4160	V
	$I_{\mathrm{rated(rms)}}$	62	A
	P_{rated}	360	kW
	ω_{rated}	1780	RPM
	f_{rated}	60	Hz
	Power factor cos(ϕ)	0.85	
	Efficiency	95	%
Low voltage induction machine	$V_{\mathrm{ph,rated(rms)}}$	690	V
	$I_{\mathrm{ph,rated(rms)}}$	360	A
	P_{rated}	355	kW
	ω_{rated}	1492	RPM
	f_{rated}	50	Hz
	Power factor cos(ϕ)	0.86	
	Efficiency	96	%
Transformer	$V_{\mathrm{rated,primary}}$	690	V
	$V_{\mathrm{rated,secondary}}$	4.16 – 3 – 0.69	kV
	S_{rated}	500	kVA
	f_{rated}	50	Hz

C. Facilities and safety

A birds eye view of the test facilities and platform can be reviewed in Fig. 5. The building in which the test platform is built offers $2\,\mathrm{MVA}$ and $800\,\mathrm{kVA}$ connections to the power grid through $20\,\mathrm{kV}$ / 20 – 10 – 6 – $3\,\mathrm{kV}$ and $20\,\mathrm{kV}$ / 0.69 – $0.4\,\mathrm{kV}$ multi-tap transformers, providing adequate power and voltage levels to test a wide range of PEC systems. For this test platform only the 800 kVA 0.4 kV output will be necessary. The test room was initially designed for destructive testing of electric parts and thus the control room is electrically and mechanically shielded from the test room. The test room has motion sensors and contact switches interlinked with the power grid switchgear in order to ensure no personnel is in the test room during testing. Multiple 2.7k resolution cameras capturing footage at 240 frames per second are installed in key positions for post-analysis of catastrophic failures. The risk of electrocution from stored energy within the test system is reduced to a minimum by designing an appropriate grounding

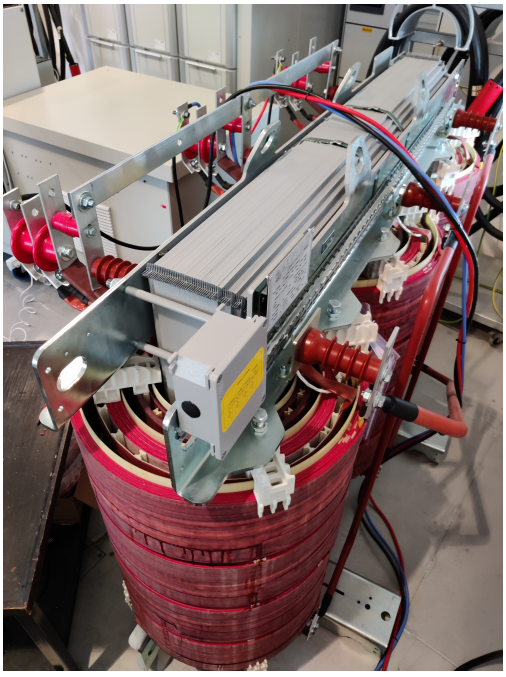

Fig. 3. Air cooled multi-tap line frequency transformer (50Hz)

Fig. 4. LV and MV inductions machines mechanically coupled.

scheme. A grounding switch seen in Fig. 6 is incorporated that shorts DC-links, MV line frequency transformer and induction machine terminals to each other and to ground, discharging the most dangerous electric lines in the test system. Under normal operating conditions DC-links will have been discharged by their respective DC-choppers before the grounding switch is engaged. Furthermore, a manual grounding stick is used as a precaution when components have to be touched. All conductive parts that can be touched casually are grounded, this includes heat sinks that are sometimes left floating to avoid common mode currents. This level of safety emboldens the researchers to push the technology to its limit and find the true potential of SiC devices.

D. Cooling system

An aspiration of this project is to achieve high precision efficiency estimations of the LV and MV PECs. In order to accomplish this, two separate cooling loops are designed and installed as shown in Fig. 7 with a schematic shown in Fig. 8. These cooling loops include high precision flow and temperature sensors as well as controllers for coolant temperature. The two cooling loops are chilled by an external liquid-to-air chiller capable of chilling all PECs. To enable full temperature controllability of the loop coolant, heaters of 2.2 kW are installed in line with the pump on the LV and MV cooling loops. These heater are turned on when the PECs are not outputting any heat in order to start an experiment at a temperature above ambient temperature. Semiconductors performance is reliant on the temperature, so it is important to have the option of controlling the coolant temperature. A mixing valve controls how much water is being chilled by the external coolant or is bypassing the heat exchanger. A fixed speed pump circulates the water at almost constant water flow and pressure levels. The readings on flow and pressure levels is used to detect if the cooling system is faulty, in which case the test platform will enter a safe state. The temperature is measured before and after each PEC, in combination with a measured flow that is common for all PECs in the same cooling line the power loss can be calculated for each PEC. The coolant has direct contact with the switching devices heat spreaders why it is argued that only a negligible amount of heat coming from the switching devices is dissipated to the atmosphere.

III. Communication and State Machine

The communication and control of the test platform is an interlink between power interface cards (PIF), digital signal processors (DSP), Labview real-time and -host programs. A schematic of the communication and control structure is shown in Fig. 9.

1) PIF cards: The PIF cards interfaces with current transducers and offer the fastest shutdown of switching devices in the case of hardware faults. The PIF cards propagate gate signals to the gate drivers and incorporates dead-time. This project uses in-house developed PIF cards for MV and proprietary PIF cards for LV. The use of proprietary and old hardware has proved to be a hurdle because it adds to the complexity of the test platform.

2) DSPs: The DSPs interfaces with the PIF cards, encoder and Labview cRIO through fiber optic connections, the LV DSP is shown in Fig. 10. The DSPs are responsible for running the control code and state machines specific for each PEC. They execute a deterministic control loop running at 5 kHz that acquires data from the PIF cards and executes control algorithms based on which PEC they run. They output a PWM signal, which the PIF card can choose to propagate or not. The

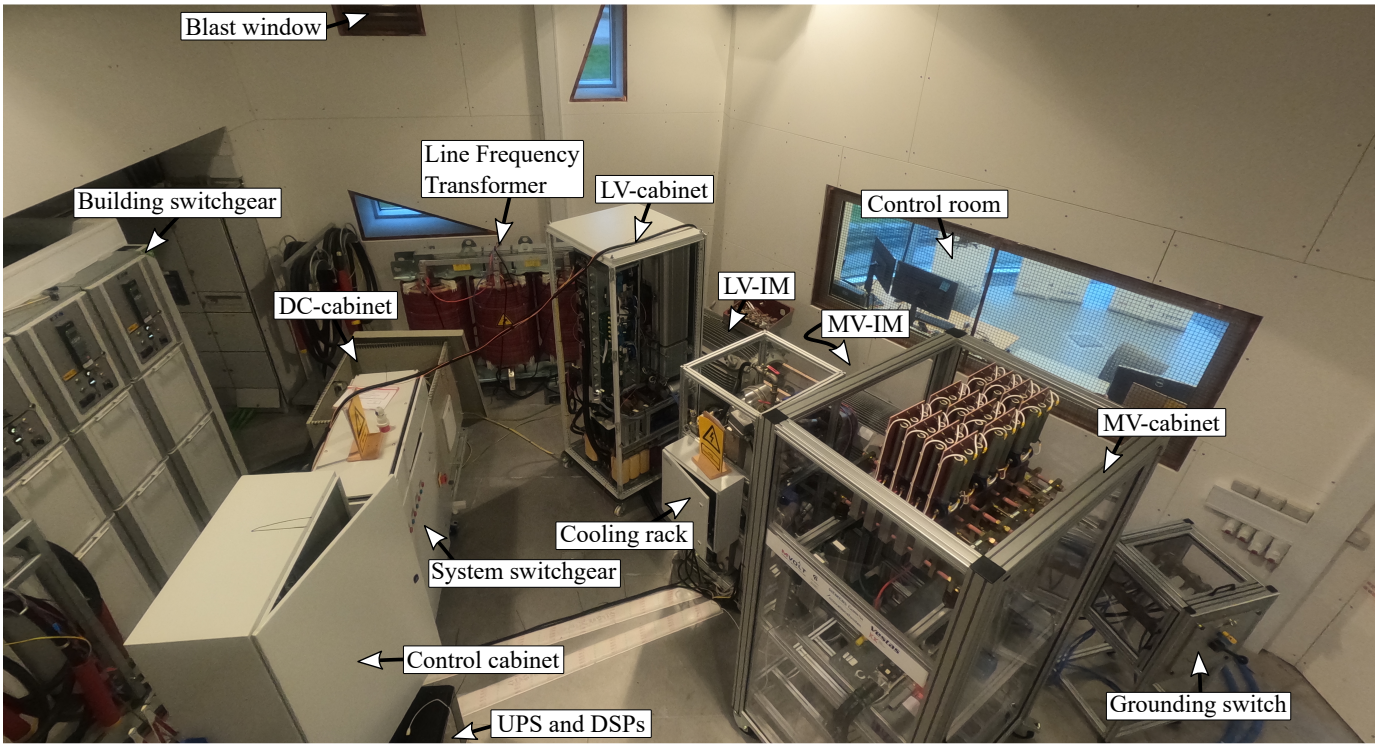

Fig. 5. Image of facilities with 500 kVA test platform installed.

Fig. 6. Grounding switch; Shorts and grounds DC-links and high potential AC 3-phase lines.

Fig. 7. Cooling system for LV and MV PECs.

DSPs also store data at the same rate as the deterministic loop in a cyclic buffer, which can be transmitted to the cRIO when desired, like in the case of a fault or just periodically. The DSPs also receive commands like start/stop, change frequency and so on from the cRIO.

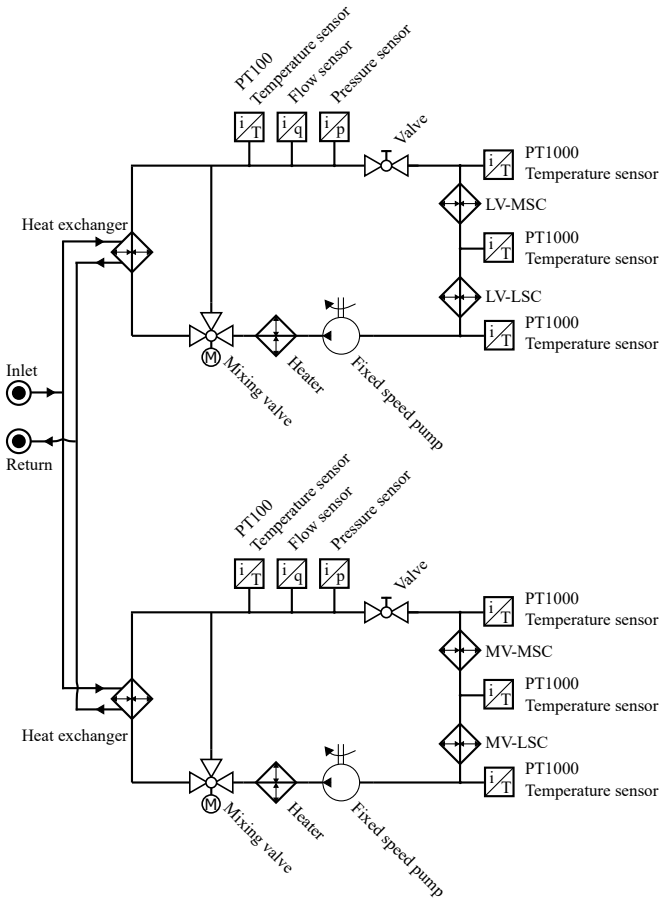

Fig. 8. Low/medium voltage cooling system.

3) Labview cRIO: The Labview cRIO executes a real-time program running at 1 kHz, which periodically acquires data like state and DC link-voltage from the DSPs and operator commands from the host computer while also reading pressure, temperature and flow from the transducers in the cooling system. In the same real-time loop coolant temperature control is also running, ensuring stable coolant temperature. The Labview real-time program acquires logic signals from the test platforms switchgear and grounding switch to detect if the system has input power and if the grounding switch is in an open position. The Labview real-time program also contain the general state machine of the test platform, which uses data from all previously described sources to determine which PECs can be running.

4) Labview host program: The host Labview program acts as the operators control of the test platform, granting supervisory information to the operator about the general state of the test platform and the state of the converters. In an event/interrupt based manner the operator can send commands to the cRIO, which can be something like start MV-IM. The cRIO may reject the command if there is no basis for executing that command. All the data sampled on the DSPs and cRIO can be plotted and/or saved to disk by using the Labview host program.

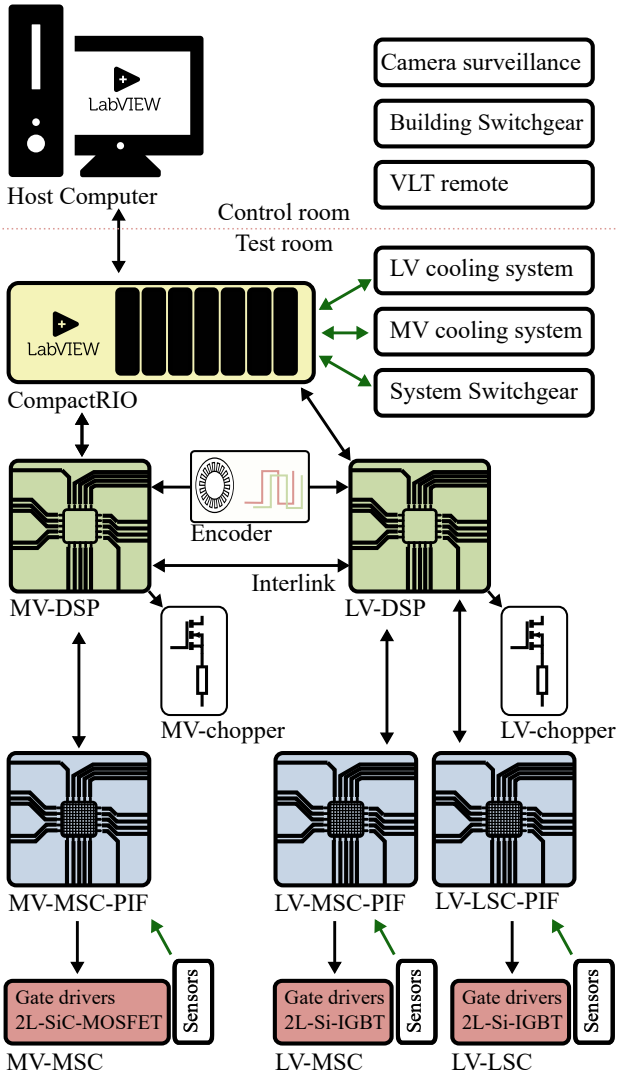

Fig. 9. Communications schematic for test platform.

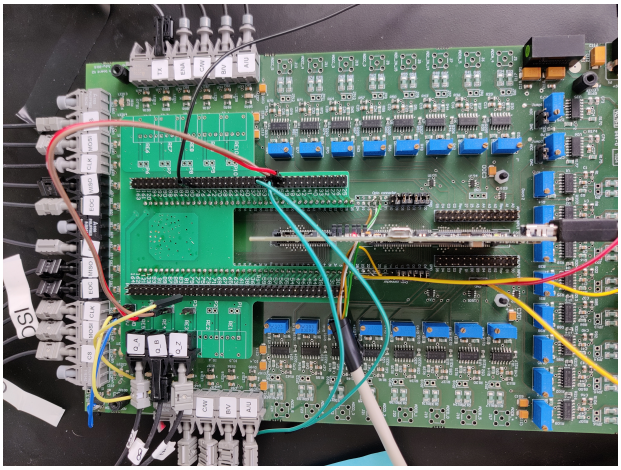

Fig. 10. LV DSP with fiber interfaces to LV-MSC-PIF, LV-LSC-PIF, encoder and CompactRIO

A. State machine

To enable power circulation in the motor mode test setup, a state machine is designed. The state machine states and

state transitions criteria are outlined in Fig. 11. The state machine can progress towards more of the test setup running if the operator wills it and conditions for state transitions are fulfilled. Reversely the state machine can decay if a fault occurs in the cooling, any converter or if the operator wills it. For example to go from cooling state to LV-LSC control the LV DC-link has to be powered, all communications has to be OK and lastly the operator has to initiate line side waveforming, then and only then will the test setup transition to LV-LSC control where the MV DC-link can be charged. If at any point there is a control system fault like missed control loops or lost communication, then the system will transition to safe state. If there is a hardware fault like over current in LV-IM then LV-MSC-PIF card will stop the propagation of the gate signals. The fault will then propagate back up the communication chain and the system will transition to safe state.

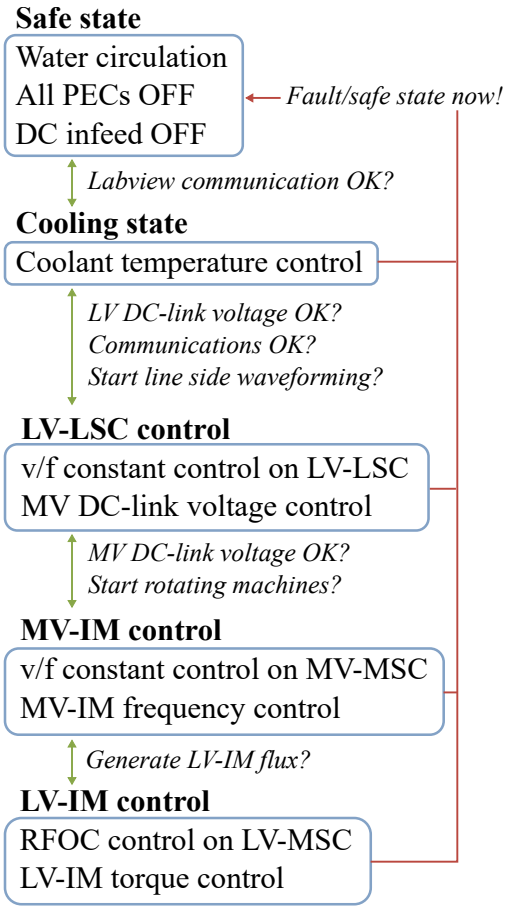

Fig. 11. State Machine for motor mode test setup.

IV. Conclusion

In this paper the principle functionalities of a 500 kVA DC-fed regenerative power circulation platform has been presented. The motor mode test setup enables comparative performance evaluation of medium and low voltage power electronic converters. The structure of the system is designed for safe and reliable testing, personnel safety is secured with an extensive but simple grounding scheme and protective facilities. Reliable testing is secured with a state machine that supervises the power circulation progress and simple but robust control of induction machines and line side waveforming. Robust cooling with temperature and flow measurements on each PEC allow for calorimetric power loss measurement of each PEC, enabling for comparative efficiency evaluation. The designed test platform is designed with an eye to future experiments and will enable extensive testing of novel SiC devices in direct comparison with commercially available Si devices. To enable the next generation of SiC devices to be used in future wind turbines or other power electronic converter systems, it is important to have a test platform like the one presented in this paper.

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