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Effect of Choke Placement on Common-Mode Noise in Three-Phase Variable Speed Drives

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***Abstract*—Three-phase variable speed drives play a key role in energy conversion systems. To comply with the electromagnetic compatibility standards for the 0–2 kHz frequency range, magnetic chokes are typically placed at the DC or AC sides of the drive systems. Recently, compatibility levels have been defined at 9–150 kHz for the public network in accordance with IEC 61000-2-2. At this frequency range, common-mode noise is an important factor affecting electromagnetic compatibility. This paper analyzes the effect of choke placement on common-mode noise at the 9–150 kHz frequency range. In particular, a comparative study on choosing either two DC-link choke inductors or three AC line inductors is carried out via mathematical calculations. To this end, single-phase common-mode equivalent models are extracted for each placement of DC and AC chokes. Subsequently, by calculating the transfer functions of the currents in the single-phase equivalent circuits, the attenuation rate of common-mode currents from the motor to the grid side is analytically modeled for each choke configuration. The developed theories prove that AC line inductors are more effective at suppressing low-frequency common-mode contents, while DC chokes are useful in attenuating high-order noise contents. Laboratory test results are used to prove the validity of the presented theoretical modeling and analysis.**

***Index Terms*—Choke, common-mode (CM), electromagnetic interference (EMI), inductor, motor drive system, variable speed drive.**

I. Introduction

GLOBAL demand for energy is increasing as a result of industrial advances in both developing and developed countries [1]. In the industrial world of today, motor drive systems acquire a significant share in energy conversion systems. Subsequently, three-phase Variable Speed Drives (VSDs) have attracted a great deal of industrial applications, such as pumps, fans, mining, oil, and gas [2]–[4]. In a typical structure of VSD as shown in Fig. 1, the grid side AC voltage passes through the front-end diode rectifier, providing the DC voltage. Then the DC voltage is converted to controllable AC output voltages through Pulse Width Modulated (PWM) inverter.

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To ensure high power quality of the electrical grid, manufacturers should meet the Electromagnetic Compatibility (EMC) standards for the frequency ranges of 0–2 kHz and 150 kHz–30 MHz [5]. Consequently, inductors are conventionally located at either DC or AC sides of the drive system to align with the EMC standards below 2 kHz [6]–[9], while Electromagnetic Interference (EMI) filters are implemented to follow the standards above 150 kHz [10]–[13]. As shown in Fig. 1, either two DC-link inductors or three AC line inductors are typically placed in the system to suppress the low order harmonics. Accordingly, the inductors at the AC line are known as AC chokes, whereas the ones at the DC link are known as DC chokes.

Lately, power electronics and semiconductor materials have made rapid advances. As a result, the switching frequency of power converters has been increased to enhance the performance and decrease the size of the system. However, the extensive use of fast switching power converters has posed emerging power quality issues to the distribution network. As shown in Fig. 2, these power electronic devices typically switch at the 2–150 kHz frequency range, creating EMC problems in the network [14]. As a result, the compatibility levels have been defined in IEC 61000-2-2 for the 9-150 kHz frequency range, which can be used as a reference to define the emission limits at the product level. Therefore, several standardization committees in NASI, IEC SC 77A, CISPR, and CIGRE have recently engaged in defining new emission limits for below 150 kHz [15]–[18]. According to the International Electrotechnical Commission (IEC) SC 77A, the 2–150 kHz frequency range is categorized into the frequency ranges of 2–9 kHz and 9–150 kHz [18]–[20]. Yet, due to the the fact that enforcing standards for this range is still at its initial steps, there is a lack of basic research on propagation of noise emissions at this range [21].

To meet the emerging EMC standard requirements below 150 kHz, the quality of grid current should be monitored. Harmonic and EMI currents can be categorized into two major types of Differential-Mode (DM) and Common-Mode (CM) currents. Splitting these two components is an important step in DM and CM filter design in order for complying with the EMC standard limits. DM currents are mainly responsible for low frequency harmonics caused by the switching of rectifier, while CM currents are the dominant components in the high frequency conducted emissions generated by the inverter switching.

In Fig. 1, a conventional configuration of EMI filter can be seen. Accordingly, C_{yac} and C_{ydc} are the AC and DC side

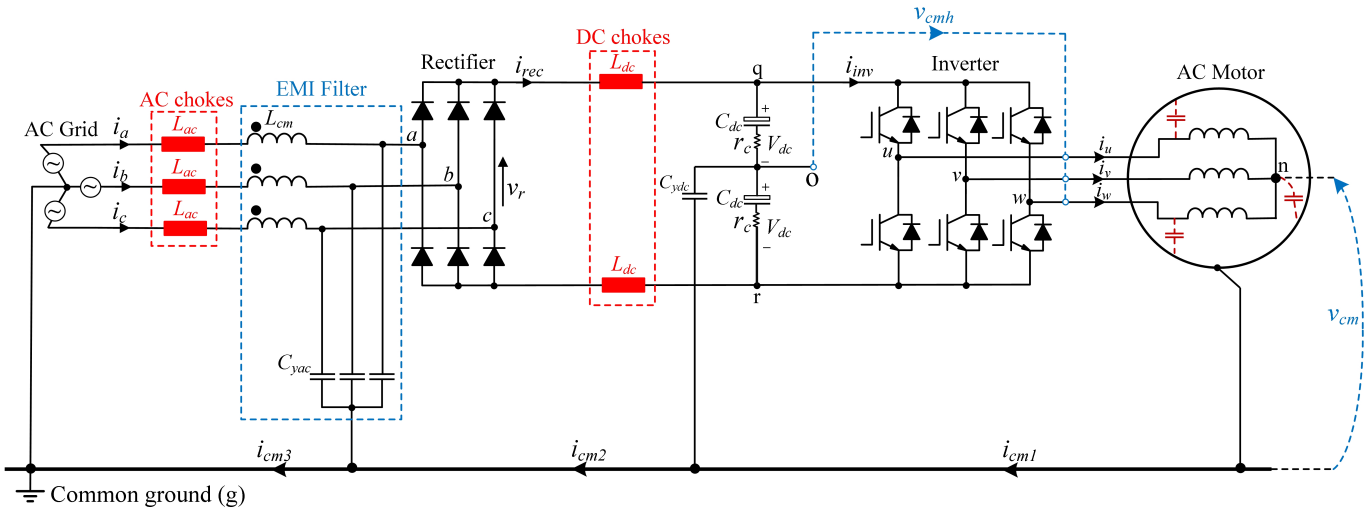


Fig. 1. Conventional motor drive system (effect of heat sink is neglected and DM components of EMI filter are removed).

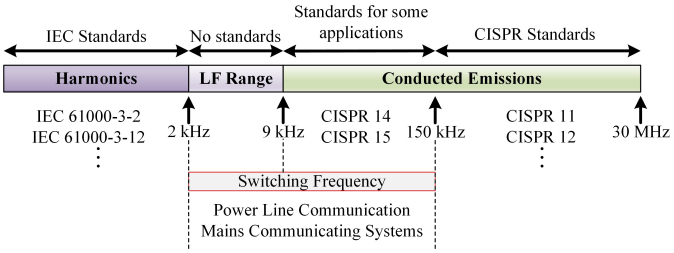


Fig. 2. Harmonics and conducted EMI frequency ranges classified by EMC standard organizations [14].

grounding capacitors of the EMI filter, which could have an effect both on DM and CM noises but the effect on DM noise is negligible. Furthermore, the coupled inductor L_{cm} is the most important part of the filter, which ideally deals with CM noise. It is worth mentioning that in this figure, only the CM component of the EMI filter is shown and the DM component has been removed for simplicity. According to Fig. 1, the CM component of the EMI filter is composed of the CM choke L_{cm} and the grounding capacitors C_{yac}. Existing EMI filters utilized in motor drives are mainly designed to reduce the emissions above 150 kHz. Nevertheless, the new EMC limits in 9-150 kHz could be challenging for drive manufacturers and it requires modification of pre-existing filters to fulfill the requirements of the new frequency range. Therefore, an effective approach could be modifying the harmonic filters including DC and AC chokes to comply with the emerging 9–150 kHz standards. For this purpose, one aspect that needs to be considered is the effect of choke placement on CM noise emissions.

So far, AC and DC chokes are the two typical configurations to suppress low order harmonics in motor drive systems. Guo *et al.* [22] presented a space vector control strategy, which could effectively attenuate the low order grid current harmonics up to 350 Hz. The presented method in [22] led to reduced DC choke size and volume. In [23], the effect of choke placement on machine's performance during input voltage imbalance and sag conditions was investigated. Accordingly, the machine's peak-to-peak torque amplitudes for DC and AC choke configurations was compared. Lee *et al.* [24] investigated the effect of DC and AC inductors on voltage resonances at the Point of Common Coupling (PCC). In [25], a calculation methodology was introduced to determine the size of DC and AC chokes for assessing the low frequency voltage harmonics at PCC. Since the ongoing efforts for emission limit standardization at the 9–150 kHz frequency range is still at its early stages, the effect of choke placement on CM noises has not been thoroughly analyzed. Nonetheless, Ganjavi *et al.* [26] compared the impact of DC and AC chokes on CM noises. Consequently, the attenuation rate of the CM currents entering to the grid from the motor side was investigated. This paper is a follow up work of [26]. The focus of study in [26] was only on simulation analysis, while mathematical investigation and experimental verification were not conducted. The additional contributions of this paper compared to the related work of [26] can be expressed as follows:

- Calculating CM sources and accurately assessing the impact of choke placement on CM noise at the grid according to the derived equations
- Providing guideline on deciding the placement of the chokes for CM current suppression at the grid in accordance with impedance mismatch criteria
- Analyzing the level of CM current penetrated to the grid by calculating the currents flowing through the CM equivalent circuit
- Validating the theoretical modeling and analysis through laboratory test results, including CM noise source measurements and conducted EMI experiments

This paper analyzes the impact of choke placement in three-phase VSDs on CM currents entering to the grid. To this end, the single-phase CM equivalent circuits of the drive are extracted according to the placements of magnetic chokes at the AC line or DC bus. Through calculating the transfer

functions of the CM currents for each choke configuration, the attenuation rate of the CM current from the motor to the grid is predicted. This analysis gives a useful insight into the relative advantages of choosing either two DC-link inductors or three AC line inductors to suppress the 9–150 kHz CM currents entering the grid.

This paper is organized as follows: In Section II, CM models of the drive are extracted for DC and AC choke configurations. Then a guideline on deciding the placement of chokes in motor drive systems is provided. Section III analyzes the attenuation rate of CM current from the motor to the grid for each DC and AC choke configuration. For this purpose, the transfer functions of the currents in the single-phase equivalent CM circuits are derived. In Section IV, laboratory test results are provided to validate the presented theoretical subjects. Finally, Section V summarizes the paper.

II. CM Circuit Modeling

CM currents go to the ground through the parasitic couplings. The major parasitic couplings contributing to the flow of CM currents are capacitive and this is why the CM currents mainly contain high frequency contents excited by the switching of the rear-end inverter. In fact, above the switching frequency, paristic capcitances create low impedance routes, causing the flow of CM currents to the ground. In this section, CM models of the drive system with DC and AC choke configurations are extracted and then CM noise sources generated by switching of rectifier and inverter are calculated.

A. Single-Phase CM Equivalent Circuit

Fig. 3 shows the single-phase CM equivalent circuit of the drive system, extracted through the standard parallel combination rules. According to Fig. 3, v_{cml} and v_{cmh} are the CM noise sources generated by the switching of the rectifier and inverter, respectively. Also, the precedure for modelling the AC motor is fully discussed in [27]. For the motor model, L_w is the stator winding inductance. Moreover, C_{s1} and C_{s2} represent the capacitance created between the windings and the stator. Also, C_w is the equivalent capacitive couplings between turns of windings as the inter-winding capacitance, which is very small compared to C_s. The resistive parameters of R_{f1} and R_{f2} represent the impedance between the stator and frame, while r_s and R_w indicate the skin effect and the eddy current losses, respectively. The parameters of the motor model for this case study can be found in Table I.

The simplified model of the equivalent CM circuit is depicted in Fig. 4. As shown in Fig. 4, Z_{yL} is the CM equivalent impedance of the load. This load could be any RLC element or a motor fed by a cable. Also, Z_{xac} and Z_{xdc} are the equivalent AC side and DC side impedances, respectively. As seen in (1) and (2), Z_{xac} includes AC chokes and CM chokes while Z_{xdc} includes DC chokes and DC link capacitors. Also, Z_{ydc} and Z_{yac} are the equivalent CM impedances of DC-link and AC line CM capacitors, respectively. These equivalent impedances can be derived as follows:

$$Z_{xac} = \frac{L_{ac}s + r_{ac}}{3} + L_{cm}s \tag{1}$$

$$Z_{xdc} = \frac{L_{dc}s + r_{dc}}{2} + \frac{1}{2C_{dc}s} + \frac{r_c}{2} \tag{2}$$

$$Z_{yac} = \frac{1}{3C_{yac}s} \tag{3}$$

$$Z_{ydc} = \frac{1}{C_{ydc}s}. \tag{4}$$

where as can be seen in Fig. 1, L_{dc} and L_{ac} are the inductance values of the DC and AC chokes, respectively, while r_{dc} and r_{ac} are their related DC Resistances (DCRs). Moreover, C_{dc} and r_c are the capacitance and the Equivalent Series Resistance (ESR) of the DC-link capacitors, respectively. Also, C_{ydc} and C_{yac} are the CM capacitors at the DC link and AC line, respectively.

TABLE I
Parameters of the Motor Model [27] (see Fig. 3)

Parameter	C_{s1}	C_{s2}	R_{f1}	R_{f2}	r_s	L_w	C_w	R_w
Value	2.04 nF	3.3 nF	6.67 Ω	4.3 Ω	3.2 Ω	3.13 mH	13.8 pF	4.23 kΩ

B. CM Noise Sources

In accordance with Fig. 1, CM voltage can be calculated using the following equations [27]:

$$\begin{aligned} v_{un} &= v_{uo} + v_{og} - v_{cm} \\ v_{vn} &= v_{vo} + v_{og} - v_{cm} \\ v_{wn} &= v_{wo} + v_{og} - v_{cm} \end{aligned} \tag{5}$$

where the CM voltage v_{cm} is specified as the voltage between the motor's neutral point (n) and ground (g). Furthermore, v_{uo}, v_{vo}, and v_{wo} are the voltages between the midpoint of the DC-link (o) and the output terminals of the drive (u, v and w), respectively. Moreover, the voltage potential between o and g is named as v_{og}. Consequently, from (5) and presuming that the system is balanced, v_{cm} can be expressed as:

$$v_{cm} = \underbrace{v_{og}}_{v_{cml}} + \underbrace{\frac{v_{uo} + v_{vo} + v_{wo}}{3}}_{v_{cmh}} \tag{6}$$

According to (6), v_{cm} is composed of low and high frequency components, defined as v_{cml} and v_{cmh}, respectively. As a matter of fact, v_{cml} is made by the grid voltage through switching of diode rectifier, while v_{cmh} is made by the output voltage via PWM switching of inverter (see Fig. 3).

1) Harmonic contents of low-frequency CM noise source (v_{cml}): To calculate the harmonic spectrum of v_{cml}, Fourier series of diode rectifier's output voltage should be derived. According to Fig. 1, v_{qr} is defined as the rectifier's output voltage, which is the voltage between the positive DC-link terminal point q and the negative DC-link terminal point r. As explained in [28], to calculate the rectifier's output voltage v_{qr}, the Fourier series can be separately calculated for the positive and negative rectifier output terminals. Therefore, the Fourier series expansion of the waveform for the positive (v_{qg}) and negative (v_{rg}) output terminals can be calculated as below:

$$v_{qg} = \frac{3\sqrt{3}V_m}{2\pi}\left(1 + \sum_{h=1}^{+\infty} \frac{2 \times (-1)^{h+1}}{9h^2 - 1} \cos\left(3h\omega_g t\right)\right) \tag{7}$$

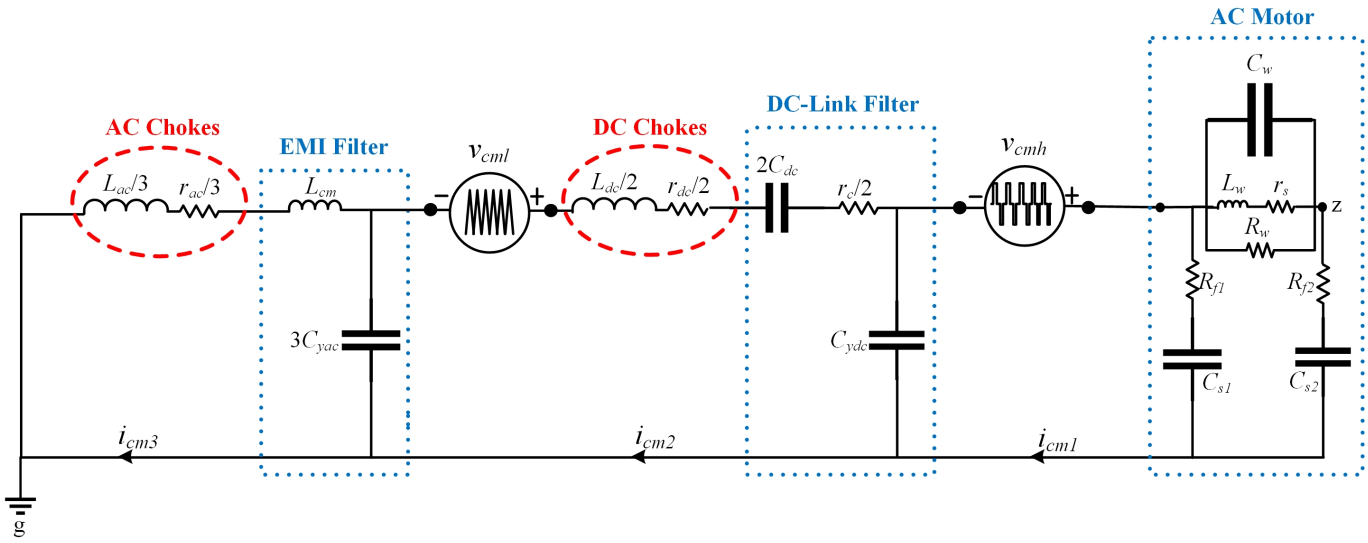


Fig. 3. CM equivalent circuit of the drive system.

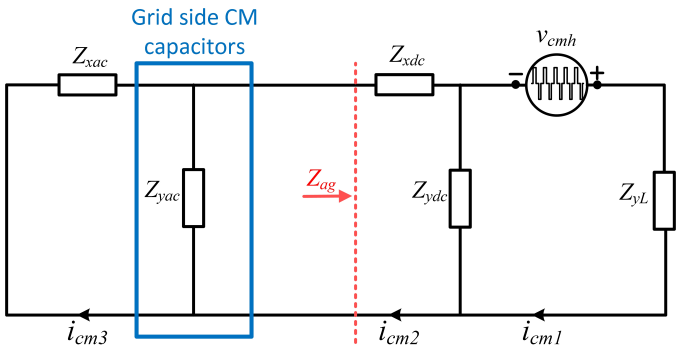


Fig. 4. Simplified CM equivalent circuit of the drive system (see Fig. 3).

$$v_{rg} = \frac{3\sqrt{3}V_m}{2\pi}(-1 + \sum_{h=1}^{+\infty} \frac{2}{9h^2-1}\cos(3h\omega_g t)) \quad (8)$$

where v_{qg} is defined as the rectifier 's positive output terminal voltage, which is the voltage between the positive DC-link terminal point q and the ground g. Also, v_{rg} is defined as the rectifier's negative output terminal voltage, which is the voltage between the negative DC-link terminal point r and the ground g (Fig. 1). It is to be noted that in (7) and (8) h is the index of summation, V_m is the peak value of the grid voltage, and ω_g is the fundamental angular frequency of the grid. Therefore, from (7) and (8), the rectifier's output voltage v_{qr} can be readily calculated by subtracting the negative terminal voltage from the positive terminal voltage, as bellow:

$$v_{qr} = v_{qg} - v_{rg} = \frac{3\sqrt{3}V_m}{\pi}(1 - \sum_{h=1}^{+\infty} \frac{2}{36h^2-1}\cos(6h\omega_g t)) \quad (9)$$

Subsequently, v_{qo} is defined as the voltage between the positive output terminal q and the mid-point of the DC link o (see Fig. 1), which can be calculated as follows:

$$v_{qo} = \frac{v_{qr}}{2} = \frac{3\sqrt{3}V_m}{2\pi}(1 - \sum_{h=1}^{+\infty} \frac{2}{36h^2-1}\cos(6h\omega_g t)) \quad (10)$$

In (6), it was shown that the low-frequency component of the CM voltage is the term v_{og}. Therefore, the low-frequency CM component can be calculated by subtracting v_{qo} (see (10)) from v_{qg} (see (7)), as bellow:

$$v_{cml} = v_{og} = v_{qg} - v_{qo} \quad (11)$$

Consequently, from (7), (10), and (11), the low-frequency component of the CM voltage (v_{cml}) can be eventually expressed as follows:

$$v_{cml} = \frac{3\sqrt{3}V_m}{\pi} \sum_{h=1,3,5,7...}^{+\infty} \frac{1}{9h^2-1}\cos(3h\omega_g t)\cdot \quad (12)$$

It is to be noted that v_{cml} is derived to depict the order of harmonics affected by the diode rectifier. According to (12), the low frequency CM noise source is composed of harmonic contents at the frequency of $(3h\omega_g)$. Therefore, this noise source has negligible effect on the total CM voltage of v_{cm}, as the dominant contents of v_{cm} are mainly flowing through the capacitive couplings excited by the switching inverter.

2) Harmonic contents of high-frequency CM noise source (v_{cmh}): To calculate the harmonic spectrum of v_{cmh}, the Fourier series of inverter's output voltages should be calculated. According to Fig. 1, the double Fourier series of the inverter's leg voltage for one phase (v_{uo}) can be extracted as follows [29]:

$$v_{uo} = MV_{dc}\cos(\omega_o t) + \frac{4V_{dc}}{\pi}\sum_{m=1}^{\infty}\sum_{k=-\infty}^{+\infty} Q_{m,k}\cos(m\omega_c t + k\omega_0 t) \quad (13)$$

$$Q_{m,k} = \frac{1}{m}J_k(m\frac{\pi}{2}M)\sin\Big([m+k]\frac{\pi}{2}\Big), \quad (14)$$

where v_{uo} is the voltage between the points u and o (see Fig. 1), M is the modulation index, and J_k is the Bessel function of order k. Moreover, ω_0=2πf_0 is the fundamental angular frequency of the output voltage and ω_c =2πf_c is the carrier angular frequency. According to Fig. 1, the average voltage across the DC-link is defined as $2V_{dc}$. The leg voltages for the phases v and w can be calculated by substituting $k[\omega_0 t - 2\pi/3]$ and $k[\omega_0 t + 2\pi/3]$ for $k\omega_0 t$ into (13), respectively. From (6) and (13), the double Fourier series of v_{cmh} can be expressed as:

$$v_{cmh} = \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{\substack{k=-\infty, \\ k=3j}}^{+\infty} Q_{m,k} \cos\left(m\omega_c t + k\omega_0 t\right) \qquad (15)$$

According to (15), the high frequency CM noise source includes harmonic contents at the frequency of $(mf_c + kf_0)$, exciting the CM capacitive couplings. In fact, this noise source excites the dominant components of CM currents. In order to assess the level of CM noises distinctively caused by the inverter and rectifier, the simulation results in MATLAB Simulink software have been compared for when the inverter is connected in the simulation platform and when it is removed. Consequently, Fig.5 shows the analysis for both DC and AC choke configurations in the drive system. As it can be seen in Fig. 5, a great deal of the CM noise is induced the inverter and the effect of rectifier at this range is almost negligible. As a result, in this paper, the effect of rectifier is neglected for the CM noise analysis at the 9–150 kHz frequency range. Therefore, as seen with Fig. 4, v_{cmh} is considered as the main noise source for CM current analysis.

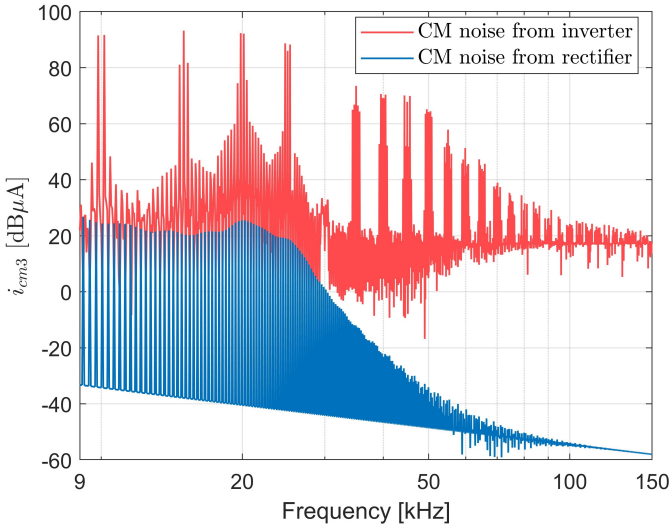
C. Guideline on Deciding the Choke Placement

It is important that the placement of the chokes be decided scientifically based on mathematical analysis rather than relying on simulation-based platforms. Consequently, a guideline is provided to decide the position of chokes according to EMC requirements at different frequency ranges. This instruction is based on the impedance mismatch criteria to attenuate the CM current at the grid side.

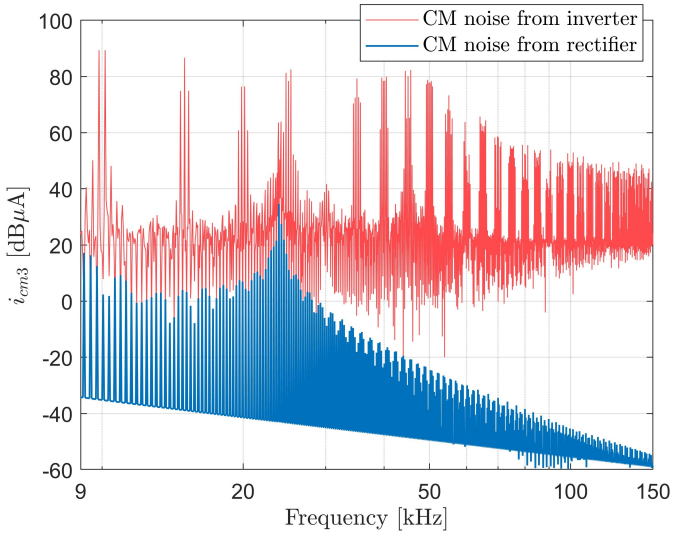
1) Concept of impedance mismatching: Fig. 6 shows the simplified equivalent circuits for modeling sources and impedance networks related to conducted EMI noise. In Fig. 6, it is assumed that V_s is the noise source. Also, Z_s and Z_o are the impedances at the source and grid sides, respectively. In order to minimize the noise transfer or maximize the signal reflection from the source to the grid, impedance mismatch is required. This is why filters are implemented to provide the impedance mismatch between the noise source and the grid. For a passive filter, insertion loss is a figure of merit to measure the attenuation capability. Accordingly, insertion loss for a filter can be defined as:

$$A = 20\log\mid \frac{V_o}{V_o'} \mid \qquad (16)$$

where V_o' and V_o are the noise voltages transferred to the grid with and without filter, respectively. In fact, the larger value for the insertion loss means the filter is more capable of noise



(a)



(b)

Fig. 5. Level of CM noises induced by the inverter and rectifier. (a) DC chokes in the system, (b) AC chokes in the system.

attenuation. Here, two common configurations of filters are considered to investigate the impedance mismatch approach to attenuate noises at the grid side.

According to Fig. 6 (a), by assuming that the filter configuration is a parallel capacitor with the capacitance value of C, the insertion loss can be calculated as follows:

$$A = 20\log\mid 1 + \frac{Z_{parallel}}{Z_c} \mid \qquad (17)$$

where

$$Z_c = \frac{1}{Cs} \qquad (18)$$

$$Z_{parallel} = \frac{Z_s Z_o}{Z_s + Z_o} \qquad (19)$$

From (17), it can be realized that to achieve high values of insertion loss, $Z_{parallel}$ should be large. Nevertheless, by assuming that according to Fig. 6 (b), the configuration of the

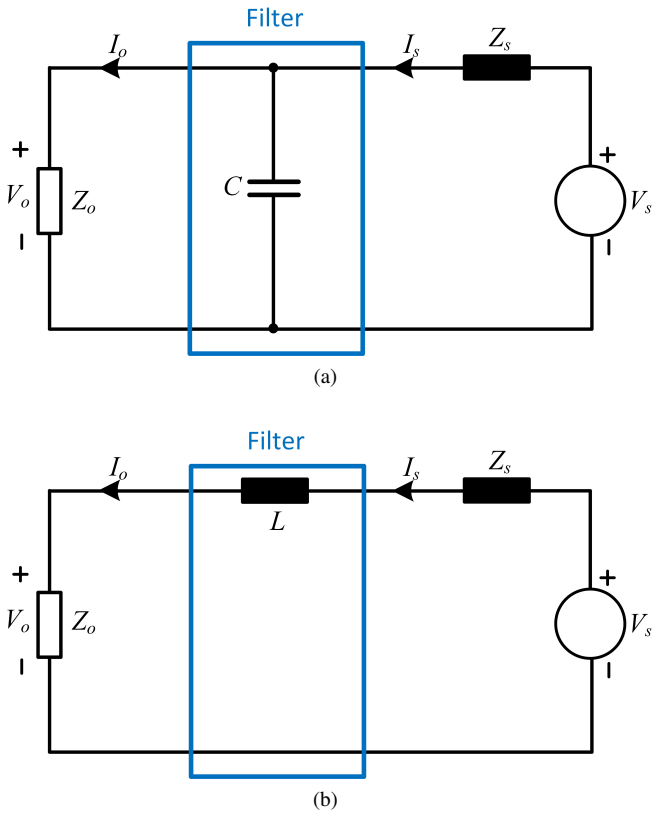


Fig. 6. Simplified equivalent circuits for modeling noise sources. (a) A parallel capacitor utilized as the filter, (b) a series inductor utilized as the filter.

filter is a series inductor with an inductance value of L, the insertion loss can be calculated as follows:

$$A = 20 \log \mid 1 + \frac{Z_L}{Z_{series}} \mid \tag{20}$$

where

$$Z_L = Ls \tag{21}$$

$$Z_{series} = Z_s + Z_o \tag{22}$$

From (20), it can be realized that to achieve high values of insertion loss, Z_{series} should be small. In brief, an inductor in series with a low impedance or a capacitor in parallel with a high impedance does provide attenuation, leading to reflection of power from the grid to noise source.

2) Impedance mismatch criteria for the drive system under study: According to Fig. 4, for the considered case study, the CM filter utilized for the noise suppression is equivalent to a parallel capacitor (with the impedance of Z_{yac}). As shown in Fig. 4, to calculate the insertion loss, the parameter of Z_{ag} has been defined as the CM impedance seen from the rectifier to the load side. Accordingly, the insertion loss can be calculated as:

$$A = 20 \log \mid 1 + \frac{Z_{parallel}}{Z_{yac}} \mid \tag{23}$$

where

$$Z_{parallel} = \frac{Z_{ag} Z_{xac}}{Z_{ag} + Z_{xac}} \tag{24}$$

From (23) and the discussion held earlier, high values of A are achieved if $Z_{parallel}$ is large, leading to a higher impedance mismatch between the grid and the CM noise source. In Fig. 7, the capability of impedance mismatching has been investigated for three different choke placements: 1- When two inductors are placed at the positive and negative sides of the DC link (DC chokes), 2- When three AC line inductors are placed at the grid side (AC chokes; see Fig. 1), and 3- When three AC line inductors are placed between the rectifier and the CM capacitors C_{yac}. It is worth mentioning that all the chokes are assumed to be identical. From (23), $Z_{parallel}$ is the determining factor for impedance mismatch and its higher values leads to the higher reflection of CM emissions from the grid. Fig. 7 depicts the magnitude of $Z_{parallel}$ for different choke placements in the drive. Based on Fig. 7, the higher value of $Z_{parallel}$ represents the more impedance mismatch and reflection between the noise source and the grid. In fact, Fig. 7 gives useful information on choosing the right choke placement for the CM noise suppression. According to Fig. 7, AC chokes can provide higher reflection of the CM noise at the low frequency range below 28.2 kHz compared to the other choke configurations (due to the higher values of $Z_{parallel}$). Also, it can be realized that moving the AC inductors to the rectifier side would not be a good solution for CM noise suppression. This can be explained by the fact that in this case, three inductors are still used in the setup while reflection from the grid is reduced compared to when the chokes are being placed at the AC line. Therefore, another configuration that could be considered is two DC-link inductors. As can be seen in Fig. 7, with two DC link inuctors, although the impedance mismatch reduces at the low frequency range, at high frequency range above 28.2 kHz, DC chokes can provide more reflection of CM noise. As a result, depending on the frequency range of interest for EMC, DC choke as the low cost solution could be an attractive alternative together with CM choke.

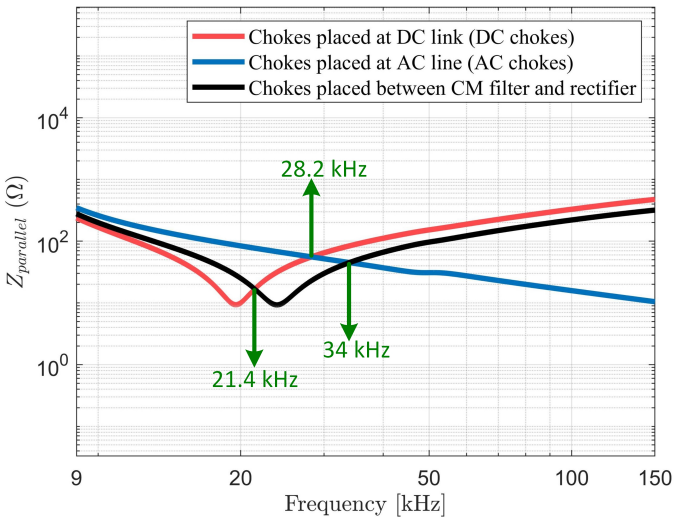


Fig. 7. Impedance mismatch for different choke placements.

3) System cost and volume considerations: Although utilizing DC chokes may have some advantages over AC chokes

such as reduced cost and volume, measures can be taken to reduce the cost and volume of the system. As an example, the designer can reduce the cost and volume of the system for DC chokes by using only one equivalent 1.25 mH × 2= 2.5 mH inductor at the positive side of the DC link instead of using two 1.25 mH DC chokes, one at the the positive and another at the negative side of the DC-link. Although this approach will reduce the total size and cost of the system, the disadvantage is that the CM impedance of the system is reduced, so more CM noises are expected to enter to the grid. Furthermore, utilizing a hybrid passive filter which is the combination of DC and AC chokes is another solution to benefit from the advantages of both configurations [30]; however, the hybrid configuration can result in higher cost and volume. This is why, conventionally, either single AC or DC chokes are implemented in the system. It is worth mentioning that according to the IEC 61000-3-12 recommendation, a practical guideline for choosing DC and AC choke inductance values are suggested. To fulfil the current harmonic requirement in compliance with IEC 61000-3-12, the AC chokes with 3% (per phase) of base impedance or the DC chokes with 5% (per phase) of base impedance is suggested for motor drive systems [31], [32].

III. CM Current Attenuation Rate Analysis

According to Figs. 1 and 4, CM currents generated by the CM noise sources are defined as i_{cm1}, i_{cm2}, and i_{cm3}. In fact, to comply with the IEC standards, filters are designed to reduce the level of CM current entering to the grid, which is described as i_{cm3} in Figs. 1 and 4. In this section, it is investigated how DC-link and AC line choke configurations can attenuate the generated CM current penetrating to the grid.

A. CM Current Calculation

To calculate the harmonic spectrum of i_{cm1}, i_{cm2}, and i_{cm3}, KVL is conducted on the CM equivalent circuit of Fig. 4, derived as follows:

$$v_{cmh} - (Z_{yL} + Z_{ydc})i_{cm1} + Z_{ydc}i_{cm2} = 0 \tag{25}$$

$$Z_{ydc}i_{cm1} - (Z_{xdc} + Z_{ydc} + Z_{yac})i_{cm2} + Z_{yac}i_{cm3} = 0 \tag{26}$$

$$Z_{yac}i_{cm2} - (Z_{xac} + Z_{yac})i_{cm3} = 0 \tag{27}$$

Eventually, by replacing v_{cmh} derived from (15) into (25)–(27), the Fourier series of the CM currents can be calculated as:

$$i_{cm1} = \frac{4V_{dc}}{\pi}\frac{\Gamma^2\Upsilon(Z_{yL} + Z_{ydc}) + Z_{ydc}(\Gamma\Upsilon Z_{ydc} + Z_{ydc}Z_{yac}^2)}{\Gamma^2\Upsilon(Z_{yL} + Z_{ydc})^2} \times \sum_{m=1}^{\infty}\sum_{\substack{k=-\infty,\\ k=3j}}^{+\infty} Q_{m,k}\cos(m\omega_c t + k\omega_0 t) \tag{28}$$

$$i_{cm2} = \frac{4V_{dc}}{\pi}\frac{\Gamma\Upsilon Z_{ydc} + Z_{ydc}^2 Z_{yac}}{\Gamma\Upsilon^2(Z_{yL} + Z_{ydc})} \times \sum_{m=1}^{\infty}\sum_{\substack{k=-\infty,\\ k=3j}}^{+\infty} Q_{m,k}\cos(m\omega_c t + k\omega_0 t) \tag{29}$$

$$i_{cm3} = \frac{4V_{dc}}{\pi}\frac{Z_{ydc}Z_{yac}}{\Gamma\Upsilon(Z_{yL} + Z_{ydc})} \times \sum_{m=1}^{\infty}\sum_{\substack{k=-\infty,\\ k=3j}}^{+\infty} Q_{m,k}\cos(m\omega_c t + k\omega_0 t) \tag{30}$$

where

$$\Gamma = (Z_{xdc} + Z_{ydc} + Z_{yac} - \frac{Z_{ydc}^2}{Z_{yL} + Z_{ydc}}) \tag{31}$$

$$\Upsilon = Z_{xac} + Z_{yac} - \frac{Z_{yac}^2}{\Gamma}. \tag{32}$$

B. CM Current Transfer Functions

1) Attenuation Rate of CM Current from the Motor to the Grid Side (i_{cm3}/i_{cm1}): To analyze the level of generated CM current absorbed to the grid, the transfer function of $H = i_{cm3}(s)/i_{cm1}(s)$ is extracted for different choke placements. Consequently, from (28)–(30), this transfer function can be calculated as:

$$H = \frac{i_{cm3}(s)}{i_{cm1}(s)} = \frac{\Gamma Z_{ydc}Z_{yac}(Z_{yL} + Z_{ydc})}{\Gamma^2\Upsilon(Z_{yL} + Z_{ydc}) + Z_{ydc}(\Gamma\Upsilon Z_{ydc} + Z_{ydc}Z_{yac}^2)}. \tag{33}$$

Thus, if $L_{ac} = r_{ac} = 0$ is applied in (33), $i_{cm3}(s)/i_{cm1}(s)$ is calculated for the DC chokes being placed in the system, while when $L_{dc} = r_{dc} = 0$ is applied, the transfer function will be calculated for AC chokes being in the system. In Fig. 8, the calculated transfer functions of $i_{cm3}(s)/i_{cm1}(s)$ are shown for DC-link and AC line chokes at the 9–150 kHz frequency range. The specifications of the drive system are depicted in Table II. Fig. 8 shows the calculated transfer function of $H = i_{cm3}(s)/i_{cm1}(s)$ (see Fig. 1) for different choke configurations. In fact, the transfer function of H shows the attenuation rate of CM current from the motor side (i_{cm1}) to the grid side (i_{cm3}), where the larger magnitude of H means the lower attenuation rate. In Fig. 8, the transfer function of H is compared for AC chokes with L_{ac}=1.25 mH, DC chokes with the same inductance value of AC chokes as L_{dc}=1.25 mH, and DC chokes with 1.5 times inductance value of AC chokes as L_{dc}=1.875 mH. According to Fig. 8, in general, low order harmonics at the grid side are more effectively attenuated when AC chokes are placed in the system, while at higher frequencies, DC chokes are more effective. However, the inductance value can affect the frequency range and level of attenuation. As can be seen in Fig. 8, with increasing the inductance value of DC chokes to 1.5 times of the AC chokes 's, the frequency range of attenuation for DC chokes improve (see the intersections of the waveforms at 24 kHz and 29 kHz). Moreover, when the inductance value of DC choke is increased to 1.5 times of the AC chokes's (L_{dc}=1.875 mH), the CM current attenuation performance of the system is improved (the magnitude of H is reduced), where at above 24 kHz, the DC chokes can more effectively suppress the CM current at the grid side.

TABLE II
VALUES OF SIMULATION AND EXPERIMENTAL PARAMETERS (SEE FIG. 1)

Symbol	Parameter	Value
$v_{a,b,c}$	Grid phase rms voltage	240 V
f_g	Grid frequency	50 Hz
L_{dc}, r_{dc}	DC choke inductance and resistance	1.25 mH, 40 mΩ
L_{ac}, r_{ac}	AC choke inductance and resistance	1.25 mH, 40 mΩ
L_{cm}	CM choke	5.3 mH
C_{ydc}, C_{yac}	DC and AC sides CM capacitors	100 nF, 470 nF
f_s	Switching frequency	2.5 kHz
P_o	Drive rated power	7.5 kW

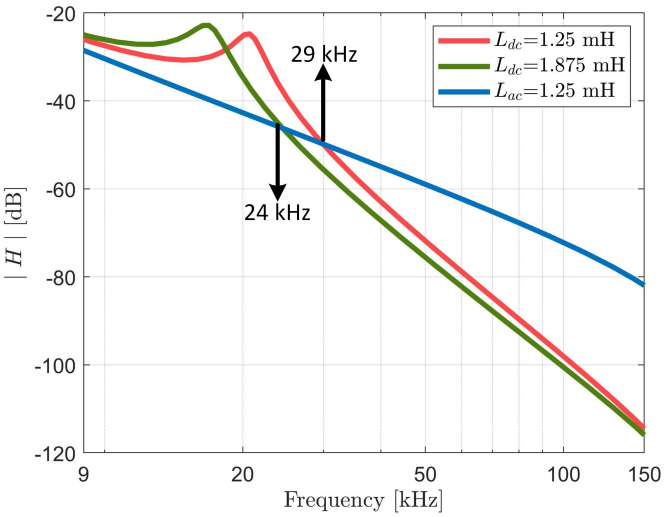


Fig. 8. Calculated transfer functions of $i_{cm3}(s)/i_{cm1}(s)$ for different volumes of DC and AC chokes in the system.

To evaluate the adopted approach, the Fast Fourier Transform (FFT) of i_{cm1} and i_{cm3} are extracted, using MATLAB software, as shown in Fig. 9. According to Fig. 9, AC chokes are more capable in attenuating the low order harmonics at the grid side, while at the higher frequency ranges, the attenuation rate for DC chokes is higher, which is fully in alliance with the analytical model shown in Fig. 8. In the following, it is shown that the system parameters can significantly affect the frequency range of attenuation for the DC and AC choke configurations.

2) Level of CM Current Penetrated to the Grid (i_{cm3}): The level of CM current entered to the grid can be analyzed through the harmonic spectrum of i_{cm3} calculated by (30). According to (30), when identical chokes are placed either at AC line or DC bus, the term $\frac{1}{\Gamma\Upsilon}$ is the determining factor affecting the grid side CM current. Therefore, as seen from (34), the parameter Λ has been defined as the ratio of i_{cm3} with DC chokes being in the system ($L_{ac} = r_{ac} = 0$) to i_{cm3} with AC chokes being in the system ($L_{dc} = r_{dc} = 0$). This parameter gives a useful insight about the effect of choke placement on the CM currents penetrated to the grid.

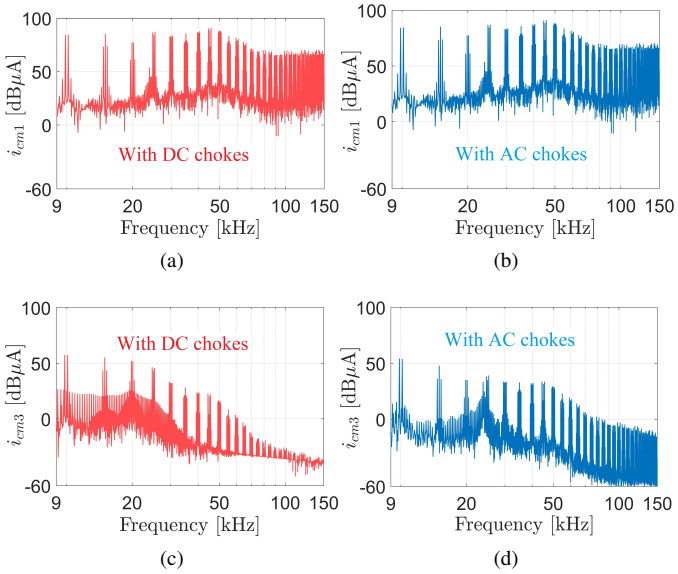


Fig. 9. Simulated CM current FFTs of the three-phase system with DC and AC chokes. (a) i_{cm1} with DC chokes in VSD, (b) i_{cm1} with AC chokes in VSD, (c) i_{cm3} with DC chokes in VSD, (d) i_{cm3} with AC chokes in VSD.

$$\Lambda = \frac{(\Gamma\Upsilon)\Big|L_{ac} = r_{ac} = 0}{(\Gamma\Upsilon)\Big|L_{dc} = r_{dc} = 0} \tag{34}$$

Figs. 10 (a) and (b) depict the parameter Λ with different values of C_{ydc} and C_{yac}, respectively (see Fig. 1). According to Fig. 10, in the range $\Lambda > 1$, it is predicted that the higher attenuation of CM current at the grid side occurs with AC chokes in the system, while in the range $\Lambda < 1$, DC chokes lead to a higher attenuation of CM currents. As can be seen in Fig. 10, when AC chokes are in the system, i_{cm3} is more effectively attenuated at low frequency ranges, while at higher frequencies, DC chokes lead to better damping of the CM current at the grid side. According to this figure, the frequency range of attenuation is significantly dependent on the system parameters, including the CM capacitors C_{ydc} and C_{yac} in this case study. Consequently, with decrease in the capacitance value of C_{ydc} and C_{yac}, the parameter Λ intersects with the line Λ=1 at higher frequencies. These figures address the fact that when analyzing the effect of choke placement on CM current, the system parameters (for example the CM capacitors of C_{ydc} and C_{yac} in this case study) should be considered and the frequency range of attenuation is significantly dependent on the system parameters. Therefore, these factors should be considered for any other motor drive configurations.

IV. LABORATORY TEST RESULTS

Fig. 11 shows the laboratory prototype utilized for the experiments. The drive system under study is a 7.5 kW FC 302 VSD from Danfoss. Specifications of the test setup are depicted in Table II. These experiments are carried out for DC and AC choke placements in the system. For DC choke configuration analysis, two chokes are utilized: One at the

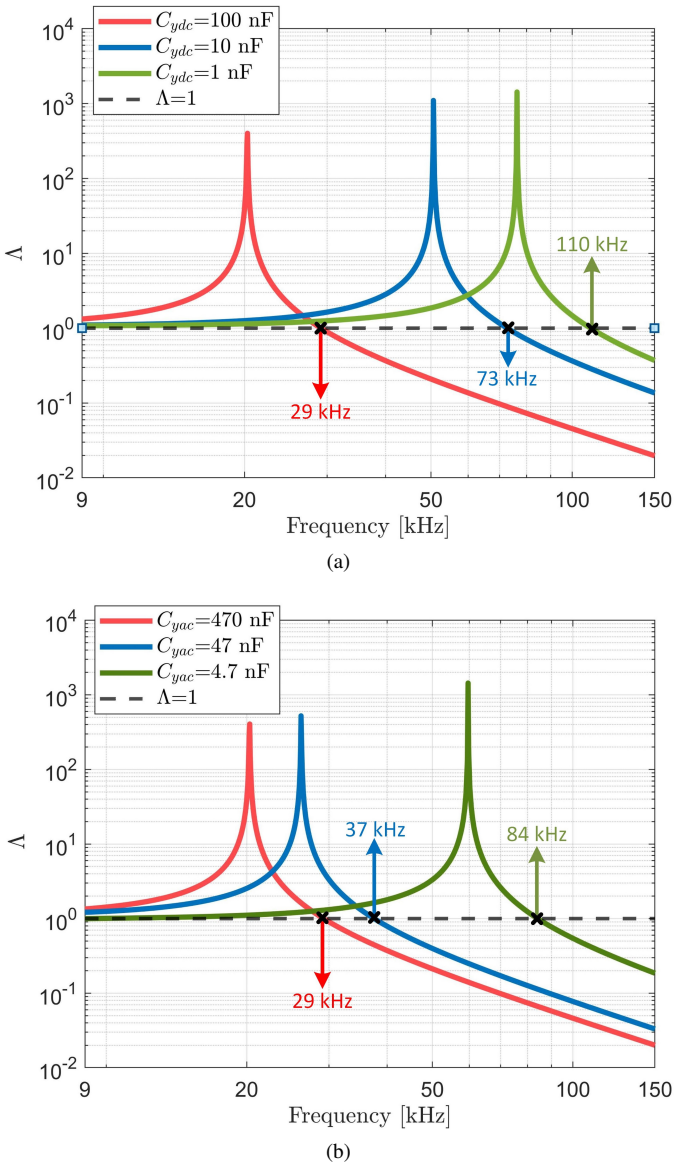


Fig. 10. Ratio of i_{cm3} with DC chokes being in the system ($L_{ac} = r_{ac} = 0$) to i_{cm3} with AC chokes being in the system ($L_{dc} = r_{dc} = 0$), calculated using (34). (a) Effect of C_{ydc}, (b) Effect of C_{yac}.

positive and the other at the negative side of the DC link (see Fig. 1). Also, for AC choke configuration analysis, the DC chokes are removed and three chokes are utilized; one for each line phase. It is worth mentioning that all the chokes have identical specifications.

A. CM Noise Source Measurements

Fig. 12 depicts the experimental waveforms of the leg phase voltage v_{uo}, the low frequency CM noise source v_{og}, the motor side CM current i_{cm1}, and the grid side CM current i_{cm3}. Figs. 12 (a) and (b) show the waveforms when DC and AC chokes are placed in the system, respectively. According to Fig. 12, v_{og} and v_{uo} make up the low and high frequency CM noise sources with the harmonic contents of $[3hf_g]$ (see (12)) and $[mf_c + kf_0]$ (see (13)), respectively. The dominant harmonic contents of the CM currents are generated by the

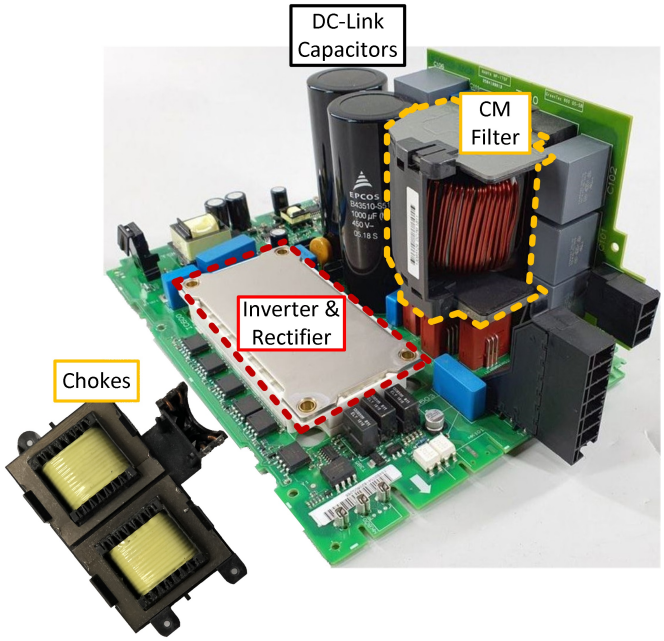


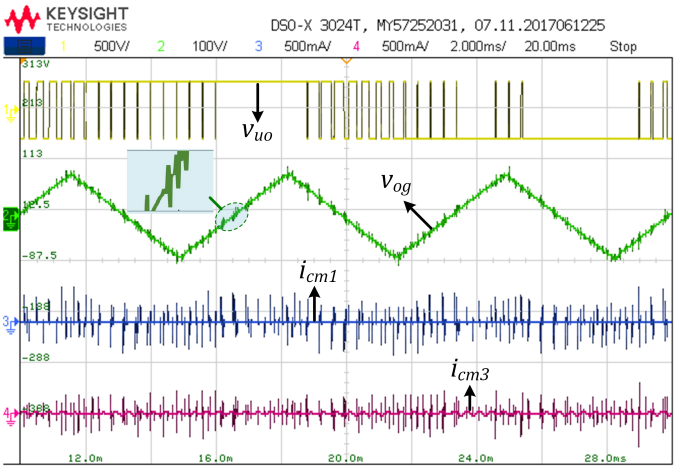
Fig. 11. Photograph of the laboratory prototype [33].

high frequency noise source. As expected from the presented theories, the effect of choke placement on the generated CM current at the motor side (i_{cm1}) is negligible, while its effect on the grid side CM current (i_{cm3}) is considerable. Moreover, as it can be seen in Fig. 12, the high frequency harmonic contents penetrate to v_{og} when DC chokes are placed in the system. This stems from the fact that, based on Fig. 1, when chokes are placed at the DC-link side, the low impedance loop containing L_{dc}, C_{ydc}, and C_{yac} is created; as a result, the high frequency voltage drop of ($L_{dc}di/dt$) will affect v_{og}.

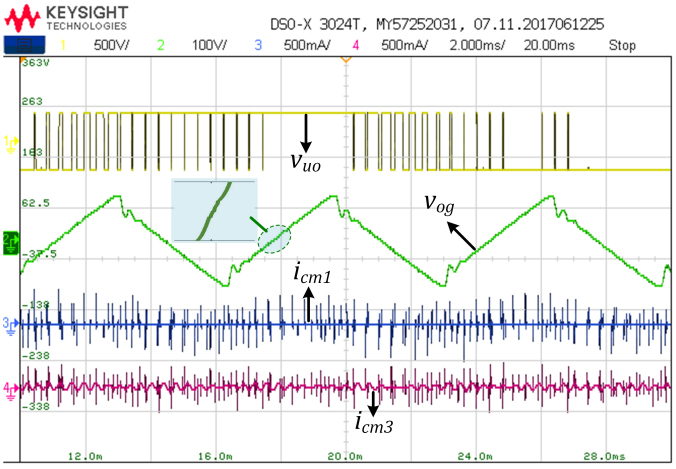
Fig. 13 (a) shows the experimental high frequency CM noise sources when DC chokes are placed in the system. Moreover, as shown in Fig. 13 (b), to validate the theoretical analysis, i_{cm1} measured through the experiment is compared with the simulation result. The simulation platform is created according to Fig. 4 in MATLAB Simulink software. Accordingly, the experimentally measured data of the inverter leg voltages v_{uo}, v_{vo}, and v_{wo} are extracted and then applied to the single-phase equivalent CM circuit in the Simulink software. In compliance with (6), to generate the CM noise source of v_{cmh} in the simulation, the measured leg voltages are all summed together and divided by three. As can be seen in Fig. 13 (b), there is an optimum match between the simulation and experiment, proving the developed theory.

In Fig. 14, FFT of i_{cm3} is extracted for DC and AC choke configurations with the motor speed of 1500 rpm. As can be seen in the figure, when AC chokes are placed in the drive, harmonic contents for i_{cm3} are smaller at below around 28 kHz, while at higher frequencies, DC chokes are more capable in damping the harmonic contents. This is in alliance with the theoretical analysis conducted in Figs. 8 and 10.

As shown in Fig. 15, the impact of motor speed has been investigated for the presented methodology. In Figs. 15 (a) and (b), the FFT of i_{cm3} has been extracted for motor speeds

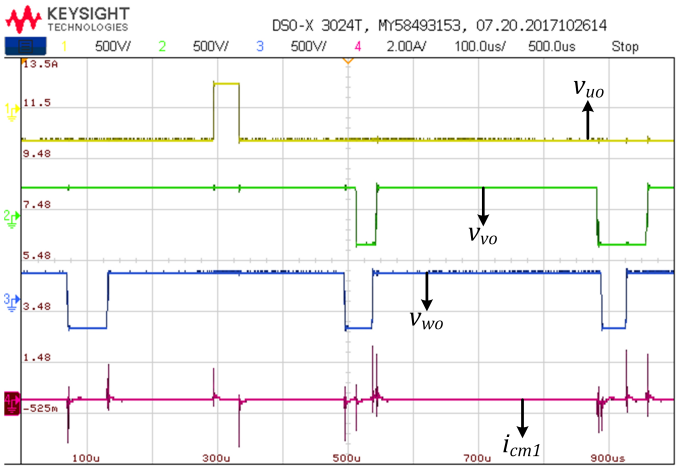


(a)

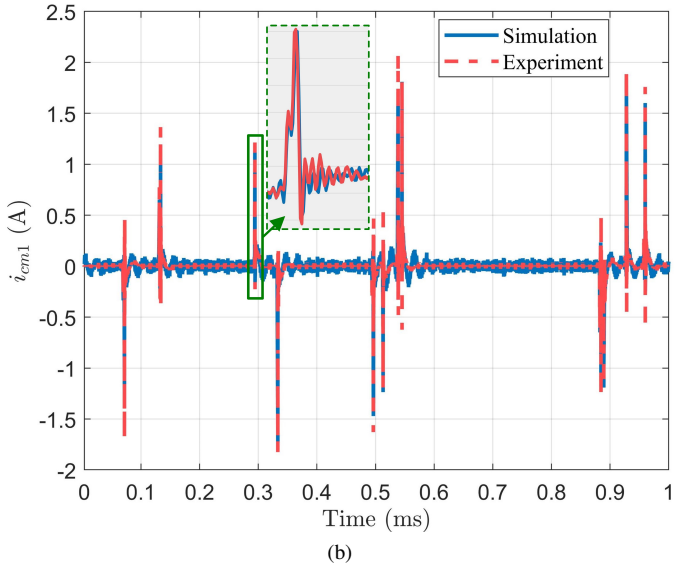


(b)

Fig. 12. Experimental waveforms of the leg phase voltage v_{uo}, the low-frequency CM noise source v_{og}, the motor side CM current i_{cm1}, and the grid side CM current i_{cm3} ($P_o = 3.8$kW). (a) DC chokes placed in the system, (b) AC chokes placed in the system.



(a)



(b)

Fig. 13. High frequency CM noise sources with DC chokes in the system. (a) experimental measurement (b) comparison between the measurement and simulation (i_{cm1}).

of 2000 rpm and 3000 rpm, respectively. As it can be seen in the figures, at different motor speeds, using AC chokes leads to smaller grid side CM current at low frequency range up to around 30 kHz in this case study, while DC chokes suppress the higher frequency harmonics more effectively. These results are in alliance with the theoretical model shown in Fig. 8. The reason that the presented methodology is valid regardless of motor speed could be attributed to the fact that the presented strategy investigates the current transfer functions of the system. These CM current transfer functions are calculated based on the high frequency CM model of the system, including motor model. However, the effect of rotor speed on CM model of the motor is negligible. This could be due to the fact that the flux entering into the rotor magnetic circuit at high frequency is very small [34]–[36]. This can be also seen in [37], [38] where the rotor's position and speed do not have any significant impact on mid to high frequency impedance features of the machine. Moreover, it is to be noted that although the motor speed may not significantly change the motor model, it is expected that the CM noise sources change with respect to motor speed. In practice, the PWM patterns at different motor speeds are not just exactly repeated at higher frequencies, but the PWM patterns completely change with respect to motor speed, giving different CM noise spectrum. Therefore, as seen in Fig. 15, while the general concept studied for the comparative performance of DC and AC chokes in CM noise suppression is valid, the level of CM noises is expected to change with respect to motor speed.

B. Conducted EMI Measurements

Line EMI of the system is measured for the drive with DC and AC choke configurations. As shown in Fig. 16, the conducted EMI is measured through Band A (9–150 kHz) Line Impedance Stabilization Network (LISN), following CISPR 16 [39]. LISN provides three important features: 1-Stable fixed impedance for the power input, 2- high frequency isolation between VSD and the main grid, and 3- repeatable measurements. According to Fig. 16, the noise voltage u_{meas} is measured in time domain and then transferred to frequency

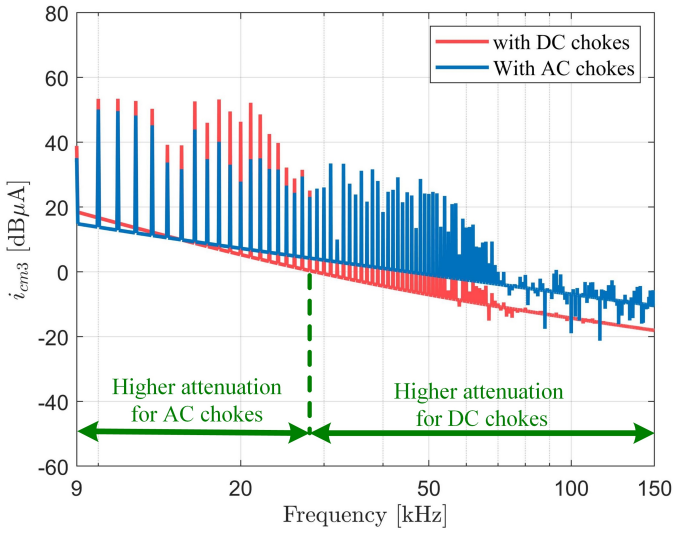


Fig. 14. FFT of the grid side CM current (i_{cm3}) with DC and AC chokes in the system with 1500 rpm motor speed.

domain using FFT for analysis. To quantify the total conducted EMI, the EMI receiver is connected to the LISN's matched measurement ports via a signal analyzer. Table III depicts specifications of the measuring equipment implemented for the EMI tests.

TABLE III
SPECIFICATIONS OF EMI MEASURING EQUIPMENT

Signal Analyzer	Keysight N9000B CXA
Transient Limiter	Com-Power LIT-930A
Attenuator	Telegärtner
LISN	NARDA PMM L3-32

Figs. 17 (a) and (b) depict the EMI measurements for DC and AC choke placements in the system, respectively. As shown in Fig. 17, the measured EMI levels are exhibited in comparison with the EMC standard following IEC 61000-2-2:2002 [40]. The measured EMI signals in Fig. 17 are the combination of DM and CM noises. According to Fig. 17, at low frequency range, AC chokes provide higher attenuation of noises while at higher frequencies, attenuation rate of DC chokes increases. The results shown in Fig. 17 are in allegiance with the theoretical analysis carried out in Section III, depicted in Figs. 8 and 10. From the simulation results it is expected that DC chokes give lower CM emissions compared to AC chokes. Although the trend is matching for each single case, comparing AC and DC results, both at higher frequency have resulted in almost same emission level around 40 [dBμV].

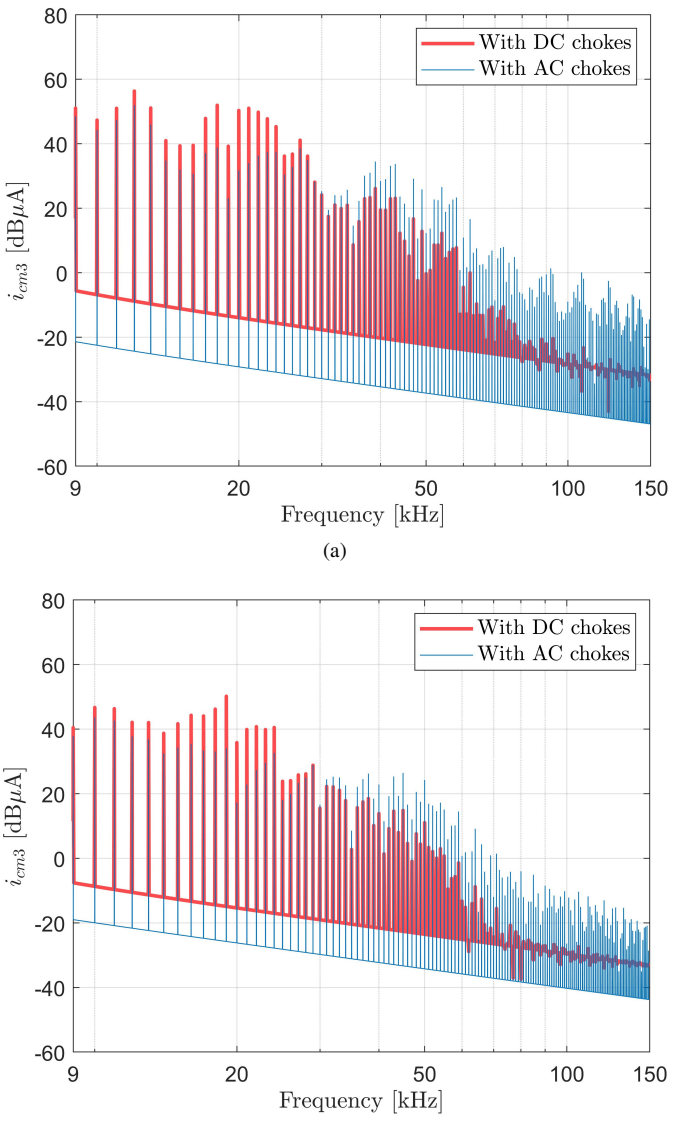


Fig. 15. FFT of the grid side CM current (i_{cm3}) for the motor speeds of: (a) 2000 rpm, (b) 3000 rpm.

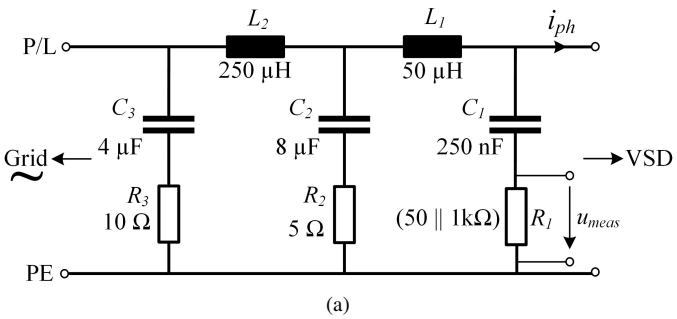
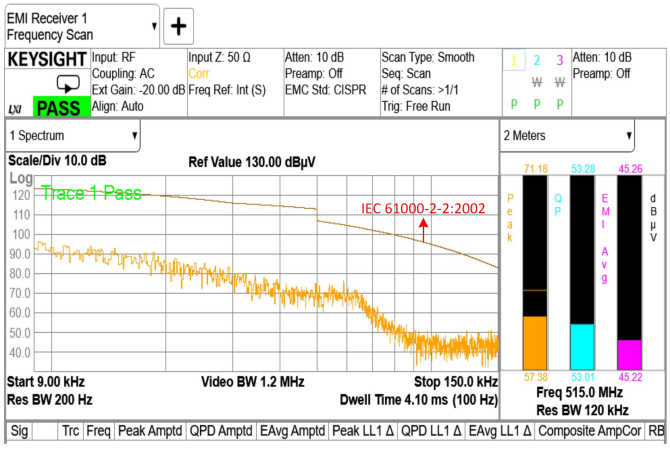


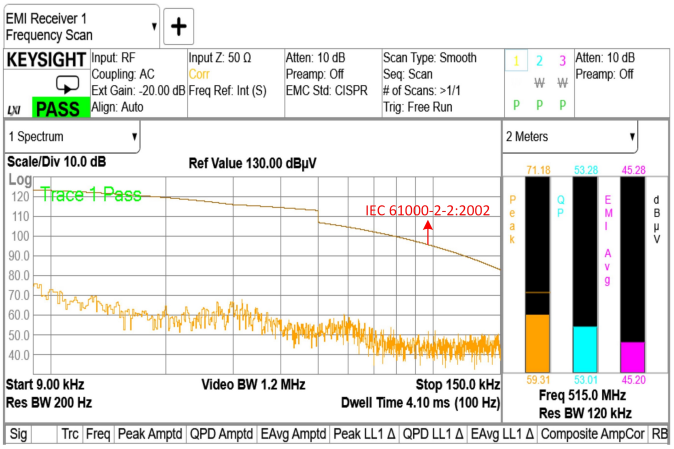
Fig. 16. LISN circuit per line according to Band A CISPR 16 [39].

V. CONCLUSION

The effect of choke placement on CM noises in three-phase VSDs has been analyzed. Accordingly, relative advantages of choosing either two DC-link inductors or three AC line inductors are investigated. For this purpose, single-phase CM equivalent circuits of the system are extracted for both choke configurations. Then the Fourier series of the CM currents entering to the grid are calculated using the inverter leg voltages and switching functions. To evaluate the impact of choke placement on CM current noise attenuation from the motor to the grid side, CM current transfer functions are calculated. The theoretical analysis proves that placing AC line inductors reduces the low frequency CM contents in the



(a)



(b)

Fig. 17. Measured EMI. (a) DC chokes in the system, (b) AC chokes in the system.

9–150 kHz frequency range, while DC chokes more effectively attenuate the high order noise contents. Moreover, it is shown that the system parameters including the CM capacitors in this case study can significantly affect the decision on making the right position of the choke placement. Although the presented methodology can be adopted for any other motor drive configurations, the drawn conclusions are valid for the EMI filter configuration considered in this case study, which is very common in commercial industrial drives. Experiments have been conducted, confirming the presented theory.

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