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A Cascaded Half-Bridge Three-Level Inverter with An Inductive DC-Link for Flexible Voltage Boosting

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***Abstract*—Voltage boosting three-level inverters may present a monotonically increasing or decreasing voltage gain when enlarging the pulse-width modulation (PWM) ratio. To produce a flexible voltage gain, this paper proposes a novel three-phase three-level PWM inverter by cascading a traditional two-level three-leg (B6) inverter with half-bridges. The proposed inverter is supplied by an inductive dc-link consisting of a dc source in series with an inductor that is charged by shooting through the half-bridges in the B6 structure. The voltages across the cascaded half-bridges are subsequently boosted, and the output voltage is stepped up due to the cascaded connection. A moderate voltage gain is achieved with proper selections of two modulation variables while maximizing the PWM ratio. In particular, when the two modulation variables are equal, a constant voltage boosting gain of two is maintained irrespective of the PWM ratio. Additionally, low voltages are induced on the components, which facilitates the use of low-voltage devices. The operating principle of the proposed inverter with a modified third-harmonic-injection (THI) PWM scheme is presented, followed with theoretical analysis, comparison, and design considerations. Experimental tests on a 1.5-kVA inverter prototype verify its feasibility.**

***Index Terms*—Three-level inverter, cascaded half-bridge, voltage boosting, THI PWM scheme, renewable energy applications.**

I. Introduction

THREE-LEVEL voltage-source inverter (VSI) is more and more commonly seen in renewable power generation systems, although the two-level one still dominates the market [1]. Compared to the two-level VSI, the three-level VSI improves the quality of the output voltage with a lower total-harmonic-distortion (THD), in addition to halving the voltage stresses on power switches [2], [3].

For renewable energy applications, however, voltage boosting is usually necessary, since the output voltages of most renewable energy sources like the photovoltaic (PV) cells are relatively low. One straightforward solution is the cascaded connection of many dc sources (e.g., PV string), which may encounter mismatching problems, and thus, it becomes less reliable [4]. Another option is to use a front-end boost dc-dc converter [5], [6]. However, more switches with their accompanied gate-driver circuits are required. It inevitably complicates the control strategy and reduces the overall conversion efficiency. Alternatively, a single-stage boost-type VSI can be adopted, which, mostly for two-level operation, has been proven to be an effective strategy [7]–[9]. However, the traditional three-level inverters including the neutral-point-clamped (NPC) [10] and flying-capacitor (FC) inverters [11] perform only a voltage-buck conversion. It is, therefore, necessary to modify the overall circuit topologies and/or PWM schemes of the three-level inverters before a step-up voltage can be achieved through a single-stage power conversion [12]–[18].

Starting from the three-level NPC VSI, its voltage boosting is obtained by integrating a *Z*-source network [12]. The resultant *Z*-source NPC (*Z*-NPC) inverter, however, requires two isolated dc sources, each conditioned by a voltage boosting network using two inductors and two capacitors. The number of passive components is thus increased, which may also lead to higher power losses. Another *Z*-NPC inverter using a single dc source and with a reduced number of inductive components is latterly presented in [13] (Fig. 1(a)). Despite that, its capacitors need to withstand a high voltage nearly double that in [12]. Therefore, high voltage-rating devices are required as input diodes [13]. The discontinuous input current drawn by the input diodes may need additional dc-dc voltage stages for filtering, as discussed in [14].

Similarly, the three-level active NPC (ANPC) inverter can also be modified to perform the voltage-boost conversion [15], [16]. It, however, uses a large number of passive components [15], or additional switches [16]. One common feature of the aforementioned PWM inverters using *Z*-source networks is that the voltage-boost ratio counters the PWM ratio (or index), which presents a monotonically decreasing voltage gain, and results in an insufficient value under a high PWM ratio.

Other voltage boosting networks may also be considered as discussed in [17], [18]. An input inductor with three diodes is applied to a traditional three-phase two-level VSI, which consists of three half-bridge legs using 6 switches in total (commonly notated as Bridge-6 or simply B6 VSI) [19], forming a split-source (SS) inverter. A similar concept is applied to the three-level FC inverter, as shown in Fig. 1(b) [18]. The resultant flying-capacitor split-source (FC-SS) inverter produces a step-up dc-link voltage (V_{dc}), and subsequently a boosted output voltage. Additionally, it draws a continuous input current, which is more friendly to renewable

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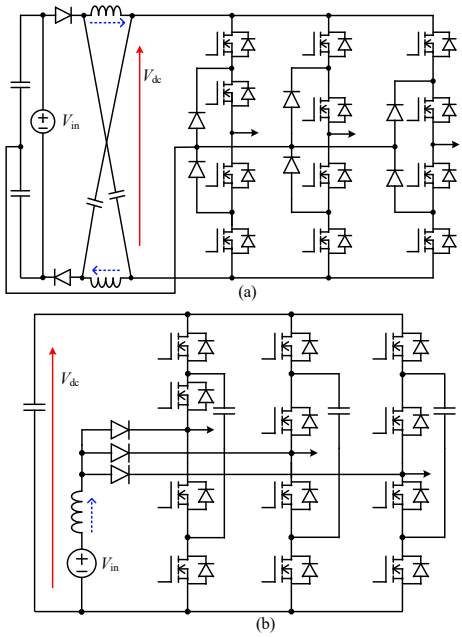

Fig. 1. The prior-art three-phase three-level (a) Z-NPC [13] and (b) FC-SS [18] inverters capable of producing a step-up ac voltage using a single dc source.

energy sources. However, a high PWM ratio necessitates a high voltage-boost ratio, which causes more conduction losses due to the charging and discharging currents of the inductor flowing through the high-voltage input diodes [17], [18]. Active switches may be used to bypass the diodes when they are forward biased, as discussed in [20]. Additionally, when the required dc-to-ac voltage conversion ratio is not very high for renewable energy applications [21], [22], a moderate voltage gain is usually preferred. Thus, the FC-SS inverter utilizes a moderate PWM ratio and to some extent, compromises the voltage utilization of the dc-link capacitor (V_{dc}).

Different from the (A)NPC and FC inverters, the three-level cascaded full-bridge (CHB) inverter can also produce a step-up line-to-line voltage without any circuit modifications. Nevertheless, its boosting capability is due to the use of multiple isolated dc sources. Moreover, the maximum line voltage is limited to $2V_{in}$. Modifications to the three-level CHB inverter using dual dc sources are recently developed in [23]–[25]. However, high voltages are induced on some of the switches [25].

Inferred from the above literature review, the conventional three-level inverters including the NPC, and FC inverters can be modified to perform voltage-boost conversion through a single stage without additional switches. However, their devices may suffer from high voltages, leading to high power losses. Furthermore, the voltage-boost ratio is either monotonically decreasing or increasing with the PWM ratio [13], [18]. A flexible voltage gain cannot be obtained once the PWM ratio is determined, and vice versa.

To tackle the aforementioned issues, this paper proposes a novel inductive-dc-link cascaded-half-bridge (abbreviated to "L-ChB") inverter, as shown in Fig. 2. The L-ChB inverter uses a B6 structure that is connected to the dc source via an input inductor L_{in}. Each leg of the B6 structure (using S_{x1} & S_{x2}, $x = a$, b, or c) is cascaded with a half-bridge (using S_{x3} & S_{x4}), assisted by a clamping diode D_x. The proposed L-ChB inverter has the following key features including:

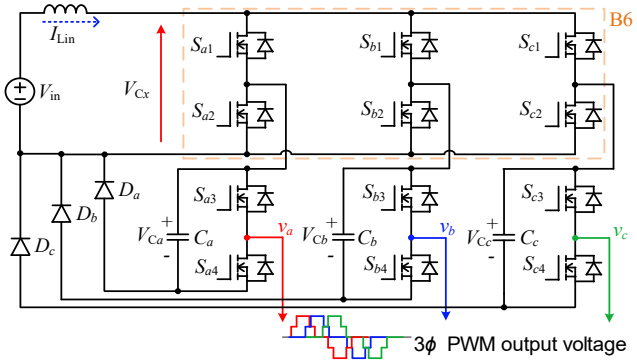

Fig. 2. Proposed three-phase (3ϕ) three-level inductive-dc-link cascaded-half-bridge (L-ChB) inverter producing a boosted PWM output voltage.

1) drawing a continuous input current suitable for renewable energy applications;
2) achieving low voltage stresses on the switches, diodes, and capacitors;
3) enabling a flexible voltage gain, particularly for the moderate voltage boosting;
4) reducing conduction losses caused by the inductor charging current.

The L-ChB inverter uses the same number of switches as that of the conventional three-level NPC or FC inverter. Different from the prior-art inverters shown in Fig. 1, the diodes D_a, D_b, and D_c are not stressed by high voltages. Neither do they conduct the charging current of the inductor, to be demonstrated in Section II, where a modified THI PWM scheme is introduced to obtain a flexible voltage gain. Section III presents detailed theoretical analyses, followed by a comparative study with the prior-art solutions and a design guideline for the main components in Section IV. Experimental results are given in Section V, and a conclusion is drawn in Section VI.

II. Operating Principle and Pulse-Width Modulation

A. Shoot-Through Voltage Boosting

For the conventional B6 VSI, it operates with eight possible switching states, where the switches S_{x1} and S_{x2} are driven complementarily to avoid the shoot-through problem [26]. In the proposed L-ChB inverter, however, due to the input inductor L_{in}, the bridge legs of the B6 structure make the most use of the shoot-through state to generate the inductor-charge duty ratio in each switching period (T_s). In the following, phase a of the L-ChB inverter is exemplified to illustrate the inductor-charge and -discharge operations as shown in Fig. 3.

Fig. 3(a) and (b) depict the inductor-charge operation by turning on both the switches S_{a1} and S_{a2}. During the charging state, the input inductor L_{in} is parallelly connected to the input dc source V_{in}. Thus, the diode D_a is reverse-biased by the capacitor C_a. For the switches S_{a3} and S_{a4}, their switching movements are independent of switches S_{a1} or S_{a2}. When the switch S_{a3} is turned on, while S_{a4} is turned off (Fig. 3(a)), the output terminal of phase a is clamped to the negative terminal of the dc source. Or else, the output voltage of phase a (v_a) is directly supplied by the capacitor V_{Ca} whenever S_{a3} is turned off and S_{a4} is on (Fig. 3(b)). Therefore, the voltage of the capacitor C_a should be replenished timely to maintain a steady value, which is achieved through the inductor-discharge operation.

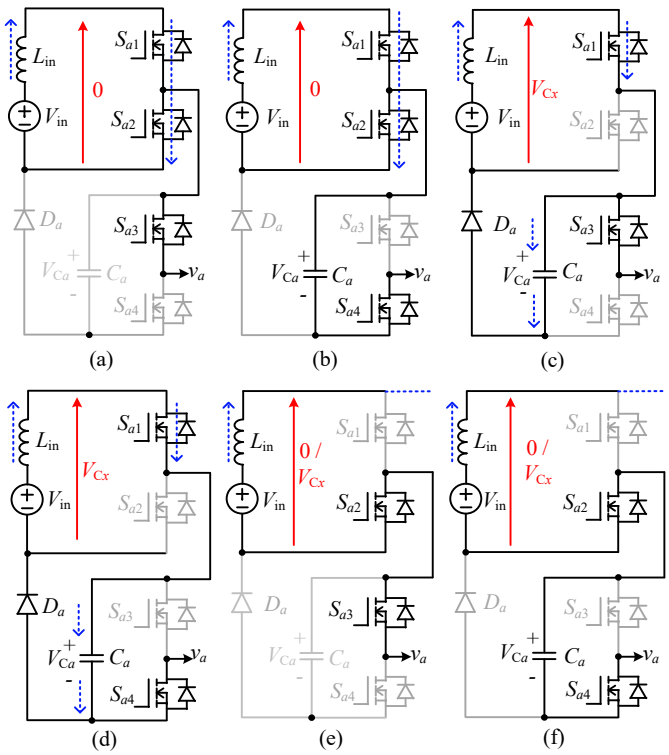

Fig. 3. Six possible equivalent states of phase a (same for b, or c) of the proposed L-ChB inverter with L_{in} (a), (b) charging and (c), (d) discharging through phase a; (e), (f) L_{in} charging/discharging through other phases (voltage across the inductive dc-link equal to 0 or V_{Cx} in all the states).

When the switch S_{a1} remains on, while S_{a2} is turned off, the inductor-discharge current flows through the capacitor C_a by freewheeling through the diode D_a, provided that the other two phases are not in the shoot-through state, as shown in Fig. 3(c) and (d). This is because if any phase is in the shoot-through operating mode, the diodes D_a, D_b, and D_c are reverse-biased and no currents are freewheeling through them. Meanwhile, if the switch S_{a3} is turned on while S_{a4} is off, the output voltage is supplied by the inductive dc-link, which is now connected to the capacitor C_a in parallel (Fig. 3(c)). Otherwise, the output terminal of phase a is clamped to the negative terminal of the dc source via the switch S_{a4} and diode D_a (Fig. 3(d)).

The other two states of phase a are shown in Fig. 3(e) and (f) with the switch S_{a1} being turned off, and thus L_{in} must be charged or discharged through phase b (or c). In either case, the average voltage across the inductor L_{in} remains as V_{in} or (V_{in} − V_{Cx}) since possible switching states of each phase have already been defined by the six equivalent states in Fig. 3. It also indicates that the capacitor C_x is charged by the input dc source in series with the input inductor, thereby maintaining a steady V_{Cx}. Among the three capacitors, the voltage balancing scheme is further elaborated as follows.

Inferred from Fig. 3, the inductor discharging current is able to flow through multiple phases during the non-shoot-through operating state. For instance, when any two of the switches (e.g., S_{a1} and S_{b1}) are turned on. It involves two possible inductor-discharge loops, in which two capacitors can be charged at the same time. Assuming that at the beginning the voltages across capacitors are equal (V_{Ca} = V_{Cb}), the inductor, therefore, discharges through two phases by freewheeling through diodes D_a and D_b, maintaining a balanced voltage for the two capacitors. If their voltages are unequal (e.g., V_{Ca} < V_{Cb}), instead of flowing through both diodes, the inductor current flows through the diode D_a, and thus, the lower-voltage capacitor C_a is getting charged. Therefore, the voltage V_{Ca} will be replenished timely and after some duration, V_{Ca} = V_{Cb} is maintained. The same analysis can be applied when switches S_{a1}, S_{b1}, and S_{c1} are all turned on during the non-shoot-through operating state.

Therefore, it can be concluded that even though the instantaneous voltages of the capacitors may be varying due to the sinusoidal phase currents, the voltages across the capacitors remain close to each other, with a common average value (V_{Cx}). Furthermore, such a voltage balancing scheme applies to the unbalanced loading condition, where the capacitor C_x can present a higher voltage ripple if phase x draws a higher current $i_{\phi x}$. Nevertheless, the average voltages of the capacitors maintain balanced without deteriorating operations of the L-ChB inverter, to be demonstrated experimentally.

With balanced voltages across the capacitors, the average discharging voltage of the inductor is equal to (V_{in} − V_{Cx}) during the non-shoot-through state, while its charging voltage is given by the input voltage V_{in} during the shoot-through state. Applying the volt-second balance to the input inductor, the following equation is obtained.

$$V_{in}\bar{d}_{st}T_s + (V_{in} - V_{Cx})(1 - \bar{d}_{st})T_s = 0 \quad (1)$$

where $\bar{d}_{st}$ is the average shoot-through duty ratio within a switching period T_s. Subsequently, the voltage V_{Cx} can be found and expressed as

$$V_{Cx} = V_{in}/(1 - \bar{d}_{st}) \quad (2)$$

which implies that a step-up voltage across the capacitor C_x is obtained with a boosting factor of $1/(1-\bar{d}_{st})$.

It should be noticed that V_{Cx} is the average voltage across the capacitor C_x. The validity of Eqs. (1) and (2) is not affected by the discharging current of the inductor flowing through any capacitors of the three phases. The voltage-boost capability of the L-ChB inverter, therefore, remains the same when operating under a balanced or unbalanced loading condition.

Undoubtedly, to keep the capacitors' voltages balanced and realize the targeted voltage gain, appropriate charging and discharging states of the input inductor need to be created. Besides, the proposed L-ChB inverter should be able to produce a three-level output voltage. For illustration, a carrier-based PWM scheme is considered to achieve all the functionalities.

B. Modified THI PWM Scheme

The key modulation signals and the carrier of the THI PWM technique are shown in Fig. 4. When it is used for the conventional PWM inverters, the THI modulation signal V_{refx1} is compared with the per-unit (pu) triangular carrier V_{tri} to generate gating signals for the switch S_{x1} [26]. The witch S_{x2} is driven complementarily with S_{x1}. Such a standard PWM strategy, however, does not support shoot-through operation, and it needs to be modified before it applies to the proposed L-ChB inverter.

In principle, the shoot-through operation can be inserted in any half-bridge legs of the B6 structure by turning on both switches S_{x1} and S_{x2} within the same leg. Unavoidably, the charging current of the inductor flows through the turn-on

switches, increasing the conduction losses. With this in view and aiming at reducing the conduction losses of the switches, the inductor-charge state is initiated by concurrently shooting through the three half-bridge legs, which means the charging current of the inductor can be divided equally by and then flow through them. Therefore, the shoot-through inductor-charge state is implemented in such a way that the switches S_{a2}, S_{b2}, and S_{c2} are turned on whenever the carrier is less than or equal to the lower envelope ($V_{\rm dn}$, in bold line in Fig. 4) formed by the three modulation signals, i.e., $V_{\rm tri} \le V_{\rm dn}$. Note that the switches S_{a1}, S_{b1}, and S_{c1} are all turned on in this state.

Another criterion for the PWM scheme is that at least one of the switches S_{a1}, S_{b1}, and S_{c1} should be turned on at any instant to avoid disrupting the inductor current. Similarly, this can be achieved in such a way that all the switches S_{a1}, S_{b1}, and S_{c1} are turned on whenever the carrier is greater than or equal to the upper envelope ($V_{\rm up}$, in bold line in Fig. 4) formed by the three modulation signals, i.e., $V_{\rm tri} \ge V_{\rm up}$. Also, note that the switches S_{a2}, S_{b2}, and S_{c2} are also turned on in this state.

With the above modifications, the gating signals for the switches S_{a1}, S_{b1}, and S_{c1} are depicted in Fig. 4(a). It is evident that at least one of the switches S_{a1}, S_{b1}, and S_{c1} remains on without switching in each carrier period. Moreover, S_{x1} presents a continuous turn-on duration in a fundamental cycle, where the "always-on" duration is highlighted with a distinct color. At the upper intersections of any two modulation signals (e.g., V_{refa1} and V_{refc1}), the two corresponding switches (S_{a1} and S_{c1}) are both turned on, which means an overlapped turn-on duration between any two of the switches S_{a1}, S_{b1}, and S_{c1} is ensured. Therefore, interrupting the inductor current is prohibited. Moreover, there are two shoot-through durations generated in every carrier period. The equivalent charging frequency of the inductor is doubled, thus, reducing the input current ripple.

For the three cascaded half-bridges consisting of switches S_{x3} and S_{x4}, the standard PWM scheme can be applied, as shown in Fig. 4(b). The same carrier $V_{\rm tri}$ has been used, while the modulation signal V_{refx3} which is in 180° phase-shift with V_{refx1} is used to generate the gating signal for switch S_{x3}. And the switch S_{x4} is driven complementarily to S_{x3}.

For an easy reference, the equivalent circuit of the shoot-through operating state is shown in Fig. 5(a), where the inductor charging current is split into three sub-charging currents (I_{ina}, I_{inb}, and I_{inc}) flowing through the three bridge legs concurrently. Assuming that the on-state resistances of the bridge legs are equal, the equality of the three sub-charging currents exists ($I_{ina} = I_{inb} = I_{inc}$) under a balanced or unbalanced loading condition. The switches S_{x1}–S_{x4}, however, indeed present different current stresses with an unbalanced three-phase load, since they conduct both the inductor current and phase current.

Additionally, one possible inductor-discharge state is shown in Fig. 5(b), where the inductor can discharge to two capacitors to balanced their voltages as discussed in the previous subsection. As can be seen, when in the inductor-charge state (Fig. 5(a)), possible line-to-line output voltages of the L-ChB inverter are 0 and ± V_{Cx}. While in the inductor-discharge state (Fig. 5(b)), possible line-to-line output voltages are 0, ±V_{Cx}, and ±2V_{Cx}. Therefore, a three-phase three-level step-up output voltage is facilitated by the modified THI PWM scheme.

With the operating states and PWM scheme of the L-ChB inverter being discussed, it is worth mentioning that the

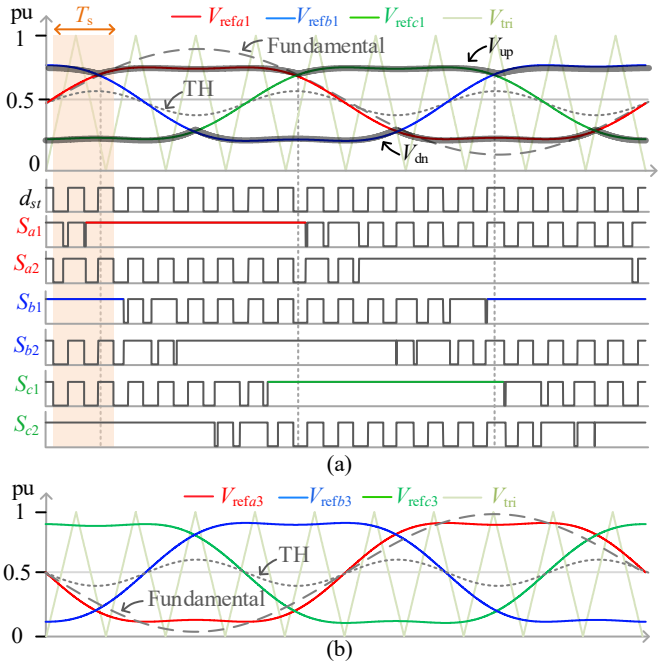

Fig. 4. Illustrations of (a) the modified THI PWM scheme for switches S_{x1} and S_{x2}, and (b) the THI PWM scheme for switches S_{x3} and S_{x4} (amplitudes of the fundamental components of V_{refx1} and V_{refx3} can be equal or unequal).

boosting voltage and continuous input current achieved through the inductive dc-link resemble those of the conventional current-type (source) inverter. For a current-type inverter, however, the phase current is defined directly by the input current (PWM current), which means the output voltage depends on the loading resistance. Unlike the current-type inverter, however, the output voltage of the L-ChB inverter is defined (PWM voltage), which is independent of the loading resistance. From this point of view, the L-ChB inverter, therefore, is a voltage-type inverter, which produces a relatively high dv/dt at the output and requires inductive (L_f) rather than capacitive output filters.

Nonetheless, like a current-type inverter, the inductor current is not allowed to be interrupted. And a large input inductor may be required to reduce the input current ripple, which increases the inverter size and volume. Another concern is that the PWM schemes for the conventional three-level voltage-type inverters may not apply to the proposed L-ChB inverter if without proper modifications as discussed previously. Other features of the proposed L-ChB inverter including the voltage/current ratings of the semiconductor devices and power losses of the components are indeed different from the prior-art inverters, as analyzed and compared in the later sections.

III. Theoretical Analysis of The L-ChB Inverter

A. Voltage-Boost Ratio

The modulation signal V_{refa1} consisting of the fundamental component and its third harmonic (TH) can be expressed as

$$V_{refa1} = \frac{1}{2}[M_{ac1}\sin(2\pi f_l t) + M_{th1}\sin(6\pi f_l t)] + \frac{1}{2} \quad (3)$$

where M_{ac1} and M_{th1} are peak-to-peak amplitudes of the fundamental component and TH, respectively; f_l is the fundamental frequency.

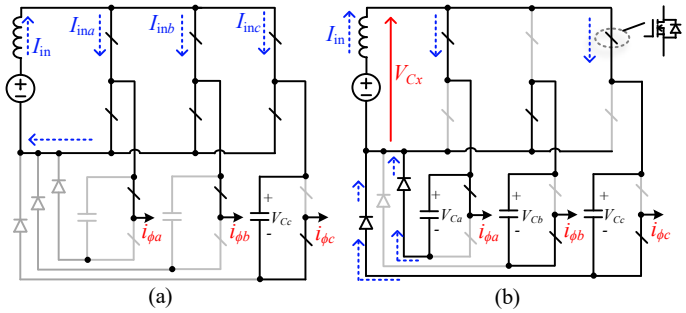

Fig. 5. Equivalent (a) inductor-charge state with three sub-charging currents (I_{ina}, I_{inb}, and I_{inc}), and (b) one possible inductor-discharge state with switches S_{a1} and S_{c1} turned on (component symbols referred to Fig. 2).

The average value of the upper envelope formed by the three modulation signals can then be calculated by

$$V_{\text{up\_avg}} = 3f_l \int_{1/(12f_l)}^{5/(12f_l)} V_{\text{refa1}}\, dt = 0.5 + \frac{3\sqrt{3}}{4\pi} M_{ac1} \quad (4)$$

from which, the average shoot-through duty ratio is found as

$$\bar{d}_{\text{st}} = 2\left(1 - V_{\text{up\_avg}}\right) = 1 - \frac{3\sqrt{3}}{2\pi} M_{ac1} \quad (5)$$

Note that the instantaneously shoot-through duty ratio (d_{st}) is essentially time-varying due to the fluctuations of the envelopes of the modulation signals (see Fig. 4(a)).

Using (2) and (5), the average value of the capacitor voltage is expressed as

$$V_{Cx} = \frac{2\pi V_{\text{in}}}{3\sqrt{3} M_{ac1}} \quad (6)$$

Consequently, the peak value of the line-to-line voltage of the L-ChB inverter is expressed as

$$V_{\text{lpk}} = \frac{\sqrt{3} V_{Cx}}{2} (M_{ac1} + M_{ac3}) = \frac{\pi}{3} (1 + \frac{M_{ac3}}{M_{ac1}}) V_{\text{in}} \quad (7)$$

where M_{ac3} is the peak-to-peak amplitude of the fundamental component of the modulation signal V_{refx3}, which can be equal or unequal to M_{ac1} (see Fig. 4(b)).

The dc-to-ac voltage gain of the L-ChB inverter is thus expressed as

$$G_{ac} = \frac{V_{\text{lpk}}}{V_{\text{in}}} = \frac{\pi}{3} (1 + \frac{M_{ac3}}{M_{ac1}}) \approx (1 + \frac{M_{ac3}}{M_{ac1}}) \quad (8)$$

It should, however, be mentioned that the TH does not appear in the line-to-line voltage according to Eqs. (7) and (8). Though the ratio between amplitudes of the TH and fundamental component (e.g., $\sigma = M_{\text{th1}}/M_{ac1}$) is usually selected within a certain fraction [26], it does not affect the range of the voltage gain. For instance, when the modulation variable M_{ac1} is varied to achieve a flexible voltage gain, the proportion of the injected TH can then remain the same by keeping a constant σ.

It is inferred from Eq. (8) that the waveforms of the modulation signals do not affect the flexibility of the voltage gain, either. Different types of modulation references (THI or/and sinusoidal waves) can be used for V_{refx1} and V_{refx3} at the same time. Notably, the THI modulation signals used for V_{refx1} reduce the fluctuation of the shoot-through duty ratio and thus reduce the input current ripple. Furthermore, the use of THI modulation signals for V_{refx3} increases the utilization of capacitor voltage (V_{Cx}).

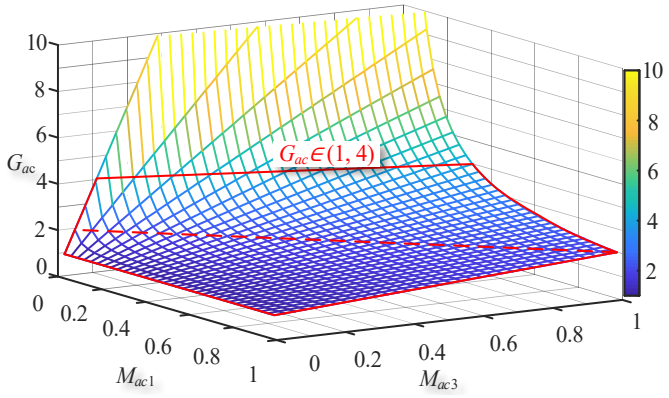

Fig. 6. A flexible gain surface enabled by two independent variables M_{ac1} and M_{ac3} (red dashed line for G_{ac} of 2 when $M_{ac1} = M_{ac3}$).

Based on (8), the voltage gain of the L-ChB inverter versus the two modulation variables M_{ac1} and M_{ac3} is plotted in Fig. 6. Due to the cascaded structure of each phase, the two modulation variables M_{ac1} and M_{ac3} are independent of each other, leading to a flexible three-dimensional gain surface. It can be seen that there are various combinations of M_{ac1} and M_{ac3} that can produce the same voltage gain. In particular, the moderate voltage boosting gain in the range of $(1, 4)$ takes up a wide range of surface. Furthermore, when both variables are equal, a constant voltage gain of 2 is obtained. Such a characteristic is rarely seen in the existing boost inverters, which is further discussed through a comparative study in Section IV.

B. Voltage and Current Ratings

Referring to Fig. 3, the voltage stresses (V_{ds}) of the switches are equal to V_{Cx}. Likewise, the diodes must be clamped by the capacitor C_x when they are reverse-biased, and their voltage stresses (V_{d}) are equal to V_{Cx}. That is, the voltage stresses on the semiconductor devices are expressed as

$$V_{\text{ds}} = V_{\text{d}} = V_{Cx} = \frac{2V_{\text{lpk}}}{\sqrt{3}(M_{ac1}+M_{ac3})} \quad (9)$$

While a uniform voltage stress is induced on the switches, the currents flow through them are not equal. The switches S_{x1} and S_{x2} conduct both the input current (I_{in}) and phase current (notated as $i_{\phi x}$, rms $I_{\phi x}$). Their current stresses are larger. As for the switches (S_{x3} and S_{x4}) used in the cascaded half-bridges, they conduct the phase current only and therefore their maximum currents are smaller. Additionally, it should be mentioned that the current stresses of the switches in different phases (e.g., S_{a1}, S_{b1}, and S_{c1}) are unequal under an unbalanced loading condition.

C. Power Losses

The conduction losses are mainly caused by the parasitic resistances of the inductor (r_{L}), the equivalent-series-resistances (ESRs) of capacitors (r_{Cx}), on-state resistances of switches (R_{on}), and the forward voltages of the clamping diodes (V_{Fd}). Assuming that the L-ChB inverter is supplying a balanced three-phase load, the power losses of each phase are regarded as the same.

The input inductor carries the input current (I_{in}). Its conduction loss is calculated with

$$P_{\text{Lcon}} = {I_{\text{in}}}^2 r_{\text{L}} \quad (10)$$

For analyzing the magnetic-core loss of the input inductor, the core loss density (P_{mc}) is used and it is regarded as a function of the flux (B) swing and operating frequency (f_s), expressed as [27]

$$P_{mc} = \lambda[(B_{max} - B_{min})/2]^{\alpha}(f_s)^{\beta} \quad (11)$$

where constants λ, α, and β are determined by curving fitting or formula specific in [28].

Furthermore, it is reported that the flux density is a non-linear function of the magnetizing field (H). Their relationship can be expressed as

$$B = [(e + fH + gH^2)/(1 + pH + qH^2)]^k \quad (12)$$

in which the constants e, f, g, p, q, and k are parameters used for BH-curve fitting [28].

Therefore, the maximum and minimum flux densities (B_{max} and B_{min}) are calculated by finding the H_{max} and H_{min}, respectively. Since H is related to the input current I_{in}, its maximum and minimum values can be respectively calculated by $H_{max} = (NI_{inmax})/L_e$, and $H_{min} = (NI_{inmin})/L_e$, with N being the number of the winding turns of the inductor and L_e the effective path length of the core. Using Eqs. (11), (12) and considering the specifications related to a toroid core 0077617A7 (*Magnetic Inc.*), the core loss is evaluated under a varied operating frequency with results shown in Fig. 7(a). As seen, both the conduction and core losses of L_{in} increase as P_o rises, which is expected since the input current increases. Besides, a higher core loss is caused by a higher frequency, while it becomes less significant as the frequency reduces.

The switches S_{x3} and S_{x4} conduct only the phase current, their conduction losses are calculated as

$$P_{sx3} = P_{sx4} = \frac{1}{2} I_{\phi x}{}^2 R_{on} \quad (13)$$

where the power switches are assumed to have the same R_{on}.

For switches S_{x1} and S_{x2}, they conduct both the input current (dc) and the phase current (ac), the instantaneous currents flowing through them are time-varying in different operating states or under different operating powers. To avoid complicating the analysis, the average currents of the switches during a fundamental cycle are used to evaluate their conduction losses. Considering that the input current (I_{in}) should be several times larger than the rms phase current ($I_{\phi x}$), the effect of the phase current resulting in an ac ripple on the currents flowing through S_{x1} and S_{x2} can then be nullified for calculating the average values over a fundamental cycle. Under the modified THI PWM, it is estimated that the switch S_{x1} conducts one-third of the average charging current of the inductor ($1/3I_{in}$) during the shoot-through state and half of the average discharging current of the inductor during the non-shoot-through state ($1/2I_{in}$). For the entire operating range under different output power, the relationships between the average currents hold. Furthermore, since every switching period (T_s) is divided into shoot-through and non-shoot-through states, the conduction loss of S_{x1} is calculated by

$$P_{sx1} = (\frac{1}{3} I_{in})^2 R_{on} \bar{d}_{st} + \left(\frac{1}{2} I_{in}\right)^2 R_{on}(1 - \bar{d}_{st}) \quad (14)$$

Similarly, the conduction loss of the switch S_{x2} is calculated by

$$P_{sx2} = (\frac{1}{3} I_{in})^2 R_{on} \bar{d}_{st} \quad (15)$$

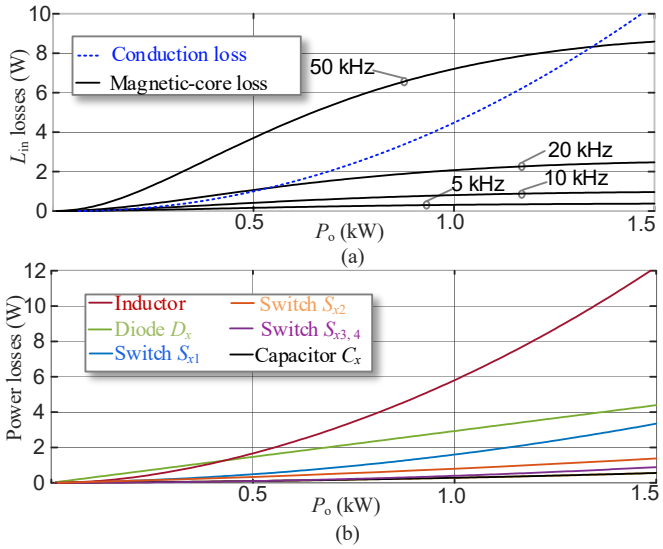

Fig. 7. Theoretical (a) conduction and core losses of the input inductor L_{in} with a varied operating frequency, and (b) power losses of phase x versus P_o considering specifications of the experiment prototype (*APT40M70LVR*/*VS30APF04M3* for switch/diode; assumed $r_L = 0.05\Omega$, and $r_{Cx} = 0.08\Omega$; $V_{in} = 100$ V, $V_{lpk} = 300$ V; switching frequency 10 kHz;).

The switching losses of a switch S_x is expressed as

$$P_{swx} = \frac{1}{2T_s} I_{ds} V_{ds} (t_r + t_f) \quad (16)$$

where t_r and t_f are the turn-on and turn-off durations of each switch; I_{ds} is the current flowing through the switch during the switching movements. For estimation, I_{ds} for switches S_{x3} and S_{x4} is approximated by the maximum phase current, while I_{ds} for switches S_{x1} and S_{x2} can be regarded as I_{in}.

Since the diode D_x is turned on during the inductor-discharge state, its conduction loss is calculated by

$$P_{dx} = \frac{1}{2} I_{in} V_{Fd} (1 - \bar{d}_{st}) \quad (17)$$

The reverse-recovery of the diode D_x is given as

$$P_{drrx} = \frac{1}{2} V_d Q_{rrx} f_s \quad (18)$$

where Q_{rrx} is the reverse-recovery charge of the diode D_x.

For the capacitor C_x, assuming its voltage is maintained at a steady value coupled with a small ac ripple caused by the sinusoidal phase current, the rms current of the capacitor during a fundamental cycle is thus approximated as the phase current. Therefore, the conduction loss of the capacitor C_x is obtained as

$$P_c = I_{\phi}{}^2 r_{cx} \quad (19)$$

With the above considerations, power losses of the L-ChB inverter are evaluated and shown in Fig. 7(b) considering the devices and specifications used in the experiment. It can be seen that the loss caused by the input inductor is the highest among all the losses. As for the switches, S_{x1} and S_{x2} take up the most power losses while S_{x3} and S_{x4} account for a small proportion of the overall loss. The total power loss of the L-ChB inverter (output filter not considered) evaluated at 1 kW is 25.3 W, giving rise to the theoretical efficiency of 97.53%, which, together with other performances is compared with the prior-art three-level boost inverters in the next section.

IV. Comparision and Design Considerations

A. Comparison with Three-Level Boost Inverters

The proposed L-ChB inverter is compared with the three-level Z-NPC [13], FC-SS [18] inverters, and a two-stage inverter formed by cascading a front-end boost dc-dc converter with a rear-end three-level NPC inverter, as shown in Table I.

In terms of the semiconductor devices, the L-ChB inverter uses the same number of switches (N_s) as those of the Z-NPC, FC-SS inverters [13], [18]. The switch count is less than that of the two-stage inverter. In addition, the number of diodes (N_d) required by the L-ChB inverter is low, equal to that of the FC-SS inverter [18]. A large number of diodes is required by the Z-NPC inverter [13]. Except for the two-stage inverter, all the inverters feature a uniform voltage stress on the switches. The normalized total voltage stress (TVS) of the semiconductor devices with respect to the peak line voltage V_{lpk} of each inverter is expressed as

$$\mathrm{TVS} = (V_{ds} \times N_s + V_d \times N_d)/V_{lpk} \tag{20}$$

The calculated TVS of each inverter can then be plotted and compared in Fig. 8. The PWM ratio M is defined as [26]

$$M = V_{\phi max}/(0.5V_{dc}) \tag{21}$$

where $V_{\phi max}$ is the maximum fundamental component of the phase voltage. For the L-ChB inverter, an average PWM ratio is considered as $M = (M_{ac1} + M_{ac3})/2$. As seen from Fig. 8, the TVS curve of each inverter exhibits a similar trend, which decreases as M is increased. The TVSs of the single-stage inverters are all smaller than that of the two-stage structure under the same PWM ratio. Among the single-stage inverters, the TVS of the L-ChB inverter is smaller than those of the Z-NPC and FC-SS inverters [13], [18].

The voltage gains versus M of the single-stage inverters are likewise compared in Fig. 9. Only the range of $M \in (0.5, 1)$ is considered for voltage boosting. An immediate observation from Fig. 9 is that a flexible voltage gain is obtained by the L-ChB inverter with different combinations of the two modulation variables M_{ac1} and M_{ac3}. For instance, when keeping M_{ac1} at unity, the gain curve rises linearly as M increases. Whereas, the gain decreases as M increases if M_{ac3} is maintained at unity. In particular, when M_{ac1} and M_{ac3} are equalized, a constant voltage gain of ≈2 is obtained irrespective of M. Therefore, it offers more flexibility in choosing a specific gain value even with the same PWM ratio M, especially for producing a moderate value ($1 < G_{ac} < 4$) that is suitable for renewable energy applications, as discussed in [21] and [22]. When a large voltage gain is required, the L-ChB and Z-NPC inverters use a smaller M. While, the FC-SS inverter uses a larger M since its voltage gain is monotonically increasing. Its gain curve, therefore, resembles that of a boost converter which produces an extreme value as M approaches unity. However, a large inductor-charge duty ratio is applied, which increases power losses [18].

Additionally, it is worth thinking that the carrier-based PWM schemes using different modulation signals applied to the Z-NPC, and FC-SS inverters may result in varied voltage gains. And it is straightforward that the THI or sinusoidal waveforms can be considered as the modulation signals for them, which is not vividly shown here. But it will not reverse the trends of the obtainable voltage gains of the Z-NPC, and FC-SS inverters in comparison with that of the L-ChB inverter.

A case-study example is provided to compare the efficiencies (η) of the inverters through simulations. All the inverters are assumed to be supplied by a 100-V dc source to produce a three-phase output voltage with the line-to-line amplitude of 300 V. The same kind of devices (*APT40M70LVR*/*VS30PF0M3*) is considered for all the inverter topologies to observe the losses of the switches/diodes. Similarly, the same parasitic resistance ($r_L = 0.05\ \Omega$) or ESR ($r_C = 0.08\ \Omega$) is assumed for each inductor or capacitor in different topologies. The simulated efficiency of

Table I. Comparison with Three-Level Boost Inverters Using A Single DC Source

Three-level inverters		Z-NPC [13]	FC-SS [18]	Proposed L-ChB	Two-stage (Boost + NPC)
Switches	Count N_s	12	12	12	13
	Total V_{ds}	$\frac{V_{lpk}}{\sqrt{3}M} \times 12$	$\frac{V_{lpk}}{\sqrt{3}M} \times 12$	$\frac{2V_{lpk}}{\sqrt{3}(M_{ac1}+M_{ac3})} \times 12$	$\frac{V_{lpk}}{\sqrt{3}M} \times 12$; $\frac{2V_{lpk}}{\sqrt{3}M} \times 1$
	Max. I_{ds}	$(I_{inmax} + I_{\phi max}) \times 12$	$(I_{inmax} + I_{\phi max}) \times 12$	$(I_{inmax} + I_{\phi max}) \times 6$; $I_{\phi max} \times 6$	$I_{\phi max} \times 12$; $I_{inmax} \times 1$
Diodes	Count N_d	8	3	3	7
	Total V_d	$\frac{V_{lpk}}{\sqrt{3}M} \times 8$	$\frac{2V_{lpk}}{\sqrt{3}M} \times 3$	$\frac{2V_{lpk}}{\sqrt{3}(M_{ac1}+M_{ac3})} \times 3$	$\frac{V_{lpk}}{\sqrt{3}M} \times 6$; $\frac{2V_{lpk}}{\sqrt{3}M} \times 1$
	Max. I_d	$I_{inmax} \times 2$; $I_{\phi max} \times 6$	$I_{inmax} \times 3$	$I_{inmax} \times 3$	$I_{\phi max} \times 6$; $I_{inmax} \times 1$
Capacitors	Count N_C	4	4	3	2
	Total V_C	$\frac{(2M)V_{lpk}}{1-M} \times 2$; $\frac{(2M-1)V_{lpk}}{2(1-M)} \times 2$	$\frac{2V_{lpk}}{\sqrt{3}M} \times 1$; $\frac{V_{lpk}}{\sqrt{3}M} \times 3$	$\frac{2V_{lpk}}{\sqrt{3}(M_{ac1}+M_{ac3})} \times 3$	$\frac{V_{lpk}}{\sqrt{3}M} \times 2$
	Capacitances	Large	Medium	Large	Medium
Inductors	Count N_L	2	1	1	1
	Frequency	High ($2/T_s$)	High ($2/T_s$)	High ($2/T_s$)	High (independent)
Theoretical G_{ac} (V_{lpk}/V_{in})		$\sqrt{3}M/[2(2M\text{-}1)]$	$\sqrt{3}M/[2(1\text{-}M)]$	$\pi/3(1+M_{ac3}/M_{ac1})$	$\sqrt{3}M/[2(1\text{-d})]$
G_{ac} used for prototype		1.73	3	3	/
Simulated η (1 kW)		94.3%	96.0%	97.53%	96.51%

Notes: $d \in (0,1)$ is the independent duty ratio for the boost converter of the two-stage structure. "/" means not applicable.

Table II. Comparison of the Number of Devices in the Current Flowing Paths

Inverter	Inductor-current flowing path (charge)				Inductor-current flowing paths (discharge)				Phase-current flowing paths (per phase)		
	N_L	N_s	N_d	N_C	N_L	N_s	N_d	N_C	N_s	N_d	N_C
Z-NPC [13]*	1	4	0	1	1	0	2	1	2 (or 1)	0 (or 1)	0
FC-SS [18]	1	2	1	0	1	2	1	1(or 2)	2	0	0 (or 1 or 2)
L-ChB	1	2	0	0	1	1	1	1	2 (or 1)	0 (or 1)	0 (or 1)
2-stage	1	1	0	0	1	0	1	2	2 (or 1)	0 (or 1)	0

*: two input inductors result in two inductor-charge and -discharge currents, respectively.

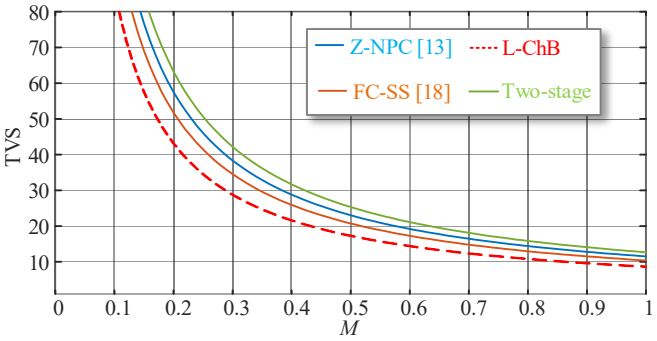

Fig. 8. Comparison of TVS versus PWM ratio M of three-level inverters.

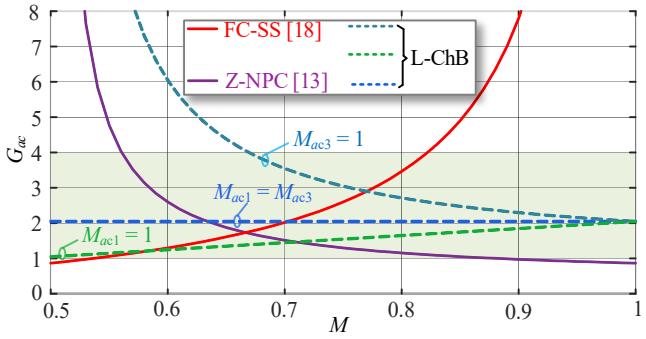

Fig. 9. Comparison of G_{ac} versus PWM ratio M of the single-stage inverters.

each inverter under operating power of 1 kW is exemplified and entered into Table I.

As seen in the last column of Table I, the L-ChB inverter achieves the highest efficiency compared to its counterparts. The FC-SS inverter and the two-stage inverter present a similar efficiency, which is slightly lower than the L-ChB inverter. The Z-NPC inverter achieves the lowest efficiency. This is because the Z-NPC inverter uses two inductors at the input-side circuit, both with average currents being I_{in}, which in addition to causing higher conduction losses on the two input diodes, increases the total loss of the inductors. Similarly, the input diodes of the FC-SS inverter are suffered from higher reverse-recovery losses due to the higher peak-inverse voltage. For the two-stage inverter, high power losses are induced on the boost switch and diode of the front-end stage. Especially a high-voltage (> 400 V) switch/diode should be considered for the front-end boost stage in practice, which may further degrade the efficiency of the two-stage inverter.

The efficiency performances of the inverters can also be interpreted by considering the number of the devices in the current flowing paths since conduction losses of the devices commonly take up a large proportion of the overall loss. For the aforementioned boost inverters, there must exist the inductor-current paths for boosting the dc voltage, and the phase-current paths. Through studying the operating states of the compared inverters [13], [18], the numbers of the devices in the mentioned current flowing paths are listed and compared in Table II. As seen, for the Z-NPC inverter, the inductor charging current must flow through four switches in series, whose total on-state resistance is thus $4R_{on}$ [13]. Likewise, the inductor charging currents of the FC-SS inverter flow through one input diode and two switches, inducing a considerably large conduction loss [18]. Two switches (S_{x1} and S_{x2}) in each phase of the L-ChB inverter are in series to conduct the inductor charging current which is divided into three sub-charging currents as discussed in Section II.B. The conduction losses of switches are thus reduced. Similar comparisons can be made for the inductor-discharge currents. As for the two-stage inverter using two additional semiconductor devices, its inductor-current flowing paths include the fewest components.

Since each phase of the compared inverters uses four switches, which can be separated into two pairs when conducting the phase current, the number of the semiconductor devices involved in the phase-current flowing path of each inverter is thus two (2 switches, or 1 switch with 1 clamping diode). It is, therefore, expected that the conduction losses caused by the phase currents are at a similar level. Whereas, conduction losses caused by charging/discharging the input inductor dominate due to the relatively high input current.

Such results agree with the efficiency comparison in Table I, confirming again the advantage of the L-ChB inverter in using low-voltage devices (switches, diodes, and capacitors) and reducing the conduction losses caused by the input inductor. Besides, it offers more flexibility in voltage boosting, especially when producing a moderate voltage gain. However, due to the cascading feature, the capacitor C_x features a low-frequency ripple, which usually requires a large capacitance. Furthermore, since the current ripple of the input inductor needs to be kept small to remain in the continuous conduction mode, the L-ChB inverter requires a careful design and selection of its devices.

B. Design Considerations

The selections of the switches and diodes are based on their voltages and current ratings, which can be found in Table I, where the voltage rating of the capacitor C_x is also given. As for the capacitance, its value should be chosen larger to reduce the voltage ripple as discussed in the following.

Under the THI PWM scheme presented in Section II.B, the inductor-charge duty ratio is inserted in each switching period when $V_{tri} \geq V_{up}$ or $V_{tri} \leq V_{dn}$, the inductor-discharge duty ratio is thus created when $V_{dn} < V_{tri} < V_{up}$. Referring to Fig. 4(a), the inductor does not discharge through phase x when the modulation signal V_{refx1} is equal to the lower envelope V_{dn}. Therefore, in this duration $(1/(3f_l))$, the capacitor C_x keeps supplying the output with its voltage decreasing. The voltage drop of the capacitor is calculated by

$$\Delta V_{Cx} = \frac{1}{C_x}\int_{7/(12f_l)}^{11/(12f_l)} i_{\phi x}\, dt \tag{22}$$

Assuming the voltage ripple $\Delta V_{Cx}/2$ less than 5% of V_{Cx}, and using (22), the capacitance C_x should fulfill

$$C_x \geq 10V_{Cx}\int_{7/(12f_l)}^{11/(12f_l)} i_{\phi x}\, dt \tag{23}$$

Similarly, the required input inductance is calculated based on the requirement of the input current ripple. Since there are two charging durations within a switching period, the inductor current increases continuously during $(0, \bar{d}_{st}T_s/2)$, which can be formulated as

$$\Delta I_{Lin} = \frac{V_{in}\bar{d}_{st}T_s}{2L_{in}} \tag{24}$$

Assuming a small current ripple, e.g., $\Delta I_{Lin}/2 \leq 20\% I_{Lin}$, the input inductance is thus selected according to

$$L_{in} \geq \frac{5V_{\text{in}}\bar{d}_{\text{st}}T_{\text{s}}}{4I_{\text{Lin}}} \quad (25)$$

With the above considerations, the reactive components used in the experiment are C_x = 1 mF, and L_{in} = 1 mH for prototyping the L-ChB inverter.

V. Experimental Results

To verify the feasibility of the proposed L-ChB inverter, an inverter prototype is built using the component listed in Table III. The input of the inverter is supplied by a constant dc source, while its output supplies a three-phase *RL* load arranged in *Y* connection (see Fig. 10). Each output is connected with a filter inductor (L_f = 1.5mH). The THI PWM scheme is implemented on a digital signal processor and the carrier frequency used is 10 kHz. During the steady-state experimental test, the modulation variable M_{ac1} is set at 0.5, while M_{ac3} is 1.

TABLE III. Specifications of the L-ChB Inverter Prototype

Specifications	Values
Voltage ratings	V_{in} = 100 V; V_{lpk} = 290 V, 50 Hz, 1.5 kVA
PWM variables	M_{ac1} = 0.5, M_{ac3} =1; σ = 1/6; $1/T_s$ = 10 kHz
Switches	*APT40M70LVR* (400 V, 57 A, R_{on} = 0.07 Ω)
Diodes	*VS-30APF04-M3* (400 V, 30 A, V_{Fd} = 1.41 V)
Inductors	L_{in} = 1 mH ($r_{\text{L}} \approx$ 0.05 Ω); L_f = 1.5 mH
Capacitors	$C_a = C_b = C_c$ = 1mF ($r_c \approx$ 0.08 Ω)

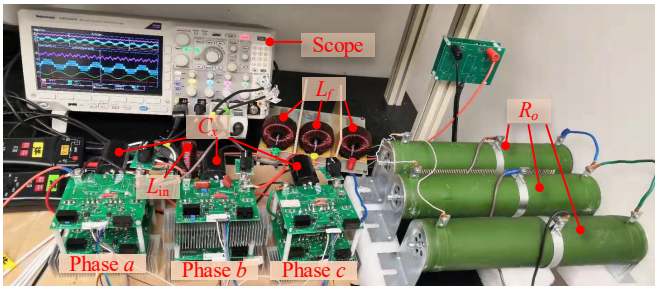

Fig. 10. Photograph of the L-ChB inverter prototype.

A. Experimental Steady-State Operation

To examine the PWM strategy presented in Section II.B, the gating signals for the switches S_{x1} and S_{x2} are tested and shown in Fig. 11. As seen, the switch S_{x1} remains turn-on for a certain duration, which agrees well with the theoretical analysis. Before one switch (S_{a1}) begins to turn on/off at a high frequency, another (S_{c1}) has entered its "always-on" duration, as indicated by the zoomed-in view in Fig. 11(a), being in good agreement with the analysis shown in Fig. 4. It ensures that at any instant, at least one of the switches S_{a1}, S_{b1}, and S_{c1} is turned on, and therefore, interrupting the inductor current is prohibited.

Under the modified THI PWM scheme, the voltages across the capacitors are boosted to be about 210 V, as shown in Fig. 12. The three-phase output voltage is shown in Fig. 13, where the maximum value of the line-to-line output voltage is 420 V. The Fast-Fourier-transform (FFT) of the line voltage is tested with the measured rms value of 205 V (peak 290 V), and thus, the voltage gain is 2.9, being close to the theoretical analysis. The FFT of the phase current is also tested and shown in Fig. 14. A low THD is shown due to the filter inductors. Fig. 14 further informs that the input current (I_{Lin}) features a low-frequency ripple, which is caused by the undulated envelopes

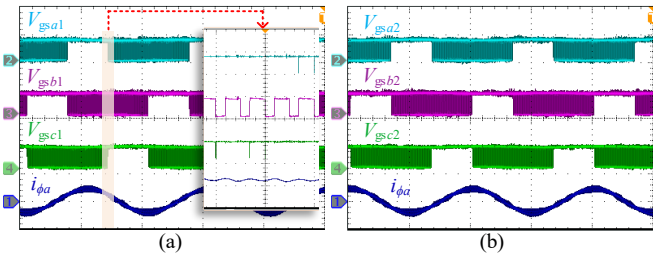

Fig. 11. Experimental gating signals (a) V_{gsx1} of the switch S_{x1} (20 V/div) and (b) V_{gsx2} (20 V/div) of the switch S_{x2}, and the phase current $i_{\phi a}$ (10 A/div).

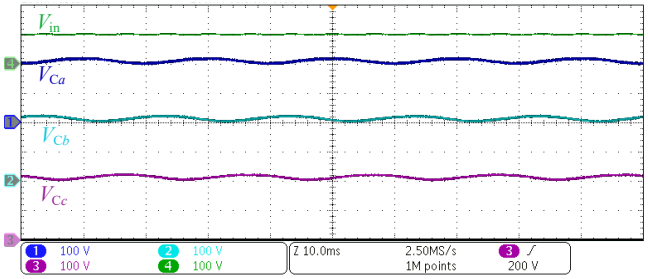

Fig. 12. Experimental waveforms of the capacitor voltages V_{Ca}, V_{Cb}, and V_{Cc}.

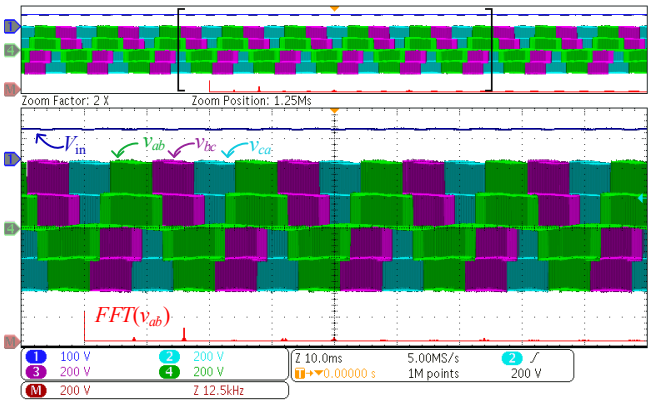

Fig. 13. Experimental waveforms of the input voltage V_{in}, line-to-line voltages v_{ab}, v_{bc}, and v_{ca}, and FFT test of v_{ab}.

of the modulation signals. However, it should be mentioned that the high-frequency current ripple of the input inductor is very low since it is charged twice during a switching period T_s (see the zoomed-in view of Fig. 14).

B. Experimental Dynamic Responses

To verify the flexible voltage gain of the L-ChB inverter, the dynamic responses of the inverter with step-changes in the modulation variable M_{ac1} from 1 to 0.5, and then 0.3 are tested, as seen in Fig. 15(a). The input voltage applied is 50 V and the capacitor voltage V_{Cx} is subsequently stepped from 60 V to 120 V, and then 200 V, which is in accordance with the theoretical analysis in (6). Accordingly, the voltage gain is increased from 2 to 3, and then 4 times, matching with the theoretical analysis presented in Fig. 9. Similarly, the step-changes are applied to the modulation variable M_{ac3} from 0.3 to 0.5, and then 1, as shown in Fig. 15(b). The input voltage applied is 150 V in this test, and the capacitor voltage V_{Cx} remains steady with an average value at 180 V since M_{ac1} keeps constant. Therefore, the voltage gain increases from 1.3 to 1.5, and then 2, which can also be inferred from the variation of the phase current $i_{\phi a}$. A

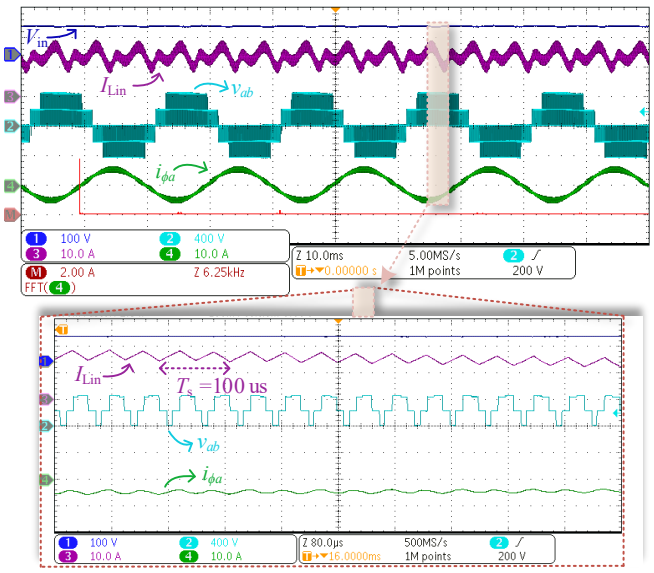

Fig. 14. Experimental waveforms of the input voltage V_{in}, input current I_{Lin}, output line voltage v_{ab}, and output phase current $i_{\phi a}$.

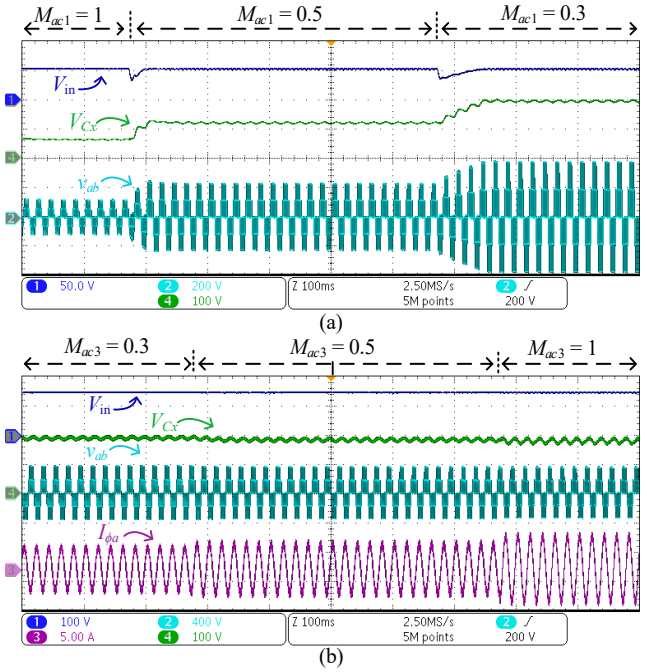

Fig. 15. Dynamic responses with step-changes in the modulation variables (a) M_{ac1} (with M_{ac3} = 1) and (b) M_{ac3} (with M_{ac1} =1).

flexible voltage gain is thus obtained even with the same average PWM ratio (M stepped from 0.65 to 0.75, and then 1 in both cases), confirming the theoretical analysis shown in Section III.A.

Similarly, the dynamic responses of the proposed L-ChB inverter with sudden changes in the output power from the full-load to half-load and then back to full-load are tested, as shown in Fig. 16. During the transients, the inverter operates normally and the output voltage is not interrupted.

C. Efficiency

The efficiency of the L-ChB inverter is measured and compared to its calculated and simulated values in Fig. 17. It

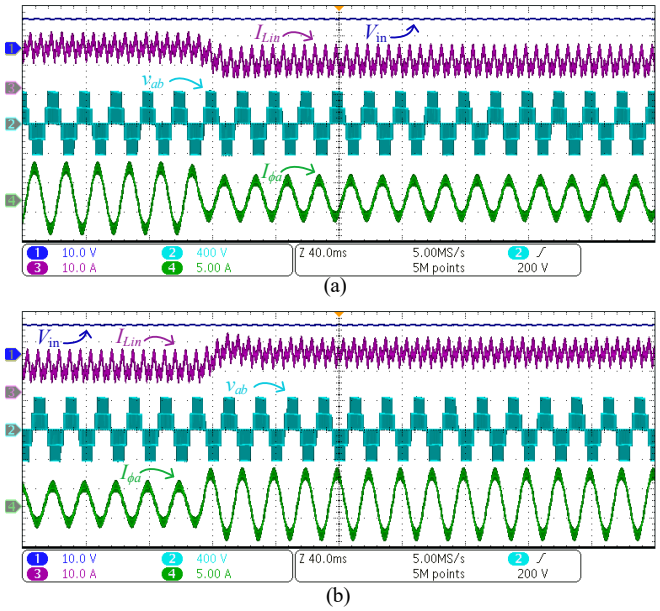

Fig. 16. Dynamic responses (a) from full-load to half-load and (b) half-load to full-load operations.

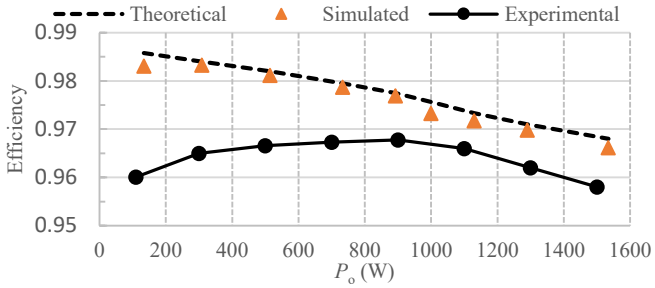

Fig. 17. Theoretical calculated, simulated, and experimental (considering L_f) efficiencies of the L-ChB inverter versus output power (P_o).

can be seen that the simulated efficiency is close to the theoretical one under the same output power, while the experimental efficiency deviates slightly from them. The differences mainly come from the additional losses of the three filter inductors (L_f), which previously were not considered during the theoretical analysis. Nonetheless, the maximum efficiency measured is 96.8% at 900 W. And over the full-load range, the achievable efficiency is well above 95.5%, which indeed provides a high-efficiency dc-to-ac power conversion.

D. Unbalanced Loading Condition

Experimental results of the L-ChB inverter under an unbalanced loading condition are shown in Fig. 18. The loading resistances arranged for the three-phase output are 20Ω, 40Ω, and 60Ω, respectively. It is observed in Fig.18(a) that the variation of the line voltage (v_{ab}) at each level (V_{Cx} or $2V_{Cx}$) becomes larger, which is caused by the increased voltage ripples of the capacitors as shown in Fig. 18(b). Similarly, the fluctuation of the input current also increases under the unbalanced loading condition. Nevertheless, the voltages of the capacitors keep close to each other and are balanced at a steady average value. The voltage boosting capability of the L-ChB inverter and the validity of Eqs. (1) and (2) are thus maintained even under the unbalanced loading condition.

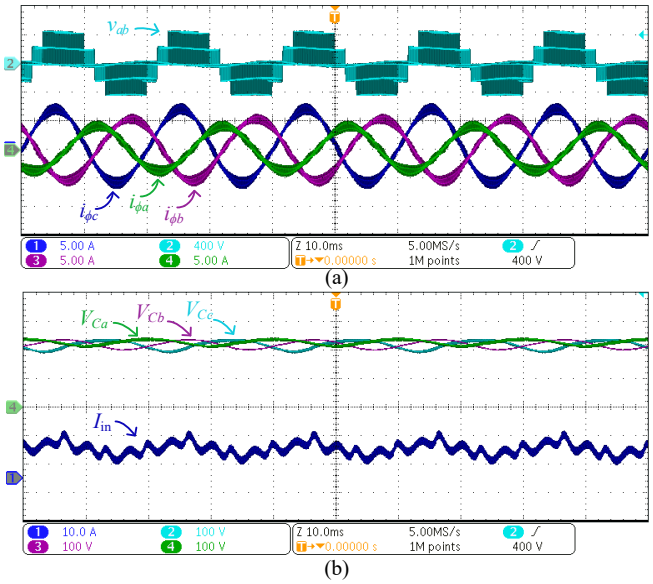

Fig. 18. Experimental waveforms including (a) line voltage v_{ab} and phase currents $i_{\phi a}$, $i_{\phi b}$, and $i_{\phi c}$, and (b) capacitors' voltages V_{Ca}, V_{Cb}, and V_{Cc} and input current I_{in} under a three-phase unbalanced loading condition.

VI. Conclusion

A novel three-phase three-level inductive-dc-link cascaded-half-bridge (L-ChB) inverter is proposed in this paper. The L-ChB inverter is supplied by a single dc source in series with an input inductor. A continuous input current is therefore ensured. The input inductor is charged by shooting through three half-bridge legs to achieve a boosted and regulated output voltage. A modified THI PWM scheme with two independent modulation variables is presented to flexibly adjust the voltage gain. Furthermore, the L-ChB inverter induces low voltage stresses on its components including capacitors, diodes, and switches. The number of components is low and it avoids the use of high-voltage devices, which theoretically reduces the power losses. Comparisons with prior-art inverters are provided to illustrate the advantages. Experimental results show that the L-ChB inverter is able to operate with a flexible voltage gain while applying a relatively large PWM ratio. The measured efficiency of $(96.3 \pm 0.5)\%$ is obtained over a wide power range. The L-ChB inverter is therefore a promising solution to renewable energy applications where a high-efficiency dc-ac voltage-boost conversion using low-voltage devices is expected.

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