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A Voltage-Based Multiple Fault Diagnosis Approach for Cascaded H-Bridge Multilevel Converters

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***Abstract*-This paper proposes a fast and robust open-circuit fault diagnosis method without additional sensors for cascaded H-bridge multilevel converters (CHBMCs). The method is based on the error between the actual input-side voltage and the estimated one, with one detection threshold and 2*n* comparators in *n* cascaded H-bridges. Benefit from the simple design of the fault location, spike elimination, and parameter estimation, with the lower implementation burden, the single and multiple faults in arbitrary positions are accurately identified within a fundamental cycle, and the diagnostic robustness is guaranteed under different transient changes. In view of the low complexity, the proposed scheme can be easily applied to the CHBMCs with arbitrary modules. The experimental results from a CHBMC prototype verify the effectiveness of the proposed method under different operating conditions and fault scenarios.[1]**

***Index Terms*—cascaded H-bridge multilevel converters (CHBMCs), open-circuit fault, voltage error, fault detection and localization, multiple switch faults**

I. Introduction

Considering the cost-effective trade-off for the medium-voltage high-power system, the multilevel converters have emerged as an important topology in industrial applications due to their superior advantages of higher efficiency, lower harmonic distortion, and flexible expandability [1], [2]. Among different multilevel converters, the cascaded H-bridge multilevel converters (CHBMCs) are one of the most valuable structures thanks to the high scalability and fault tolerance [3], popularly applied to the photovoltaic systems [4], static synchronous compensators (STATCOM) [5], solid-state transformers [6], and traction applications [7]. The CHBMCs generally operate as a single-phase rectifier in the traction system [8], where every cascaded H-bridge (CHB) has a dc-link capacitor. With the increased number of semiconductor switches, the failure rate of the CHBMCs also increases, and various fault-tolerant operation schemes have been researched, mainly involved in the power distribution and the smooth switching of redundant cells [9]-[11]. However, the fast fault detection and location should be first executed so that fault-tolerant methods involving the software and hardware are active rapidly.

A survey has shown that failures from semiconductor switches account for 38% of converter faults [12], where the switch faults emerge two types of short-circuits and open-circuits. The thermal runaway or thermal surges generally causes short-circuit faults, which are destructive and commonly damage the complementary switch [13]. Due to the fast fault response, the driving circuits with monitoring and protection devices decrease the destructive effect [14]. The bond wire lift-off and the gate driver failure usually result in open-circuit faults [15], which do not immediately crash the system. However, the distorted grid current and ac input-side voltage may result in cascading failures because of the imbalanced dc-link voltages and high charging current. Thus, fast detection and localization for open-circuit faults are urgently required to ensure fault-tolerant control performance and reduce system loss.

Different diagnosis methods have been proposed to detect and identify open-circuit faults in the multilevel converters and they can be classified as current-based methods, voltage-based methods, and hybrid-based methods. Analyzing the current path under the zero-voltage switching state and the current slope, the proposed method in [16] can detect the fault and localize the faulty switch, but the diagnosis time is more than two fundamental cycles. Furthermore, the estimation model of the sensed current is established to explore the changes of current error under the different operating states [17]-[20]. The circulating current is estimated and compared with the measured current to detect the fault in a modular multilevel converter (MMC) [17]. The assumption-verification method is adopted to locate the faulty switch within 50ms, taking a longer locating time when multiple faults occur. Similarly, the estimation error of grid current is used for the fault detection, and the modulation method is changed for fault localization in [18], where the specific time instants need to be obtained, and the changed modulation results in increased current harmonics. According to the model predictive control (MPC) features, the literature [19] compares the predicted current with the actual one to detect the fault, and single or multiple open-circuit faults are diagnosed by the

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TABLE I Comparison of switch fault diagnostic methods in the multilevel converters

Methods	Needed sensors	Diagnosis time (single faults)	Diagnosis time (multiple faults)	Diagnosis capability	Implementation complexity	Robustness
Slope calculations and comparison [16]	Control system	< 3 fundamental cycles	Not applicable	Cell and switch	Moderate	Good but affected by the low current
Residual calculation and assumption-verification [17]	Control system	< 2.5 fundamental cycles	Longer time	Cell and switch	Moderate	Good
Residual calculation and modulation change [18]	Control system	< 1 fundamental cycle	Not applicable	Cell	Moderate	Good but affected by the parameter changes
Residual calculation and localization matrix [19]	Control system	< 1/4 fundamental cycle	< 1 fundamental cycle	Cell and switch	Moderate	Good but affected by the parameter changes
Residual calculation and comparison [20]	Control system	< 1/4 fundamental cycle	< 1 fundamental cycle	Cell and switch	Moderate	Good
DFT and comparisons [21]	Extra voltage sensors	< 1 fundamental cycles	Not applicable	Cell	High	Good
FFT and principle component analysis [22]	Extra voltage sensors	< 3 fundamental cycles	< 7 fundamental cycles	Cell and switch	High	Good
Voltage comparison and verification [23]	Extra voltage sensors	< 1 fundamental cycles	Not applicable	Cell	Moderate	Good
Residual calculation and modulation change [24]	Extra voltage sensor	< 1/4 fundamental cycle	< 1 fundamental cycle	Cell	Moderate	Good
Mean voltage prediction [25]	Extra voltage sensor	< 1 fundamental cycles	< 1 fundamental cycles	Cell and switch	Moderate	Good
Voltage error and counting comparison [26]	Control system	< 1/4 fundamental cycle	Not applicable	Cell and switch	low	Good
Voltage error and correlation coefficients [27]	Control system	< 1 fundamental cycle	Not applicable	Cell and switch	Moderate	Good but affected by the parameter changes
Extraction of voltage changes [28]	Control system	< 1/2 fundamental cycle	< 1 fundamental cycle	Cell and switch (limited)	Moderate	Good but affected by the noise and light load
Voltage error and counting comparison [29]	Control system	< 1/4 fundamental cycle	< 1 fundamental cycle	Cell and switch (limited)	low	Affected by the noise and parameters
Extraction of dc components [30]	Control system	< 1/2 fundamental cycle	< 1/2 fundamental cycle	Cell and switch pairs	Moderate	Good
Residual calculation and signal injection [31]	Control system	< 1/4 fundamental cycle	Not applicable	Cell and switch	Moderate	Good but affected by the parameter changes

fault location matrix, where the update process is relatively complicated and the parameter uncertainty may affect the accuracy and speed of fault diagnosis. Moreover, the fault location in [20] is completed by analyzing the residual features of output current, where the diagnostic variable is separately designed for each switch. However, a large number of methods enhancing the robustness have been introduced, increasing the application complexity.

The terminal voltage or capacitor voltage for each cell contains the obvious fault information, and a series of voltage-based methods have been studied. The fault features of the terminal voltage are indirectly extracted by using frequency harmonic analysis and the principal component analysis (PCA) in [21] and [22], with the high computational burden. Furthermore, the measured terminal voltage is compared with the estimated one [23], [24]. The fault location is finished by clearing the potential faulty switches and reverifying the faulty position in [23]. The method in [24] needs to obtain a switching transition only one H-bridge undergoes and changes the modulation. Half-cycle mean values of bridge voltages are also adopted to identify the faults in [25]. However, the terminal voltage or the pole-to-pole voltages for the above methods are obtained by using voltage sensors. Instead of using sensors, the measured arm voltages and the estimated ones are expressed by the circuit mathematical equations and the former control signals in the MPC [26], respectively. Considering the difference of the capacitor voltages before and after fault, the correlation coefficients between two capacitor voltages are defined to identify the fault cell in [27]. Nevertheless, they cannot complete the fault localization for the multiple faults. Recently, a capacitor voltage changes-based diagnosis method is proposed in [28], where the count variable corresponding to each IGBT is configured to detect the single or multiple faults. But the diagnosis fails when multiple faults occur in the same cell. Similarly, the method in [29] also cannot distinguish the multiple faults with similar fault features in different cells.

Combing the fault characteristics of current and voltage, some hybrid-based methods are adopted for the CHBMCs. [30] uses a sliding-mode observer to extract the dc components of the grid current and capacitor voltages, in which the design of the observer is involved in many tunning parameters. The residuals of the grid current and capacitor voltages are investigated to detect and locate the single fault in [31], where the driving signals of the control system are changed and the robustness against parameter uncertainty is not considered.

The mentioned fault diagnostic methods are also evaluated and compared with respect to the required sensors, diagnosis time of single and multiple faults, diagnosis capability, implementation complexity, and robustness, as shown in Table I. Due to the limitation of the signal processing methods and the controller, the methods of extracting the fault features from the voltage and current signals themselves have a relatively long diagnosis time. Whereas, the switching states

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for different switches are directly related to the fault features, resulting in that techniques based on residual analysis are widely used to locate faults more quickly. However, if the multiple faults are considered without extra sensors, implementation complexity and robustness against the noise and parameter uncertainty are a huge challenge for the residual-based diagnostic methods. The diagnostic methods in [19] and [20] have made great efforts in these aspects, but the algorithm implementation is still relatively complicated.

To achieve a simple and robust diagnosis for single and multiple faults in the CHBMCs, this paper presents an improved diagnosis approach from [29], mainly increasing multiple fault diagnosis capability and the robustness against noises and parameter changes under the condition of simple implementation. The main contributions of the proposed method are listed as follows.

1) The multiple faults in arbitrary positions are more simply identified by clearing the fault features of the located faulty switch in the model and restarting the counting comparison, providing new thinking for multiple fault diagnosis in the CHBMCs.

2) Through the simple design of spike elimination and parameter estimation, the threshold definition is simplified and the diagnostic robustness is guaranteed without significantly increasing the complexity.

3) The low complexity of the diagnostic algorithm, only with a normalized threshold and two counting comparators in each H-bridge, makes it easily applied to the CHBMCs with arbitrary subcells.

4) The proposed method achieves a good balance between diagnosis time, diagnosis capability, implementation complexity, and robustness, more suitable for the actual applications.

II. Description of the CHBMCs

A. System Description

As shown in Fig. 1, n H-bridge cells connected in series construct the single-phase CHBMCs, where each H-bridge is formed using four semiconductor switches, marked as T_{i1}, T_{i2}, T_{i3}, and T_{i4} (i=1, 2, …, n), with anti-parallel diodes. C_i and R_i represent the output filter capacitor and the resistive load connected to the dc-side of each H-bridge. u_N and i_N are the grid voltage and current, respectively. u_{ab} is the input-side voltage of cascaded H-bridges. L_N and R_N are the filter inductor and parasitic resistor of the ac-side. In the normal operation, dc-link voltage u_i fluctuates around the given value, while the grid voltage and grid current achieve the same phase when using voltage and current two-loop controllers. The phased-shifted pulse width modulation (PS-PWM) with π/n phase-shift is adapted to generate the driving signals, i.e., s_{i1}, s_{i2}, s_{i3}, and s_{i4} to the active switches T_{i1}, T_{i2}, T_{i3}, and T_{i4}, respectively.

B. Voltage error of the CHBMCs

Defining that K_{ia} and K_{ib} are the logical presentation of two legs in one H-bridge, the on/off state for any switch or anti-parallel diode is described by:

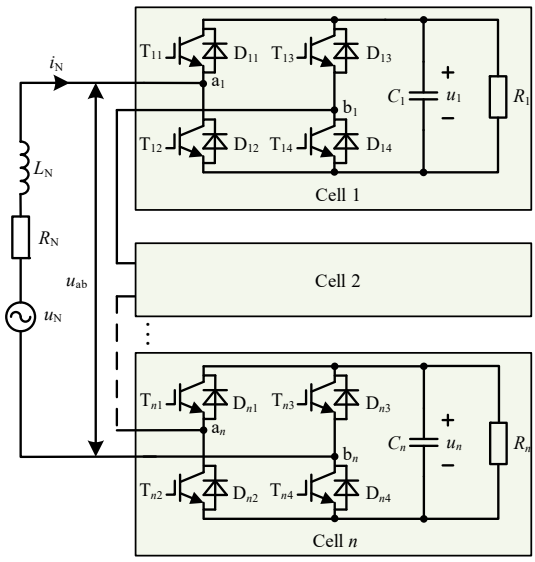

Fig. 1 Topology of the CHBMCs.

$$K_{ia}=\begin{cases}1, \mathrm{T}_{i1} \text{ or } \mathrm{D}_{i1} \text{ on}\\ 0, \mathrm{T}_{i2} \text{ or } \mathrm{D}_{i2} \text{ on}\end{cases},\quad K_{ib}=\begin{cases}1, \mathrm{T}_{i3} \text{ or } \mathrm{D}_{i3} \text{ on}\\ 0, \mathrm{T}_{i4} \text{ or } \mathrm{D}_{i4} \text{ on}\end{cases}, i=(1,2,...,n) \tag{1}$$

In the analysis process, δ=1 indicates the positive current and δ=0 represents otherwise. Based on all of the switching states and Karnaugh map simplification, the expression for K_{ia} and K_{ib} can be given as:

$$\begin{cases}K_{ia}=s_{i1}\overline{\delta}+\overline{s}_{i2}\delta\\ K_{ib}=s_{i3}\delta+\overline{s}_{i4}\overline{\delta}\end{cases} \tag{2}$$

where $\overline{\delta}$, $\overline{s}_{i2}$, and $\overline{s}_{i4}$ indicate the opposite logic of variables. and '+' represents logical OR operation. On/off states during the dead zones are considered in these Boolean equations, neglecting on-resistance, forward voltage, and transient characteristics of transistors [31].

According to the circuit structure and discretization of digital controllers, the actual input-side multilevel voltage of the CHBMCs can be calculated by:

$$u_{\mathrm{ab\_}r}(k)=u_{\mathrm{N}}(k)-L_{\mathrm{N}}\frac{i_{\mathrm{N}}(k)-i_{\mathrm{N}}(k\text{-}1)}{T_{\mathrm{c}}}-i_{\mathrm{N}}(k)R_{\mathrm{N}} \tag{3}$$

where $u_N(k)$, $i_N(k)$, and $i_N(k$-1) are the grid voltage and current at time instant k and k-1, respectively. T_c is the control cycle. However, the pure differentiation of the grid current may be computed with large errors because of the measurement noise. In practice, a state variable filter (SVF) that is asymptotically

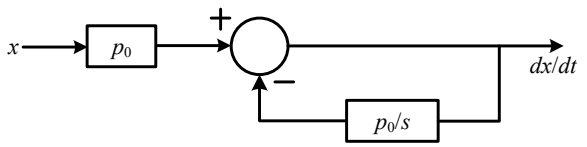

Fig. 2 Structure of the state variable filter.

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stable can be applied to avoid resorting to pure differentiation [32]. The basic structure is illustrated in Fig. 2, where p_0 is the pole of the filter. It can be selected by a trade-off between the sensitivity to the measurement noise and the accuracy of the derivative calculation.

Furthermore, based on the driving signals in the former control cycle, the estimated input-side multilevel voltage can be expressed by

$$u_{ab\_e}(k)=\sum_{i=1}^{n}u_{a_ib_i}(k)=\sum_{i=1}^{n}SF_i(k)u_i(k) \tag{4}$$

where $u_{a_ib_i}(k)$ is the pole-to-pole voltage of the i^{th} cell. $SF_i(k)=K_{ia}(k)-K_{ib}(k)$ is the switching state of i^{th} H-bridge between the time instant k-1 and k. $u_i(k)$ is the dc-link voltage at time instant k.

Comparing the actual input-side voltage with the estimated one, the normalized voltage error is defined as

$$u_r(k)=(u_{ab\_r}(k)-u_{ab\_e}(k))/U_{dc} \tag{5}$$

where U_{dc} is the reference value of dc-link voltages. When the CHBMCs work normally, the voltage error is close to zero. While the open-circuit fault appears, the fault features in the error are illustrated because of the difference between the estimated value and the actual one.

III. Operation Modes Under Different Scenarios

Due to the cascaded structure of the CHBMCs, the single H-bridge cell can be selected as an analyzed option, reducing the difficulty of failure analysis. To understand the relationship between input-side voltage errors and faulty switches, the H-bridge current path and operation modes are investigated in detail under the different scenarios.

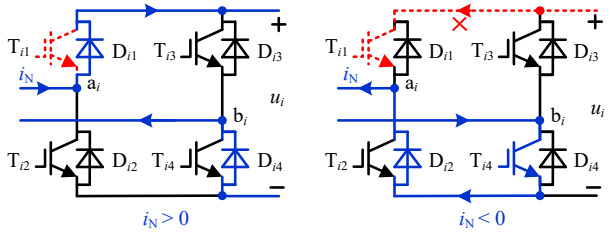
A. Normal operating scenarios

The switching state of each H-bridge cell is $SF_i \in \{-1, 0, 1\}$. Meanwhile, the power transmission is achieved by following three modes under the normal operating conditions:

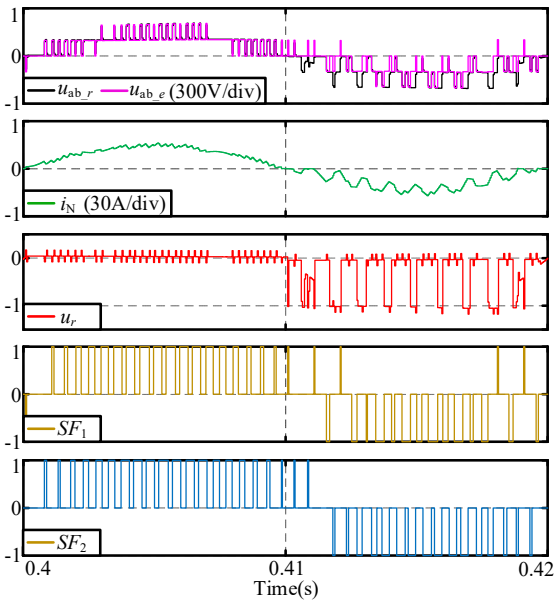
1) Charging mode: $[u_{a_ib_i}, SF_i, i_N]=\{[+u_i, 1, >0], [-u_i, -1, <0]\}$, where the power is transferred from the grid-side to the dc-side and charges the capacitor of the i^{th} H-bridge. During this period, the grid current only flows through diodes and the switches are not active.

2) Discharging mode: $[u_{a_ib_i}, SF_i, i_N]=\{[+u_i, 1, <0], [-u_i, -1, >0]\}$, where the power is transferred from the dc-side to the grid-side and discharges the capacitor of the i^{th} H-bridge. The grid current flows through T_{i1} and T_{i4} when $SF_i = 1$ while T_{i2} and T_{i3} are active under the opposite switching state.

3) Freewheeling mode: $[u_{a_ib_i}, SF_i, i_N]=\{[0, 0, <0], [0, 0, >0]\}$, where the power is not transferred between the grid-side and the dc-side. During $i_N < 0$, T_{i1} or T_{i4} is active to flow the

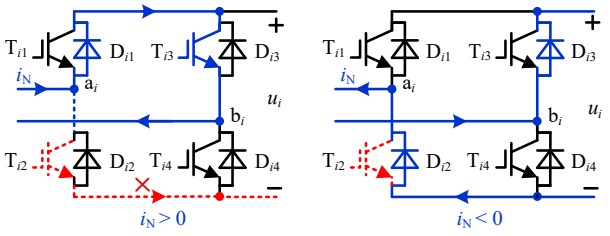


(a) The current path for T_{i1} fault during switching states of (1001).

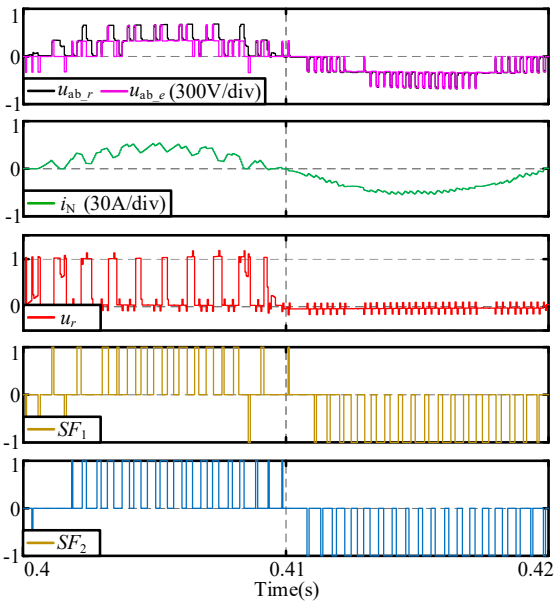


(b) The voltage error and switching states after T_{11} fault.

Fig. 3 Analysis results of the current path and voltage error after T_{i1} fault.



(a) The current path for T_{i2} fault during switching states of (0110).



(b) The voltage error and switching states after T_{12} fault.

Fig. 4 Analysis results of the current path and voltage error after T_{i2} fault.

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current while T_{i2} or T_{i3} is active when $i_N > 0$.

B. Open-circuit fault scenarios

As two diagonal switches, T_{i1} and T_{i4} conduct the grid current only when $i_N < 0$ while T_{i2} and T_{i3} only conduct the positive grid current, illustrating a similar current path. Therefore, a single T_{i1} open-circuit or T_{i2} open-circuit is selected for fault mode analysis. Likewise, different cases for multiple open-circuit faults can be analyzed by a similar logic.

As shown in Fig. 3(a), during the switching states of (1001), the positive current only flows through anti-parallel diode D_{i1} and D_{i4}, not affected by the T_{i1} open-circuit. On the contrary, the negative current path has to be changed from the path of T_{i1} and T_{i4} to the path of D_{i2} and T_{i4}, where the discharging mode of $[u_{ai}b_i, SF_i, i_N] = [+u_i, 1, <0]$ are replaced by the freewheeling mode of $[u_{ai}b_i, SF_i, i_N] = [0, 0, <0]$.

Starting from the switching state, T_{i1} open-circuit can equate with the driving signal s_{i1}=0, and then the actual switching state of the faulty cell can be expressed as:

$$SF_i' = \overline{s}_{i2}\delta - (s_{i3}\delta + \overline{s}_{i4}\overline{\delta}) \tag{6}$$

Subsequently, the actual input-side voltage can be described as follows, which is equivalent to u_{ab_r}.

$$u_{ab} = SF_i' u_i + \sum_{j=1}^{n} SF_j u_j,\ j \neq i \tag{7}$$

Furthermore, the theoretical expression of the normalized voltage error can be obtained.

$$u_r = -s_{i1}\overline{\delta} u_i / U_{dc} \approx -1 \tag{8}$$

Under the condition of the active switching state and the negative current direction, the normalized voltage error is almost equal to -1. Simulations on a case study specified in Table III in Section V are built and numerical values are shown in Fig. 3 and Fig. 4, where two H-bridges are cascaded, the switching frequency is 1000 Hz, and the fault trigger of switches are all set at t=0.4s. As shown in Fig. 3(b), the voltage errors close to -1 only appear in the switching states of 1 and 0 for the faulty cell. However, there are still situations where the fault features appear during the switching state of -1 for the normal cell, showing an obvious difference between the faulty cell and the normal ones.

Similarly, under the active switching state of (0110) in Fig. 4(a), the positive current path is affected by the T_{i2} open-circuit fault, causing that the discharging mode of $[u_{ai}b_i, SF_i, i_N] = [-u_i, -1, >0]$ are replaced by the freewheeling mode of $[u_{ai}b_i, SF_i, i_N] = [0, 0, >0]$. The negative current path is not affected. During the fault period, the driving signal s_{i2} is equivalent to zero and the actual switching state of the faulty cell can be expressed as

$$SF_i' = s_{i1}\overline{\delta} + \delta - (s_{i3}\delta + \overline{s}_{i4}\overline{\delta}) \tag{9}$$

And then, the theoretical values of the normalized voltage error are given by

$$u_r = s_{i2}\delta u_i / U_{dc} \approx 1 \tag{10}$$

When the positive current flow through T_{i2} during the T_{i2} open-circuit, with the switching states of -1 or 0, the voltage error is approximately equal to 1, as illustrated in Fig. 4(b). Similarly, only for the normal cell, the voltage errors close to one may appear in the switching state of 1.

TABLE II Detectable fault features of i^{th} H-bridge cell

Switching state SF_i	Current direction	Faulty switch	Voltage error u_r
+1	$i_N < 0$	T_{i1}	≈ -1
		T_{i4}	≈ -1
0_U	$i_N < 0$	T_{i1}	≈ -1
	$i_N > 0$	T_{i3}	≈ +1
0_L	$i_N < 0$	T_{i4}	≈ -1
	$i_N > 0$	T_{i2}	≈ +1
-1	$i_N > 0$	T_{i2}	≈ +1
		T_{i3}	≈ +1

From the above analysis, it can be concluded that a fault can be detected only when the grid current in the original operating mode flows through the switch itself rather than its anti-parallel diode. The detectable fault features in the i^{th} H-bridge cell are summarized in Table. II, where 0_U is the case in which the upper arm switch T_{i1} or T_{i3} is turned on and 0_L is the case where the lower arm switch T_{i2} or T_{i4} is turned on. These fault phenomena are used as the basis of the diagnostic design.

IV. Fault Diagnosis Method

According to the operating modes under the normal and fault cases in Session III, a voltage error-based open-circuit fault diagnosis approach is presented in this section. The whole flowchart of the diagnostic scheme is illustrated in Fig. 5, including three diagnostic steps of fault detection, faulty cell location, and faulty switch location. Firstly, the detection variable u_{rd} is designed to monitor the operating state of the CHBMCs. Once the fault is detected, the fault location process is implemented. The faulty cell can be determined in the location stage by designing the counting comparators t_{i1} and t_{i2} for each cell. Finally, the faulty switch is identified and the fault signature F_{ij} (j=1, 2, 3, 4) is output by directly matching the fault features with the driving signals. Furthermore, after a faulty switch is located, the driving signal of the detected switch in the voltage estimation is set to zero. And the counting comparators are reset by checking the change feature of the sum of fault signatures, i.e., $D(k)$, to detect further and locate more faulty switches. A more detailed explanation is given below.

A. Fault Detection

Based on the above analysis, when the detectable fault features appear, the absolute values of voltage errors are always close to 1. Thus, the fault detection can be carried out by introducing a threshold T_{th}. If the voltage error satisfies $|u_r| > T_{th}$, the fault can be detected. However, sampling errors of different sensors, measurement noise, estimation errors, and electromagnetic interference (EMI) in the actual hardware circuits may generate a transient spike, occasionally exceeding the threshold and leading to false detection.

In order to avoid the false fault detection, a counting-based elimination method is adopted, as shown in Fig. 6, where m and h are the counting variables, and k is the counting threshold. The initial values of m and h are set to 0 before starting the detection algorithm. During fault detection, m and h are used to count fault events at the control cycle level. If the

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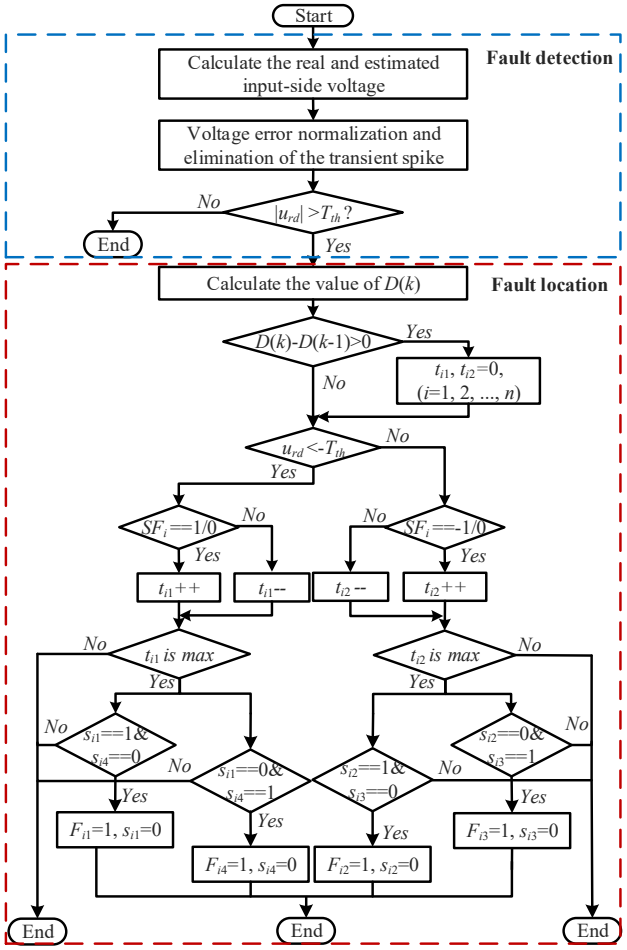

Fig. 5 Flowchart of the proposed diagnostic method.

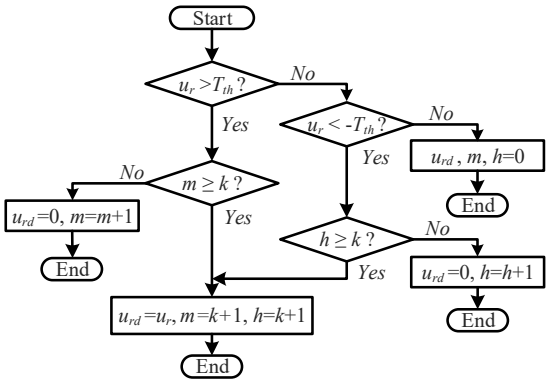

Fig. 6 Flowchart of the counting-based elimination method.

fault event has occurred continuously k times, the voltage error in this control period is output to the detection variable u_{rd}. If fault events continue to occur at the next control period, the counting judgment condition is directly satisfied to output the voltage error. On the contrary, once the voltage error does not satisfy the threshold condition, the counting variables are reset to zero and the voltage error is not output. k can be chosen by evaluating the maximum duration of transient spikes in the actual control system. Therefore, the fault can be accurately detected as long as the detection variable satisfies $|u_{rd}| > T_{th}$.

B. Faulty Cell Location

According to the fault features in Table II, the voltage errors of less than the negative threshold only appear in the switching state 1 and 0 when T_{i1} or T_{i4} open-circuit fault occurs. While the fault features for T_{i2} or T_{i3} open-circuit are only illustrated under the switching state -1 and 0, where the voltage errors are more than the positive threshold. Thus, two kinds of counting comparators for each cell i.e., t_{i1} and t_{i2}, can be designed. Before that, the reset of the counting comparators should be considered to meet the needs of multiple fault locations. The sum of fault signatures for all cells is calculated by

$$D(k) = F_{i1}(k) + F_{i2}(k) + F_{i3}(k) + F_{i4}(k), i = 1, 2, ..., n \quad (11)$$

Only if the value of $D(k)$-$D(k$-1) is more than zero, indicating the existence of the located faulty switch, the counting comparators are reset to identify further whether the system has other faults. During the counting comparison, if u_{rd} is less than the negative threshold, indicating the failure possibility in T_{i1} and T_{i4}, the counting comparator t_{i1} is updated by using the following rules.

$$\begin{cases} t_{i1}+=1, if\ (u_{rd} < -T_{th}\ \&\ SF_i == 0\ or\ 1) \\ t_{i1}-=1, if\ (u_{rd} < -T_{th}\ \&\ SF_i == -1) \end{cases} \quad (12)$$

If the switching state SF_i is equivalent to 1 or 0 under the condition of $u_{rd} < -T_{th}$, the counter of the i^{th} cell increases by one, and the counters of other cells decrease by one. In contrast, if $u_{rd} > T_{th}$, indicating the failure possibility in T_{i2} and T_{i3}, the counting comparator t_{i2} is designed and the update rules are defined as

$$\begin{cases} t_{i2}+=1, if\ (u_{rd} > T_{th}\ \&\ SF_i == 0\ or\ -1) \\ t_{i2}-=1, if\ (u_{rd} > T_{th}\ \&\ SF_i == 1) \end{cases} \quad (13)$$

The update process of t_{i2} is similar to that of t_{i1}. Because the faulty cell exhibits fault features the most times, the cell with the largest counting value is localized as a faulty cell.

C. Faulty Switch Location

After the faulty cell is identified, the specific faulty switch can be located by matching the fault features with the switching state of the corresponding faulty cell. Among the detectable fault features, the switching states of +1 and -1 cannot be used to distinguish the faulty switches because the current flows through the bodies of the two switches themselves simultaneously. In such a situation, whether the fault occurs on one or two switches cannot be judged.

Thus, zero switching states where the current only flows through the body of one switch itself are adopted to identify the location of the faulty switch. Under the condition that the largest counting value appears in the comparator t_{i1} and the detection variable is not zero, if the system operates under the zero switching state of s_{i1} = 1 and s_{i4} = 0, the switch T_{i1} is identified as a faulty switch. Similarly, the other faulty switches are also located as long as the specific zero switching state is matched with the fault features.

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When a faulty switch T_{ij} is identified, the corresponding fault signature F_{ij} jumps to 1, and the driving signal of T_{ij}, s_{ij}, is adjusted to zero in the switching state SF_i of Eq. (4) while the driving signals of the actual system are not changed. Through this adjustment, the estimated ac input voltage can be equivalent to the actual input voltage corresponding to T_{ij} fault, clearing the fault information of T_{ij} from the voltage error. And then, the fault detection is re-executed by comparing the detection variable with the threshold. If $|u_{rd}|>T_{th}$, the counting comparators of each cell, i.e., t_{i1} and t_{i2}, are reset because the value of D(k)-D(k-1) is more than zero. Subsequently, another faulty switch can be identified by restarting the location algorithm of the faulty cell and faulty switch. Therefore, as long as the new fault features are detected after clearing the fault information of the located faulty switches, the location algorithm is restarted to identify more faulty switches, not affected by the number and position of the faulty switches.

D. Parameter Sensitivity

The component parameters may not match with their reference values due to the performance degradation or tolerances. The adjustment of the detection threshold cannot make the voltage calculation insensitive to the large parameter changes. In calculating actual input-side voltage, the inductor parameter is the main factor changing the calculation accuracy because of the small parasitic resistor R_N, thereby affecting the accuracy and speed of fault detection and location. In this paper, the recursive least square (RLS)-based parameter estimation method is adopted to estimate online the component parameters [33].

Firstly, the voltage across the inductor can be expressed as

$$u_L(k) = u_N(k) - u_{ab\_e}(k) - i_N(k)R_N \tag{14}$$

Meanwhile, the relationship between the grid current and the voltage across the inductor can be described as

$$u_L(k) = L_N \frac{i_N(k) - i_N(k\text{-}1)}{T_c} = L_N i'_N(k) \tag{15}$$

Afterward, a second-order lowpass filter (LPF) with the natural frequency of 100Hz is introduced to decrease the influence of the measurement noise and switching process on the calculation of inductor voltage and current derivative. And the pure differentiation can be avoided by using the SVF.

Furthermore, the estimated parameter can be updated and converged to near the actual value in the RLS algorithm. The estimated inductor value is obtained by the following equation when applying the RLS to (15).

$$\begin{aligned}\hat{L}_N(k) = \hat{L}_N(k\text{-}1) + \gamma(k) LPF[i'_N(k\text{-}1)] \times \\ [LPF[u_L(k-1)] - \hat{L}_N(k\text{-}1) LPF[i'_N(k\text{-}1)]]\end{aligned} \tag{16}$$

where $\gamma(k)$ is considered as a constant gain and can be selected by a trial-and-error method in the simulation and experimental tests. By using the above simple parameter estimation, the inaccuracy of the inductor parameter is significantly reduced, simplifying the threshold definition and improving the robustness against the parameter uncertainty.

V. Experimental Results and Discussions

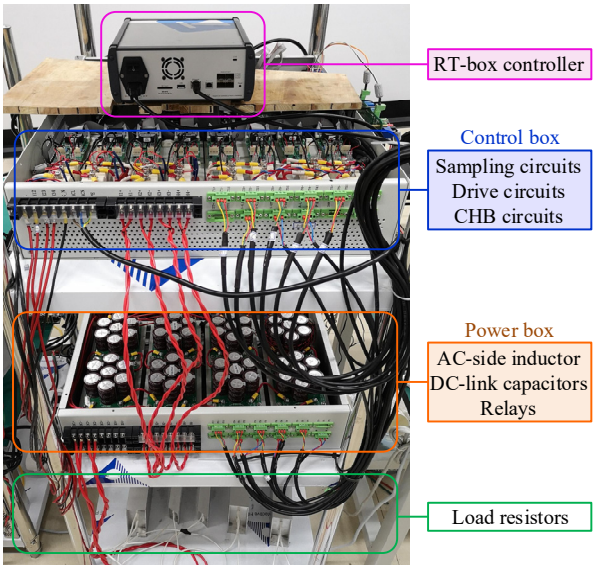

Fig. 7 The experiment platform of the CHBMCs.

TABLE III Test Parameters of the Single-Phase CHBMCs

Parameter	Simulation and test value
Grid voltage u_N (RMS)	100 V
Equivalent filter inductor L_N	3 mH
Parasitic resistor R_N	0.1 Ω
Reference dc-link voltage U_d	100 V
dc-link capacitor C_i	2.8 mF
Rated equivalent load R_i	20 Ω
Number of cascaded H-bridges n	2
Switching frequency f_s	1000 Hz
Control cycle T_c	50 μs
Grid frequency f_g	50 Hz
Detection threshold T_{th}	0.8
The pole of the SVF -p_0	2e4
Constant gain of the RLS γ	2e-12

In order to test the diagnostic accuracy and robustness of the proposed method, the experimental verification is implemented by the experiment platform of the CHBMCs, as shown in Fig. 7. As the controlled objects, CHB circuits are placed in the control box, together with sampling and drive circuits. Besides, the power box contains the ac-side inductor, dc-link capacitors, and relays. An RT-box digital controller is used to complete the control, modulation, and fault diagnosis algorithm. In the experiment process, open-circuit faults are emulated by isolating the driving signals of switches. The experimental parameters are listed in Table III, which is the same as the simulation parameters.

Firstly, the normal operating state is shown in Fig. 8, where the same phase between the grid voltage and current of the CHBMCs is achieved and the dc-link voltage can track the reference values. And then, the immunity of the diagnostic algorithm to the transient spikes, different operating changes, and inductor parameter is further evaluated.

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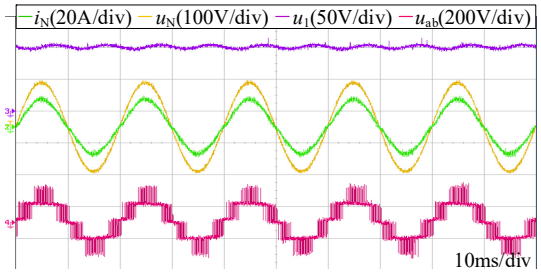


Fig. 8 The experiment results under the normal operation.

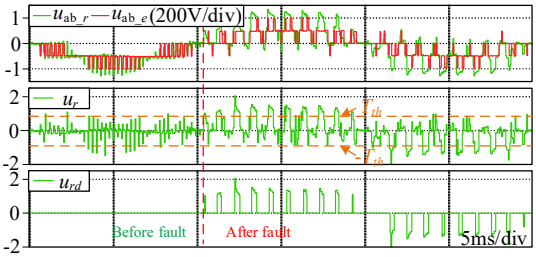
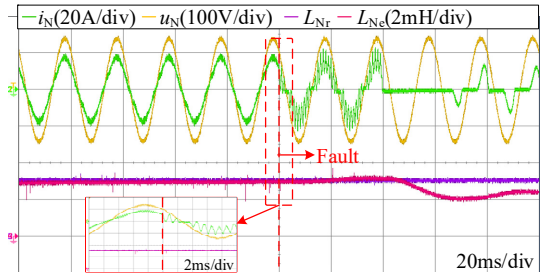
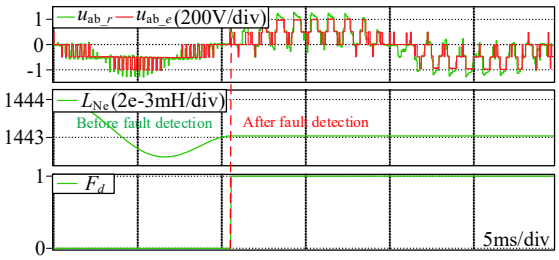


Fig. 9 Change results of detection variable before and after fault.



(a)



(b)

Fig. 10 Change results of the estimated inductor values (a) before and after fault and (b) before and after fault detection.

A. Immunity analysis of the proposed method

The transient spikes caused by the measurement noise and calculation error appear from time to time. Fig. 9 shows that the voltage error u_r contains some transient spikes near ±1 under the normal condition and the consecutive fault features fluctuating around ±1 appear after T_{11} and T_{12} faults. Considering a trade-off between the diagnostic accuracy and the detection time, the detection threshold is set to 0.8 and the counting threshold is selected to 1 for eliminating the effect of the transient spikes. The consecutive fault events of more than the detection threshold T_{th}, are extracted effectively as the detection variable, avoiding the false trigger.

Subsequently, the estimation performance of the inductor parameter is investigated. Fig. 10(a) shows the change results of the estimated inductor values before and after fault, where L_{Nr} is the reference value and L_{Ne} is the estimated value. The estimation errors are very small even under the fault condition because the fault location is completed quickly. And then the switching state SF_i of the estimation algorithm is changed to make it the same as that of the actual faulty cell. To protect the hardware circuits, the isolation of driving signals is carried out after the fault lasts for two fundamental cycles, where the estimation errors increase gradually but the diagnosis has been finished during the fault period. Considering that the inductor values are not changed significantly in a period of time, as shown in Fig. 10(b), the estimated value is latched after fault detection signature F_d jumps to 1 and remains unchanged during the whole fault period, reducing the influence of estimation errors on the diagnosis.

Moreover, the generation of the detection variable mainly relies on the grid voltage u_N, the grid current i_N, and the dc-link voltage u_i. Thus, the transient changes of these signals are performed in Fig. 11 to investigate the robustness for fault detection. Fig. 11(a) shows the step changes of grid voltage between 100V and 120V, causing the amplitude change of the grid current. Under the given dc-link voltage, Fig. 11(b) illustrates the transient process of the grid current during load step changes between half-load and full-load. Furthermore, the reference dc-link voltage is adjusted between 100V and 80V in Fig. 11(c), where the grid current increases and decreases accordingly. Considering the worst operating condition, the load transient between the empty-load and full-load is also tested in Fig. 11(d). Because of the regulation process of dc-link voltages during the load changes, the amplitude of transient spikes fluctuates but these spikes still only last for at most one control cycle. Under the different transient changes in these signals, the transient spikes in the voltage errors sometimes appear but detection signature F_d never outputs false detection events, demonstrating the good immunity of the diagnostic algorithm to different transient changes.

Additionally, different fault scenarios are emulated to test the effectiveness and speed of diagnosis. In diagnostic analysis, the interval time from the beginning moment of the grid current distortion, where the voltage error changes significantly, to the moment where all of the faults are localized is defined as the diagnosis time. The test results are displayed by the waveforms of the grid voltage, grid current, and fault triggering F_t from the oscilloscope, and the online values of diagnostic variables and fault signatures from the RT-box.

B. Single open-circuit fault scenarios

Fig. 12(a) illustrates that the fault is triggered in the negative current cycle and the current distortion appears at t_0, illustrating the significant difference between the real input voltage and the estimated voltage. Due to the counting-based elimination method, the detection variable shows the fault features after one control interval, where the detection

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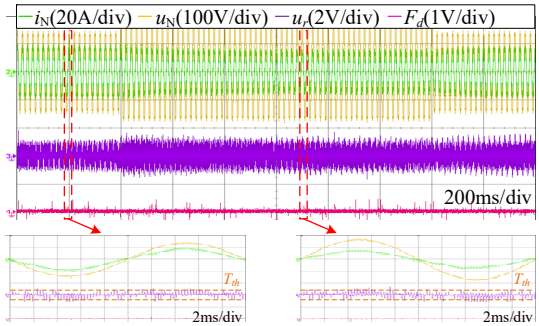
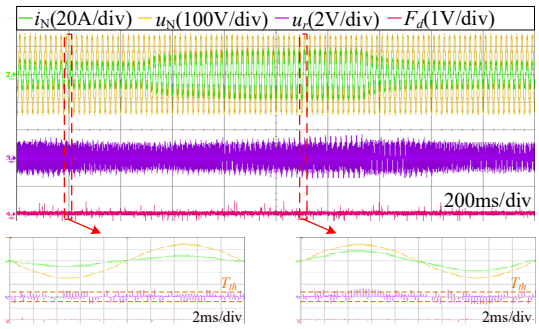
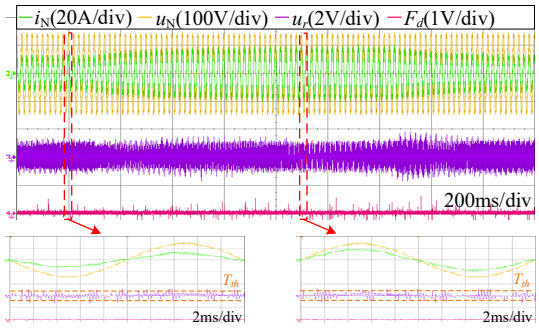


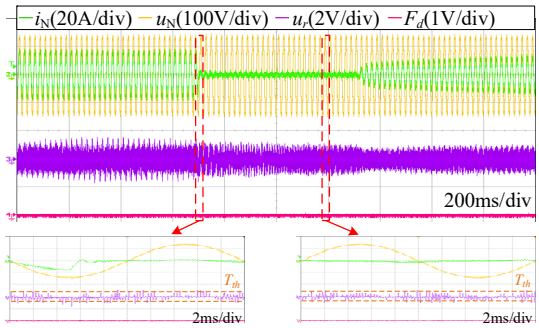
(a) The step changes of u_N



(b) The step changes of the load



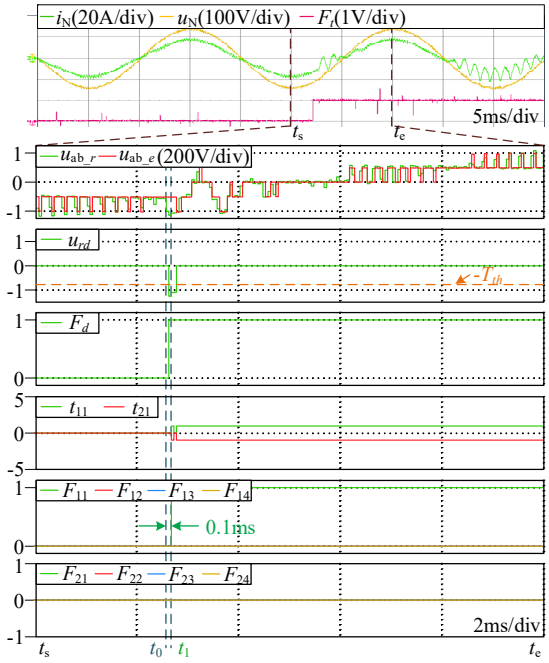
(c) The step changes of u_i



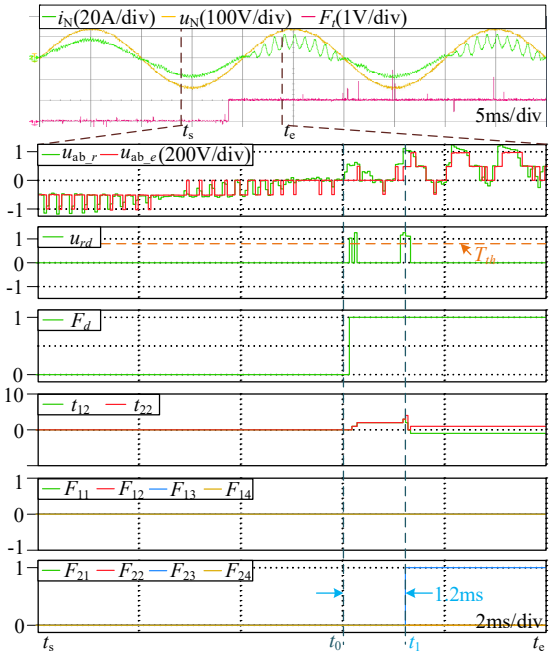
(d) The changes between empty-load and full-load

Fig. 11 Experiment results under (a) the step change of u_N between 100V and 120V, (b) the step changes of the load between half-load (50%) and full-load (100%), (c) the step changes of u_i between 80V and 100V, and (d) the load changes between empty-load and full-load.

signature jumps to 1 and the counting comparators in two H-bridges operate to locate the faulty cell. After one control cycle, the largest value of all comparators is obtained at t_{11}, indicating cell 1 as a faulty cell. And then, the zero switching



(a) T_{11} open-circuit fault



(b) T_{23} open-circuit fault

Fig. 12 Experimental results for the single open-circuit fault in cell 1 and cell 2.

state of s_{11}=1 and s_{14}=0 is precisely matched with the fault features, identifying T_{11} as a faulty switch at t_1. After that, no new fault signature is output, indicating that the fault diagnosis is completed within 0.1ms.

Similarly, the fault triggering of Fig. 12(b) also occurs in the negative current but the consecutive fault features appear till t_0. And then, the fault is detected and all comparators start to count and compare each other. At t_1, the comparator t_{22}

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shows the largest value, indicating the fault occurs in cell 2. At this moment, the fault features are precisely matched with the zero switching state of s_{23}=1 and s_{22}=0, identifying T_{23} as a faulty switch. And then, the fault features disappear after the driving signal of T_{23} in SF_2 is set to zero, illustrating that the whole diagnosis time is 1.2ms.

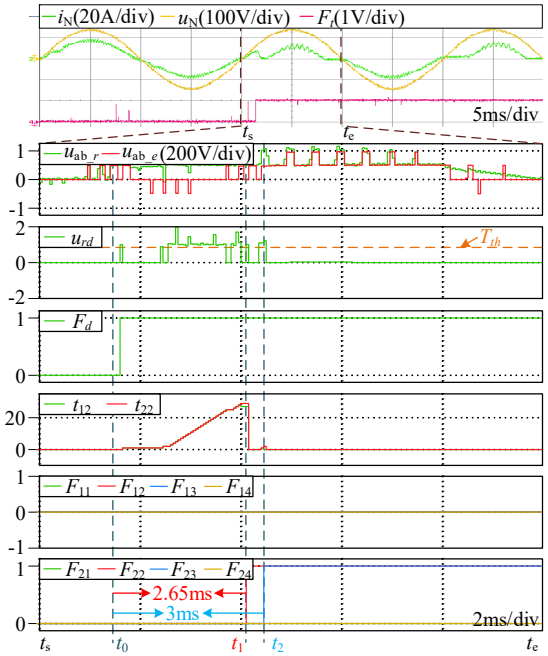
C. Multiple open-circuit fault scenarios

In terms of multiple faults in one cell, as illustrated in Fig. 13(a), the fault setting in the positive current cycle immediately causes the distorted current at t_0. After the fault is detected, the comparators t_{12} and t_{22} start to count because of the positive voltage errors. When the comparator t_{22} has the largest value, cell 2 is located as a faulty cell but the fault features are not matched with the zero switching states of s_{23}=0 and s_{22}=1 until t_1, where the fault of T_{22} is first identified. After that, the driving signal of T_{22} in SF_2 is set to zero and all of the comparators are reset to zero for restarting the fault location. At t_2, the largest value reappears in the comparator t_{22}, and the zero switching state of s_{23}=1 and s_{22}=0 is exactly matched with the fault feature, determining that T_{23} is another faulty switch in cell 2. The whole diagnosis is completed within 3ms.

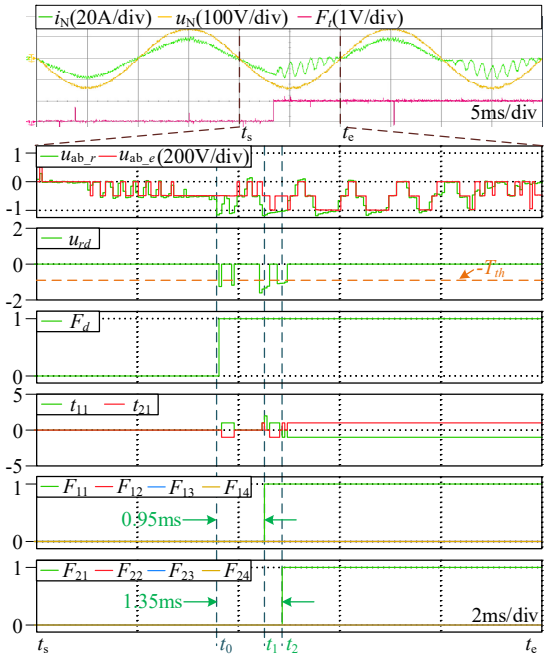
Furthermore, in Fig. 13(b), the simultaneous multiple open-circuit faults in different cells are triggered in the negative current cycle, where the current distortion occurs at t_0 and the fault is detected after one control cycle. When the largest counting value first appears in the comparator t_{11}, the values of the detection variable u_{rd} change to zero, causing that the faulty switch cannot be identified. Until t_1, the maximum counting value appears again and the fault features precisely correspond to the zero switching state of s_{11}=1 and s_{14}=0, indicating that T_{11} is a faulty switch. When the fault of T_{21} is identified at t_2, the fault detection and location is finished, taking the diagnosis time of 1.35ms.

D. Diagnosis results under low-load conditions

To investigate the diagnostic ability under the low-load condition, Fig. 14 gives the diagnostic results for multiple faults in one and different cells under the low-load. The multiple open-circuit faults occur when the grid current is more than zero in Fig. 14(a). The fault features first correspond to the zero switching state of s_{23}=1 and s_{22}=0 at t_1, and the fault signature of T_{23} jumps to 1. Until t_2, the second faulty switch is identified, causing the diagnosis time of 6.55ms. As shown in Fig. 14(b), multiple faults of different cells with similar fault features are also triggered in the positive cycle of the current. The fault of T_{22} is firstly identified after 1.2ms from the beginning of the current distortion. Entering the negative cycle of the grid current, different fault features appear and T_{14} open-circuit fault is located, where the comparator t_{11} has the largest value and the zero switching state of s_{11}=0 and s_{14}=1 is matched with the fault feature. The diagnosis time takes 11.85ms, less than one fundamental cycle, illustrating the good availability of the proposed scheme under the low-load condition.



(a) T_{22} and T_{23} open-circuit faults



(b) T_{11} and T_{21} open-circuit faults

Fig. 13 Experimental results for the multiple open-circuit faults in cell 1 and cell 2.

E. Diagnosis results under different modulation indexes

Furthermore, the diagnosis results under different modulation indexes are investigated. In n cascaded H-bridges, the input-side voltage levels depend on the modulation index M. For two cascaded H-bridges in experiment tests, the input-side voltage is three levels for $0<M<0.5$ and five levels for $0.5<M<1$. The diagnosis results under five-level voltage have

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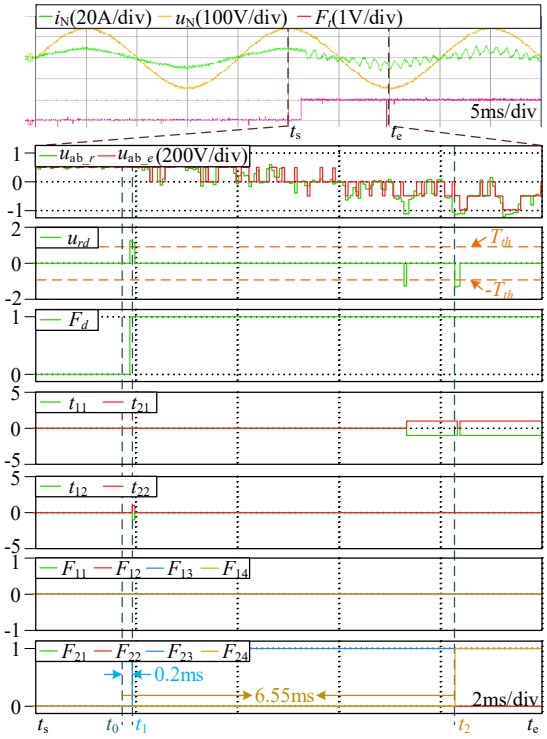
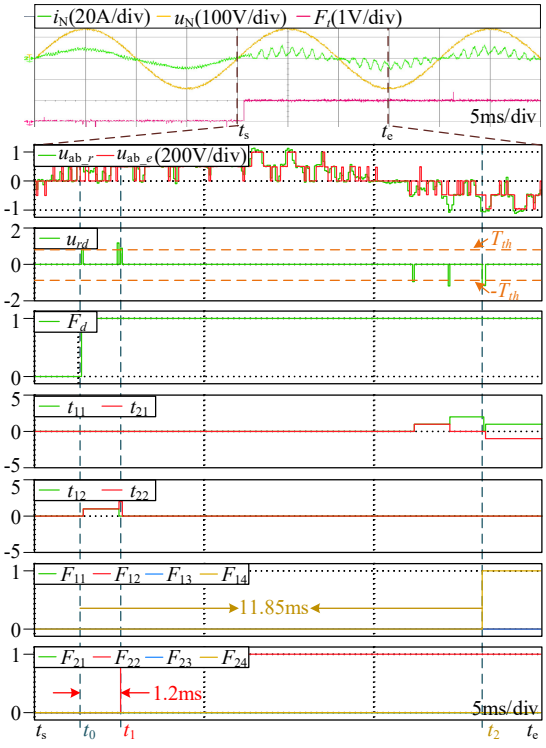


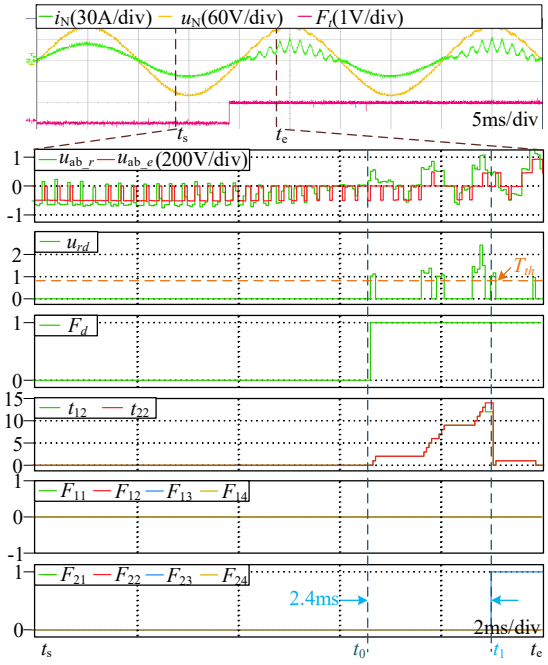
(a) T_{23} and T_{24} open-circuit faults



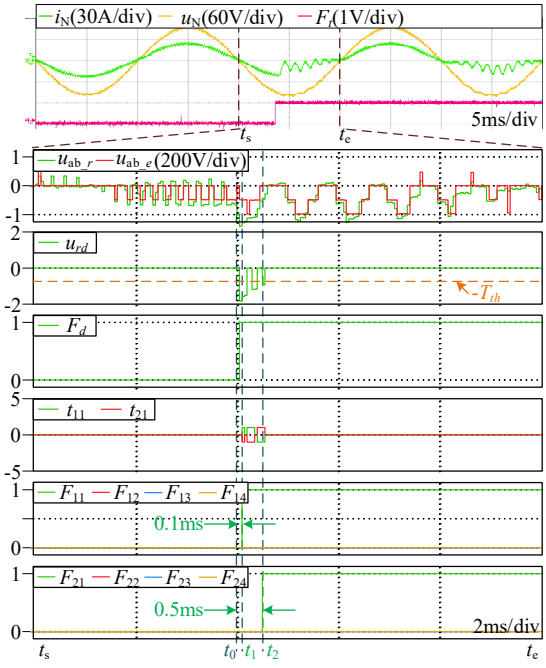
(b) T_{14} and T_{22} open-circuit faults

Fig. 14 Experimental results for the multiple open-circuit faults under the low-load condition.

been illustrated in the above analysis, so experimental results for the three-level voltage under M=0.49 are shown in Fig. 15.



(a) T_{23} open-circuit faults



(b) T_{11} and T_{21} open-circuit faults

Fig. 15 Experimental results for the different open-circuit faults under the low modulation index.

The faults are triggered at similar moments to Fig. 12(b) and Fig. 13(b), respectively. It can be seen that the faults can be still detected quickly but the diagnosis of T_{23} fault is completed after 2.4ms, where more overlap of zero switching states for two cells causes a longer location time during the low current period. In contrast, the zero switching states of the two cells are less overlapped during high current periods, resulting in the faster diagnosis speed for T_{11} and T_{21} faults,

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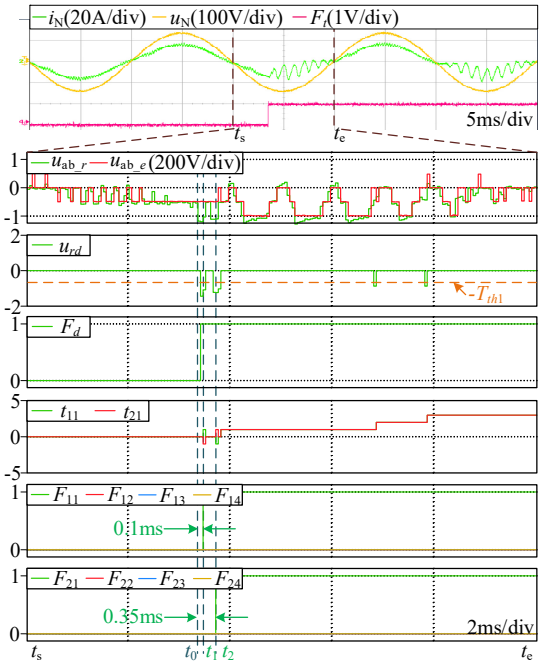
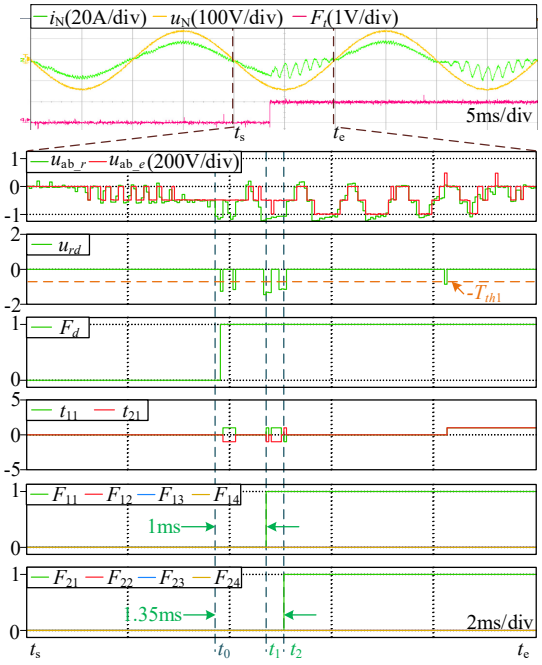


(a) T_{th1}=0.7 and k=1



(b) T_{th1}=0.7 and k=2

Fig. 16 Experimental results for T_{11} and T_{21} open-circuit faults under the different threshold values.

compared to the results in Fig. 13(b).

F. Diagnosis results under different threshold values

The thresholds directly affect the detection accuracy and diagnostic speed in the proposed method. Considering the different detection threshold T_{th} and counting threshold k, the experimental results for T_{11} and T_{21} open-circuit faults are shown in Fig. 16. For T_{th1}=0.7 and k=1, the detection accuracy

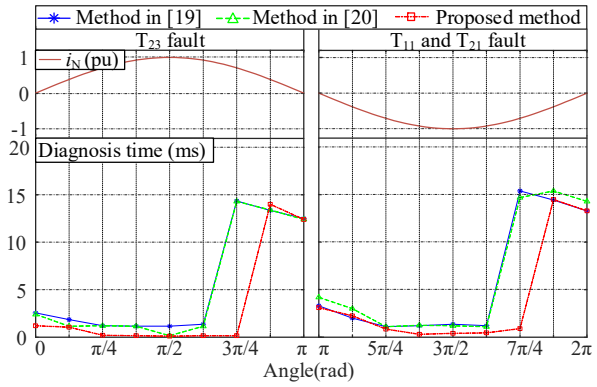


Fig. 17 Diagnostic time of different methods under single and multiple faults.

Table IV Comparison of the maximum implementation time

Digital controller	With the method in [19]	With the method in [20]	With the proposed method
Maximum implementation time (μs)	5.81	8.97	3.66

is guaranteed but fault features appear more in u_{rd}, causing shorter diagnosis time, compared to the results in Fig. 13(b). However, when T_{th1}=0.7 and k=2, the extracted fault features in u_{rd} are decreased, resulting in that the diagnosis is completed after 1.35ms. Therefore, the threshold selection needs to consider the tradeoff of accuracy and speed.

G. Comparison with existing methods

The methods in [19] and [20] have the similar diagnostic performance to the proposed technology. Therefore, under the same control and modulation algorithms, the differences in the diagnosis time, complexity, and robustness between the three methods are investigated. Firstly, Fig. 17 presents the diagnosis time of T_{23} fault and multiple faults of T_{11} and T_{21} at different fault moments in a fundamental cycle, which is calculated during the distorted current period. Among them, the proposed technique exhibits a shorter diagnostic time during most of the fundamental cycle. Furthermore, the three diagnosis algorithms are separately added to the RT-box controller, testing the implementation time of the whole algorithm. The comparison results in Table. IV show that the digital controller with the proposed method has the shortest execution time. Benefit from the simple design of the spike elimination and parameter estimation, compared to [19] and [20], the diagnostic robustness of the proposed method can be also guaranteed under the lower implementation burden.

H. Further discussions of the proposed method

The detection threshold and counting threshold need to be designed. Because the initial fault features are always equivalent to a single switch fault when more than one faults appear, the detection threshold can be selected according to u_r under the normal and single fault conditions. Through the theory analysis, the absolute values of u_r are always between 0

and 1. Generally, a low detection threshold can obtain fast detection speed but low detection accuracy, while a large detection threshold can greatly improve the algorithm accuracy but decrease the diagnostic speed. In addition, the designed thresholds need to deal with the challenges of various transient changes. Transient test results in Fig. 11 have shown that most of the voltage errors fluctuate always in the range of ±0.5 except for some transient spikes. Meanwhile, the dc-link voltages fluctuate and may deviate from the reference value after a fault. Considering the safety margin and trade-off between the detection accuracy and diagnostic speed, the detection threshold of 0.8 can guarantee a relatively robust diagnosis. In practice, T_{th} can be adjusted between 0.5 and 1.

Moreover, the selection of counting threshold is a key issue to eliminate transient spikes, which is mainly determined by the maximum duration of transient spikes. Under the different transient results in Fig. 11, the spikes whose absolute values exceed the detection threshold last up to one control cycle. Therefore, the counting threshold k should be greater than or equal to 1. A larger counting threshold can guarantee accurate detection but reduce the feature extraction of detection variable u_{rd}, which affects output results of counting comparators and may extend fault location time. Considering the trade-off between the accurate elimination of spikes and fault location speed, the counting threshold k is selected to 1.

For selecting p_0 in the SVF, it should be a compromise between the sensitivity to the current noise and the accuracy of the derivative approximation. A large p_0 can make the cutoff frequency of the filter high enough to obtain the derivative of the input signal approximately, but it may cause the high noise in the output of the SVF. In contrast, too small p_0 may result in that the output of the SVF is delayed with respect to the actual current derivative. Thus, a relatively large p_0 should be chosen to obtain good derivative performance. In this paper, p_0 is set to 2e4 by a trial-and-error method in the experiment.

The constant gain of the RLS directly affects the convergence speed and the estimation accuracy. A large γ can speed up the algorithm convergence speed, but the estimated value is extremely susceptible to the interference of the input signals, resulting in large fluctuations. A small value of γ will slow the convergence rate but the estimated value is relatively stable. Finally, a relatively small γ, i.e., 2e-12, is chosen in this paper to obtain a good balance between the convergence speed and the estimation accuracy.

Afterward, when the system operates at a faster switching speed and higher dc voltage, the sampling /control frequency can be increased under the condition that the controller can complete the calculation, reducing the calculation errors of the input-side multilevel voltage. Meanwhile, combined with the suitable design of detection threshold and counting threshold, the misdetection can be also avoided even at relatively high switching frequencies.

VI. Conclusion

This paper presents a simple and fast diagnosis algorithm for single or multiple open-circuit faults in the cascaded H-bridge multilevel converters (CHBMCs). The input-side voltage is considered as a monitored signal where the difference between the real and estimated values is compared and used for fault detection and localization, without the increasing of sensors. Compared with the existing methods, the multiple faults are more simply located by clearing the fault information of the detected switch and further matching fault features. The proposed method only requires a normalized threshold and two counting comparators for each H-bridge to locate faulty cells and faulty switches, greatly simplifying the complexity of the diagnostic algorithm and easily applied to the CHBMCs with more subcells. Meanwhile, the simple spike elimination and parameter estimation enhance the robustness and reliability of the algorithm, without the significant increase of complexity. The experiment results reveal that a single fault can be located within 1/4 fundamental cycle and multiple faults are also identified within one fundamental cycle regardless of the number and position of faulty switches and failure cells. The proposed method shows good diagnostic performance at different fault moments, different loads, and different modulation indexes, expanding the adaptability of the diagnostic algorithm.

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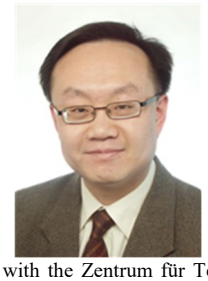

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