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Generic PLL-Based Grid-Forming Control

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Abstract—In grid-forming control, the swing equation of a synchronous machine is emulated by a power controller. Thereby, frequency droop, power-oscillation damping, and/or virtual inertia can be obtained. In this letter it is shown that a phase-locked loop (PLL)—which is normally grid following—can be designed so as to, in turn, emulate a generic power controller, thus, becoming grid forming.

Index Terms—Grid-connected converters, grid-forming control, phase-locked loops, voltage-source converters.

I. Introduction

GRID-FORMING CONTROL of a voltage-source converter has two fundamental properties.

- *Property 1:* The back electromotive force of a synchronous machine is emulated, giving a stiff converter voltage.
- *Property 2:* The swing equation of a synchronous machine is emulated, giving an active-power response to grid-frequency variations.

Schemes based on vector current control are normally grid following. Yet, in [1], it is shown that Property 1 can be fulfilled by a vector-current-control scheme, designed for correspondence to power-synchronization control (PSC).

Property 2 is, in conventional PSC, fulfilled by a power controller (PC) [2]. In [1], a hybrid synchronization controller (SC) is proposed, where the PC is combined with a phase-locked loop (PLL). A similar scheme is suggested in [3]. In PSC, the PLL is needed for synchronization at startup [2] as well as to prevent loss of synchronism when converter-current limitation is applied [4]. During normal operation, the PLL can be disengaged and the PC solely be relied upon.

Unfortunately, as a consequence, during current limitation, an on/off chattering behavior of the PLL may occur. One way of preventing this would be somehow to make the PLL fulfill Property 2, allowing the PC to be eliminated, thus, simplifying the structure of the SC. Steps in that direction have been taken. A PLL is in [5] shown to have structural similarities to the swing equation, and can reproduce certain characteristics thereof if tuned properly [6], [7].
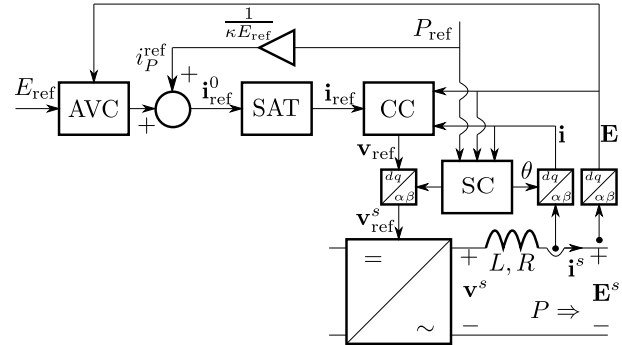
Fig. 1. Circuit and controller block diagram.

The contribution of this letter—in relation to prior art, where certain special cases are considered—is the design of a PLL-based grid-forming control (PLL-GFC) scheme that emulates a generic PC.[1] See Section III. The emulation is not exact, but the accuracy is sufficient as seen from the fairly slow time scale of grid-frequency variations. Thus, Property 2 is fulfilled. Design for PSC correspondence, fulfilling also Property 1, is considered in Section IV. (The design in Section IV summarizes the key results of [1], but PC emulation by the PLL is not considered in [1].) Experimental evaluation with performance comparison of PLL-GFC and PSC is made in Section V.

II. Preliminaries

Boldface letters denote complex space vectors. The superscript s denotes a vector referred to the stationary $\alpha\beta$ reference frame. The corresponding vector referred to the synchronous dq reference frame, which has angle θ as reference, is denoted without a superscript. Italic letters denote scalar variables and real transfer functions. The reference for a controlled variable is denoted by appending the sub- or superscript ref. The Laplace variable s is to be considered as the operator $s = d/dt$, where appropriate.

Fig. 1 illustrates the main circuit and the controller block diagram. The former consists of an inductor, with inductance L and inner resistance R, between the converter and point-of-common-coupling (PCC) buses. The respective voltage vectors are $\mathbf{v}^s$ and $\mathbf{E}^s$, whereas the output current is $\mathbf{i}^s$. The active output power at the PCC is calculated as

$$P = \kappa\mathrm{Re}\{\mathbf{E}^s(\mathbf{i}^s)^*\} = \kappa\mathrm{Re}\{\mathbf{Ei}^*\}, \qquad \kappa = \frac{3}{2K^2} \quad (1)$$

[1]Important special cases of the generic PC are: pure proportional, giving frequency droop; proportional–integral, giving power-oscillation damping and virtual inertia; and lead–lag, giving frequency droop, power-oscillation damping, and virtual inertia [8].
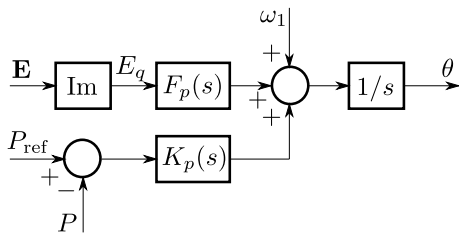
Fig. 2. Hybrid SC, combining a PLL with controller $F_p(s)$ with a PC $K_p(s)$.
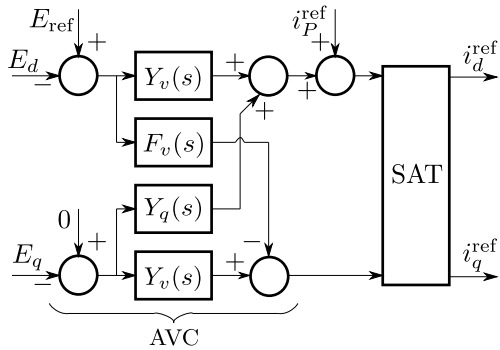

Fig. 3. Generalized AVC with current-reference selection and SAT.

where the superscript $*$ denotes complex conjugate and K is the space-vector scaling constant. The dq frame is statically aligned with the PCC voltage, so that $\mathbf{E} = E$ (i.e., real), giving $P = \kappa E i_d$ in the steady state.

Voltage reference $\mathbf{v}_{\text{ref}}$ is computed by a current controller (CC). The ideal current reference is set as

$$\mathbf{i}_{\text{ref}}^0 = i_P^{\text{ref}} + \text{AVC}(E_{\text{ref}}, \mathbf{E}), \qquad i_P^{\text{ref}} = \frac{P_{\text{ref}}}{\kappa E_{\text{ref}}} \qquad (2)$$

where the second term is the complex output of a generalized ac-bus-voltage controller (AVC), see Section III for details. To avoid absolute values exceeding the maximum permissible current, vector saturation (SAT) is then applied, forming $\mathbf{i}_{\text{ref}} = \text{SAT}(\mathbf{i}_{\text{ref}}^0)$. The CC and the AVC are assumed to be tuned such that the resulting closed-loop step-response rise times are in the ranges of tens and hundreds of milliseconds or less, respectively. In addition, zero static control errors are assumed, i.e., $\mathbf{i} = \mathbf{i}_{\text{ref}}$ and $E_d = E_{\text{ref}}$ statically. The latter achieved by the AVC adjusting i_q^{ref}.

III. MAIN RESULT

Fig. 2 shows the hybrid SC of [1], where ω_1 is the nominal angular grid frequency. The objective is now to make the PLL emulate the PC, i.e., the signal path through $F_p(s)$ should have a similar effect [for $K_p(s) = 0$] as the signal path through $K_p(s)$ [for $F_p(s) = 0$]. Clearly then, a mechanism that forces the PLL input signal E_q to be proportional to the PC input signal $P_{\text{ref}} - P$ is needed. A static relation between the two input signals cannot be obtained, so an exact emulation is impossible. However, a quasi-stationary relation, which captures the dynamics of grid-frequency variations well enough, can be obtained, as will now be demonstrated.

Since active power, according to (1), is produced by i_d, the first step is to create a coupling from E_q to i_d^{ref}, in turn, giving

a coupling to P. This can be accomplished by implementing (2) as shown in Fig. 3, in equation form

$$\begin{aligned} \text{AVC}(E_{\text{ref}}, \mathbf{E}) =& Y_v(s)(E_{\text{ref}} - \mathbf{E}) - Y_q(s)E_q \\ &- jF_v(s)(E_{\text{ref}} - E_d). \end{aligned} \qquad (3)$$

Here, $F_v(s)$ is a conventional AVC, coupling from E_d to i_q^{ref}. It needs to have integral action to make $E_d = E_{\text{ref}}$ statically. $Y_v(s)$ is an active damper consisting of a gain (active conductance) G_a in cascade with a low-pass filter. It is vital for fulfilling Property 1, see Section IV. $Y_q(s)$ similarly consists of a gain (active susceptance) B_a in cascade with a low-pass filter. It creates the required coupling from E_q to i_d^{ref}.

Let us now analyze the impact of (3) seen from the time scale of grid-frequency variations. This time scale is given by the characteristic inertia constant of the grid, which is typically in the range of seconds. This is substantially slower than the closed-loop-system rise times assumed in Section II. Consequently, in the time scale of grid-frequency variations, the static relations $\mathbf{i} = \mathbf{i}_{\text{ref}}$ and $E_d = E_{\text{ref}}$ can be considered. In addition, the filters in $Y_v(s)$ and $Y_q(s)$ are assumed to have high enough bandwidths to be considered statically as well, i.e., $Y_v(0) = G_a$ and $Y_q(0) = B_a$. Assuming that SAT is not effectuated, (2) and (3) then yield

$$\mathbf{i} = i_P^{\text{ref}} - B_a E_q - j\underbrace{(G_a E_q + i_v)}_{-i_q} \qquad (4)$$

where i_v is the quasi-static value of the integrator of the conventional AVC. Substitution in (1) yields

$$P = \kappa \text{Re}\{\mathbf{E}\mathbf{i}^*\} = P_{\text{ref}} - \kappa(E_{\text{ref}}B_a - i_q)E_q. \qquad (5)$$

Solving for E_q in (5) gives the desired proportionality between the PC and PLL input signals as

$$E_q = \frac{1}{\kappa(E_{\text{ref}}B_a - i_q)}(P_{\text{ref}} - P). \qquad (6)$$

Consequently, for the PLL to emulate the PC, the PLL controller should be selected as

$$F_p(s) = \kappa(E_{\text{ref}}B_a - i_q^f)K_p(s) \qquad (7)$$

where i_q^f is a low-pass filtering of i_q (or, if preferred, i_q^{ref}). Low-pass filtering is desired to suppress noise in the variable gain of (7).

The working principle of the proposed scheme is perhaps easiest understood by expressing the PCC voltage in polar form as $\mathbf{E}^s = Ee^{j\theta_p} \Rightarrow \mathbf{E} = Ee^{j\Delta\theta}$, $\Delta\theta = \theta_p - \theta$, giving $E_q = E\sin\Delta\theta$. Suppose that $\Delta\theta = 0$ initially. A variation in the grid frequency, let us say a drop, results in θ_p lagging θ, i.e., $\Delta\theta$ becomes negative. Via the second term in (3), this causes an active-power injection. The characteristics thereof are determined solely by $K_p(s)$; due to the factor $\kappa(E_{\text{ref}}B_a - i_q^f)$ in (7), the characteristics are invariant of B_a. A larger B_a merely results in smaller transients in $\Delta\theta$ and, thus, in E_q. At the very least, to avoid the risk that the gain of (7) changes sign, $B_a > \max(i_q)/E_{\text{ref}}$ should be selected. Normally, $\max(i_q)/E_{\text{ref}} \leq 1$ per unit (p.u.).
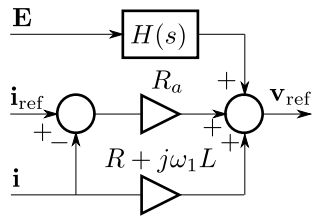
Fig. 4. Proportional–decoupling–feedforward CC.

TABLE I
CONTROLLER SELECTIONS

	PSC	PLL-GFC
$K_p(s)$	$K_{p0}(s)$	0
$F_p(s)$	0	$\kappa(E_{\text{ref}}B_a - i_q^f)K_{p0}(s)$
$Y_v(s)$	$\frac{1}{R_a}(1+\frac{\alpha_a}{s})H(s)$	$\frac{1}{R_a}H(s)$
$F_v(s)$	0	$\frac{\kappa K_{p0}(s)E_{\text{ref}}^2 H(s)}{R_a^2 s}$
$Y_q(s)$	0	$B_a H(s)$

IV. DESIGN FOR PSC CORRESPONDENCE

As long as the assumptions relied upon in Section III are fulfilled, the CC and blocks $Y_v(s)$ and $F_v(s)$ of the AVC can be chosen freely. However, of particular interest is a design giving near equivalence between PLL-GFC and the slightly modified PSC variant considered in [1], thus, ensuring that Property 1 is fulfilled. As shown in [1], such a design is obtained by using a proportional–decoupling–feedforward CC (see Fig. 4)

$$\mathbf{v}_{\text{ref}} = R_a(\mathbf{i}_{\text{ref}} - \mathbf{i}) + (R + j\omega_1 L)\mathbf{i} + H(s)\mathbf{E}. \quad (8)$$

In the PCC-voltage feedforward term, the recommended low-pass filter selection is $H(s) = \alpha_c/(s+\alpha_c)$, where $\alpha_c = R_a/L$ is the bandwidth of the closed current control loop that results from (8).

With $K_{p0}(s)$ as the desired PC (to be implemented in PSC and emulated in PLL-GFC), Table I shows the controller selections, with reference to Figs. 2 and 3, for PSC and PLL-GFC, respectively. The following should be noted (see [1] for details).

- To fulfill Property 1, the active conductance is selected as $G_a = 1/R_a$.
- PSC uses neither a conventional AVC, nor a PLL. To ensure that $\mathbf{E} = E_{\text{ref}}$ statically despite that, an integral part (with gain α_a) is included in $Y_v(s)$.
- For PLL-GFC, in addition to $F_p(s)$, also $F_v(s)$ is made proportional to $K_{p0}(s)$. Under idealized conditions, this gives the same small-signal dynamics as the PC.
- For simplicity, the low-pass filter in $Y_q(s)$ is chosen identical to that in $Y_v(s)$.

V. EXPERIMENTAL AND SIMULATION RESULTS

The experimental setup—see Table II for data—uses back-to-back converters, allowing dc-bus-voltage control from the converter not being studied. There is a shunt capacitor (with capacitance C) at the PCC, forming an inductive–capacitive–inductive filter with the grid inductance L_g behind the grid-voltage source.

TABLE II
EXPERIMENTAL SETUP DATA

Variable/parameter	Actual value	Normalized value
Rated power	12.5 kVA	1 p.u.
Rated voltage	$\sqrt{2/3}\cdot 400$ V	1 p.u.
Rated current	$\sqrt{2}\cdot 18$ A	1 p.u.
Maximum current	$1.5\cdot\sqrt{2}\cdot 18$ A	1.5 p.u.
Base impedance	12.8 Ω	1 p.u.
Filter inductance L	3.3 mH	0.081 p.u.
Filter resistance R	0.51 Ω	0.040 p.u.
Filter capacitance C	8.8 μF	0.036 p.u.
Fundamental frequency	50 Hz	1 p.u.
Rated dc-bus voltage	650 V	2 p.u.
Sampling frequency	10 kHz	200 p.u.
Switching frequency	5 kHz	100 p.u.

Performance comparisons of PLL-GFC and PSC, designed according to Section IV, are made. A proportional–integral PC is considered as

$$K_{p0}(s) = K_p + \frac{1}{Ms}. \quad (9)$$

As shown in [8], the proportional part corresponds to a power-oscillation damper and the integral part to a virtual inertia. The following p.u. parameter values are selected:

$$R_a = 0.2 \qquad K_p = 0.05 \qquad M = 1000$$
$$B_a = 5 \qquad \alpha_a = 0.1. \quad (10)$$

First, L_g is selected to get a short-circuit ratio of 1. The grid voltage is 1 p.u. In Fig. 5, the grid frequency $\omega_g/(2\pi)$ is ramped from 50 Hz (1 p.u.) down to 49 Hz (0.98 p.u.) with the rate of change 5 Hz/s. As can be observed, near-identical inertial responses in P are obtained from the two schemes. Due to the proportional (damping) part of (9), there are no power oscillations. The transient in E_q for PLL-GFC results in a slightly different transient in i_q compared to PSC.

Next, the configuration is changed to islanded operation, with zero grid voltage. L_g is reduced to 0.5 p.u. and a 6-p.u. load resistance is put in series. M is made infinite, giving a proportional-only PC, i.e., a frequency droop [8]. In Fig. 6, at $t = 0.2$ s, the load resistance is decreased to 2 p.u., giving an increased power draw and, as a result, a frequency reduction. It is interesting to note that the instantaneous frequencies of PSC and PLL-GFC deviate transiently. This is because the PLL emulation of the PC is not exact. Yet, the active-power responses are virtually identical, showing that the quasi-stationary design principle in Section III is relevant.

The experimental setup unfortunately does not facilitate multiple converters. To show that PLL-GFC has the capability of islanded operation with multiple converters, the experimental setup is replicated in Simulink, but with two converters (I and II) connected in parallel at the PCC. The converters and their controls are identical, but to introduce an asymmetry, they have slightly different filter inductances: $L_{\text{I}} = 1.1L$ and $L_{\text{II}} = 0.9L$. As can be observed in Fig. 7, the converters share the load power equally. In fact, the curves (for voltage, E_q only) replicate the corresponding experimental curves in Fig. 6, but scaled with $1/2$ due to the load sharing.
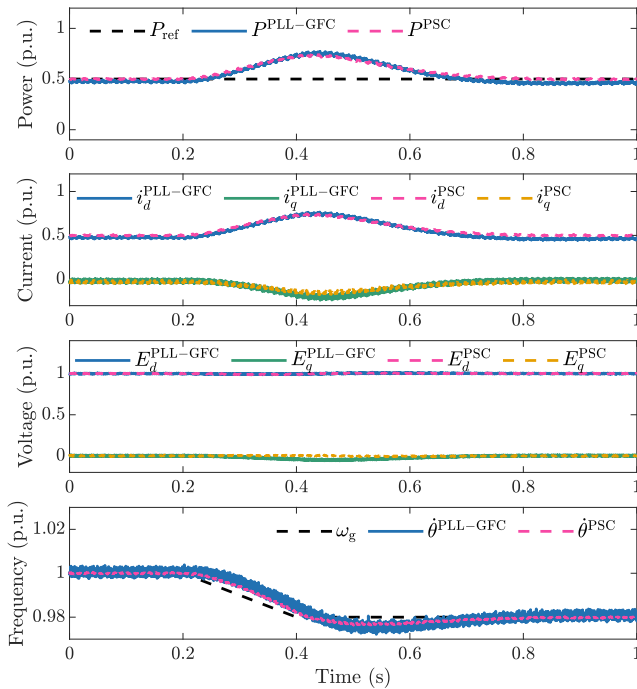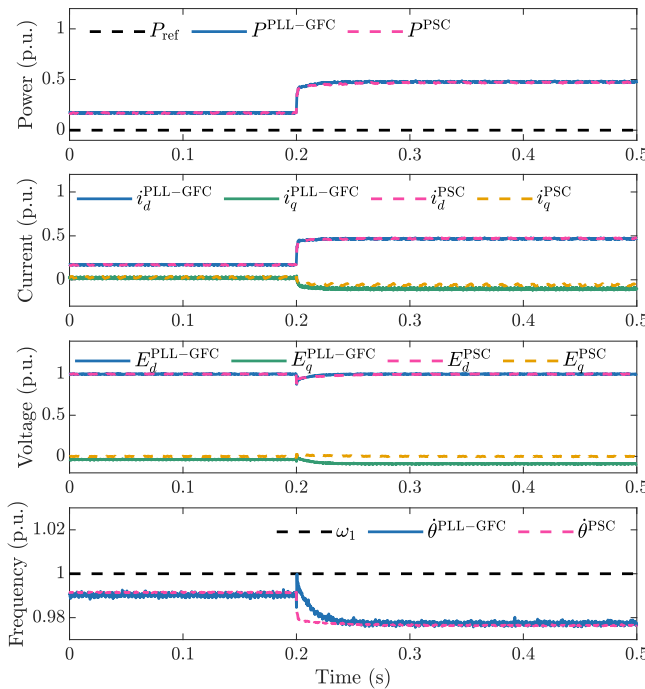
Fig. 5. Grid-frequency ramp.

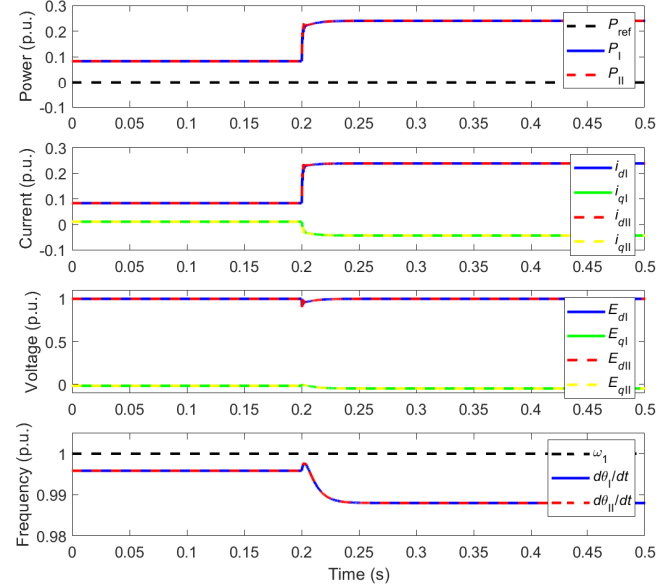Fig. 6. Islanded operation with load-resistance step.

Fig. 7. Islanded operation with load-resistance step; simulation of two parallel converters (I and II) using PLL-GFC.

near identical performance. The most notable difference is that, in PLL-GFC, transients in P are reflected by transients in E_q (and vice versa). This is caused by the coupling from E_q to i_d^{ref}, with gain B_a, introduced to fulfill Property 2. The transients in E_q diminish as B_a is increased.

VI. CONCLUSION

Previous findings concerning the similarity between a PLL and the swing equation of a synchronous machine were generalized. The scheme PLL-GFC results, where the PLL is designed to emulate a generic PC, fulfilling Property 2. Design for PSC correspondence was considered, fulfilling also Property 1.

Experimental comparison of PLL-GFC and PSC showed

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